UM10752

OM13489 16-bit GPIO Daughter Card User Manual

Rev. 2.0 — 09 January 2014 **User manual**

Document information

Info	Content
Keywords	Fm+ Development Kit, OM13320, GPIO, OM13303
Abstract	Installation guide and User Manual for the OM13489 16-bit GPIO Daughter Card that connects to OM13320 Fm+ Development Kit. This board permits easy and simple evaluation of most of NXP's 16-bit I^2C GPIO portfolio of products.

Revision history

Rev	Date	Description
2.0	20140109	Added A0 jumper hardware fix and CN5 schematic – changed from 14-pin to 18-pin with 4 pins not connected for correct connector seating on the Fm+ board. Active pins remain the same. Labels for JP7 and JP8 (A1 and A2 address jumpers) are incorrect; 1 connects to ground and 0 connects to V_{DDP}
1.0	20131011	Initial Release

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1. Introduction

The OM13489 16-bit I²C GPIO Daughter Card connects to the OM13320 Fm+ Development kit and permits easy evaluation of most of NXP's 16-bit I²C GPIO portfolio of products.

Table_1 lists the supported devices.

The OM13489 16-bit I²C GPIO Daughter Card is shipped with no GPIO device soldered to the board. The user must purchase the device he is interested in evaluating in a TSSOP24 package (the ordering part number suffix should be "PW" and the package designation should be SOT355-1). These leaded packages should be relatively easy to solder to the board with a low wattage, fine tipped soldering iron.

NOTE pin 1 orientation pointing toward C1.

Please note that a fix is needed for correct operation of the A0 jumper JP1. A wire must be soldered between pin 2 of JP1 and the via directly below to make connection to pin 21 on the device under test IC1. See Section 3.2 for additional details.

Table 1. Devices Supported by OM13489 16-bit I²C GPIO Daughter Card

Device	Description	Orderable Part Number
PCA6416A	Low-voltage translating 16-bit I²C-bus/SMBus I/O expander with interrupt output, reset, and configuration registers	PCA6416APW
PCA8575	Remote 16-bit I/O expander for I²C-bus with interrupt	PCA8575PW
PCA9535A	Low-voltage 16-bit I²C-bus I/O port with interrupt	PCA9535APW
PCA9535C	16-bit I²C-bus and SMBus, low power I/O port with interrupt	PCA9535CPW
PCA9535	16-bit I²C-bus and SMBus, low power I/O port with interrupt	PCA9535PW
PCA9539A	Low voltage 16-bit I²C-bus I/O port with interrupt and reset	PCA9539APW
PCA9539	16-bit I²C-bus and SMBus low power I/O port with interrupt and reset	PCA9539PW
PCA9539R	16-bit I²C-bus and SMBus low power I/O port with interrupt and reset	PCA9539RPW
PCA9555A	Low-voltage 16-bit I²C-bus I/O port with interrupt and weak pull-up	PCA9555APW
PCA9555	16-bit I²C-bus and SMBus I/O port with interrupt	PCA9555PW
PCA9671	Remote 16-bit I/O expander for Fm+ I²C-bus with reset	PCA9671PW
PCA9673	Remote 16-bit I/O expander for Fm+ I²C-bus with interrupt and reset	PCA9673PW
PCA9675	Remote 16-bit I/O expander for Fm+ I²C-bus with interrupt	PCA9675PW
PCAL6416A	Low-voltage translating 16-bit I²C-bus/SMBus I/O expander with interrupt output, reset, and configuration registers	PCAL6416APW
PCAL9535A	Low-voltage 16-bit I²C-bus I/O port with interrupt and Agile I/O	PCAL9535APW
PCAL9539A	Low-voltage 16-bit I²C-bus and SMBus low power I/O port with interrupt and reset	PCAL9539APW
PCAL9555A	Low-voltage 16-bit I²C-bus GPIO with Agile I/O, interrupt and weak pull-up	PCAL9555APW
PCF8575	Remote 16-bit I/O expander for I²C-bus	PCF8575PW

The pin configuration of these devices varies only a bit and the different pin selections are made via jumpers.

2. Features of the OM13489 16-bit GPIO Daughter Card

- Direct connection to OM13320 Fm+ Development kit
- Footprint for a TSSOP24 package, user solderable
- Jumper configuration accommodates most NXP 16-bit GPIO
- Flexible power supply configuration: 3.3V, 5V or external supply
- Direct connection to OM13303 GPIO Target board for I/O visualization
- Jumper configuration of device I^2C address
- LED indicators for power and $\overline{INT}$
- Scope ground connection loop

3. Pin Configuration of 16-bit GPIO Devices

The different 16-bit GPIO devices pin configurations differ only slightly between devices. See Fig 1 for a description of the different pinouts.

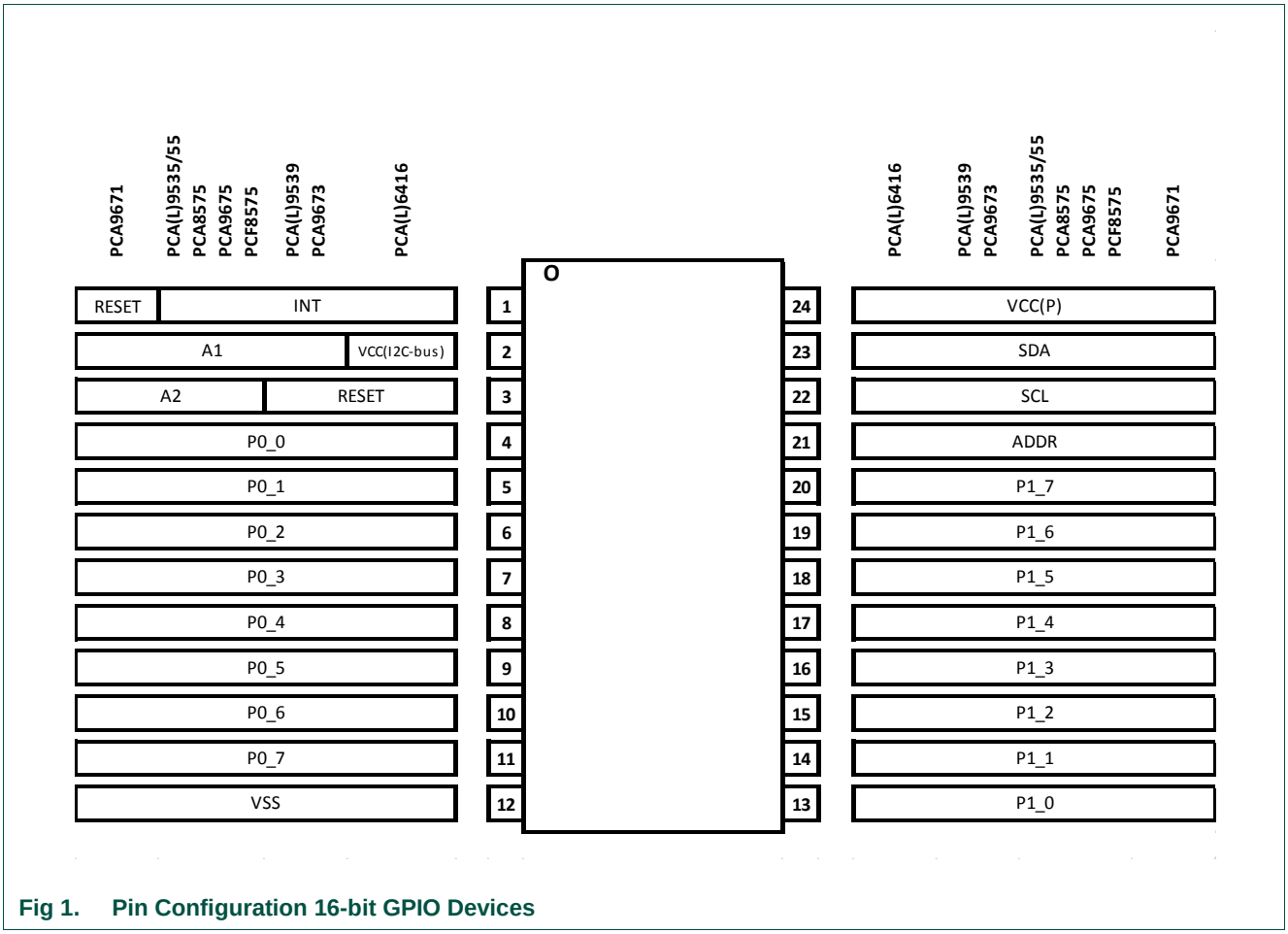


Fig 1. Pin Configuration 16-bit GPIO Devices

3.1 Power Supply Setup

Power supply voltages may be selected from the tester connector CN4 or the Fm+ board CN5. If one selects Fm+ CN5, either 3.3V or 5V can be chosen. Additionally, the PCA(L)6416 device implements two power supplies which are separately chosen, i.e. one can be 3.3V and the other 5V for voltage level translation evaluation. Both of these power supplies can be supplied externally by using TP1 and TP2 near the tester connector CN4. See the schematic section at the end of this document for more details.

The jumpers for power supply selection are CN3, JP3, and JP4

3.2 Reset, Interrupt, and Address pins selection

The Reset, Interrupt and Address pins are used in combinations on various devices. The selection matrix on the 16-bit GPIO board sends pins 1, 2, and 3 to determine if the pins are address or function on JP9, JP10, and JP11. Then, if they are determined address pins, JP1, JP7 and JP8 tie them to logic high or low. If they are determined to be function pins, the other position of JP9, JP10 and JP11 tie them to the correct connector function pins. See the schematic section at the end of this document for more details.

The logic high level for the address pins is VDDP .

Please note that a fix is needed for correct operation of the A0 jumper JP1. A wire must be soldered between pin 2 of JP1 and the via directly below to make connection to pin 21 on the device under test IC1. Use 30 AWG wire wrap wire for the easiest connection. The solder mask on the board will prevent any short circuits.

Please note that A1 and A2 jumpers are incorrectly labeled. JP7 and JP8 program I2C addresses when selected. The labels show that A1 and A2 pins will be connected to ground when the jumper shorts pin 1 and 2 (toward the bottom edge of the board). In fact, this is a connection to V_{DDP} or high. The schematic is correct, only the labels are incorrect.

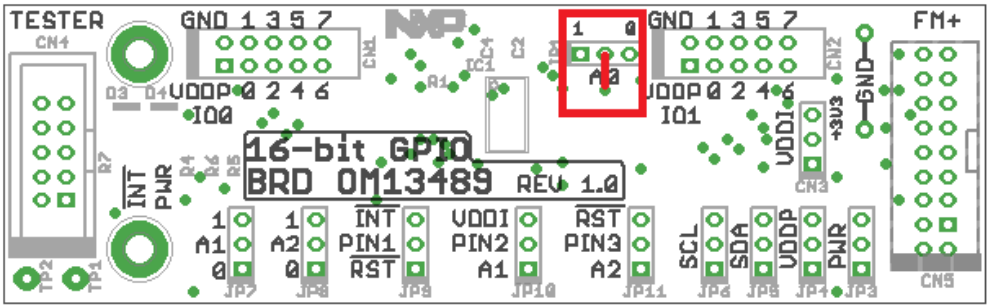


Fig 2. Fix needed for correct operation of A0 jumper JP1

4. Board Jumper Set Up

4.1 Power Supply Jumpers

The power supply selections for the OM13489 is very flexible and allows for detailed analysis and evaluation of all the NXP 16-bit GPIO devices. JP3 labeled PWR selects between 5V supplied from the tester connector CN4 (jumper between pin 2 and 3 labeled TSTR) and the Fm+ board connector CN5 (jumper between pin 1 and 2). If 3.3V or external power operation is desired, no jumper is required.

CN3 selects between 5V and 3.3V for a second power supply needed for PCA(L)6408A. If the device under test is not PCA(L)6408A, leave this jumper open.

JP4 selects between 5V and 3.3V for the main power supply on pin 16 of the device under test. Add a jumper between pins 2 & 3 for 3.3V or 1 & 2 for 5V.

For external power supply operation, do not jumper CN3, JP3 and JP4 and connect a voltage source to TP2 for the main power supply connected to pin 16 of the device under test. Connect another external voltage source to TP1 if the device under test is PCA(L)6408A.

See the schematic section at the end of this document for more details.

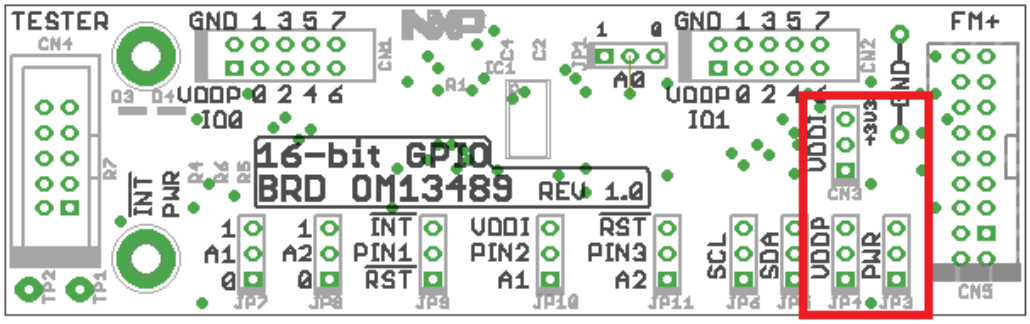


Fig 3. Power Jumpers and External Power Test Points

4.2 SCL and SDA Jumpers

The I2C-bus signals SDA and SCL supplied to the device under test can be sourced from either the Fm+ board via CN5 or the tester via CN4. Jumpers JP5 and JP6 select the source. Shorting pins 1 to 2 source from the Fm+ board while shorting pins 2 to 3 source from the tester connector CN4.

See the schematic section at the end of this document for more details.

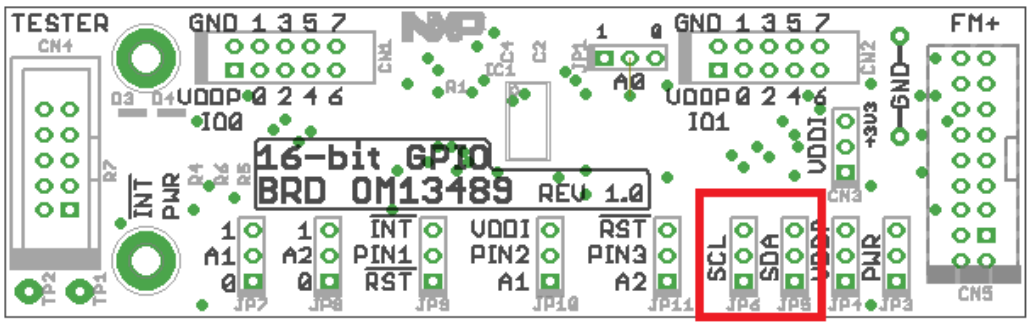


Fig 4. SDA and SCL Jumpers

4.3 PCA8575, PCA9535A, PCA9535C, PCA9535, PCA9555A, PCA9555, PCA9675, PCAL9535A, PCAL9555A, PCF8575

The PCA8575, PCA9535/A/C, PCA9555/A, PCA9675 and PCF8575 series implement three address pins and $\overline{INT}$. This configuration ignores the power supply setup, but normally, only JP4 with a jumper between pins 2 & 3 need be applied to power the device at 3.3V.

To configure the function pins, apply jumpers between pins 1 & 2 on JP10 and JP11 to configure device pin 2 and pin 3 as addresses. Apply a jumper between pins 2 & 3 on JP9 to configure device pin 1 as $\overline{INT}$.

Then, apply jumpers to JP1, JP7 and JP8 to configure the desired I^2C address. Logic high or logic low is labeled on the board, but is incorrect for JP7 and JP8. Using the labels, a 0 is actually a 1 and a labeled 1 is actually a 0. The schematic is correct and note the square solder pad is pin 1.

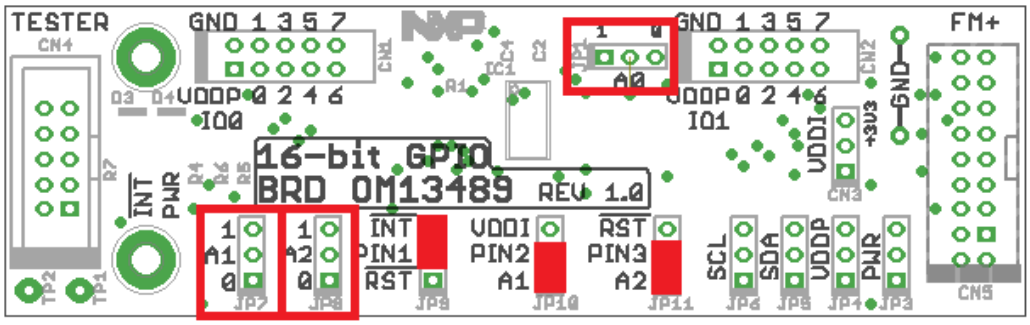


Fig 5. Jumper Configuration for PCA8575, PCA9535A, PCA9535C, PCA9535, PCA9555A, PCA9555, PCA9675, PCAL9535A, PCAL9555A, PCF8575

4.4 PCA9671

The PCA9671 implements three address pins and $\overline{RST}$. This configuration ignores the power supply setup, but normally, only JP4 with a jumper between pins 2 & 3 need be applied to power the device at 3.3V.

To configure the function pins, apply jumpers between pins 1 & 2 on JP9, JP10 and JP11 to configure pin 2 and pin 3 as addresses and pin 1 as $\overline{RST}$.

Then, apply jumpers to JP1, JP7 and JP8 to configure the desired I^2C address. Logic high or logic low is labeled on the board, but is incorrect for JP7 and JP8. Using the labels, a 0 is actually a 1 and a labeled 1 is actually a 0. The schematic is correct and note the square solder pad is pin 1.

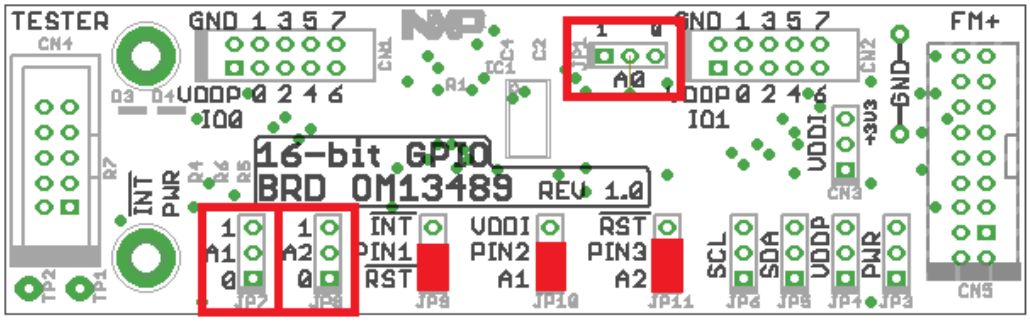


Fig 6. Jumper Configuration for PCA9671

4.5 PCA9673, PCAL9539A, PCA9539A, PCA9539R, PCA9539

The PCA9673 and PCA9539 series implement two address pins, $\overline{RST}$ and $\overline{INT}$. This configuration ignores the power supply setup, but normally, only JP4 with a jumper between pins 2 & 3 need be applied to power the device at 3.3V.

To configure the function pins, apply jumpers between pins 2 & 3 on JP9 and JP11 to configure device pin 3 as $\overline{RST}$ and device pin 1 as $\overline{INT}$. Apply a jumper between pins 1 & 2 on JP10 to configure device pin 2 as an address.

Then, apply jumpers to JP1 and JP7 to configure the desired I^2C address. Logic high or logic low are labeled on the board. Leave JP8 open. The labels are incorrect for JP7 and JP8. Using the labels, a 0 is actually a 1 and a labeled 1 is actually a 0. The schematic is correct and note the square solder pad is pin 1.

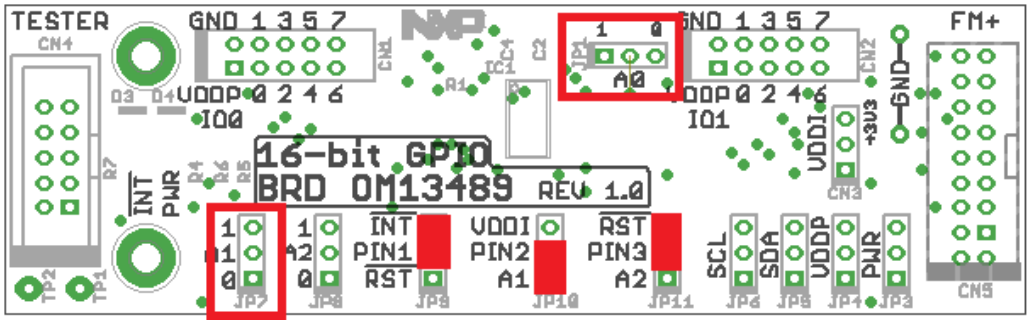


Fig 7. Jumper Configuration for PCA9673, PCAL9539A, PCA9539A, PCA9539R, PCA9539

4.6 PCAL6416A, PCA6416A

The PCA(L)6416A devices are level translating, Agile I/0 Expanders with two power supplies, one address pin, $\overline{RST}$ and $\overline{INT}$. The two power supplies may operate at different voltages to translate from the I^2C-bus voltage domain to a higher or lower I/O voltage. CN3 and JP4 may be set to the same or different voltages, or left open and external voltage sources connected to TP1 and TP2. See the datasheet for more details on voltage level translation.

Note that the 10K pull up resistors SDA and SCL, R5 and R6, are connected to VDDP which may cause incorrect current readings if two different supplies are used.

To configure the function pins, apply jumpers between pins 2 & 3 on JP9, J10 and JP11 to configure device pin 2 as a power supply, device pin 3 as $\overline{RST}$ and device pin 1 as $\overline{INT}$.

Then, apply a jumper to JP1 to configure the desired I^2C address. Logic high or logic low are labeled on the board. Leave JP7 and JP8 open.

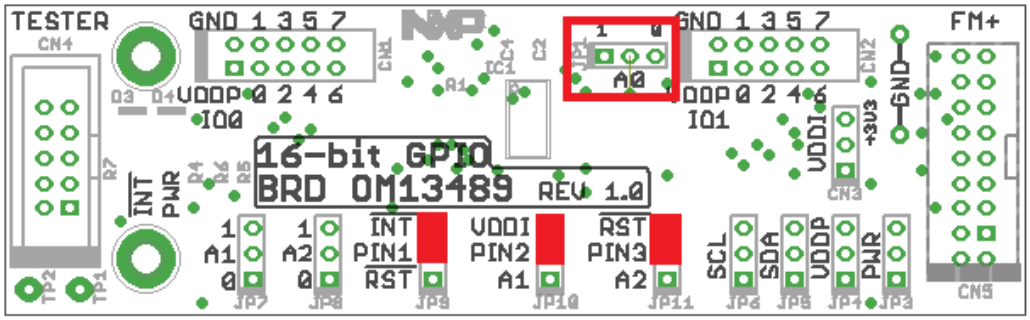


Fig 8. Jumper Configuration for PCA(L)6416

5. Connector Pinouts

5.1 CN1 GPIO Target Board Connector

The OM13303 GPIO Target Board consists of eight LEDs and eight switches and connects directly to the 16-bit GPIO board through CN1. The switches and LEDs permit easy exercise of the I/O functionality of the device under test. The LEDs light red when the voltage on that channel is below VCC x 0.3V and lights green when the voltage is above VCC x 0.7V. The LEDs remain off when the voltage is between those two levels.

Table 2. CN1 GPIO Target Board Connector Pinout

CN1 Pin Number	Function	Board Connection
1	VDD	VDDP
2	Ground	GND
3	IO0	U1 pin 4
4	IO1	U1 pin 5
5	IO2	U1 pin 6
6	IO3	U1 pin 7
7	IO4	U1 pin 9
8	IO5	U1 pin 10
9	IO6	U1 pin 11
10	IO7	U1 pin 12

5.2 CN5 Fm+ Development Board Connector

The OM13489 can connect directly to the OM13320 Fm+ Development kit via CN5. This connector provides power, I^2C signals and other ancillary signals.

Note: The connector on the Fm+ board is a male, shrouded 14 pin type, while the connector on the GPIO board is female, 18 pin.. The reason lies with the shroud around the 14 pin connector. To ensure correct mating of the female with the male, two pin positions on both of the female sides are unused.

Table 3. CN5 Fm+ Board Connector

CN5 Pin Number	Function	Board Connection
1	—	No connect
2	—	No connect
3	SCL	SCL Bus 1 to U1 pin 14
4	SDA2	SDA Bus 2 not used
5	INT	Interrupt to INT LED and JP9 pin 3
6	RESET	JP9 pin 1, JP11 pin 3
7	+5V	JP3 pin 1
8	+3.3V	CN3 pin 3 and JP4 pin 3
9	GND	
10	GND	
11	+3.3V	CN3 pin 3 and JP4 pin 3
12	+5V	JP3 pin 1
13	RESET	JP9 pin 1, JP11 pin 3
14	INT	Interrupt to INT LED and JP9 pin 3
15	SDA	SDA Bus 1 to U1 pin 15
16	SCL2	SCL Bus 2 not used
17	—	No connect
18	—	No connect

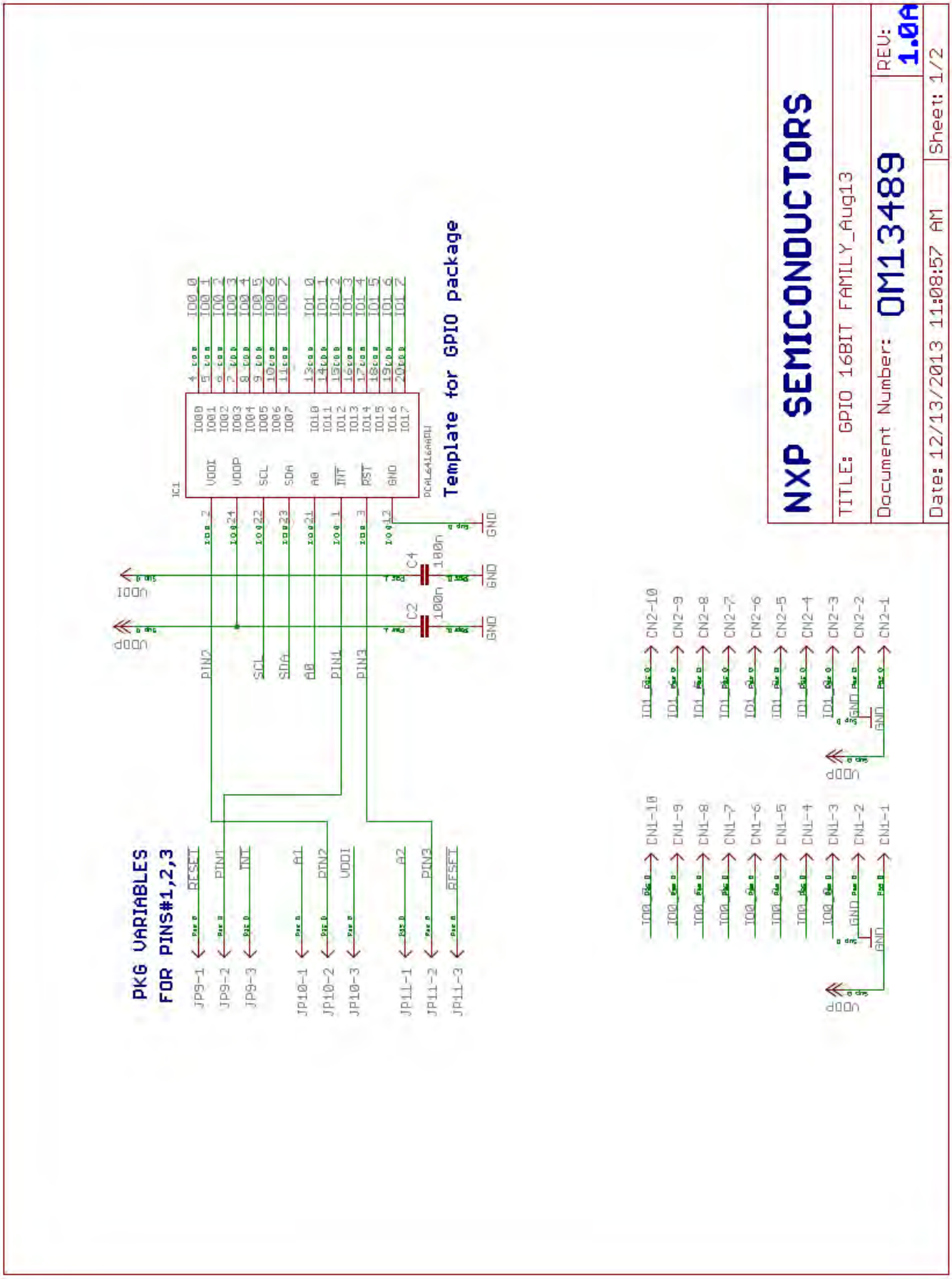
5.3 CN4 Tester Connector

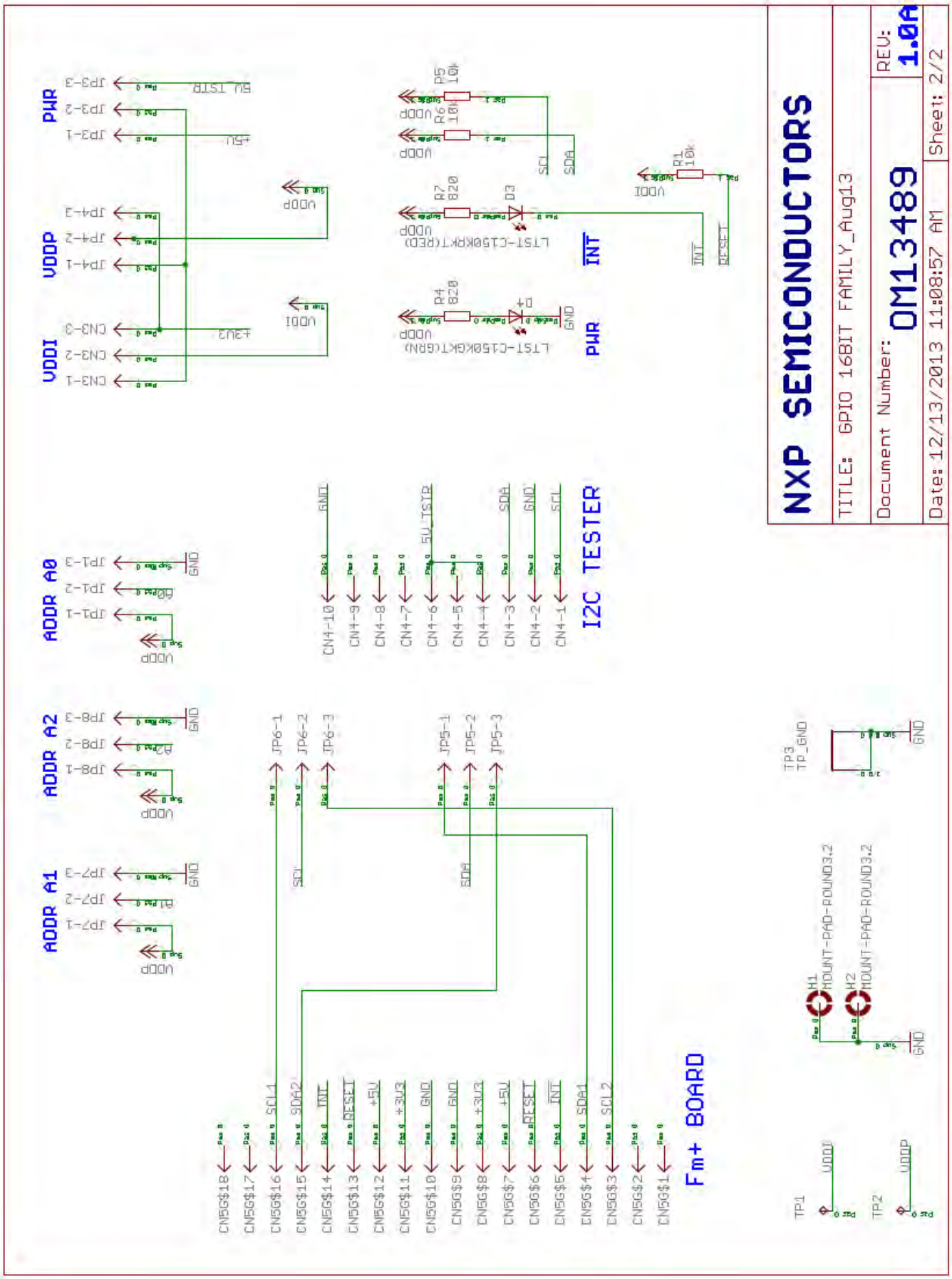
Generation, inspection and logging of I^2C-Bus data is easily achieved with third party development tools from Total Phase (www.totalphase.com) There are two tools called Aardvark and Beagle that direct connect to this board through CN4.

Note: Since SDA and SCL are both connected to the device under test, the Aardvark and the Fm+ Development board cannot be used simultaneously. The Beagle, a bus sniffer, does not have any issues.

Table 4. CN4 Tester Connector

CN4 Pin Number	Function	Board Connection
1	SCL	U1 pin 14
2	Ground	
3	SDA	U1 pin 15
4	+5V	JP3 pin 3
5	+5V	JP3 pin 3
6	+5V	JP3 pin 3
7	—	
8	—	
9	—	
10	Ground	





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