The Future of Analog IC Technology

HR1001

Enhanced LLC Controller with Adaptive Dead Time Control

DESCRIPTION

The HR1001 is an enhanced LLC controller which provides new features of adaptive dead time adjustment (ADTA) and capacitive mode protection (CMP).

The adaptive dead time adjustment automatically inserts a dead time between the two complimentary gate outputs. This is ensured by keeping the outputs off while sensing the dv/dt current of the half-bridge switching node. The ADTA features easier design, lower EMI, and higher efficiency.

HR1001 incorporates anti-capacitive mode protection which prevents potentially destructive capacitive mode switching if the output is shorted or has a severe over load. This feature protects the MOSFET during abnormal condition, making the converter robust.

HR1001 has a programmable oscillator that sets both the maximum and minimum switching frequencies. It starts up at a programmed maximum switching frequency and decays until the control loop takes over to prevent excessive inrush current.

HR1001 enters a controlled burst-mode operation at light-load to minimize the power consumption and tighten output regulation.

HR1001 provides rich protection features which include two-level OCP with external latch shutdown, auto-recovery, brown in/out, CMP, and OTP, improving converter design safety with minimal extra components.

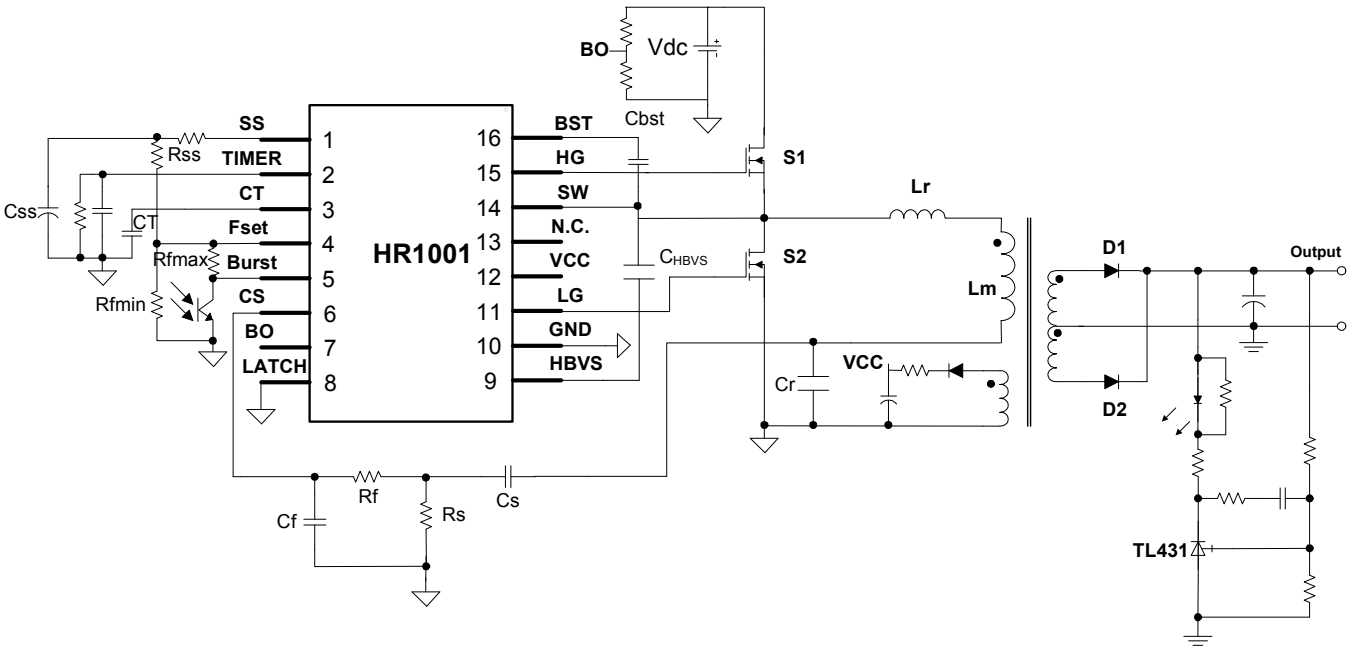
FEATURES

- Adaptive dead-time adjustment
- Capacitive mode protection
- 50% Duty Cycle, Variable Frequency Control For Resonant Half-Bridge Converter
- 600V High-Side Gate Driver with Integrated Bootstrap Diode with High dv/dt immunity
- High-Accuracy Oscillator
- Operates up to 600kHz
- Two-Level Over-Current Protection: Frequency-Shift and Latched Shutdown with Programmable Duration Time
- Latched Disable Input for Easy Protections
- Remote ON/OFF Control and Brown-Out Protection through the BO Pin
- Programmable Burst-Mode Operation at Light-Load
- Non-Linear Soft-Start for Monotonic Output Voltage Rise
- SOIC-16 package

APPLICATIONS

- LCD and PDP TVs
- Desktop PCs and Servers
- Telecom SMPS
- AC-DC Adapter, Open-Frame SMPS
- Video Game Consoles
- Electronic Lighting Ballast

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
HR1001GS	SOIC-16	*See Below*

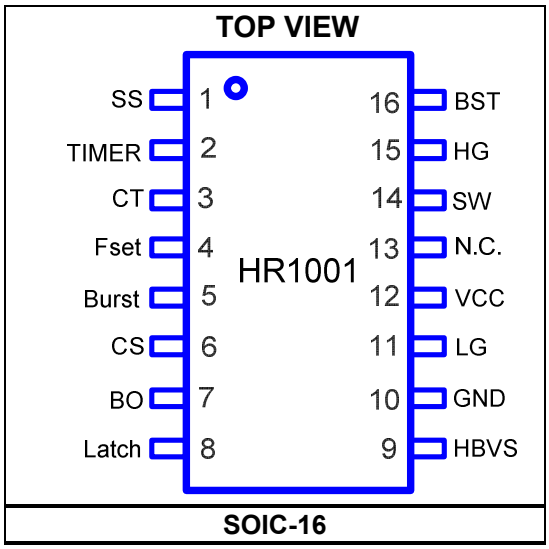
* For Tape & Reel, add suffix –Z (e.g. HR1001GS–Z)

TOP MARKING

MPSYYWW
HR1001
LLLLLLLLL

MPS: MPS prefix:
YY: year code;
WW: week code:
HR1001: part number;
LLLLLLLLL: lot number;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

BST pin voltage……..... -0.3V to 618V
SW pin voltage ……. ..... -3V to 600V
Max. voltage slew rate of SW pin….. .....50V/ns
Supply voltage V_{CC}…….. .....Self limited
Sink current of HBVS pin…….....± 65mA
Voltage on HBVS pin …..... -0.3V to Self limited
Source current of FSET pin….. .....2mA
Voltage rating LG……. ..... -0.3V to V_{CC}
Voltage on CS pin ……..... -3V to 6V
Other Analog inputs and outputs..... -0.3V to 6V
Continuous power dissipation (T_A = +25°C) (2)
P_{IC} ……. 1.56W
Junction Temperature…. .....150°C
Lead Temperature…….. .....260°C
Storage Temperature…….....-65°C to +150°C
ESD immunity :
BST, HG, SW passes HBM 2.5kV,
Other pins can pass HBM 4kv.

Recommended Operating Conditions (3)

Supply Voltage VCC….. .....13V to 15.5V
Analog inputs and outputs.....-0.3V to 6V
Operating Junction Temp (T_J) -40°C to + 125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOIC16	80.....	35°	C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VCC=13V, C_{HG}=C_{LG}=1nF; CT=470pF, R_{FSET}=12kΩ, T_J=-40°C ~ 125°C, Min & Max are guaranteed by characterization, typical is test under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IC supply voltage (VCC)						
VCC operating range			8.9		15.5	V
VCC high threshold, IC switch-on	V_{CCH}		10.3	11	11.7	V
VCC low threshold, IC switch-off	V_{CCL}		7.5	8.2	8.9	V
Hysteresis	V_{hys}			2.8		V
VCC clamp voltage	V_{Clamp}	I_{Clamp} =1mA		16.5		V
IC supply current (VCC)						
Start-up current	$I_{start-up}$	Before the device turns on, VCC=VCC_H-0.2V		250	320	μA
Quiescent current	I_q	Device on, V_{Burst}<1.25V, RFSET=12k,(Fmin=60kHz)		1.2	1.5	mA
	I_{q-f}	Device on, V_{Burst}<1.25V RFSET=3.57k,(Fburst=200k)		1.42	1.8	mA
Operating current	I_{op}	Device on, V_{Burst}=V_{FSET}		3	5	mA
Residual consumption	I_r	VCC<8V or V_{LATCH}>1.85V or V_{CS}>1.5V or V_{TIMER}>3.5V or V_{BO}<1.75V or V_{BO}>5.5V or OTP.	240	350	420	μA
High-side floating-gate-driver supply (BST, SW)						
BST pin leakage current	I_{LKBST}	V_{BST}=600V, T_J=25°C			12	μA
SW pin leakage current	I_{LKSW}	V_{SW}=582V, T_J=25°C			12	μA
Current Sensing (CS)						
Input bias current	I_{CS}	V_{CS}=0 to $V_{CSlatch}$			2	μA
Frequency shift threshold	V_{CSx}		0.71	0.78	0.85	V
OCP threshold	V_{CS-OCP}		1.41	1.5	1.59	V
Current polarity comparator ref. when HG turns off	V_{CSPR}		50	85	131	mV
Current polarity comparator ref. when LG turns off	V_{CSNR}		-131	-85	-50	mV
Line voltage sensing (BO)						
Start up threshold voltage	V_{th-on}			2.30	2.4	V
Turn off threshold voltage	V_{th-off}		1.72	1.81		V
Clamp level	V_{clamp}		5.1	5.5	5.9	V

ELECTRICAL CHARACTERISTICS *(continued)*

VCC=13V, C_{HG}=C_{LG}=1nF; CT=470pF, R_{FSET}=12kΩ, T_J=-40°C ~ 125°C, Min & Max are guaranteed by characterization, typical is test under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Latch function (LATCH)						
Input bias current (V_{LATCH}=0 to V_{th})	I_{LATCH}				1	μA
LATCH threshold	V_{th}		1.72	1.85	1.95	V
Oscillator						
Output duty cycle	D	T_J=25C	48	50	52	%
		T_J=-40 ~ 125C	47	50	53	%
Oscillation frequency	f_{osc}	CT≤150pF, R_{FSET}≤2k			600	kHz
CT peak value	V_{CFp}			3.8		V
CT valley value	V_{CFv}			0.9		V
Voltage reference at FSET pin	V_{REF}		1.87	2	2.05	V
Dead-Time	t_{DMIN}	C_{HBVS}=5pF typically	180	235	290	ns
	t_{DMAX}			1		μs
	$t_{D\ float}$	HBVS pin floating	260	300	400	ns
Timer for CMP	$t_{D\text{-}CMP}$			52		μs
Half Bridge Voltage Sense(HBVS)						
Voltage clamp	$V_{HBVS\text{-}C}$			7.6		V
Minimum voltage change rate can be detected	dv_{min}/dt	C_{HBVS}=5pF typically			180	V/μs
Turn on delay	Td	Slope finish to turn on delay		100		ns
Soft start function (SS)						
Discharge resistance	R_d	V_{CS}>V_{CSx}		130		Ω
Standby function (Burst)						
Disable threshold	V_{th}		1.17	1.23	1.28	V
Hysteresis	V_{hys}		30		150	mV
Delayed shutdown (TIMER)						
Charge current	I_{CHARGE}	V_{TIMER}=1V, V_{CS}=0.85V T_J=25C	80	130	180	μA
Threshold for forced operation at maximum frequency	V_{th1}		1.80	2	2.10	V
Shut down threshold	V_{th2}		3.2	3.5	3.7	V
Restart threshold	V_{th3}		0.21	0.28	0.35	V
Low-side gate driver (LG, referenced to GND)						
Peak source current (5)	$I_{sourcepk}$			0.75		A
Peak sink current (5)	I_{sinkpk}			0.87		A
Sourcing resistor	R_{source}	LG_R@Isrc=0.1A		4		Ω
Sinking resistor	R_{sink}	LG_R@Isnk=0.1A		2		Ω
Fall time	t_f			30		ns

ELECTRICAL CHARACTERISTICS *(continued)*

VCC=13V, C_{HG}=C_{LG}=1nF; CT=470pF, R_{FSET}=12kΩ, T_J=-40°C ~ 125°C, Min & Max are guaranteed by characterization, typical is test under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Rise time	t_r			30		ns
UVLO saturation		VCC=0 to VCC_H, I_{sink}=2mA			1	V
High side gate driver (HG, referenced to SW)						
Peak source current (5)	$I_{sourcepk}$			0.74		A
Peak sink current (5)	I_{sinkpk}			0.87		A
Sourcing resistor	R_{source}	HG_R@Isrc=0.01A		4		Ω
Sinking resistor	R_{sink}	HG_R@Isnk=0.01A		2		Ω
Fall time	t_f			30		ns
Rise time	t_r			30		ns
Thermal Shutdown						
Thermal shutdown threshold(5)				150		°C
Thermal shutdown recovery threshold(5)				120		°C

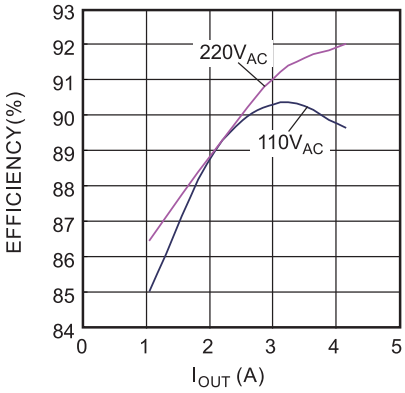
Notes:

5) Guaranteed by design

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

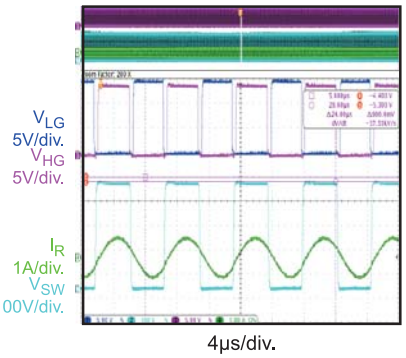
Performance waveforms are generated using the evaluation board built with design example on page 22, VAC=120V, V_{out}=24V, I_{out}=4.16A, T_A=25°C, unless otherwise noted.

Efficiency



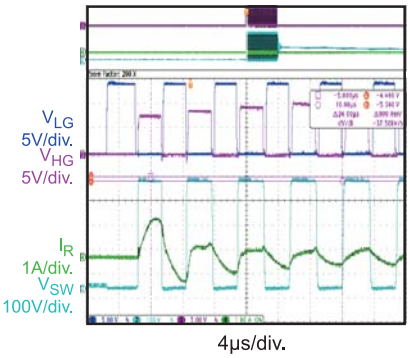
Steady State

V_{OUT}=24V, I_{OUT}=4.16A



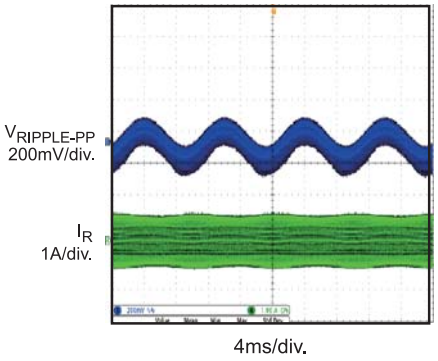
Steady State

V_{OUT}=24V, I_{OUT}=0A



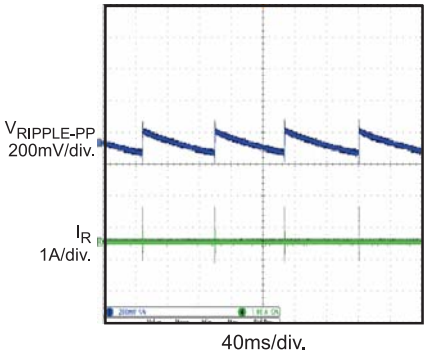
Steady State

V_{OUT}=24V, I_{OUT}=4.16A



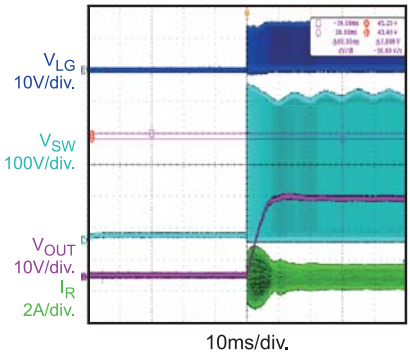
Steady State

V_{OUT}=24V, I_{OUT}=0A



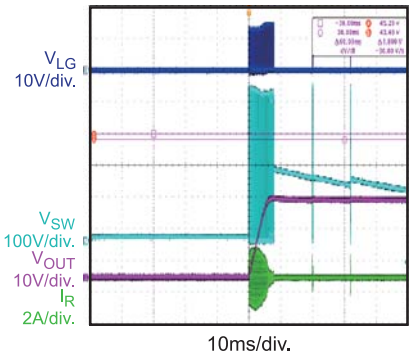
Start-Up

V_{OUT}=24V, I_{OUT}=4.16A



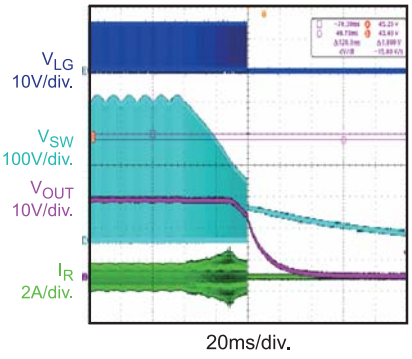
Start-Up

V_{OUT}=24V, I_{OUT}=0A



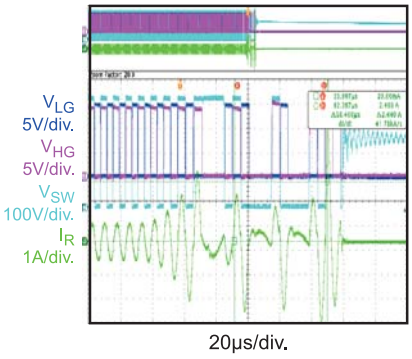
Shut-Down

V_{OUT}=24V, I_{OUT}=4.16A



Capacitive Mode Protection

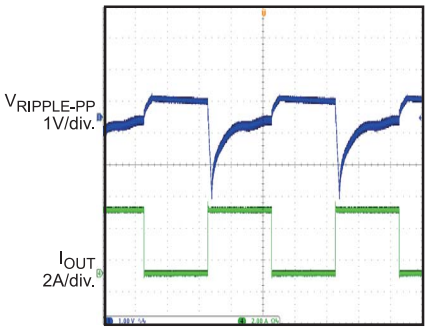
V_{OUT} Short



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

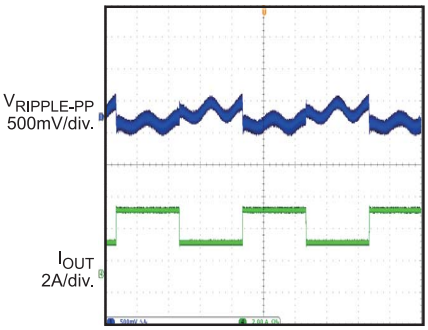
Performance waveforms are generated using the evaluation board built with design example on page 22, VAC=120V, V_{out}=24V, I_{out}=4.16A, T_A=25°C, unless otherwise noted.

Transient
2.08A to 4.16A



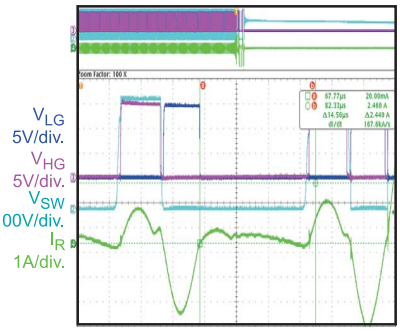
10ms/div.

Transient
2.08A to 4.16A



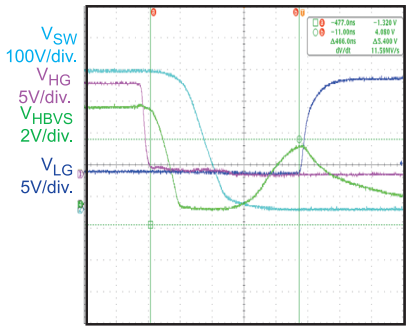
10ms/div.

Capacitive Mode Protection
V_{OUT} Short



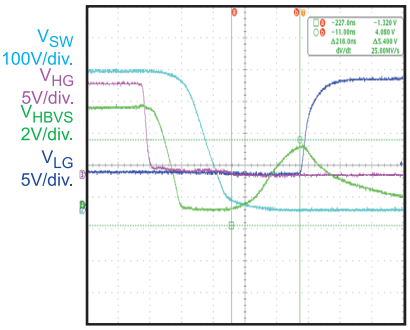
4µs/div.

Dead Time when HG Turns off



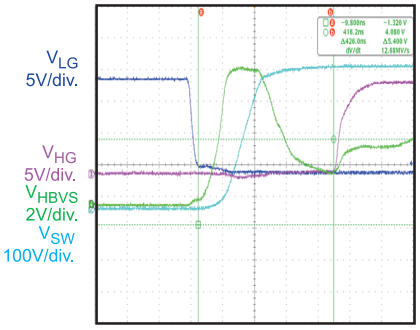
100ns/div.

Delay Time when HG Turns off



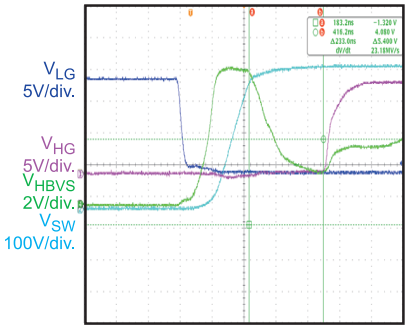
100ns/div.

Dead Time when LG Turns off



100ns/div..

Delay Time when LG Turns off



100ns/div.

PIN FUNCTIONS

Pin #	Name	Description
1	SS	Soft-start. Connect an external capacitor with from pin to GND and a resistor to FSET pin to set the maximum oscillator frequency and the time constant for the frequency shift during start-up. An internal switch discharges the capacitor when the chip turns off (VCC < UVLO, BO < 1.81V or > 5.5V, LATCH > 1.85V, CS >1.5V, TIMER > 2V, thermal shutdown) to guarantee soft-start.
2	TIMER	Period between over-current and shutdown. Connect a capacitor and a resistor from this pin to GND to set both the maximum duration from an over-current condition before the IC stops switching, and the delay before the IC resumes switching. Each time the CS voltage exceeds 0.8V, an internal 130μA source charges the capacitor; an external resistor slowly discharges this capacitor. If the pin voltage reaches 2V, the soft-start capacitor discharges completely, raising its switching frequency to its maximum value. The 130μA source remains on. When the voltage exceeds 3.5V the IC stops switching and the internal current source turns off, and the pin voltage decays. The IC enters soft-start when the voltage drops below 0.3V. This converter works intermittently with very low average input power under short-circuit conditions.
3	CT	Time-Set. An internal current source programmed by an external network connected to FSET charges and discharges a capacitor connected to GND. This determines the converter's switching frequency.
4	FSET	Switching Frequency Set. Provides a precise 2V reference. A resistor connected from this pin to GND defines a current that sets the minimum oscillator frequency. Connect the phototransistor of an opto-coupler to this pin through a resistor to close the feedback loop that modulates the oscillator frequency to regulate the converter's output voltage. The value of this resistor will set the maximum operating frequency. An R-C series connected from this pin to GND sets frequency shift at start-up to prevent excessive inrush energy.
5	BURST	Burst-Mode Operation Threshold. The pin senses the voltage related to the feedback control, which is compared to an internal reference (1.25V). When BURST voltage is lower than this reference, the IC enters an idle state and reduces its quiescent current. When the feedback drives BURST above 1.35V (100mV hysteresis), the chip resumes switching. Soft-start is not invoked. This function enables burst-mode operation when the load falls below a programmed level, determined by connecting an appropriate resistor to the opto-coupler to FSET (see block diagram). Connect BURST to FSET if burst-mode is not used.
6	CS	Current Sense of Half-bridge. Uses a sense resistor or a capacitive divider to sense the primary current, this pin has multiple function as following: **1. Over Current Regulate:** As the voltage exceeds a 0.8V threshold (with 50mV hysteresis), the soft-start capacitor on pin 1 discharges internally: The frequency increases, limiting the power throughput. Under an output short circuit, this normally results in a nearly-constant peak-primary current. TIMER limits the duration of this condition. **2. Over Current Protection:** If the current continues to build up despite the frequency increase, when Vcs>1.5V, OCP is triggered in Latch mode: requiring cycling the IC supply voltage to restart: The latch is removed as the VCC voltage drops below the UVLO threshold. **3. Capacitive Mode Protection**: At the moment of LG turns off, CS compares with V_{CSNR} CMP threshold, if CS> V_{CSNR}, it blocks HG gate turn-on until slope is detected or the CMP timer is complete. At the moment of HG turns off, CS compares with V_{CSPR} CMP threshold, if CSHB< V_{CSPR}, it block the LS gate turn-on until slope is detected or the CMP timer is complete. Connect the pin to GND if the function is not used.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
7	BO	This pin sensing the input voltage and provide brown out and brown in protection. If the pin voltage is larger than 2.3v, then IC enable the gate driver. And if the pin voltage is below 1.9V, then disable the IC.
8	LATCH	IC Latch Off. When LATCH exceeds 1.85V, the IC shuts down and lowers its bias current to its near pre-start-up level. LATCH is reset when VCC voltage discharges below its UVLO threshold. Connect LATCH to GND if not used.
9	HBVS	Half bridge dv/dt sense. In order to detect the dv/dt of the half-bridge, a high voltage capacitor is connected between SW and HBVS, The dv/dt current through this HVBS is used to adaptively adjust the dead-time between high side gate and low side gate.
10	GND	Ground. Current return for both the low-side gate-driver and the IC bias. Connect all external ground connections with a trace to this pin; one for signals and a second for pulsed current returns.
11	LG	Low-Side Gate Driver output. The driver is capable of 0.8A source/sink peak current to drive the lower MOSFET of the half-bridge. The pin is pulled to GND during UVLO.
12	VCC	Supply Voltage. Supplies both the IC bias and the low-side gate driver. A small bypass capacitor (e.g., 0.1μF) can help provide a clean bias voltage for the IC signal.
13	N.C.	High-Voltage Spacer. Not internally connected—isolates the high-voltage pin and eases compliance with safety regulations (creepage-distance) on the PCB.
14	SW	High-Side Switch Source. Current return for the high-side gate-drive current. Requires careful layout to avoid large spikes below ground.
15	HG	High-Side Floating Gate-Driver output. Capable 0.8A source/sink peak current to drive the upper MOSFET of the half-bridge. An internal resistor connected to SW ensures that the pin does not float during UVLO.
16	BST	Bias for Floating Voltage Supply, High-Side Gate Driver. Connect a bootstrap capacitor between this pin and SW. This capacitor is charged by an internal bootstrap diode driven in-phase with the low-side gate-drive.

FUNCTIONAL BLOCK DIAGRAM

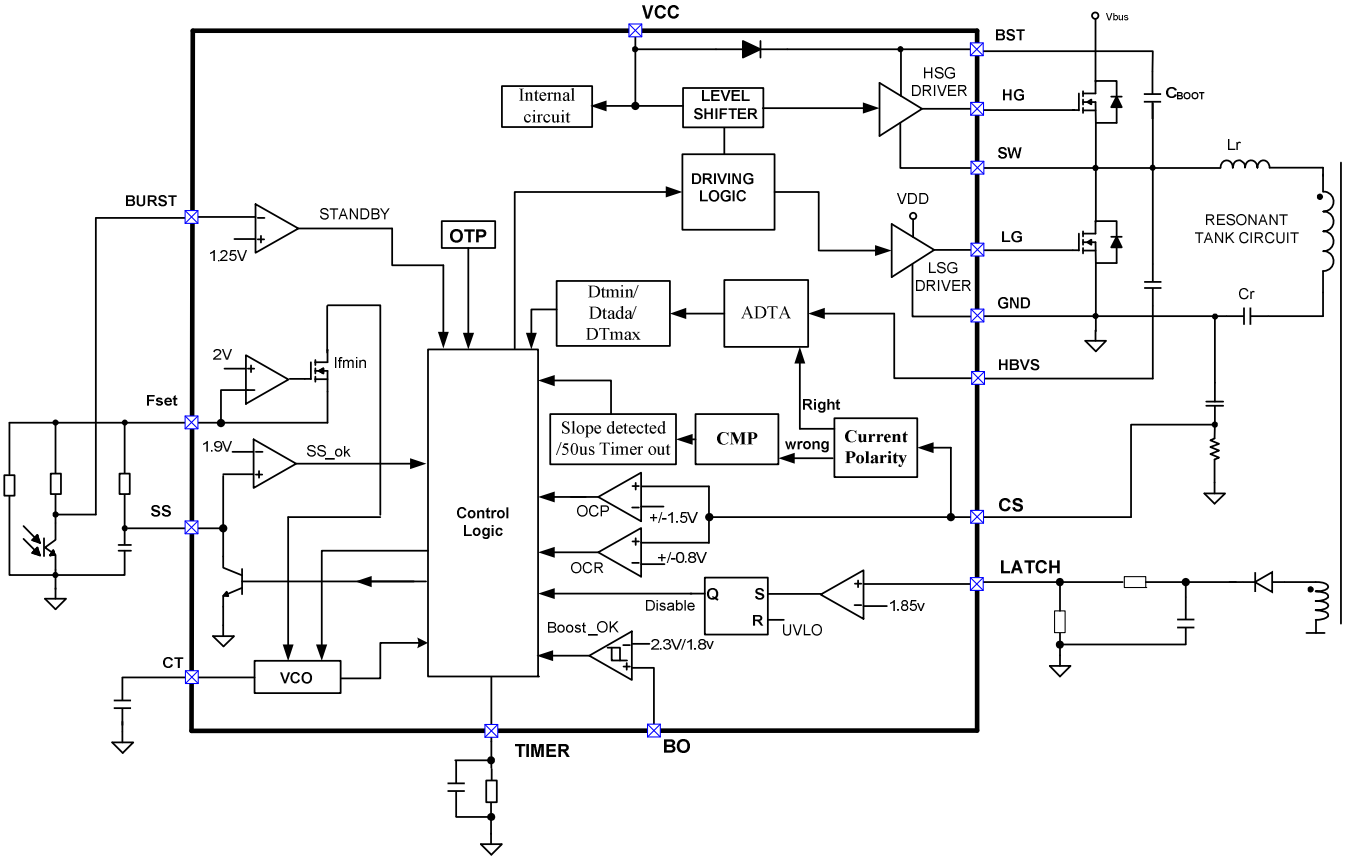


Figure 1: Block Diagram

APPLICATION INFORMATION

Oscillator

Figure 2 shows the block diagram of the oscillator. A modulated current repeatedly charges and discharges the CT capacitor between its peak valley thresholds which determines the oscillator frequency.

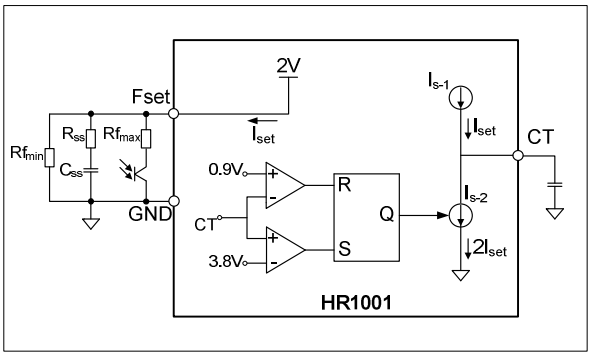


Figure 2: Oscillator Block Diagram

As can be seen by figure 2, FSET sets the CT charging current, Iset (I_{S-1}). When CT passes its peak threshold (3.8V), the latch is set and a discharge current source of twice the charge current is enabled. The difference of these two currents forces the charge and discharge of CT to be equal. When the voltage on the CT capacitor falls below its valley threshold (0.9V), the latch is reset, turning off I_{S-2}. This starts a new switching cycle. Figure 3 shows the detailed waveform of the oscillator.

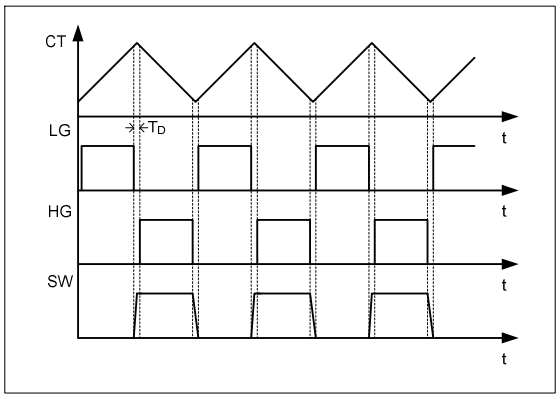


Figure 3: CT Waveform and Gate Signal

The RC network externally connected to FSET pin determines normal switching frequency as well as the soft start switching frequency.

1. Rf_{min} from FSET to GND contributes the maximum resistance of the external RC network when the phototransistor does not conduct. This sets the FSET minimum source current, which defines the minimum switching frequency
2. Under normal operation, the phototransistor adjusts the current flow through Rf_{max} to modulate the frequency for output voltage regulation. When the phototransistor is saturated, the current through Rf_{max} is at its maximum, setting the frequency at its maximum.
3. An RC in series connected between FSET and GND shifts the frequency at start-up. (Please see the soft-start section for details.)

Based on the above description, the following equations describe the minimum and maximum frequency:

$$f_{min} = \frac{1}{3 \cdot CT \cdot Rf_{min}}$$

$$f_{max} = \frac{1}{3 \cdot CT \cdot (Rf_{min} \,||\, Rf_{max})}$$

Typically, the CT capacitance is between 0.1nF and 1nF. The values of Rf_{min} and Rf_{max} are calculated by the following equations:

$$Rf_{min} = \frac{1}{3 \cdot CT \cdot f_{min}}$$

$$Rf_{max} = \frac{Rf_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

It is recommended to use a CT capacitor (<=330pF) for best overall temperature performance.

Soft-Start Operation

For the resonant half-bridge converter, the power delivered is inversely proportional its switching frequency. To ensure the converter starts or restarts with safe currents, the soft start forces a high initial switching frequency until the value is controlled by the closed loop.

The soft start is achieved using an external RC series circuit as shown in Figure 4.

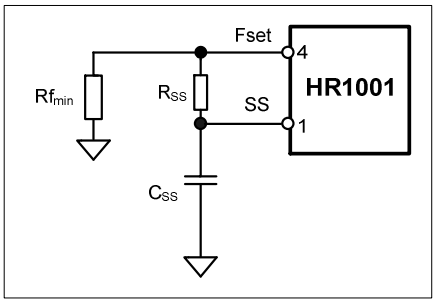


Figure 4: Soft-Start Block

When start-up begins, the SS voltage is 0V, so the soft-start resistor (R_{SS}) is in parallel to Rf_{min}: Rf_{ming} and R_{SS} determine the initial frequency as:

$$f_{start} = \frac{1}{3 \cdot CT \cdot (Rf_{min} || R_{ss})}$$

During start-up, the C_{SS} charges until its voltage reaches the reference (2V), and the current through R_{SS} decays to zero. This period takes about 5× (R_{SS}×C_{SS}). During this period, the switching frequency change follows an exponential curve: the C_{SS} charge initially reduces the frequency relatively quickly but the rate gradually decreases.

After this period ends, the output voltage is still not regulated, and the feedback loop will take over start-up.

With soft-start, the input current increases gradually until the output voltage is regulated.

Select the soft-start RC network using the equations below:

$$R_{ss} = \frac{Rf_{min}}{\frac{f_{start}}{f_{min}} - 1}$$

$$C_{ss} = \frac{3 \cdot 10^{-3}}{R_{ss}}$$

Select an initial frequency, f_{start}, at least $4 \times f_{min}$. Select C_{SS} as a trade-off between the desired soft-start operation and the OCP speed (see the next section for details).

Adaptive Dead-Time Adjustment

When operating in inductive mode, the soft switching of the power MOSFETs results in high efficiency of the resonant converter. A fixed dead time may result in hard switching at light load and much larger Lm. A dead time too long may lead to loss of ZVS, the current may change polarity during dead time, which results in capacitive mode switching. The adaptive dead-time control automatically adjusts the dead-time by detecting the dv/dt of half-bridge switch node (SW).

HR1001 incorporates an intelligent ADTA logic circuit, which detects SW's dv/dt and automatically inserts the proper dead time. The external circuit is quite simple, connecting a capacitor (5pF typically) between SW and HBVS to sense dv/dt. Figure 5 shows the simplified block diagram of ADTA and Figure 6 shows operation waveform of ADTA respectively.

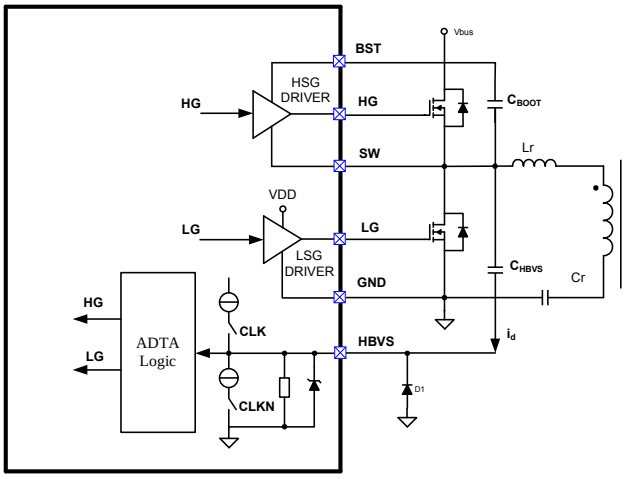


Figure 5: Block Diagram of ADTA

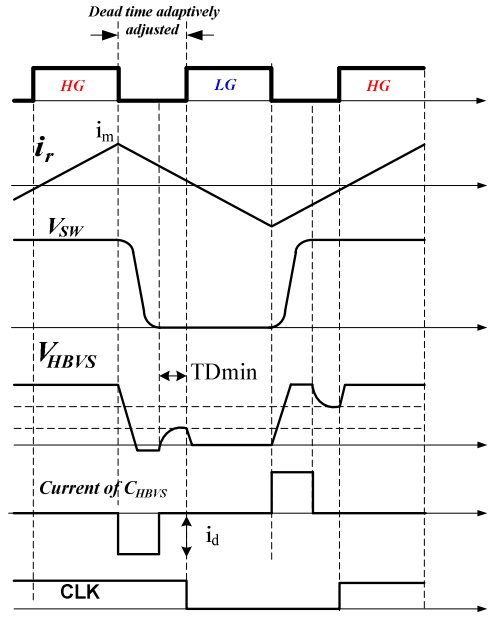


Figure 6: Operation waveform of ADTA

When HG switches off, SW voltage swings from high to low due to the resonant tank current *ir*, accordingly this negative dv/dt will pull current from HBVS via C_{HBVS}. HBVS will be pulled down by the dv/dt current from C_{HBVS}. If the dv/dt current is higher than the internal comparison current, then HBVS is pulled down clamped at zero. When SW stops slewing and the differential current stops, then HBVS starts to ramp up. LG turns on after a delay, which is the minimum dead time. The time duration of HG turn-off to LG turn-on is defined as the dead time.

When LG switches off, SW voltage swings from low to high, and a positive dv/dt current is detected via C_{HBVS}. The dead time between LG turn-off and HG turn-off is automatically maintained when sensing the dv/dt current.

To avoid damaging HBVS, care must be taken in selecting C_{HBVS}. to keep the dv/dt current lower than 65mA. Use the expression below to keep the current below 65mA.

$$i_d = \left| C_{HBVS} \frac{dv}{dt} \right| < 65mA$$

If C_{HBVS} is designed too low to sense the dv/dt, the minimum voltage change rate dvmin/dt must be accounted for to design the right C_{HBVS}.

First, calculate the peak magnetizing current I_m:

$$I_m = \frac{V_{in}}{8 \cdot L_m \cdot f_{max}}$$

Then, C_{HBVS} can be designed as:

$$C_{HBVS} > \frac{700uA}{I_m} \frac{C_{oss}}{2}$$

Where, C_{oss} is the output capacitance when Vds is near zero volts (user can refer to the Coss characteristics curve in MOSFET's datasheet). In a typical design, Lm=870uH, Vin=450Vdc, fsmax=140kHz, C_{HBVS} is calculated to be 4.5pF, indicating 5pF is suitable for most MOSFETs.

Figure 7 illustrates a possible dead time by ADTA logic. Note that there are three kinds possible dead time; minimum dead time (DTmin), Maximum dead time (DTmax), and adjusted dead time (DTadj), which is between TDmin and TDmax. ADTA logic sets a DT_{min}=235ns. When the SW's transition time is smaller than DTmin, the logic does not let the gate turn which guards against shoot-through between the low side and high side FETs. A maximum dead-time (DTmax=1us) forces the gate to turn on, preventing the lost of duty cycle or soft switching.

ADTA automatically adjusts the dead time and ensures ZVS. It enables more flexibility in MOSFET and Lm selection. It prevents hard switching if the design does not carefully account for light or no load. At light load switching frequency goes high and magnetizing current goes low, risking hard switching that can lead to a thermal or reliability issue.

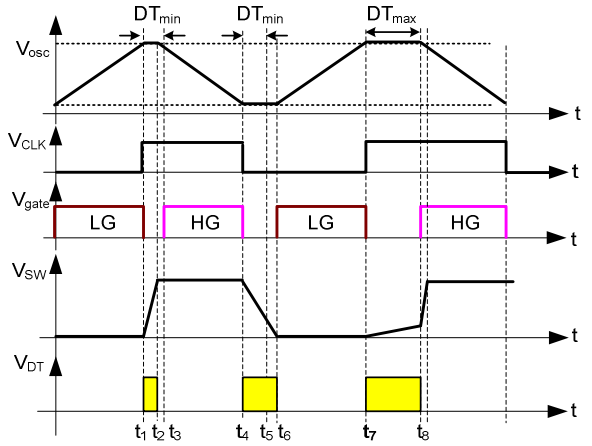


Figure 7: Dead Time Style in ADTA

If HBVS is not connected, the internal circuit never detects differential current from HBVS, keeping the dead time fixed at 300ns.

Figure 8 and Figure 9 show the waveforms of the dead time when HG turns off and when LG turns off respectively. ADTA logic automatically inserts the dead time according to the transition shape of SW.

If HBVS pin is pulled down too low from the negative current of C_{HBVS}, the dead time from HG turn-off to LG turn-on may be too long. In order to clamp HBVS at zero, and ensure optimum dead time, a SCHOTTKY diode D1, like BAT54, is strongly recommended connected on HBVS to GND.

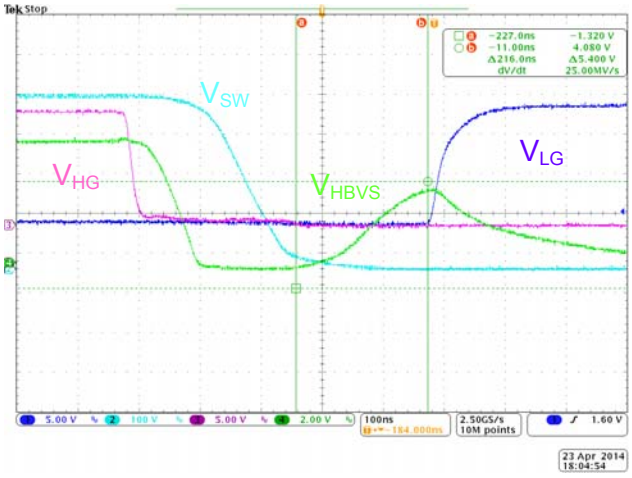


Figure 8: Dead Time at High-to-Low Transition

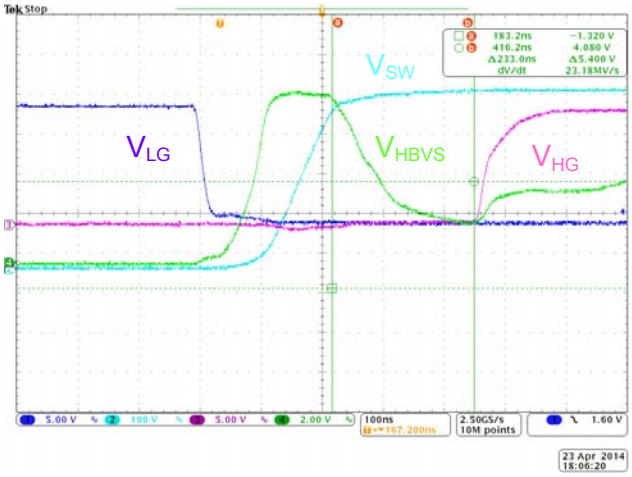


Figure 9: Dead Time at Low-to-High Transition

Capacitive Mode Protection.

When the resonant HB converter output is in over-load or short circuit, it may cause the converter to run into capacitive region. In capacitive mode, the voltage applied to resonant tank is lagging the current of the resonant tank. Under this condition, the body diode of the one MOSFET is conducting, and the turn-on of the other MOSFET should be prevented to avoid device failure.

The functional block diagram of CMP is shown in Figure 10.

Figure 11 shows the operating current principle of the capacitive mode protection. CSPOS and CSNEG stands for the current polarity, which is generated by comparing voltage of CS with internal V_{CSNR} and V_{CSPR} voltage reference.

At time t0 LG is turned off. CSNEG is high, which means the current is in the correct direction, operating in inductive mode.

At time t1, HG is turned off. CSPOS is high, which also means the current is in the correct direction, operating in inductive mode.

At time t2, it is the second instance of LG turning off. CSNEG is low, indicating the current is in the wrong direction (low side MOSFET body diode is conducting). This means the converter is operating in capacitive mode.

SW does not swing high until the current returns to the correct polarity. DT stays high and Vosc is stopped, preventing the other MOSFET from turning on. It effectively avoids capacitive switching.

At time t3, the current returns back to the correct polarity, and the other MOSFET turns on after the dv/dt is current detected.

Between times t2 to t5, the correct current polarity cannot be detected or the current is so little that it is unable to pull down or up SW.

Eventually, the timer (52us) for CMP expires, and the other MOSFET will be forced to switch on. As shown in dash line.

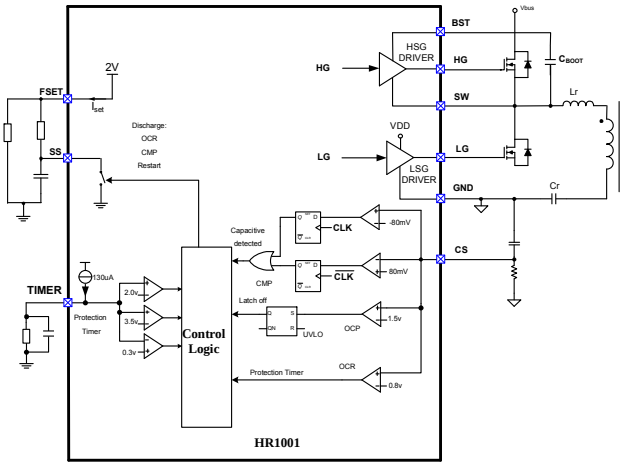


Figure 10: Block diagram of CMP and OCP

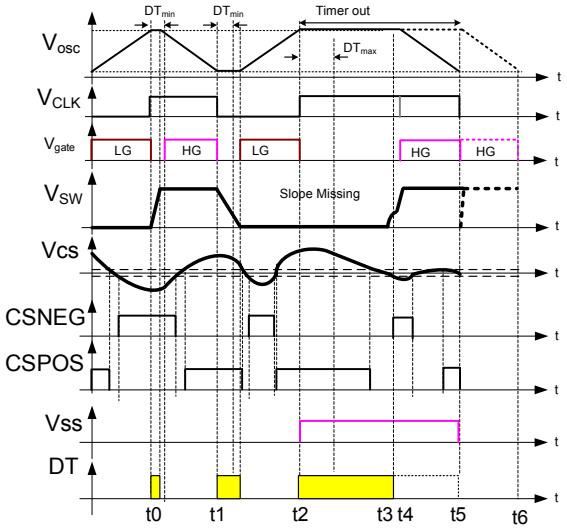


Figure 11: Operating Principle of CMP

When capacitive mode operation is detected, Vss-control signal goes high, turning on an internal MOSFET to discharge Css. This increases the frequency very high and quickly to limit output power. Vss-control is reset and softstart in activated when the first gate driver is switched off after CMP. The switching frequency will smoothly decrease until the control loop takes over.

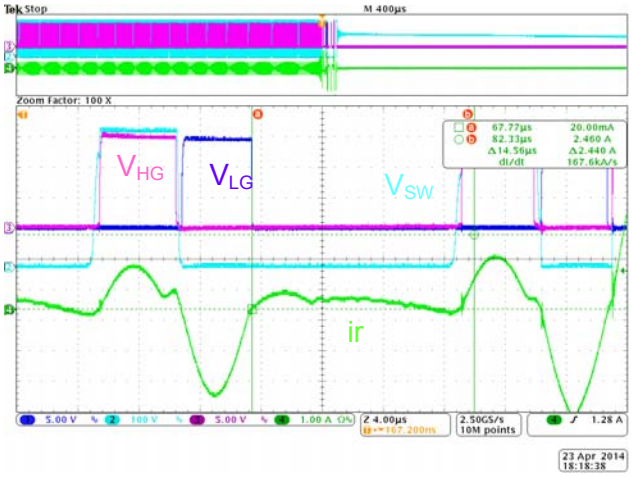


Figure 12: Capacitive Mode Protection Waveform

Figure 12 shows the CMP behavior when output is shorted. The current polarity goes wrong at the time when LG switches off, the CMP logic immediately detects this capacitive mode and prevents HG's turn-on. This avoids destructive capacitive switching. As soon as current ***ir*** goes to the right polarity, SW ramps up, dv/dt is detected, and HG turns on at ZVS condition.

Over Current Protection (OCP)

HR1001 provides a two levels over-current protection as is shown in the Figure 10.

1. The first level occurs when the voltage on CS exceeds 0.8V, two actions will take place.

First, the internal transistor connected between SS and GND turns on for at least 10us, which discharges C_{SS}. This creates a sharp increase in the oscillator frequency, reducing the energy transferred to the output.

Second, an internal 130μA current source turns on to charge C_{Timer}, ramping TIMER voltage.

If the CS voltage drops below 0.8v(10mv hysterisis) before TIMER reaches 2V, then Css is enabled and the charging of C_{TIMER} is stopped. The converter returns to normal operation.

t_{OC} is the time for the voltage on C_{Timer} to rise from 0V to 2V. It is a delay time for over current regulation. There is no simple relationship between t_{OC} and C_{Timer}. Select C_{Timer} based on experimental results (based on experiments: C_{Timer} may increase operating time by 100ms).

If CS voltage is still larger than 0.8V after the C_{Timer} rises to 2V , Css is discharged. At the same time, the internal 130uA continues to charge C_{TIMER} until the voltage of TIMER reaches 3.5v, and turns off all gate drivers.

The time that TIMER voltage rises from 2v to 3.5v is approximately:

$$t_{OP} = 10^4 \cdot C_{Timer}$$

The above condition continues until TIMER voltage decreases to 0.3V due to R_{Timer} slowly discharging C_{Timer} at which time the IC restarts. This time period is:

$$t_{OFF} = R_{Timer} \cdot C_{Timer} \cdot \ln\frac{3.5}{0.3} \approx 2.5 R_{Timer} \cdot C_{Timer}$$

2. The second level over-current protection triggers when the CS voltage rises to 1.5V. This condition normally happens when the CS voltage continues to rise during a short circuit. The IC stops switching immediately and latches off until Vcc drops below UVLO.

The operation's time sequence of OCP is shown in the Figure 13. OCP limits the energy transferred from the primary to the secondary during an over-load or short-circuit condition. Excessive power consumption due to high continuous currents can damage the secondary-side windings and the rectifiers. The TIMER provides additional protection to reduce the average power consumption: When OCP triggers, the converter enters a hiccup-like protection mode that operates intermittently.

Refer to below timing for above procedure.

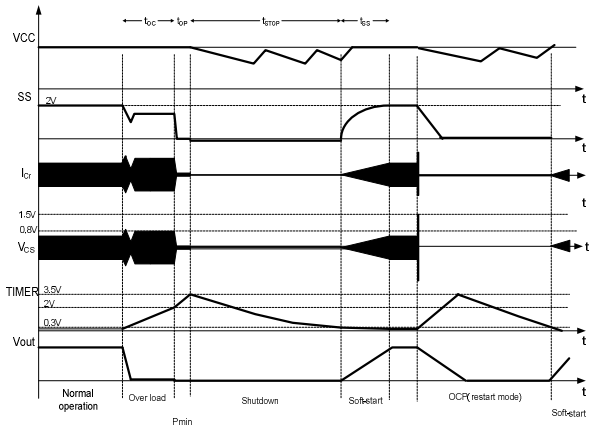


Figure 13: OCP Timing Sequence

Current Sensing

There are two current sensing methods:

Generally, lossless current sensing solution is commonly used in high power application, As shown in Figure14.

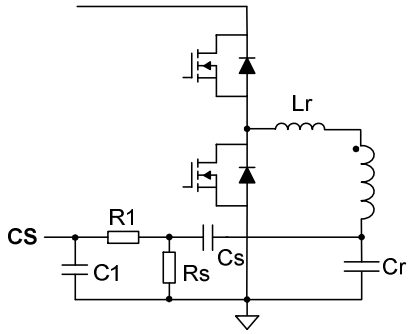


Figure 14: Current Sensing with Lossless Network

To design the lossless current sensing network, Use the equations below:

$$Cs \le \frac{Cr}{100}$$

To avoid triggering the capacitive detection threshold V_{CSNR} or V_{CSNR} , Rs should fulfill the condition below:

$$R_S > \frac{85mV}{I_m}(1+\frac{C_r}{C_S})$$

In addition, Rs must be lower than the equation below:

$$Rs < \frac{0.8}{I_{Crpk}} \cdot (1+\frac{C_r}{C_S})$$

I_{Crpk} is the peak current of the resonant tank at low input voltage and full load which is expressed as:

$$I_{Crpk} = \sqrt{(\frac{NV_O f_s}{4L_m})^2 + (\frac{I_O \pi}{2N})^2}$$

Where, N is the turns ratio of the transformer, Io and Vo is the output current and voltage, fs is the switching frequency, and Lm is the magnetizing inductance.

R1 and C1 network is used to attenuate switching noise on CS. The time constant should be in the range of 100ns.

An alternate solution uses a sense resistor in series with the resonant tank, as shown in the Figure15. This method is simple but causes unnecessary power loss on the sense resistor.

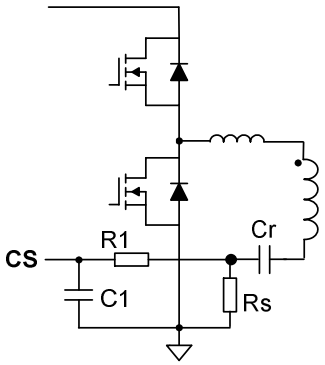


Figure 15: Current Sensing with a Sense Resistor

Design the sense resistor from follow the equation:

$$R_S = \frac{0.8}{I_{Crpk}}$$

Input Voltage Sensing (BI/BO)

The HR1001 stops switching when the input voltage drops below a specified value, and restarts when the input voltage goes back to normal. This function guarantees that the resonant half-bridge converter always operates within the specified input voltage range. The IC senses voltage on BO through the tap of a resistor divider connected to the rectified AC voltage or the PFC output.

Figure 16 shows the line-sensing internal block diagram.

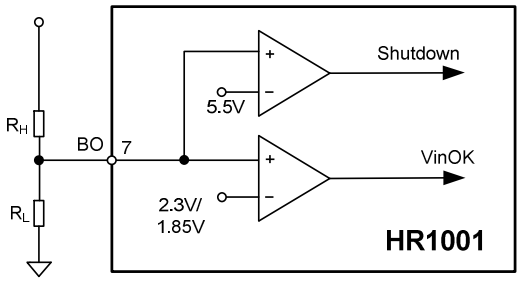


Figure 16: Input Voltage Sensing Block

If the BO voltage is higher than 2.3V, then the IC provides gate driver output; the IC won't shut down the gate driver until the BO voltage drops below 1.81V.

First, select a value for R_H large enough to reduce power loss at no load. Then R_L is calculated by:

$$R_L = R_H \cdot \frac{1.81}{V_{IN\text{-}min} - 1.81}$$

For additional protection, when the BO voltage exceeds the internal 5.5V clamp voltage, the IC shuts down. When the BO voltage is between 2.3 V and 5.5V, the IC operates normally.

Burst-Mode Operation

Under light-load or in the absence of a load, the maximum frequency limits the resonant half-bridge switching frequency. To control the output voltage and limit power consumption, the HR1001 enables compatible converters to operate in burst-mode to greatly reduce the average switching frequency, thus reducing the average residual magnetizing current and the associated losses.

Operating in burst-mode requires setting BURST on the HR1001. If the voltage on the BURST drops below 1.25V, HR1001 will shut down the HG and LG gate drive outputs, leaving only the 2V reference voltage on FSET and SS to retain the previous state and minimize HR1001's power consumption. When the voltage on BURST exceeds 1.25V by 100mV, HR1001 resumes normal operation.

Based on the Burst-mode operating principle, the BURST voltage must connect to the feedback loop. Figure 17 shows a typical circuit, connecting the BURST to the feedback signal for narrow-input–voltage range applications:

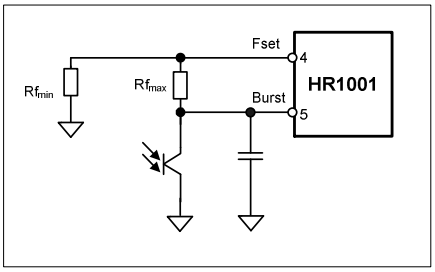


Figure 17: Bust-Mode Operation Set-Up

In addition to setting the oscillator maximum frequency at start up, Rf_{max} also determines the maximum burst-mode frequency. After confirming f_{max}, calculate Rf_{max} as below:

$$Rf_{max} = \frac{3}{8} \cdot \frac{Rf_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

Here, f_{max} corresponds to a load point, P_{Burst}, where the peak current flow through the transformer is too low to cause audible noise.

The above introduction is based on a narrow input voltage range. As a property of the resonant circuit, input voltage also determines the switching frequency. That means the P_{Burst} has a large variance over the wide input voltage range. To stabilize P_{Burst} over the input range, use the circuit in Figure 18 to insert the input voltage signal into feedback loop.

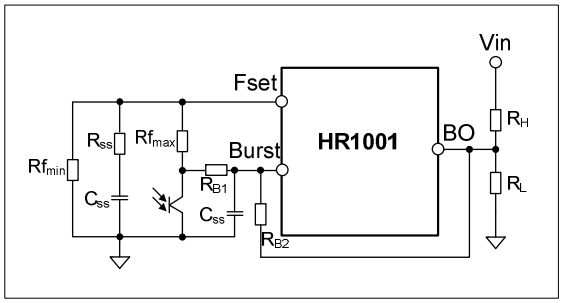


Figure 18: Bust-mode Operation Set-up for Wide Input Voltage Range

R_{B1} and R_{B2} from Figure 18 correct against the wide input voltage range. Select both resistors based on experimental results. Note that the total resistance of R_{B1} and R_{B2} should be much bigger than R_H to minimize the effect on BO voltage.During burst-mode operation, when the load is lower than P_{Burst}, the switching frequency is clamped at the maximum frequency. The output voltage must rise over the set value, which would increase the current flowing through the opto-coupler. Therefore, the voltage on Rf_{max} must rise due to the increased opto-transistor current. The BURST voltage would then drop below 1.25V, triggering the gate signal OFF state. Until the output voltage falls below the setting value, the current flow through opto-coupler then decreases, causing BURST voltage to rise. When the voltage exceeds 1.25V+100mV, the IC restarts to generate the gate signal. The IC will continue to operate in this mode under no-load or light-load to decrease average power consumption.

Latch Operation

The HR1001 provides a simple latch-off function through LATCH. Applying an external voltage over 1.85V causes the IC to enter a latched shutdown. After IC is latched, its consumption drops, as shown by the residual current in the EC table. Resetting the IC requires dropping the VCC voltage below the UVLO threshold.

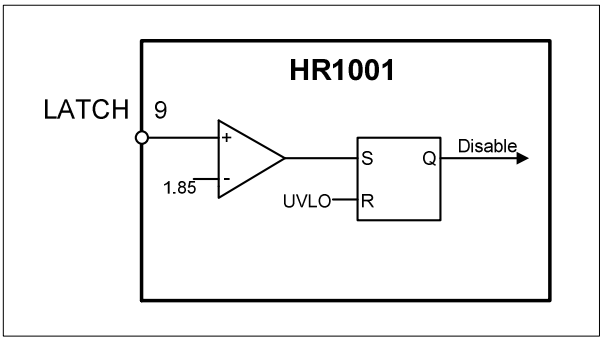


Figure 19: Latch Function Block

High-Side Gate Driver

The external BST capacitor provides energy to the high-side gate driver. An integrated bootstrap diode charges this capacitor through VCC. This diode simplifies the external driving circuit for the high-side switch, allowing the BST capacitor to charge when the low side MOSFET is on.

To provide enough gate driver energy and considering the BST capacitor charge time, use a 100nF-to-470nF capacitor for the BST capacitor.

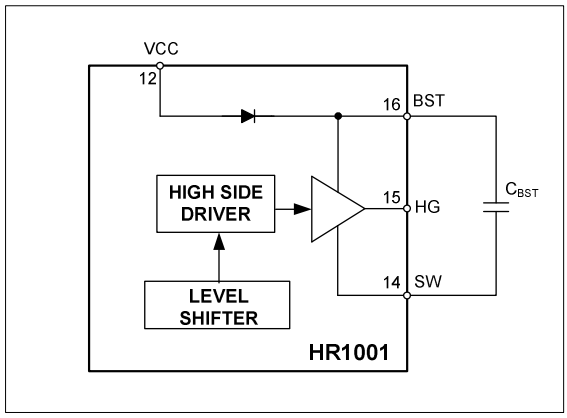


Figure 20: High-Side Gate Driver

Low-Side Gate Driver

LG provides the gate driver signal for the low-side MOSFET. The maximum absolute rating table shows that the maximum LG voltage is 16V. Under some conditions, a large voltage spike occurs on the LG due to oscillations from the long gate-driver wire, the MOSFET parasitic capacitance, and the small gate-driver resistor. This voltage spike is dangerous to the LG, so a 15V Zener diode close to the LG and GND pins is recommended..

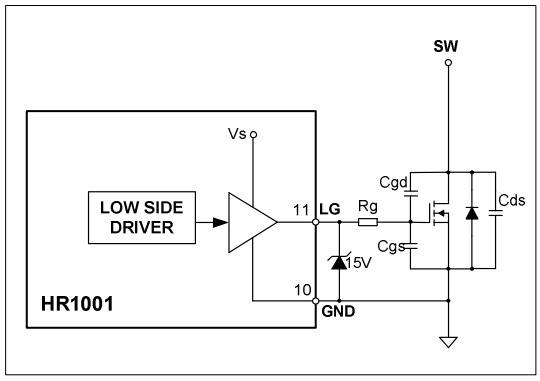


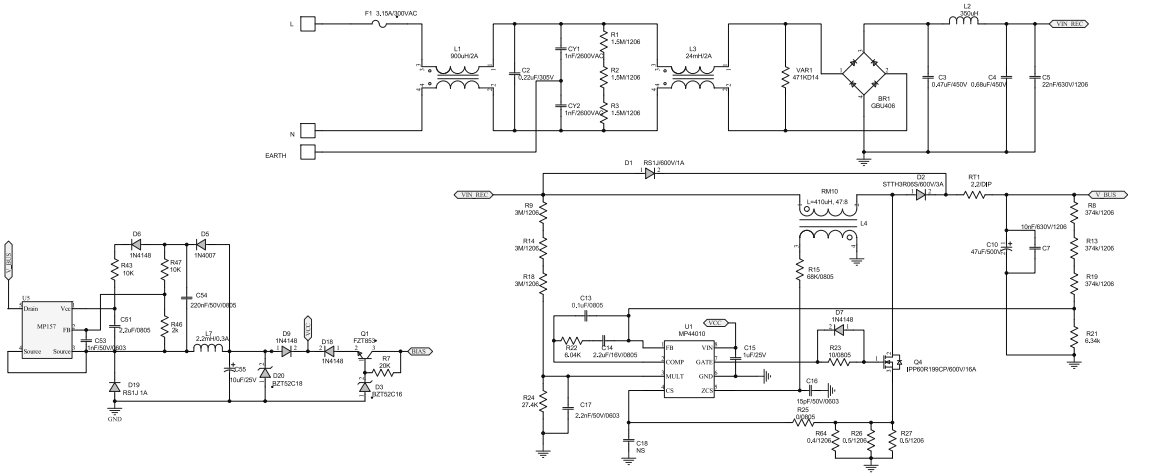
Figure 21: Low-Side Gate Driver

Design Example

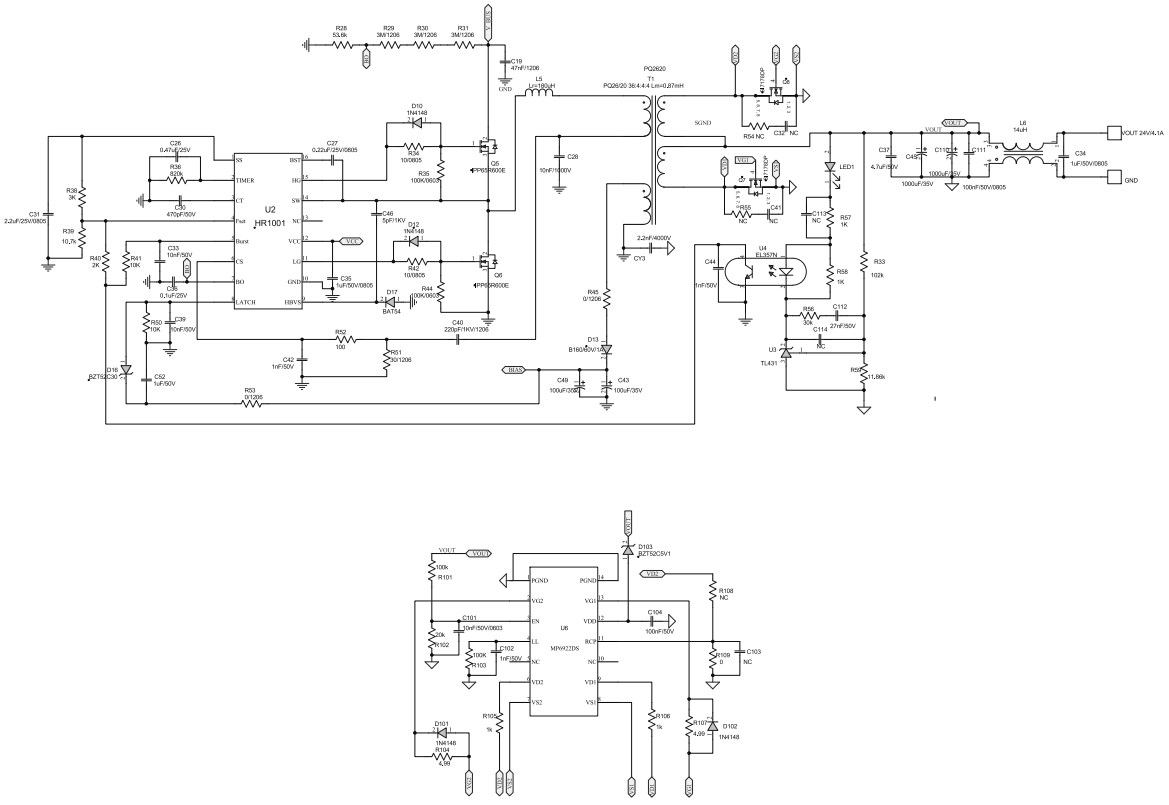
A 100W LED Driver is designed with below specifications:

Input AC voltage	90-305VAC
Output voltage	24V
Output current	4.16A

Figure Figure 22 shows the detailed application schematic. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section.



PFC Stage



LLC Stage

Figure 22: Design Example for 24V/4.16A Output

CONTROL FLOW CHARTS

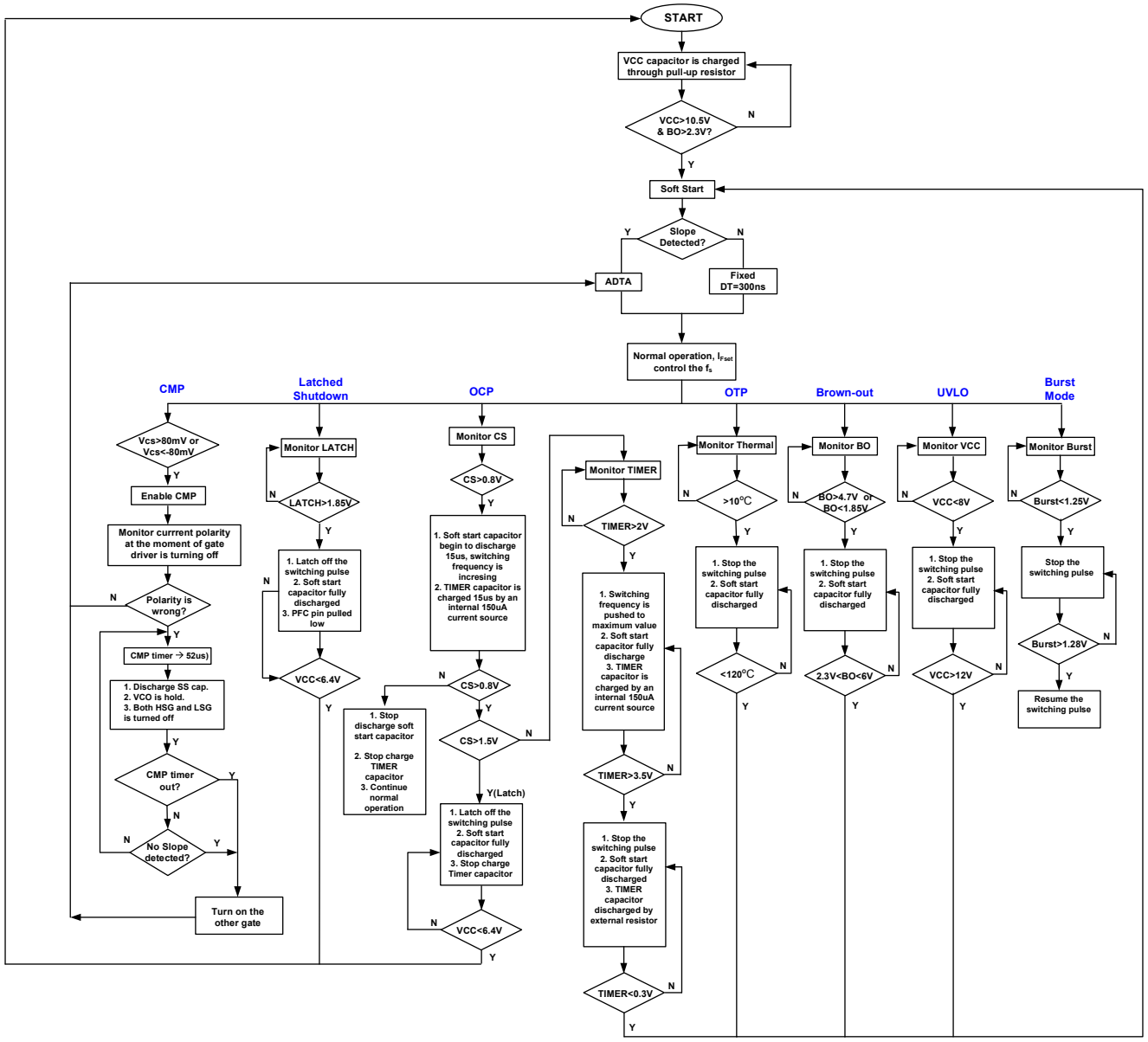


Figure.23: Control flow chart

TYPICAL APPLICATION CIRCUITS

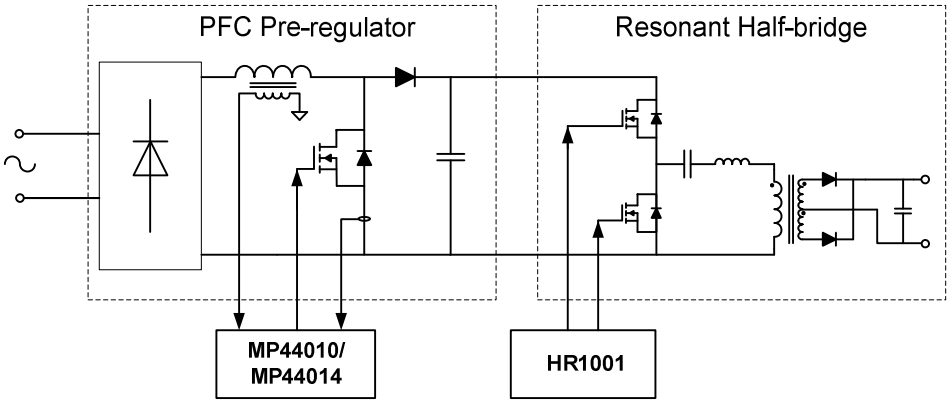
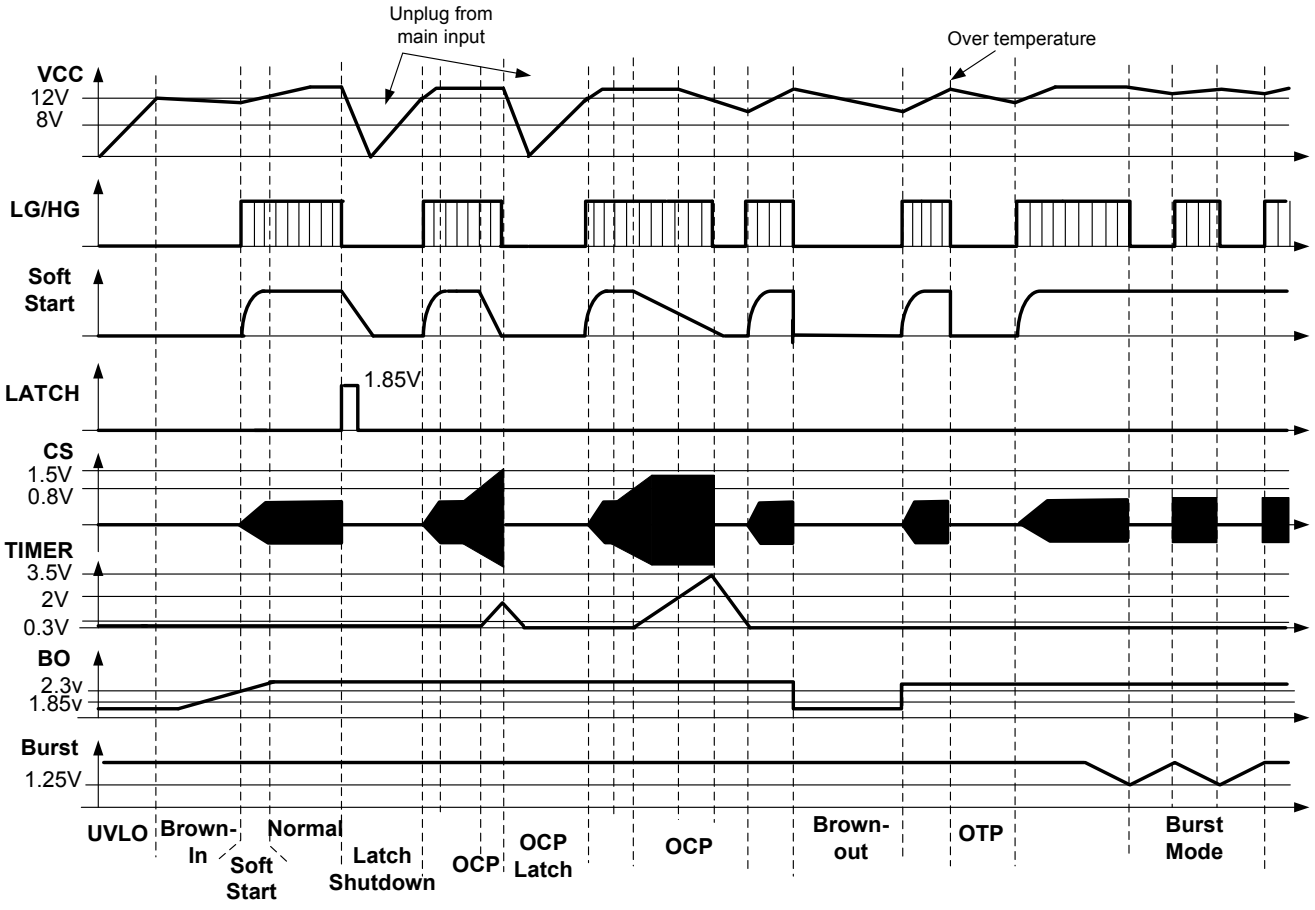


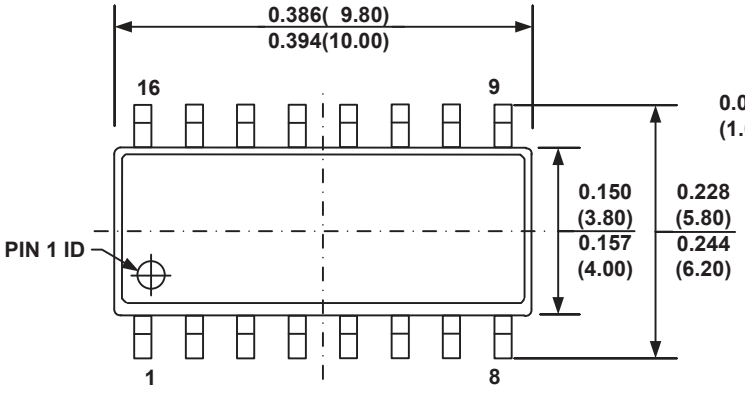
Figure 24: Application Circuit

SYSTEM TIMING

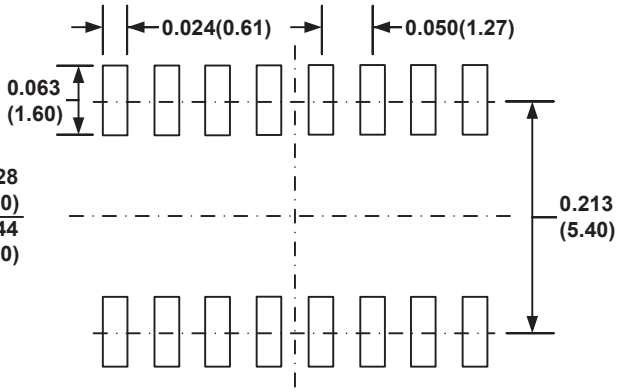


PACKAGE INFORMATIO

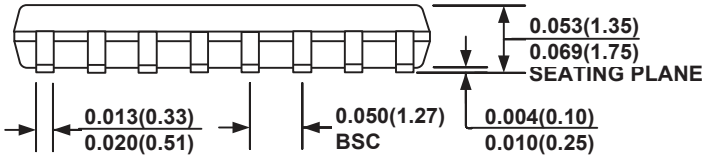
SOIC16



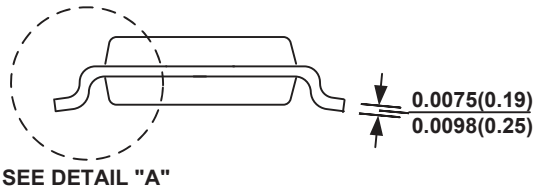
TOP VIEW



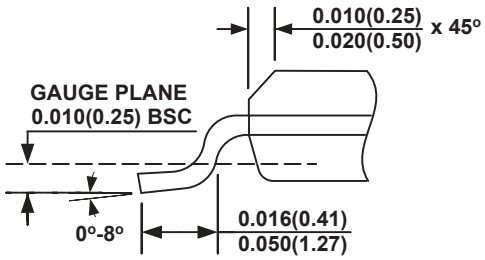
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.