MP2496M

2.5A, 36V, Frequency Selectable Step-Down Converter with Single USB Charging Port

DESCRIPTION

The MP2496M integrates a monolithic, step-down, switch-mode converter and a single USB current-limit switch with charging port identification circuits. It achieves 2.5A of continuous output current with excellent load and line regulation over a wide input supply range.

The output of the USB switch is current limited. The MP2496M provides a USB dedicated charging port (DCP) which supports battery charging specification 1.2 (BC1.2), divider mode, and 1.2V/1.2V mode without the need of outside user interaction. The output voltage has programmable line-drop compensation.

Full protection features include hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MP2496M requires a minimum number of readily available, standard, external components and is available in a QFN-26 (4mmx4mm) package.

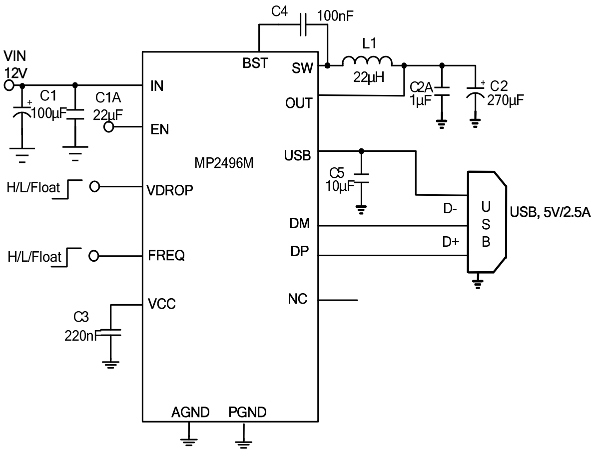
FEATURES

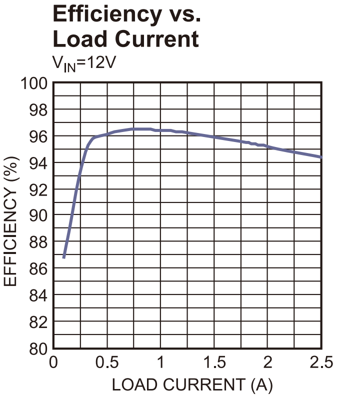
- EMI Reduction Technique
- Wide 7V to 36V Operating Input Voltage Range
- Fixed 5V Output Voltage with Line Drop Compensation
- Accurate USB Output Current Limit
- 40mΩ/32mΩ Low-$R_{DS(ON)}$ Internal Buck Power MOSFETs
- 24mΩ Low-$R_{DS(ON)}$ Internal USB Power MOSFET
- 350kHz/250kHz/150kHz Frequency Selectable
- Programmable Line Drop Compensation
- Output Over-Voltage Protection (OVP)
- Hiccup Current Limit
- Supports DCP Scheme for BC1.2, Divider Mode, and 1.2V/1.2V Mode
- ±8kV HBM ESD Rating for USB, DP, and DM
- Available in a QFN-26 (4mmx4mm) Package

APPLICATIONS

- USB Dedicated Charging Port (DCP)
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2496MGR	QFN-26 (4mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (eg. MP2496MGR–Z)

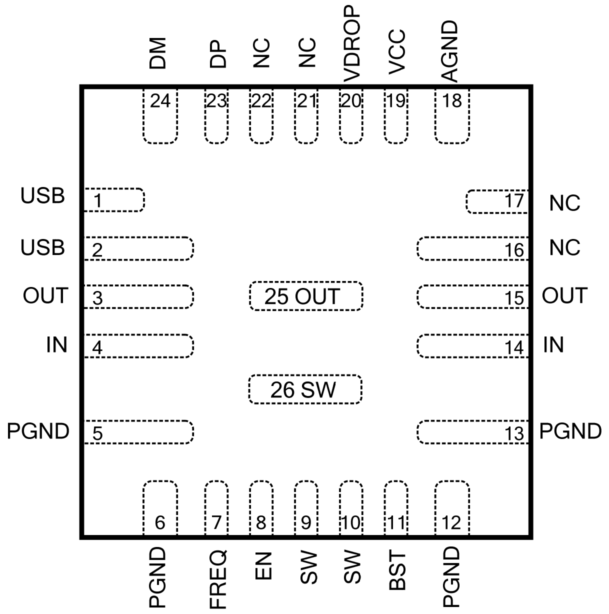
TOP MARKING

MPSYWW
M2496M
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M2496M: Product code
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-26 (4mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN})	40V
V_{SW}	-0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST}	V_{SW} + 6.5V
V_{EN}	-0.3V to 10V (2)
All other pins	-0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (3)	
QFN-26 (4mmx4mm)	2.8W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions (4)

Operation input voltage range	7V to 36V
Output current	2.5A for USB
Operating junction temp. (T_J)	-40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
QFN-26 (4mmx4mm)	44	9	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS MAX rating, please refer to the "Enable Control" section on page 11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C[6]. Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V,T_J = +25°C			1	μA
		V_{EN} = 0V,T_J = -40°C to +125°C			5	
Supply current (quiescent)	I_{Q_OL}	No switching		1.6	2.5	mA
EN rising threshold	V_{EN_Rising}		1.33	1.43	1.52	V
EN hysteresis	$V_{EN\_Falling}$		110	140	170	mV
EN input current	I_{EN}	V_{EN} = 2V, T_J = +25°C	1.1	1.8	2.5	μA
		V_{EN} = 2V,T_J = -40°C to +125°C	0.8	1.8	3	
		V_{EN} = 0V		0		
Thermal shutdown[7]	T_{STD}			165		°C
Thermal hysteresis[7]	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}		4.75	5.1	5.45	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 5mA		1	2	%
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}	T_J = +25°C	5.2	5.7	6.2	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			1		V
HS switch-on resistance	R_{DSON_HS}			40		mΩ
LS switch-on resistance	R_{DSON_LS}			32		mΩ
Output voltage	V_{OUT}	7V < V_{IN} < 36V, no load, T_J = +25°C	5	5.05	5.1	V
		7V < V_{IN} < 36V, no load, T_J = -40°C to +125°C	4.95	5.05	5.15	
Output over-voltage protection	V_{OVP_R}		5.65	6	6.4	V
OVP recovery	V_{OVP_F}	T_J = -40°C to +125°C	5.4	5.75	6.1	V
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = +25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = -40°C to +125°C			5	
Current limit[7]	I_{LIMIT}	Over 0-90% duty cycle	4			A
Oscillator frequency	f_{SW1}	FREQ = high, T_J = +25°C	310	350	410	kHz
		FREQ = high, T_J = -40°C to +125°C	300	350	420	
	f_{SW2}	FREQ = low, T_J = +25°C	220	250	300	
		FREQ = low, T_J = -40°C to +125°C	190	250	330	
	f_{SW3}	FREQ = float, T_J = +25°C	125	150	180	
		FREQ = float, T_J = -40°C to +125°C	110	150	185	
Maximum duty cycle	D_{MAX}	FREQ = 350kHz	84	88		%
Minimum on time[7]	T_{ON_MIN}	T_J = +25°C		130		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C$^{(6)}$. Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-start time	t_{SS}	Output from 10% to 90%, T_J = +25°C	1	1.65	2.3	ms
		Output from 10% to 90%, T_J = -40°C to +125°C	0.9	1.65	2.4	
USB Switch						
Under-voltage lockout threshold rising	V_{USB_UVR}	T_J = +25°C	3.8	4	4.3	V
		T_J = -40°C to +125°C	3.75	4	4.33	
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}		220	270	320	mV
Switch-on resistance	R_{DSON_SW}			24		mΩ
Current limit	I_{Limit}	T_J = +25°C	2.6	2.75	2.9	A
Line drop compensation	V_{DROP_COM1}	Max load 2.4A, V_{DROP} = float, T_J = +25°C	300	400	500	mV
	V_{DROP_COM2}	Max load 2.4A, V_{DROP} = high		280		mV
	V_{DROP_COM3}	Max load 2.4A, V_{DROP} = GND		130		mV
FREQ, VDROP high level	V_{HIGH}		V_{CC}-0.4V			V
FREQ, VDROP middle level	V_{MIDDLE}			2.5		V
FREQ, VDROP low level	V_{LOW}				0.4	V
V_{BUS} soft-start time	T_{SS}	V_{OUT} = 5V, from 10% to 90%, T_J = +25°C	1	1.6	2.2	ms
		V_{OUT} = 5V, from 10% to 90%, T_J = -40°C to +125°C	0.9	1.6	2.4	
Discharge resistance	R_{DCHG}	T_J = +25°C		50	70	Ω
		T_J = -40°C to +125°C		50	75	
On time of hiccup mode	T_{HICP_ON1}	V_{OUT} = 5V, V_{BUS} connected to GND		3$^{(7)}$		ms
	T_{HICP_ON2}	V_{OUT} = 5V, V_{BUS} > 2V, OC T_J = +25°C	3.5	5	6.5	
		V_{OUT} = 5V, V_{BUS} > 2V, OC T_J = -40°C to +125°C	3	5	7	
Off time of hiccup mode	T_{HICP_OFF}	V_{OUT} = 5V, V_{BUS} connected to GND, T_J = +25°C	6.5	8.5	10.5	s
		V_{OUT} = 5V, V_{BUS} connected to GND, T_J = -40°C to +125°C	6	8.5	11	
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = +25°C		125	155	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +125°C		125	160	
Divider Mode						
DP/DM output voltage	$V_{DP/DM\_Divider}$	V_{OUT} = 5V, T_J = +25°C	2.54	2.7	2.82	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	2.5	2.7	2.85	
DP/DM output impedance	$R_{DP/DM\_Divider}$	T_J = +25°C	20	22	23	kΩ
		T_J = -40°C to +125°C	18	22	28	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C(6). Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V, T_J = +25°C	1.16	1.25	1.34	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	1.15	1.25	1.35	
DP/DM output impedance	$R_{DP/DM\_1.2V}$	T_J = +25°C	60	68	75	kΩ
		T_J = -40°C to +125°C	55	68	88	

NOTES:

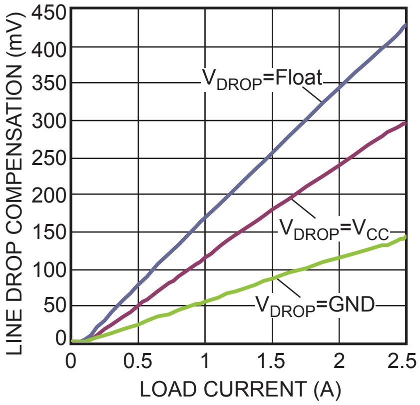
6) All min/max parameters are tested at T_J = 25°C. Limits over temperature are guaranteed by design, characterization, and correlation.

7) Guaranteed by design.

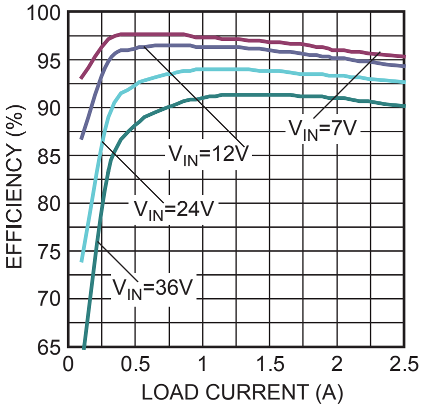
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 22μH, f_S = 250kHz, T_A = 25°C, unless otherwise noted.

Line Drop Compensation vs. Load Current



Efficiency vs. Load Current

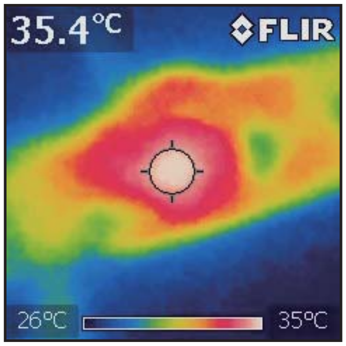


Thermal Test

2 Layer PCB, 4.78cm x 1.38cm

T_A=25°C, No Airflow

V_{IN}=12V, USB_I_{OUT}=1.1A

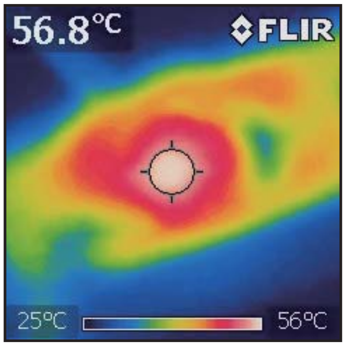


Thermal Test

2 Layer PCB, 4.78cm x 1.38cm

T_A=25°C, No Airflow

V_{IN}=12V, USB_I_{OUT}=2.5A

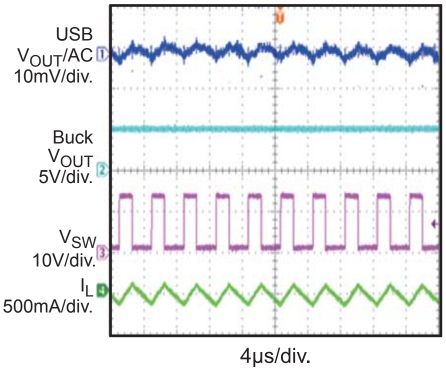


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 22µH, f_S = 250kHz, T_A = 25°C, unless otherwise noted.

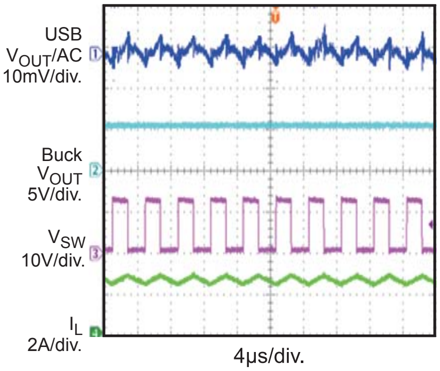
Output Ripple

V_{IN} = 12V, USB_I_{OUT} = 0A



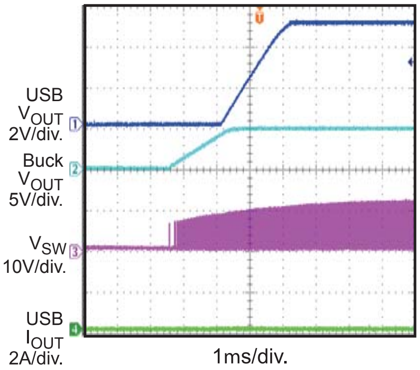
Output Ripple

V_{IN} = 12V, USB_I_{OUT} = 2.5A



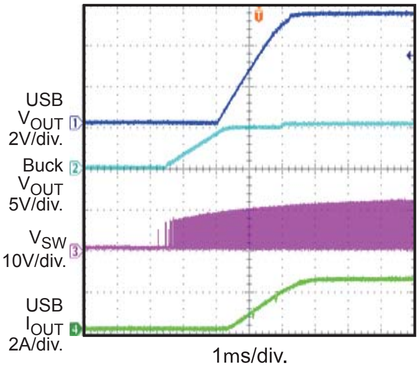
Power Start-Up

V_{IN} = 12V, USB_I_{OUT} = 0A



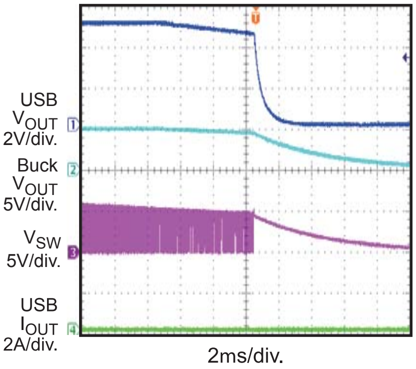
Power Start-Up

V_{IN} = 12V, USB_I_{OUT} = 2.5A,
CRL Load



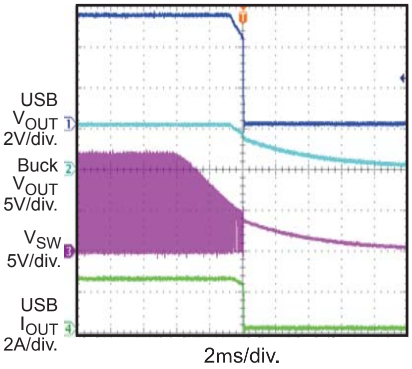
Power Shutdown

V_{IN} = 12V, USB_I_{OUT} = 0A

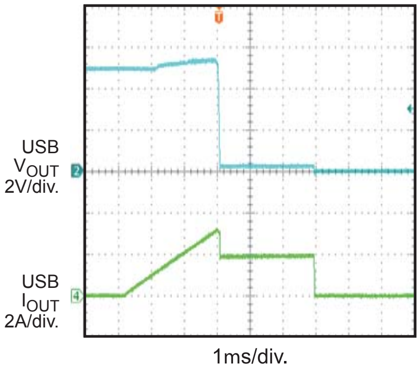


Power Shutdown

V_{IN} = 12V, USB_I_{OUT} = 2.5A,
CRL Load



USB Over-Current Protection



PIN FUNCTIONS

QFN-26 Pin #	Name	Description
1, 2	USB	**USB output.**
3, 15, 25	OUT	**Buck output.** OUT is the USB's power input. Internal circuits sense the OUT voltage and regulate it to 5V.
4, 14	IN	**Supply voltage.** The MP2496M operates on a 7V to 36V input voltage. C_{IN} is needed to prevent large voltage spikes at the input. Place C_{IN} as close to the IC as possible. IN is the drain of the internal power device and the power supply for the whole chip.
5, 6, 12, 13	PGND	**Power ground.** PGND is the reference ground of the regulated output voltage. PGND requires extra care during PCB layout. Connect to GND with copper traces and vias.
7	FREQ	**Frequency selection.** Float FREQ to set the frequency to 150kHz. Pull FREQ to ground to set the frequency to 250kHz. Pull FREQ to high to set the frequency to 350kHz.
8	EN	**On/Off control input.**
9, 10, 26	SW	**Switch output.** Connect using a wide PCB trace.
11	BST	**Bootstrap.** Requires a 0.1μF capacitor between SW and BST to form a floating supply across the high-side switch driver.
16, 17	NC	**No connection.** NC can be connected to OUT for better thermal dissipation.
18	AGND	**Analog ground.** Connect AGND to PGND.
19	VCC	**Internal 5V LDO regulator output.** Decouple VCC with a 0.22μF capacitor.
20	VDROP	**Line drop compensation selection.** Refer to the EC table for detailed specifications.
21, 22	NC	**No connection.** NC must be left floating.
23	DP	**D+ data line to the USB connector.** Input/output used for handshaking with portable devices.
24	DM	**D- data line to the USB connector.** Input/output used for handshaking with portable devices.

FUNCTIONAL BLOCK DIAGRAM

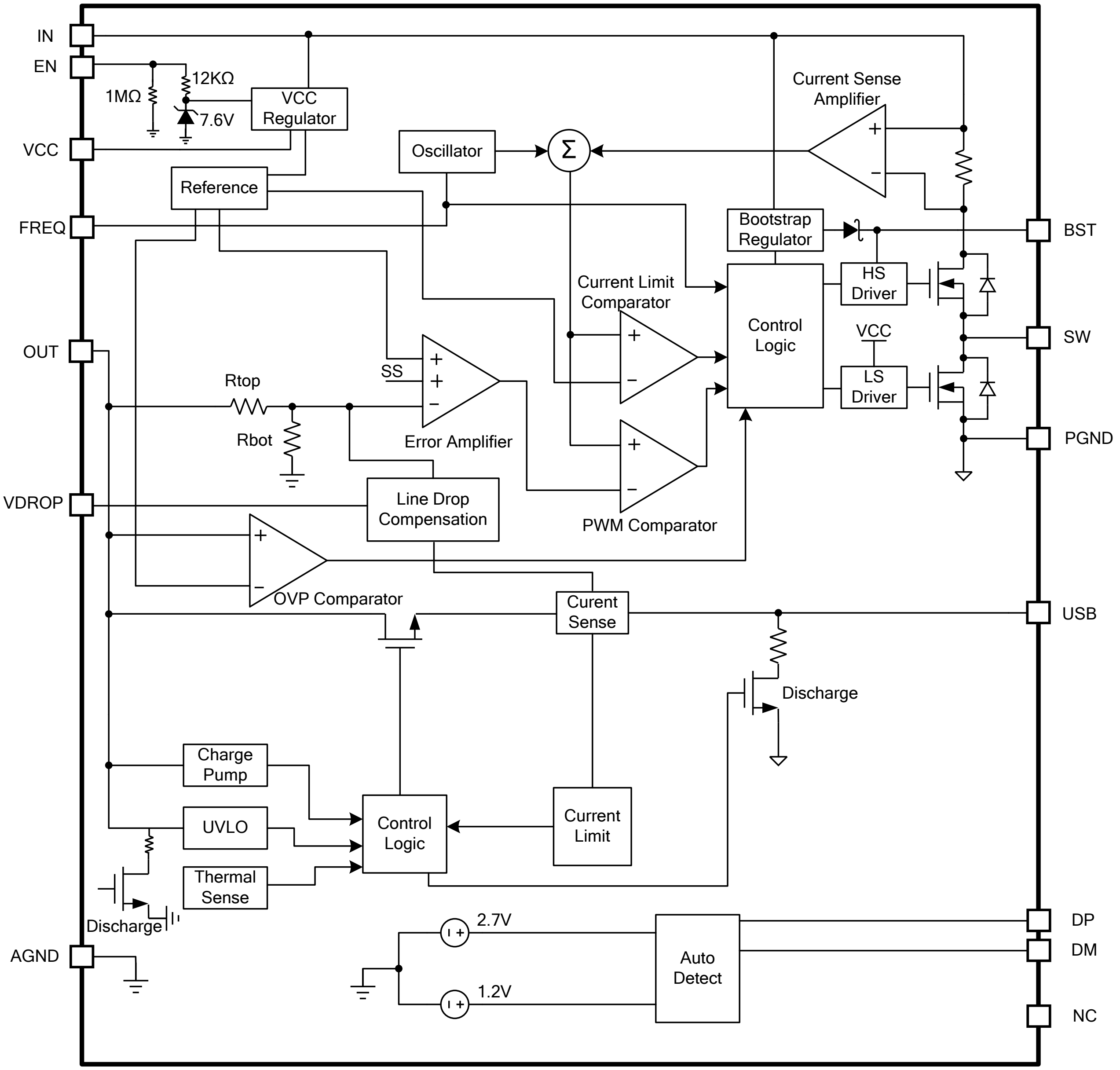


Figure 1: Functional Block Diagram

OPERATION

BUCK CONVERTER SECTION:

The MP2496M integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and a USB current-limit switch with charging port auto-detection. It offers a very compact solution that achieves 2.5A of continuous output current with excellent load and line regulation over a wide input supply range.

The MP2496M operates in a fixed-frequency, peak current-mode control to regulate the output voltage. The internal clock initiates the PWM cycle, turning on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by V_{COMP}. If the power switch is off, it remains off until the next clock cycle starts. If the duty cycle reaches 88% (350kHz switching frequency) in one PWM period, the current in the power MOSFET does not reach the value set by V_{COMP} and is forced off.

Error Amplifier (EA)

The error amplifier compares the internal feedback voltage against the internal 1V reference (REF) and outputs the COMP voltage, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

VCC Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 5.0V, the output of the regulator is in full regulation. When V_{IN} is lower than 5.0V, the output voltage decreases with V_{IN}. An external 0.22µF ceramic capacitor is required for decoupling.

Enable Control (EN)

The MP2496M has an enable control (EN). Pulling EN high enables the IC; pulling EN low disables the IC. Connect EN to V_{IN} through a resistor for automatic start-up. An internal 1MΩ resistor connected from EN to GND allows EN to float to shut down the IC.

EN is clamped internally using a 7.6V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to the voltage on V_{IN} limits the EN input current to less than 230µA and the amplitude of the voltage source below 10V, preventing damage to the Zener diode.

For example, connect 36V to V_{IN}, $R_{PULLUP} \geq (36V – 10V)/230\mu A = 113k\Omega$.

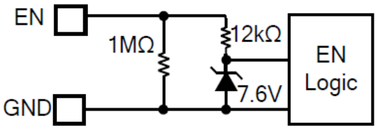


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2496M's UVLO comparator monitors the input voltage. The UVLO rising threshold is 5.7V while its falling threshold is 4.7V.

Internal Soft Start (SS)

The soft start prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is internally set to 1.65ms.

If the output of the MP2496M is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the internal feedback voltage.

Buck Over-Current Protection (OCP)

The MP2496M has a cycle-by-cycle, over-current limit for when the inductor peak current exceeds the current limit threshold and FB voltage drops below the under-voltage (UV) threshold, typically 70% below the reference. Once UV is triggered, the MP2496M enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the regulator. The MP2496M exits hiccup mode once the over-current condition is removed.

Buck Output Over-Voltage Protection (OVP)

The MP2496M buck converter has output over-voltage protection (OVP). If the output is higher than 6V, the high-side switch stops turning on, and the low-side switch turns on to discharge the output voltage until the output decreases to 5.75V. The chip then resumes normal operation.

If the output over-voltage can't be discharged to 5.75V, the low-side switch turns off after the inductor current reaches a negative current limit and remains off until the next clock cycle is triggered.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C2 (see Figure 3). If V_{BST}-V_{SW} exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4.

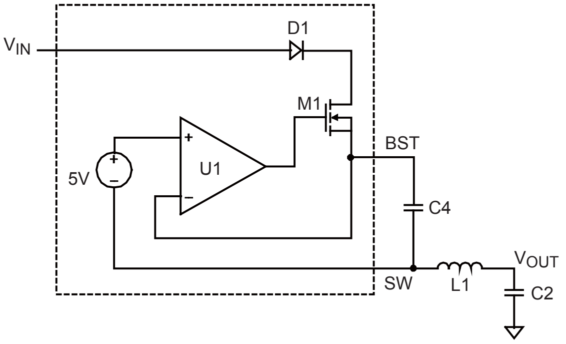


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Buck Output Discharge

The buck portion uses a discharge function to provide a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO, enable off) and is done in a very limited amount of time. After V_{CC} is discharged below 1V, the buck output discharge resistor disconnects.

USB CURRENT-LIMIT SWITCH SECTION:

Current-Limit Switch

The MP2496M has a single-channel, USB, current-limit switch. It provides built-in, soft-start circuitry that controls the rising slew rate of the output voltage to limit inrush current and voltage surges.

When the load current reaches the current limit threshold (typically 2.75A), the USB power MOSFET switches into a foldback current limit mode, 70% of the current limit (see Figure 4). If the over-current limit condition lasts for more than 3ms, the chip enters hiccup mode with 3ms of on-time and 8.5s of off-time.

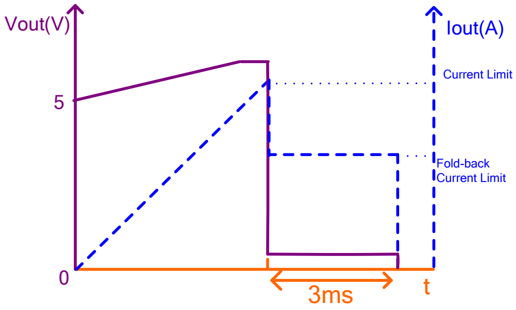


Figure 4: Over-Current Limit

During V_{IN} or EN start-up, the CC load current does not exceed 70% of the current limit to avoid triggering the foldback current limit and start-up failure.

Output Line Drop Compensation

The MP2496M is capable of compensating for an output voltage drop (such as a high impedance caused by a long trace) to keep a fairly constant 5V load-side voltage. The MP2496M uses the internal current sense output voltage of the current-limit switch to compensate for the line drop voltage. Since the trace resistance varies for different cables, the MP2496M provides selectable line drop compensation through VDROP. The line drop compensation amplitude increases linearly as the load current increases and also has an upper limitation.

USB Output Over-Voltage Protection (OVP)

In order to protect the device at the cable terminal, the USB switch's output has a dynamic over-voltage protection threshold. The MP2496M adjusts the OVP threshold based on different USB loading currents. The MP2496M has intelligent line drop compensation and a dynamic over-voltage protection control scheme to ensure the voltage at the cable terminal meets the 4.75V-5.25V specification.

USB Output Discharge

Each USB portion involves a discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO, enable off) and is done in a very limited amount of time.

Auto-Detection

The MP2496M integrates the USB dedicated charging port auto-detect function, which recognizes most mainstream portable devices. It supports the following charging schemes:

- USB battery charging specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode

The auto-detect function is a state machine that supports all of the above DCP charging schemes.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. When the temperature falls below its lower threshold, typically 145°C, the chip is enabled again.

APPLICATION INFORMATION

Selecting the Inductor

Use an inductor with a DC current rating at least 25% higher than the maximum load current for most applications. Select an inductor with a small DC resistance for best efficiency. The inductor value for most designs can be estimated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is calculated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

A 22µH inductance is recommended to improve EMI.

Selecting the Buck Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. For best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients. For CLA applications, a low ESR 100µF electrolytic capacitor and two-piece 10µF ceramic capacitors are recommended for EMI reduction.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worse-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic capacitors, place two high-quality ceramic capacitors as close to the IC's IN as possible. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For tantalum or electrolytic capacitors, ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor affect the stability of the regulation system. Low ESR electrolytic capacitors are recommended for a low output ripple and good control loop stability. For CLA applications, a 270µF polymer capacitor or an electrolytic capacitor with ~20mΩ ESR, and one 1µF ceramic capacitor are recommended.

PCB Layout Guidelines(8)

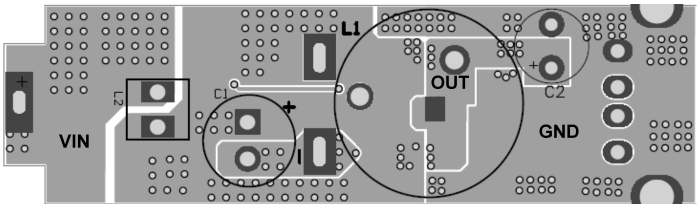
Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 5 and follow the guidelines below.

1. Connect the IC's OUT with short, direct, and wide traces. It is highly recommended to add vias under the IC and route the OUT trace on both PCB layers.
2. Use a large copper plane for PGND. Multiple vias should be added for better thermal dissipation.
3. Connect AGND to PGND.
4. Use a large copper plane for SW and USB.
5. Place the USB output capacitor close to USB.
6. Place two ceramic input decoupling capacitors as close to IN and PGND as possible to improve EMI performance.
7. Place the VCC decoupling capacitor as close to VCC as possible.

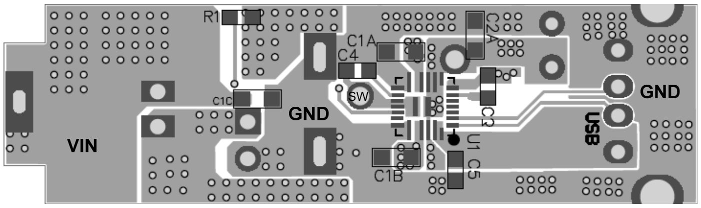
NOTE:

(8) The recommended layout is based on Figure 6: Typical Application Circuit on the next page.

Top Layer



Bottom Layer



(4.78cmx1.38cm)

Figure 5: Recommended Layout

TYPICAL APPLICATION CIRCUIT

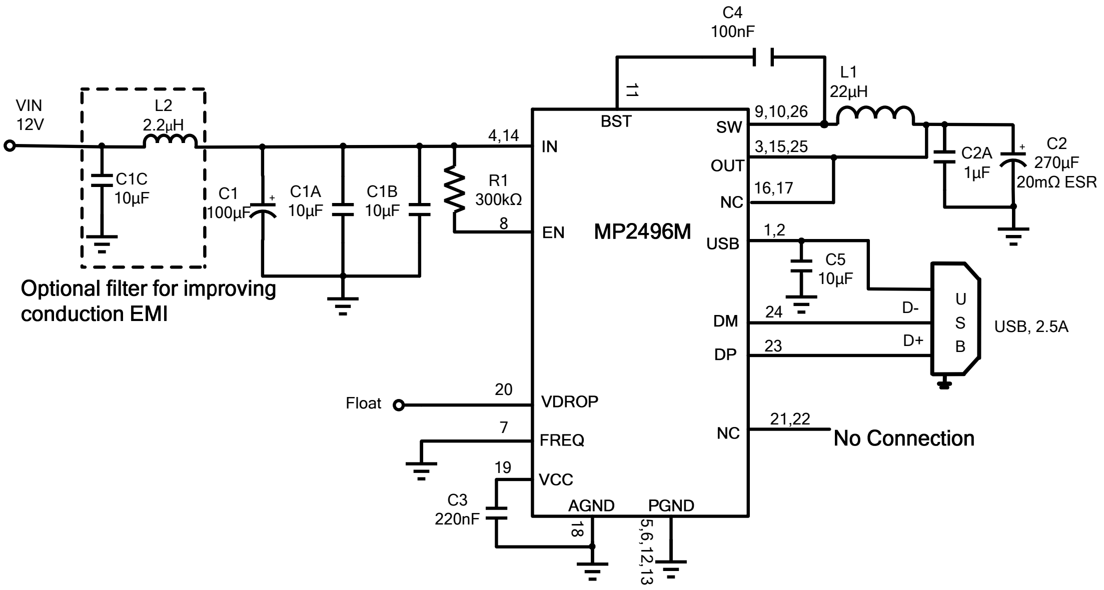
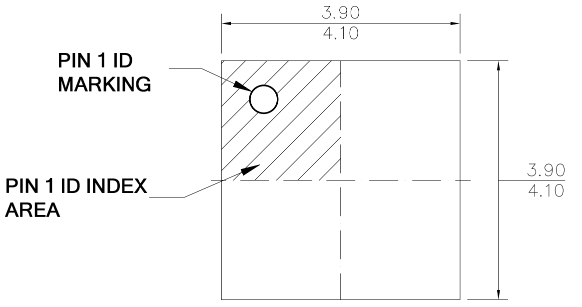


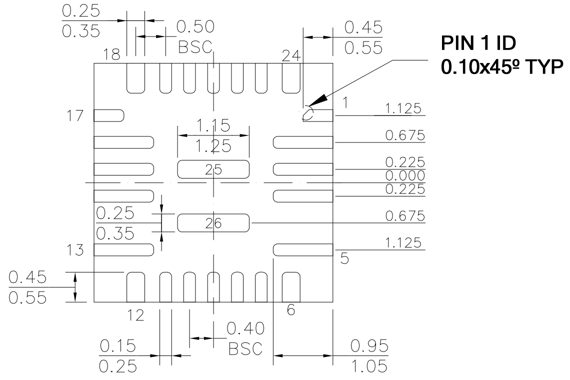
Figure 6: V_{IN} = 12V, USB = 5V/2.5A

PACKAGE INFORMATION

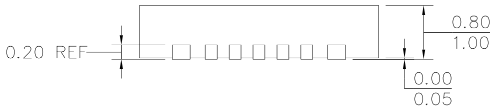
QFN-26 (4X4mm)



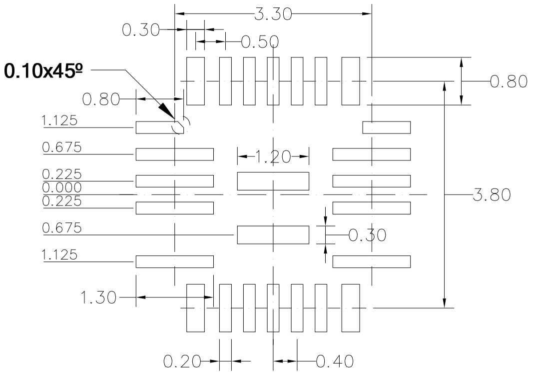
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.