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Evaluating the SSM3525 30 W, Filterless, Class-D, Output Sensing Audio Amplifier

FEATURES

15.3 W into 4 Ω at 12 V with a 1% THD + N

EVALUATION KIT CONTENTS

USBi USB interface board
USB cable
EVAL-SSM3525Z evaluation board

DOCUMENTS NEEDED

SSM3525 data sheet
EVAL-SSM3525Z user guide
DLL for SigmaStudio

GENERAL DESCRIPTION

The EVAL-SSM3525Z is an evaluation board for the SSM3525, which is an integrated mono 30 W, high efficiency, stereo Class-D audio amplifier with digital input. The application circuit requires a few external components and can operate from a single 4.5 V to 17 V supply. It is capable of delivering 15.3 W of continuous output power into a 4 Ω load from a 12 V power supply, with <1% total harmonic distortion plus noise (THD + N).

The SSM3525 features a high efficiency, low noise modulation scheme that requires no external inductor/capacitor (LC) output filters. This scheme continues to provide high efficiency even at low output power.

The SSM3525 operates with 92.1% efficiency at 9 W into an 8 Ω load, and it has a typical output noise voltage of 37.5 µV rms, A weighted.

This user guide describes how to configure and use the EVAL-SSM3525Z evaluation board. Read this user guide in conjunction with the SSM3525 data sheet, which provides specifications, internal block diagrams, register map, and application guidance for the amplifier IC.

Figure 1 shows the top view of the evaluation board, and Figure 2 shows the bottom view of the evaluation board.

EVALUATION BOARD PHOTOGRAPHS

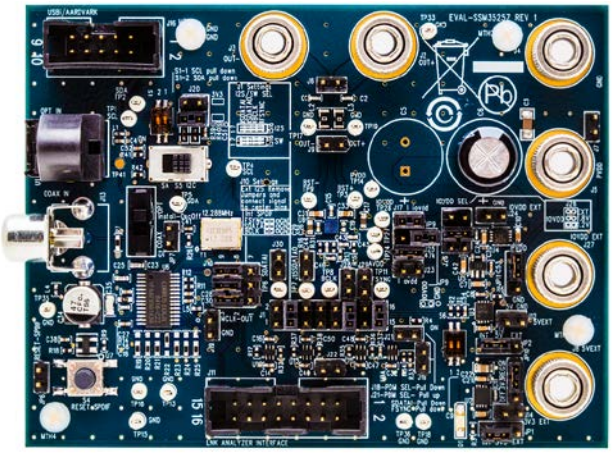

Figure 1. SSM3525 Evaluation Board Top View

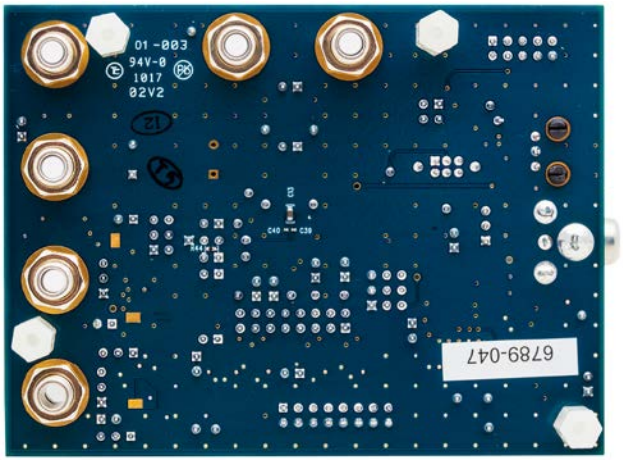

Figure 2. SSM3525 Evaluation Board Bottom View

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REVISION HISTORY

1/2018—Revision 0: Initial Version

SETTING UP THE HARDWARE

INPUT CONFIGURATION

There are several ways to source audio to the SSM3525 on the EVAL-SSM3525Z evaluation board. The evaluation board can accept direct inter-IC sound/time division multiplexed (I^2S/TDM) data or it can convert from Sony/Philips Digital Interface (S/PDIF)/ optical digital audio data to I^2S using an on-board digital audio receiver, U6. The EVAL-SSM3525Z can also accept a SoundWire® interface.

Use the 3 × 3 way header (J10) to make a connection from either the on-board S/PDIF audio receiver circuitry or the external digital audio signals to the SSM3525 device pins. The EVAL-SSM3525Z comes set with three jumpers set for receiving the S/PDIF audio data. The logic level for the inputs at J10 is 3.3 V.

To use the external I2S/TDM data, the three jumpers must be removed, and the signal source (FSYNC, BCLK, and SDATA) must be connected to the J10 center pins.

If the user does not have a direct I^2S or TDM source, the on-board digital audio receiver can accept S/PDIF data from a digital audio source, such as the digital audio output of a CD player. In this case, select either optical or coaxial using the S2 switch to properly connect the desired input to the digital audio receiver.

The voltage/current sense, analog-to-digital converter (ADC) output data is available at the J15 jumper at the IOVDD logic level or at the J22 jumper at the 3.3 V logic level. Refer to the SSM3525 data sheet for more information on placement options.

CONTROL PORT

The SSM3525 supports I^2C control for setting the internal registers. The J16 10-way header is used for connecting the external I^2C master for controlling the EVAL-SSM3525Z. The evaluation board can be set for the desired I^2C address by using two headers (JP9 and J25). The JP9 is used for setting the pull-up or pull-down to the IO_{VDD} and GND voltages on the printed circuit board (PCB), whereas J25 can be used for bypassing the 47 kΩ resistor. Refer to the SSM3525 data sheet for address selection options. Remove the jumper across J25 to insert the 47 kΩ resistor in the signal path for pull-up or pull-down operation. To properly float the ADDR pin to a no connect state, do not insert jumpers on JP9 or J25. By default, the J25 is inserted, and JP9 is set so that the ADDR pin is pulled to ground. Setting the ADDR pin to ground sets the 7-bit device address to 0x24.

OUTPUT CONFIGURATION

The binding post output terminals (OUT+ and OUT−) provide an option to connect the speaker with standard banana connectors. In addition, 2-pin, 0.100-inch headers (J6 and J9) are provided as alternate option.

To reduce the system radiated emission, especially if the speaker cable length exceeds 20 cm, it may be necessary to include an output filter. The recommended filter uses two ferrite beads (L2 and L3) and two capacitors (C1 and C2). See Figure 10 for more details.

Note the addition of the ferrite beads other than the one used on the evaluation board may affect the total harmonic distortion (THD) and signal-to-noise ratio (SNR) performance as specified in the SSM3525 data sheet. For best performance, the Murata output ferrite beads in Table 1 are recommended.

Table 1. Recommended Output Ferrite Beads

Part No.	Manufacturer[1]	Impedance (Z) (Ω at 100 MHz)	Maximum Current (I_{MAX}) (mA)	Direct Conversion Receiver (DCR) (Ω)	Size (mm)
NFZ2MSM101SN10	Murata Manufacturing Co.	100	4000	0.014	2.0 × 1.6 × 0.9
NFZ2MSM181SN10	Murata Manufacturing Co.	180	3400	0.020	2.0 × 1.6 × 0.9
NFZ2MSM301SN10	Murata Manufacturing Co.	300	3100	0.024	2.0 × 1.6 × 0.9

[1] Contact Murata Manufacturing Co. for further options.

POWER SUPPLY CONFIGURATION

The binding posts, J5 (PVDD) and J4 (GND), provide the power supply to the evaluation board. Care must be taken to connect the dc power with the correct polarity and voltage. Reverse polarity or overvoltage can damage the EVAL-SSM3525Z permanently. Permissible supply voltages range from 4.5 V to 17 V; higher voltages may damage the amplifier. In addition, use an appropriate current rated power supply to the evaluation board. Typically, a 5 A rating supply is recommended if using 4 Ω speakers and 12 V.

The EVAL-SSM3525Z has an option to generate the 5 V (AVDD), 3.3 V, 1.8 V, and 1.2 V from the PVDD supply. These voltages are generated using the linear regulators on the evaluation board: U3 for 5 V, U2 for 3.3 V, U4 for 1.8 V, and U5 for 1.2 V. The 5 V and 3.3 V regulators can be turned off using Jumper JP11 for 5 V and Jumper JP10 for 3.3 V. The 3.3 V regulator is used for the on-board S/PDIF digital audio receiver and I²C pull-up. The 1.8 V/1.2 V must be provided as IOVDD to the SSM3525. The 5 V (AVDD) can be provided externally or generated internally by the SSM3525. By default, the evaluation board is set up for generating the 5 V, 3.3 V, 1.8 V, and 1.2 V using on-board regulators; however, only PVDD and IOVDD (1.8 V) are supplied to the SSM3525, and 5 V (AVDD) is generated from on-chip LDO. After power-up, the SSM3525 generates the AVDD (5 V) from the on-chip regulator. The on-chip regulator for AVDD can be enabled in Register 0x04 via I²C. By default, the on-chip regulator is disabled. Jumper J23 is open, and Jumper J17 must be fitted.

The J17 and J23 jumpers are provided to measure the IOVDD and AVDD currents. If using the on-board regulators as a source for the AVDD and IOVDD, Jumper J17 and Jumper J23 must be fitted, and the on-chip AVDD regulator must be disabled in Register 0x04.

EDGE MODE

To reduce the radiated emissions from the SSM3525 amplifier, an edge rate control mode is available. Register 0x05, Bit 2 (EDGE) controls the edge rate of the switching. To enable low electromagnetic interference (EMI) mode, set Bit 2 of Register 0x05 to 1. To return to normal operation, set Bit 2 of Register 0x05 to 0.

COMPONENT SELECTION

Selecting the proper components is the key to achieving the performance required at the cost budgeted.

Output Decoupling Capacitors

There are two output filter capacitors (C1 and C2) that work with the L2 and L3 ferrite beads. Use small size (0603 or 0402), multilayer ceramic capacitors of dielectric type X7R or COG (NPO) materials. The recommended value is 220 pF.

Output Ferrites

If ferrite beads are preferred for EMI filtering at the output nodes, Table 1 shows the recommended output ferrite beads to use to avoid excessive noise induced by the nonlinear behavior of the ferrite beads.

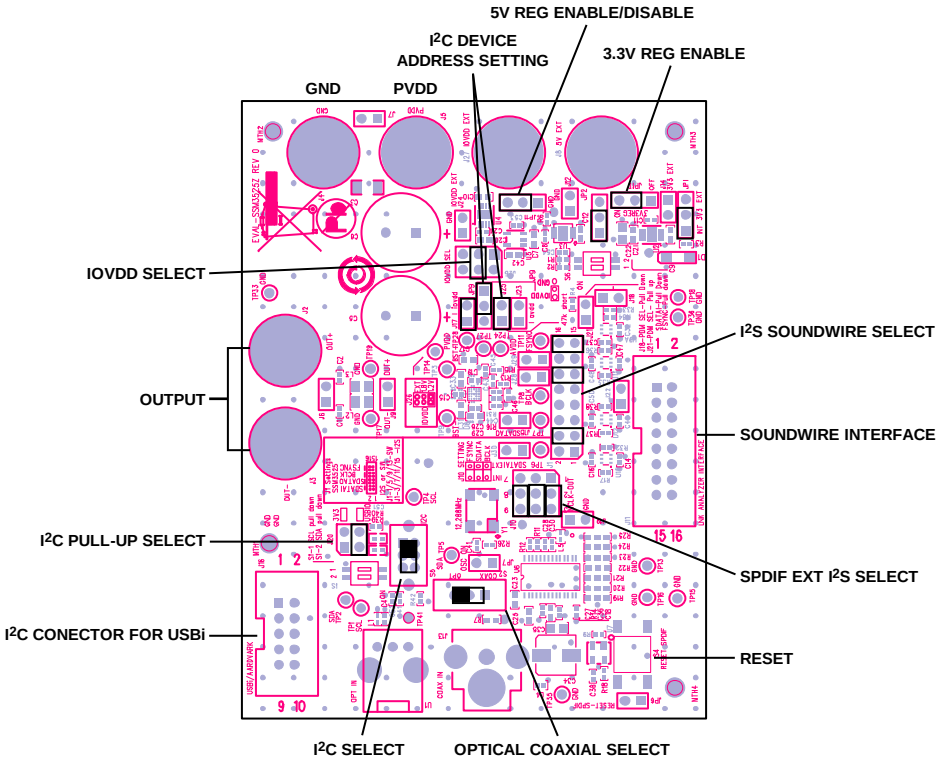

Figure 3. Board Settings for I²C to I²S Mode

GETTING STARTED

To set up the amplifier to work in a simple single-supply configuration for quick evaluation, follow these steps:

1. Download the SigmaStudio® software to the PC, and follow the installation steps provided suitable for the PC.
2. Connect the USBi to the USB port on the PC and ensure that the USB driver for the USBi board is installed.
3. Copy the provided SSM3525 DLL file to the **C:\Program files\Analog Devices** folder on your PC.
4. After installing the SigmaStudio software, the SigmaStudio icon appears on the desktop. Double click on the icon to open the SigmaStudio project screen.
5. Start a new project by pulling the USBi and SSM3525 to the **Hardware Configuration** tab.
6. Connect the USBi to the SSM3525 block on the **Hardware Configuration** schematic. See Figure 4.

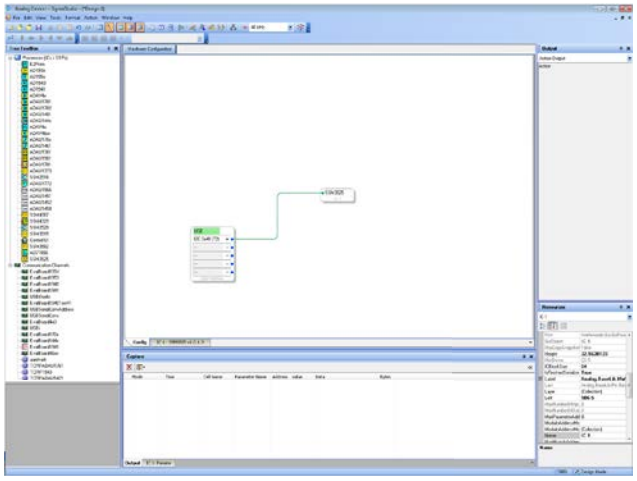

*Figure 4. **Hardware Configuration** Tab*

7. Connect the 12 V power supply source to the EVAL-SSM3525Z.
8. Connect the USBi to J16 on the evaluation board.
9. Select the digital audio source for the SDATAI, FSYNC, and BCLK pins of the SSM3525. By default, the evaluation board is set for the S/PDIF source. Connect the optical or coaxial cable to the appropriate connector on the evaluation board.
10. Ensure that the jumpers are inserted across all three rows of JP10 to establish direct connection of the digital audio signal lines to the inputs of the SSM3525. See Figure 3 for setting the jumpers and switches.
11. Connect the speakers across OUT+ (J2) and OUT– (J3) binding posts.
12. If using the on-board S/PDIF to I²S circuitry, press the **S4** button to synchronize the audio signals, which resets the digital audio receiver.
13. Click the **IC-1SSM3525** tab. If you click the **Read Info** button, the **35** appears in the **Device ID 1** field, **25** appears in the Device ID 2 field, and the die revision number appears in the **Revision** field. See Figure 5.
14. Go to the **Chip & DAC CTRL** tab.

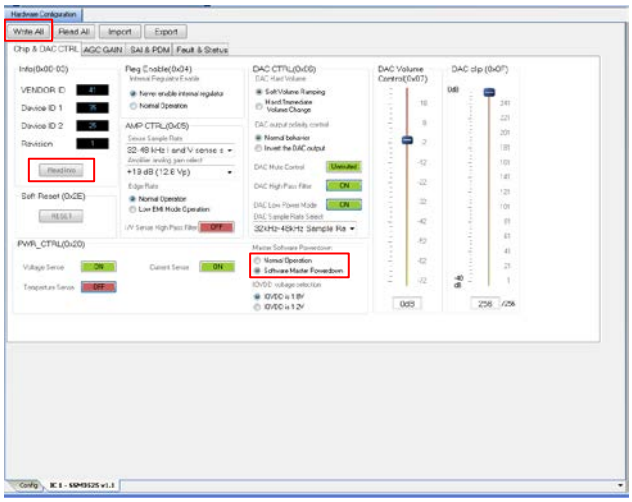

*Figure 5. **Chip & DAC CTRL** Tab*

15. Click **Write All** button.
16. Under **Master Software Powerdown**, select **Normal Operation**. The SSM3525 then powers up with audio on the output.

SUGGESTED SYSTEM LEVEL AND AUDIO TESTS

It is recommended that users test the following:

- SNR
- Output noise, ensuring that an A-weighted filter is used to filter the output before reading the measurement meter
- Maximum output power
- Distortion
- Efficiency

EVALUATION BOARD SCHEMATICS AND ARTWORK

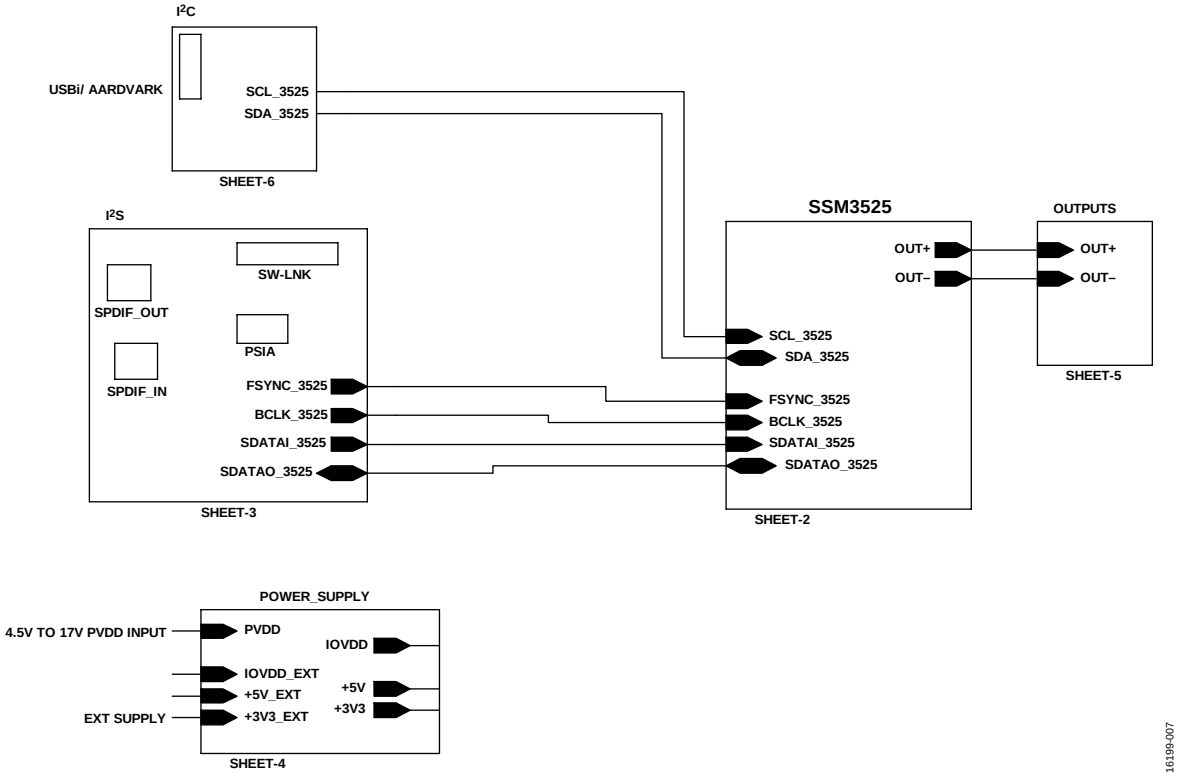

Figure 6. Schematic of the EVAL-SSM3525Z Evaluation Board Block Diagram

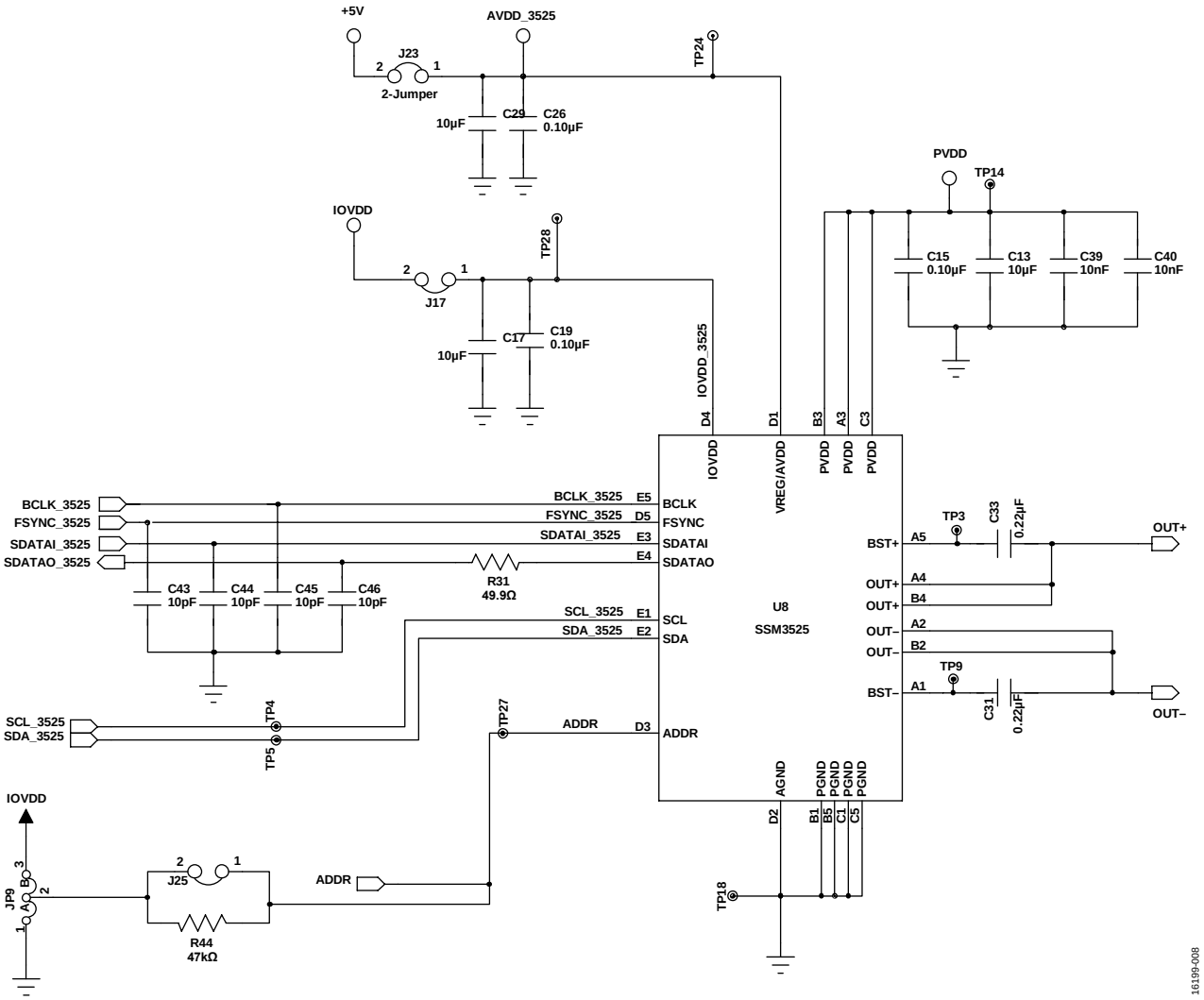

Figure 7. Schematic of the EVAL-SSM3525Z Evaluation Board SSM3525 Section

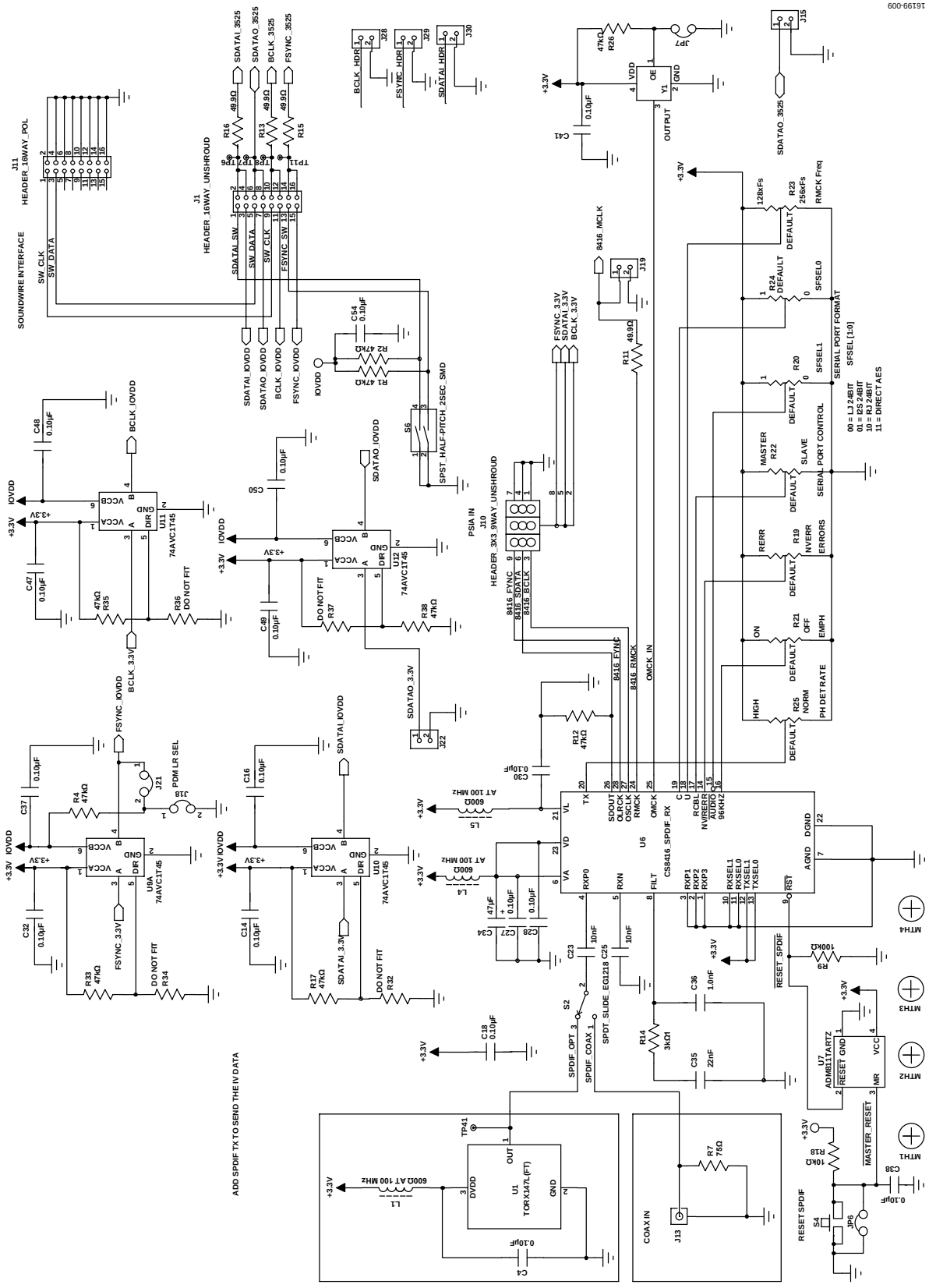

Figure 8. Schematic of the EVAL-SSM3525Z Evaluation Board I²C Digital Input Section

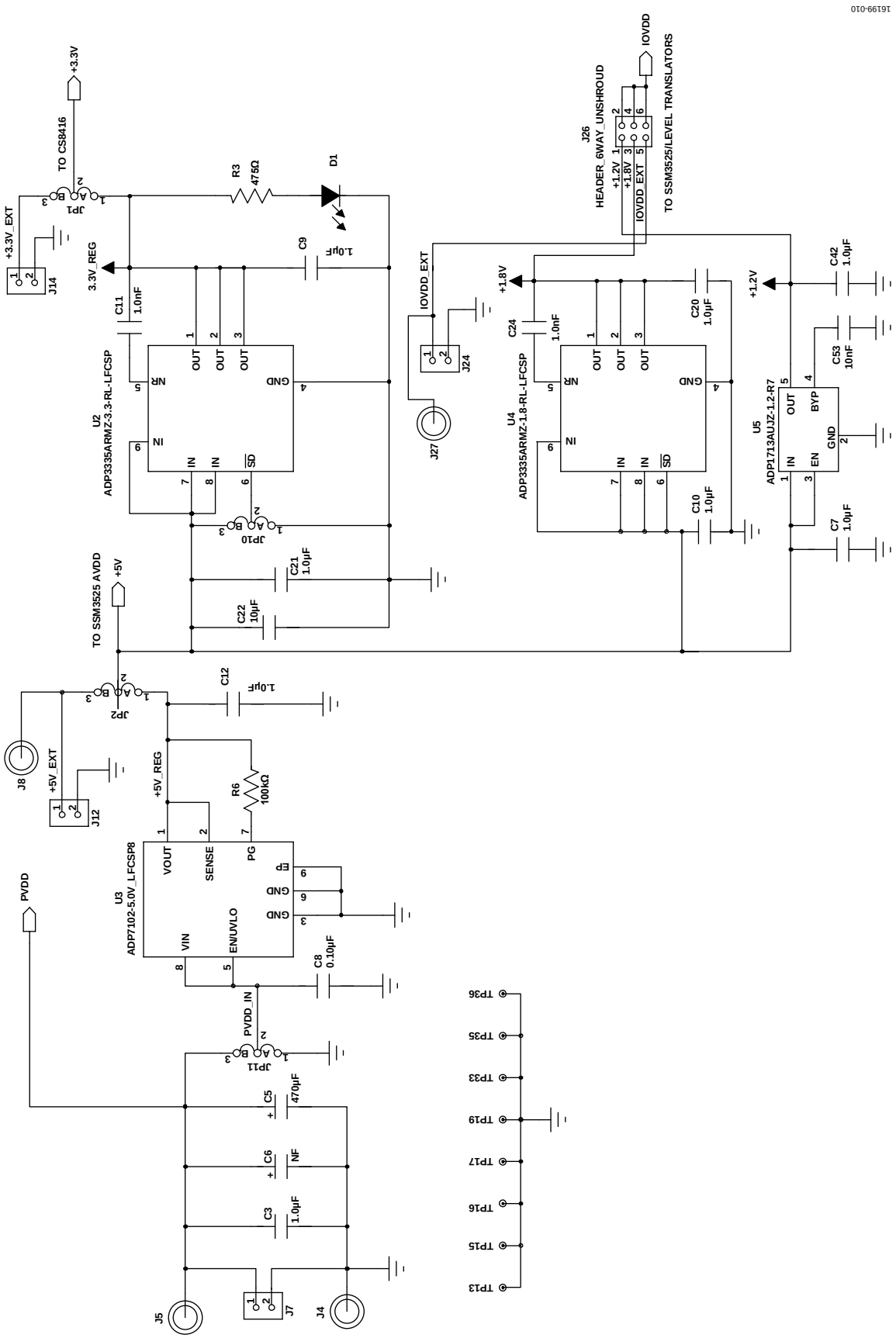

Figure 9. Schematic of the EVAL-SSM3525Z Evaluation Board Power Supply Section

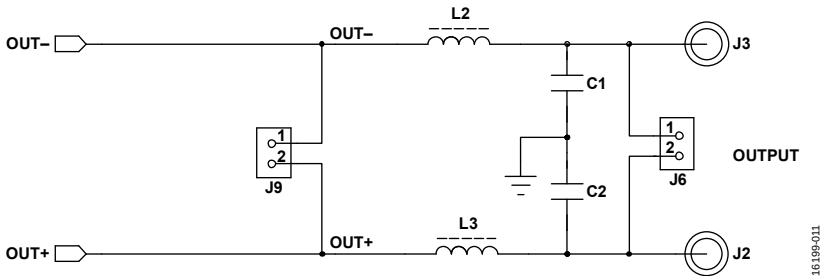

Figure 10. Schematic of the EVAL-SSM3525Z Evaluation Board Output Section

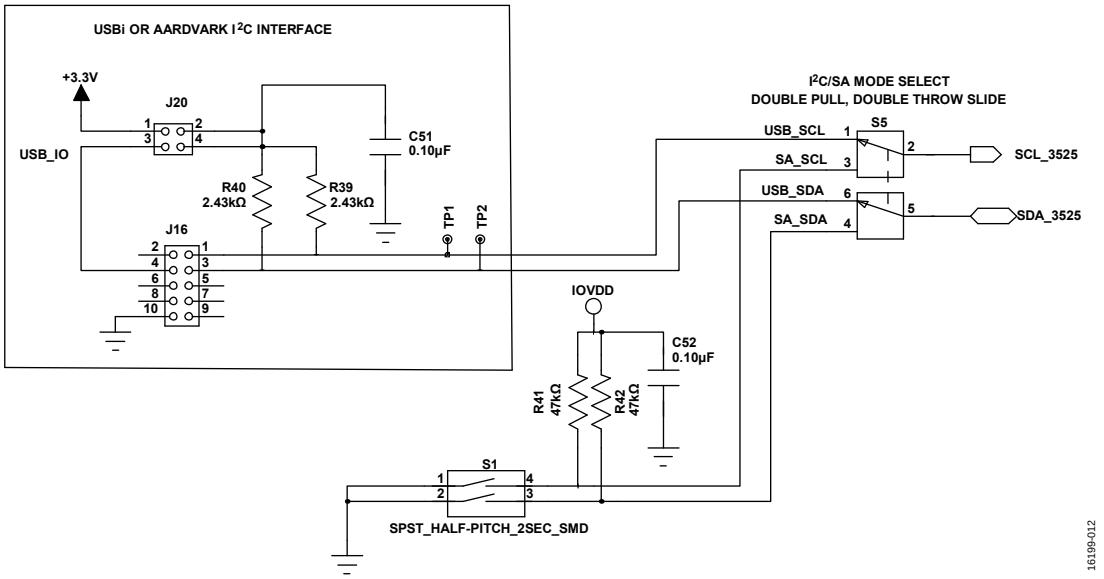

Figure 11. Schematic of the EVAL-SSM3525Z Evaluation Board I²C Section

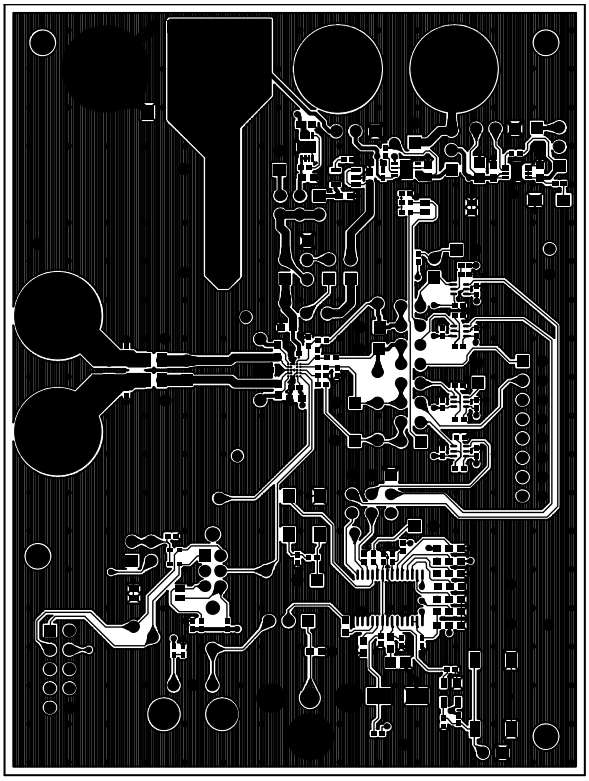

Figure 12. EVAL-SSM3525Z Evaluation Board Top Layer Copper

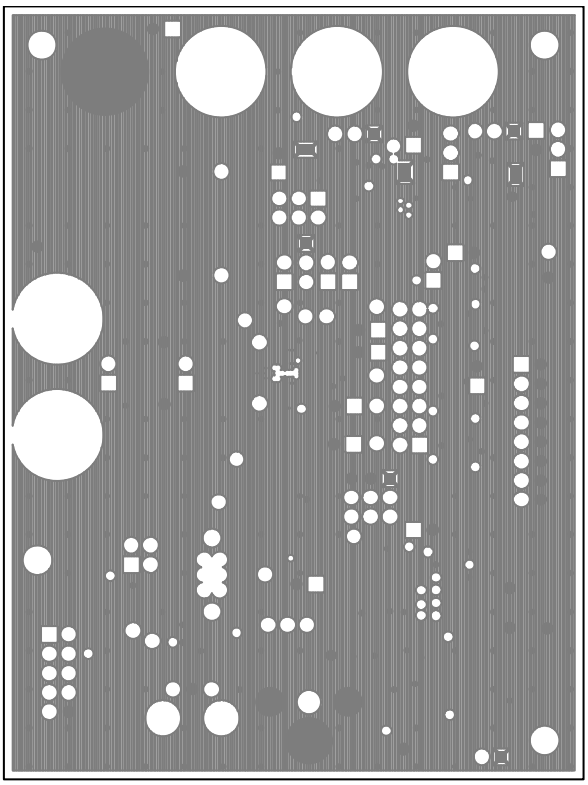

Figure 13. EVAL-SSM3525Z Evaluation Board Second Layer Copper

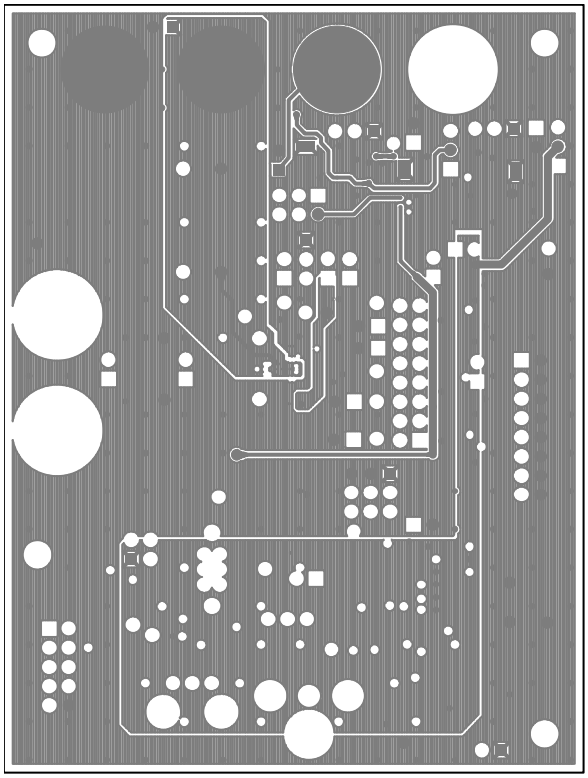

Figure 14. EVAL-SSM3525Z Evaluation Board Third Layer Copper

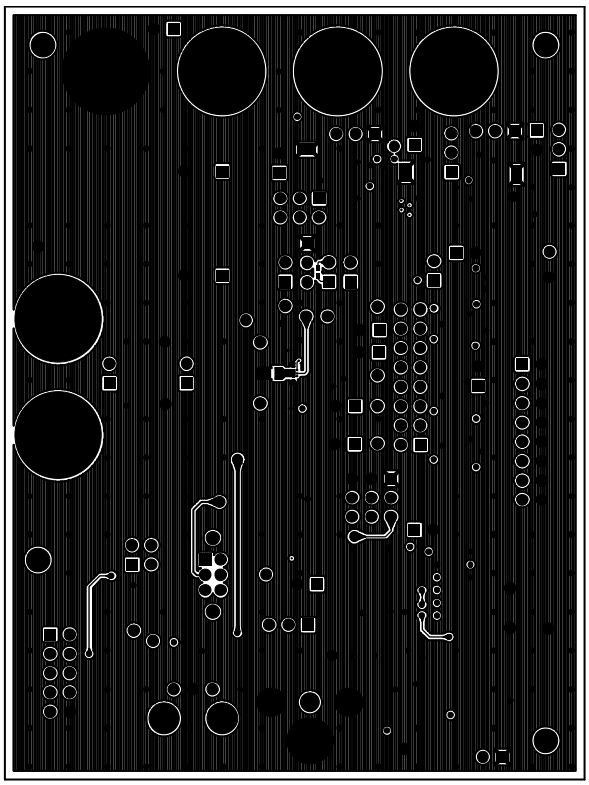

Figure 15. EVAL-SSM3525Z Evaluation Board Bottom Layer Copper

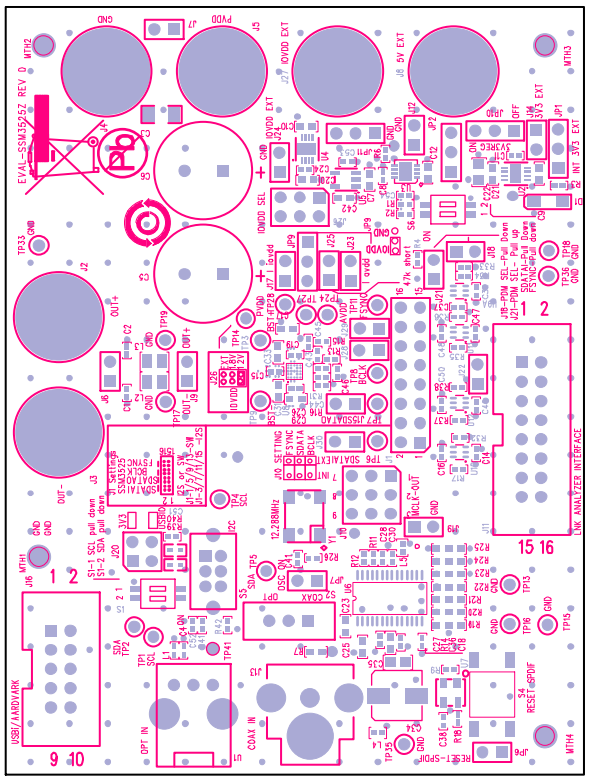

Figure 16. EVAL-SSM3525Z Evaluation Board Top Silkscreen

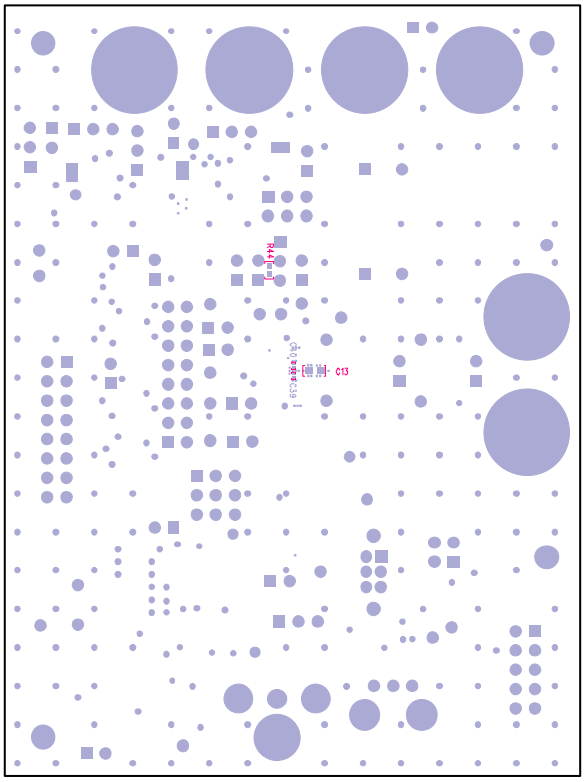

Figure 17. EVAL-SSM3525Z Evaluation Board Bottom Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty.	Reference Designator	Description	Supplier	Part No.
1	Board	Evaluation board EVAL-SSSM3525Z, 4-layer, 4" × 3"		
2	C1, C2	Multilayer ceramic capacitors, 220 pF, 50 V, NP0 (0402)	Murata Electronics North America (ENA)	GRM1555C1H221JA01D
1	C3	Multilayer ceramic capacitor, 1 µF, 25 V, X7R (1206)	Murata ENA	GRM31CR71H105KA61L
20	C4, C14, C16, C18, C19, C26 to C28, C30, C32, C37, C38, C41, C47 to C52, C54	Multilayer ceramic capacitors, 0.1 µF, 16 V, X7R (0402)	Murata ENA	GRM155R71C104KA88D
1	C5	Aluminum electrolytic capacitor, 470 µF, HE, 105°C, 5 mm	Nichicon	UHE1E471MPD6
NF[1]	C6	Aluminum electrolytic capacitor, HE, 105°C, 5 mm	Nichicon	UHE1E471MPD6
7	C7, C9, C10, C12, C20, C21, C42	Multilayer ceramic capacitors, 1 µF, 16 V, X7R (0603)	Murata ENA	GRM188R71C105KA12D
2	C8, C15	Multilayer ceramic capacitors, 0.1 µF, 35 V, X7R (0402)	TDK Corporation	CGA2B3X7R1V104K050BB
3	C11, C24, C36	Multilayer ceramic capacitors, 1 nF, 50 V, NP0 (0402)	Murata ENA	GRM1555C1H102JA01D
3	C13, C17, C29	Multilayer ceramic capacitors, 10 µF, 25 V, X5R (0603)	TDK Corporation	C1608X5R1E106M080AC
1	C22	Multilayer ceramic capacitor, 10 µF, 10 V, X7R (0805)	Murata ENA	GRM21BR71A106KE51L
2	C23, C25	Multilayer ceramic capacitors, 10 nF, 25 V, NP0 (0603)	TDK Corporation	C1608C0G1E103J
2	C31, C33	Multilayer ceramic capacitors, 0.22 µF, 25 V, X7R (0603)	Murata ENA	GRM188R71E224KA88D
1	C34	Aluminum electrolytic capacitor, 47 µF, FC, 105°C, SMD_D	Panasonic EC	EEE-FC1C470P
1	C35	Multilayer ceramic capacitor, 22 nF, 25 V, NP0 (0805)	Murata ENA	GRM21B5C1H223JA01L
2	C39, C40	Multilayer ceramic capacitors, 10 nF, 25 V, X7R (0201)	Murata ENA	GRM033R61E103KA12D
4	C43 to C46	Multilayer ceramic capacitors, 10 pF, 50 V, NP0 (0402)	Samsung Electro-Mechanics America	CL05C100JB5NNNC
1	C53	Multilayer ceramic capacitor, 10 nF, 25 V, X7R (0402)	Murata	GRM155R71E103JA01J
1	D1	Red diffused 6.0 millicandela, 635 nm, 1206	Lumex Opto	SML-LX1206IW-TR
1	J1	16-way unshrouded header	3M	PBC080DAAN or cut PBC36DAAN
7	J2 to J5, J8, J27	Binding post mini uninsulated base, through hole	Johnson	111-2223-001
12	J6, J7, J9, J12, J14, J15, J19, J22, J24, J28 to J30	2-pin header, unshrouded jumper, 0.10", use Tyco shunt 881545-2	Sullins Electronics Corporation	PBC02SAAN or cut PBC36SAAN
1	J10	9-way unshrouded header	TE Connectivity	103817-2
1	J11	16-way shroud polarized header	3M	N2516-6002RB
1	J13	RCA jack, printed circuit board (PCB), through hole mount, R/A yellow	Connect-Tech Products Corporation/CUI Inc.	CTP-021A-S-YEL/RCJ-014
1	J16	10-way shroud, polarized header	3M	N2510-6002RB
4	J17, J8, J21, J25	2-pin header, unshrouded jumper, 0.10", use Tyco shunt 881545-2	Sullins Electronics Corporation	PBC02SAAN or cut PBC36SAAN
1	J20	4-way unshrouded header	3M	PBC02DAAN or cut PBC36DAAN
1	J23	2-pin header, unshrouded jumper, 0.10", use Tyco shunt 881545-2	Sullins Electronics Corporation	PBC02SAAN or cut PBC36SAAN
1	J26	6-way unshrouded header	3M	PBC06DAAN or cut PBC36DAAN

Qty.	Reference Designator	Description	Supplier	Part No.
5	JP1, JP2, JP9 to JP11	3-position session initiation protocol (SIP) header	Sullins Electronics Corporation	PBC03SAAN or cut PBC36SAAN
2	JP6, JP7	2-pin header, unshrouded jumper, 0.10", use Tyco shunt 881545-2	Sullins Electronics Corporation	PBC02SAAN or cut PBC36SAAN
3	L1, L4, L5	Chip ferrite bead, 600 Ω at 100 MHz	TDK Corporation	MMZ1005S601C
2	L2, L3	Ferrite bead for Class D output	Murata	NFZ2MSM181
4	MTH1 to MTH4	Nylon screw pan Phillips 4-40 and hex standoff, 4-40 nylon 1/2" standoff, round 4-40THR, 0.500"	Keystone Electronics and B&F Fastener	NY PMS 632 0025 PH and 1903C
16	R1, R2, R4, R12, R17, R26, R32 to R38, R41, R42, R44	Chip resistor, 47 kΩ, 1%, 63 mW, thick film, 0402	Yageo	RC0402FR-0747K0L
1	R3	Chip resistor, 475 Ω, 1%, 63 mW, thick film, 0402	Vishay/Dale	CRCW0402475RFKED
2	R6, R9	Chip resistor, 100 kΩ, 1%, 100 mW, thick film, 0402	Panasonic Electronic Components Group (ECG)	ERJ-2RKF1003X
1	R7	Chip resistor, 75 Ω, 1%, 100 mW, thick film, 0603	Panasonic ECG	ERJ-3EKF75R0V
5	R11, R13, R15, R16, R31	Chip resistor, 49.9 Ω, 1%, 63 mW, thick film, 0402	Yageo	RC0402FR-0749R9L
1	R14	Chip resistor, 3.01 kΩ, 1%, 100 mW, thick film, 0603	Rohm	MCR03EZPFX3011
1	R18	Chip resistor, 10 kΩ, 1%, 63 mW, thick film, 0402	Rohm	MCR01MZPF1002
7	R19 to R25	Chip resistor, 47.5 kΩ, 1%, 100 mW, thick film, 0603	Panasonic ECG	ERJ-3EKF4752V
2	R39, R40	Chip resistor, 2.43 kΩ, 1%, 63 mW, thick film, 0402	Vishay/Dale	CRCW04022K43FKED
2	S1, S6	Switch dual inline package (DIP), 4-poles sealed surface-mount device (SMD) (half-pitch)	Omron	A6H-2102
1	S2	Single-pole, double throw (SPDT) slide switch, PC mount	E-Switch	EG1218
1	S4	Tact switch, 6 mm gull wing	Tyco/Alcoswitch	FSM6JSMA
1	S5	Double pole, double throw (DPDT) slide switch, vertical	E-Switch	EG2207
23	TP1 to TP9, TP11, TP13 to TP19, TP24, TP27, TP28, TP33, TP35, TP36	Mini test point white, 0.1" outside diameter	Keystone Electronics	5002
1	TP41	Gold pad only	Nothing to stuff	Nothing to stuff
1	U1	15 Mbps fiber optic receiving module with shutter	Toshiba	TORX147L(FT)
1	U2	High accuracy, ultralow IQ, 500 mA, any capacitor low dropout regulator	Analog Devices, Inc.	
1	U3	Fixed 5 V output, 20 V input, 300 mA, low noise, complementary metal oxide semiconductor, low dropout	Analog Devices	ADP7102ACPZ-5.0
1	U4	High accuracy, ultralow IQ, 500 mA, any capacitor low dropout regulator	Analog Devices	ADP3335ACPZ-1.8-RL
1	U5	Fixed low dropout voltage regulator, 1.2 V	Analog Devices	ADP1713AUJZ-1.2-R7
1	U6	192 kHz digital receiver 28-TSSOP	Cirrus Logic	CS8416-CZZ
1	U7	Microprocessor voltage supervisor, logic low, reset output	Analog Devices	ADM811TARTZ-REEL7
1	U8	30 W, filterless, Class D output sensing audio amplifier	Analog Devices	SSM3525BCBZ-RL
4	U10 to U12, U9A	Transceiver, 1-bit 74AVC1T45, 6TSSOP	NXP	74AVC1T45GW,125
1	Y1	12.288 MHz, fixed SMD oscillator, 3.3 V to 5 V dc	Cardinal Components	CPPFX C 7 L T - A7 BR - 12.288 MHz TS

[1] NF means not fitted.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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