KYOCERA Display Corporation

Document Title	TVL-55683D116U-LW-I-AAN Product Information		Page No.	1/31
Document No.		Issue date	2013/02/21	Revision	00

<u>Product Information</u>

To:

Product Name: TVL-55683D116U-LW-I-AAN

Document Issue Date: 2013/02/21

Note: 1. Please contact Kyocera Display Company. before designing your product based on this product.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by KYOCERA DISPLAY for any intellectual property claims or other problems that may result from application based on the module described herein.

_____

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FQ-7-30-0-009-03C

Revision	Date	Page	Old Description	New Description	Remark
00	2012/05/10	All	--	First issued	

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Contents

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1.0 General Descriptions

1.1 Introduction

The TVL-55683D116U-LW-I-AAN is a color active matrix thin film transistor (TFT) TN liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has an 11.6-inch diagonally measured active display area with WXGA resolution (1366 vertical by 768 horizontal pixel array).

1.2 Features

■ 11.6"WXGA TFT LCD Panel

■ LED Light-bar Backlight System

■ Supported WXGA (V:1,366 lines, H:768 pixels) resolution

■ Compatible with RoHS Standard

1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	11.6	Inch
Active Area	256.125 (H) x 144.000(V)	mm
Pixels H x V	1,366 (x3) x 768	-
Pixel Pitch	0.1875x0.1875	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally White (TN)	-
White Luminance	220 (Typ.) 5 points average	cd/ m^2 (20mA of per LED)
Contrast Ratio	500（Typ.）	-
Response Time	8(Typ.)	ms
View Angle(L/R/U/D)	75/75/50/60(Typ.)	-
Input Voltage	+3.3 (Typ.)	V
Power Consumption	4.2 (Max.)	Watt
Module Weight	235 (Max.)	g
Outline Dimension (Max)	278.5(H) x 168.0(V) x3.7(D)	mm
Electrical Interface (Logic)	LVDS	-
Support Color	262 K	-
Color Gamut	45%(Typ)	-
Optimum Viewing Direction	6 o'clock	-
Surface Treatment	Anti-Glare	-

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1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module

Figure 1 Block Diagram
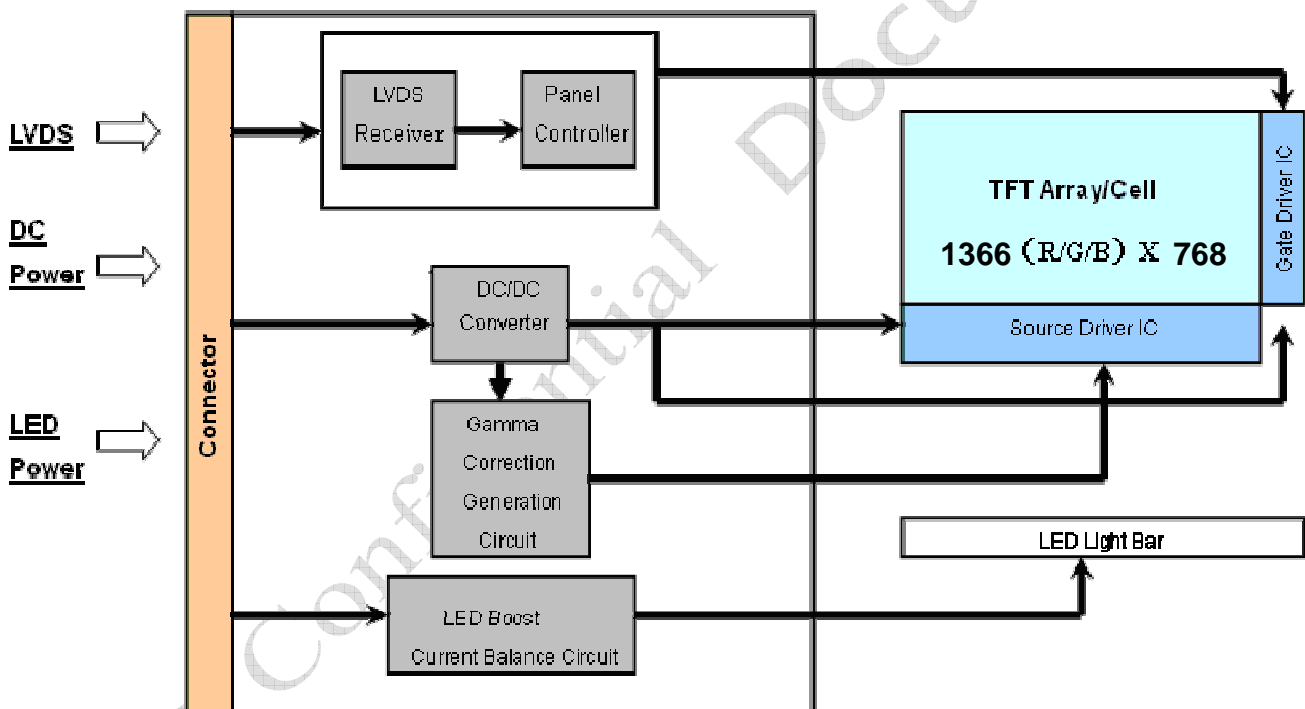
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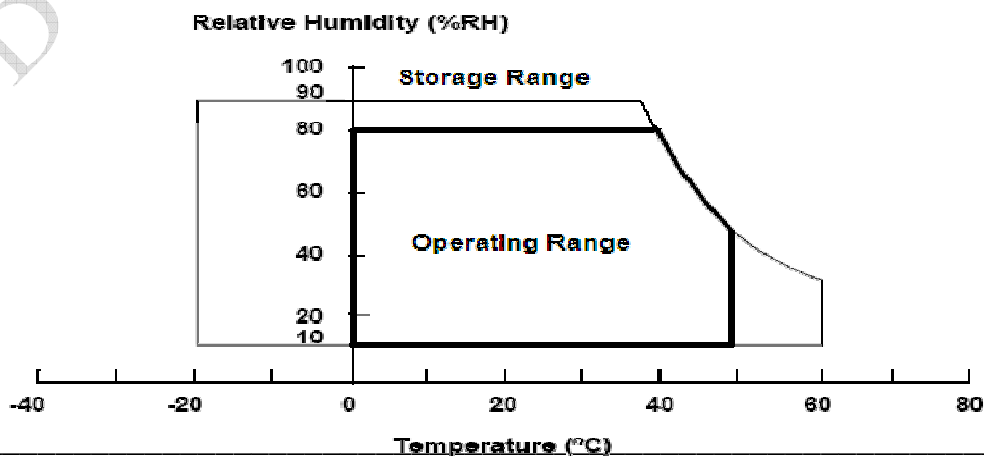
2.0 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	4.0	V	Typ.=3.3V
Supply V_{LED} Voltage	V_{LED}	6	21	V	
Input Signal		-0.3	2.7	V	LVDS signals
Operating Temperature	TOP	0	50	deg. C	(Note 3)
Operating Humidity	HOP	10	80	%RH	(Note 3)
Storage Temperature	TST	-20	60	deg. C	(Note 3)
Storage Humidity	HST	10	90	%RH	(Note 3)
Vibration	Level	-	1.5G	G	30min for X, Y, Z axis
	Bandwidth		10~500Hz	Hz	
Shock	Level	-	220	G	Half sine wave,2ms

Note

(1) Maximum Wet-Bulb should be 39 degree C. No condensation.
(2) When you apply the LCD module for OA system. Please make sure to keep the temperature of LCD module is less than 60℃
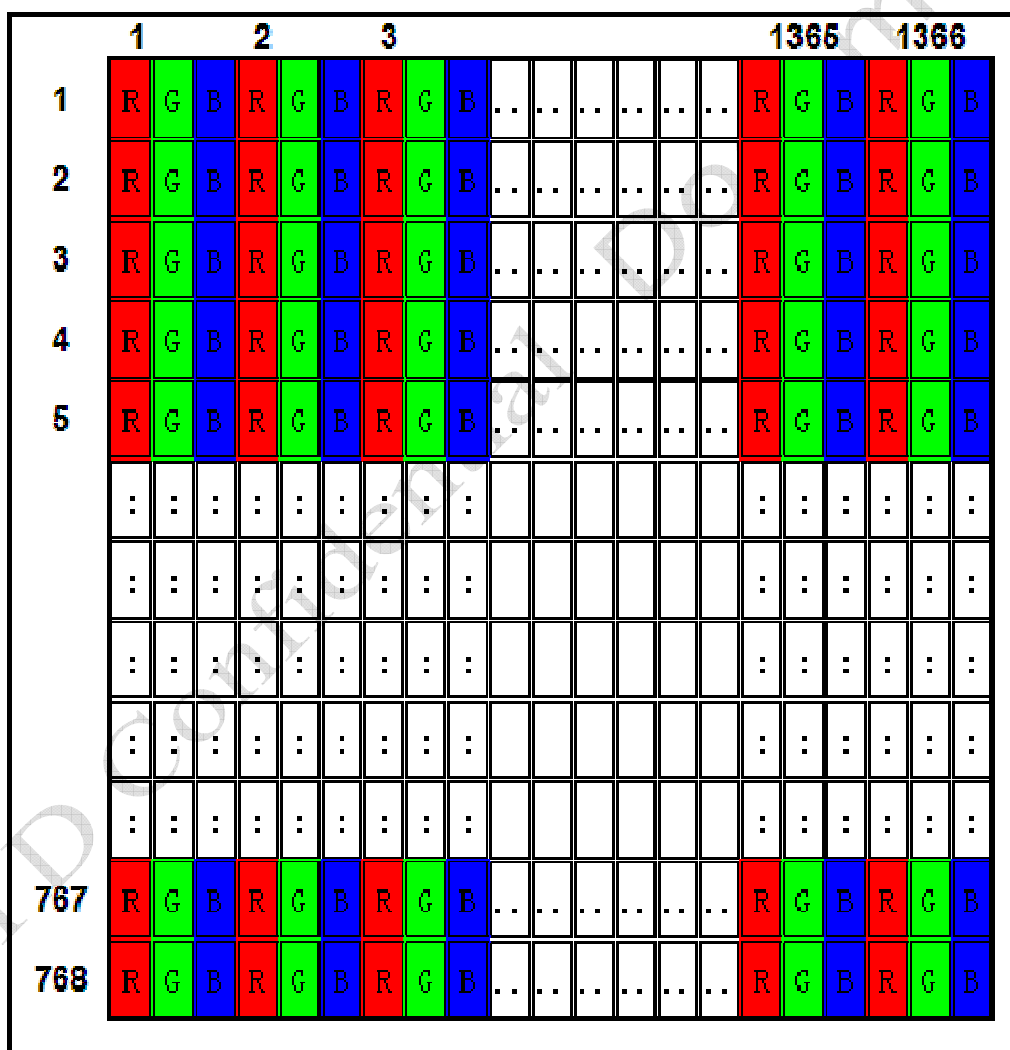(3) Storage /Operating temperature

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3.0 Pixel Format Image

Figure 2 shows the relationship of the input signals and LCD pixel format image.

Figure 2 Pixel Format

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4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes

Table 2 Optical Characteristics

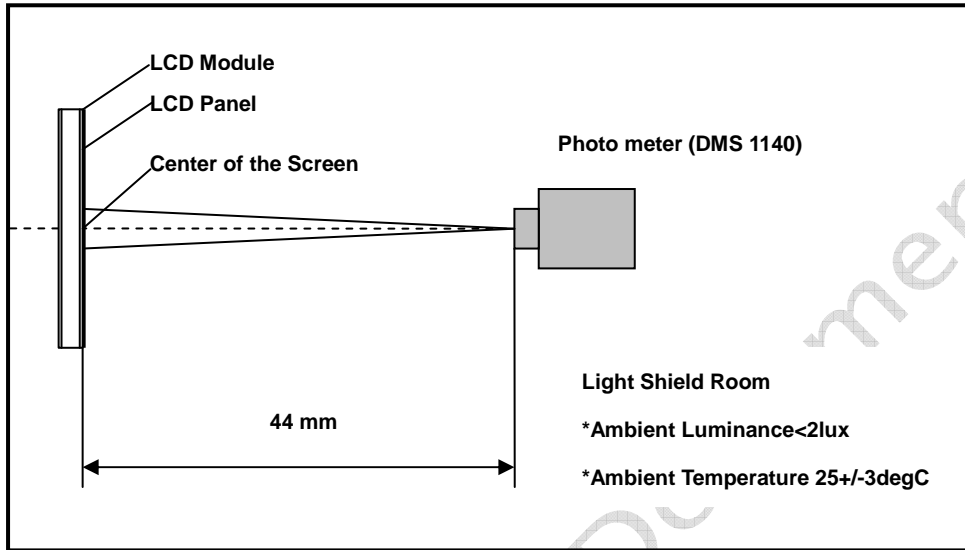| Item	Conditions		Specification			
			Min	Typ.	Max	Note
Viewing Angle [degrees] K=Contrast Ratio>10	Horizontal	Left	70	75	-	A, B
		Right	70	75	-	
	Vertical	Up	45	50	-	
		Down	55	60	-	
Contrast ratio	Center		350	500	-	A, C
Response Time [ms]	Rising + Falling		-	8	16	A, D
Color Chromaticity (CIE1931)	Red	x	Typ. -0.03	0.581	Typ. +0.03	A,
	Red	y		0.343		A,
	Green	x		0.334		A,
	Green	y		0.570		A,
	Blue	x		0.156		A,
	Blue	y		0.130		A,
	White	x	0.263	0.313	0.363	A,
	White	y	0.279	0.329	0.379	A,
White Luminance [cd/m^2]	I-LED=20.0mA		200	220	-	5point A, E
Luminance Uniformity [%]	I-LED =20mA, 13points		60	-	-	A, F
	I-LED =20mA, 5points		80	-	-	

Note: A. Measurement Setup:

The LCD module should be stabilized at 25□ for 15 minutes to avoid

abrupt temperature change during measuring. In order to stabilize the luminance, the

measurement should be executed after lighting backlight for 15 minutes in a windless
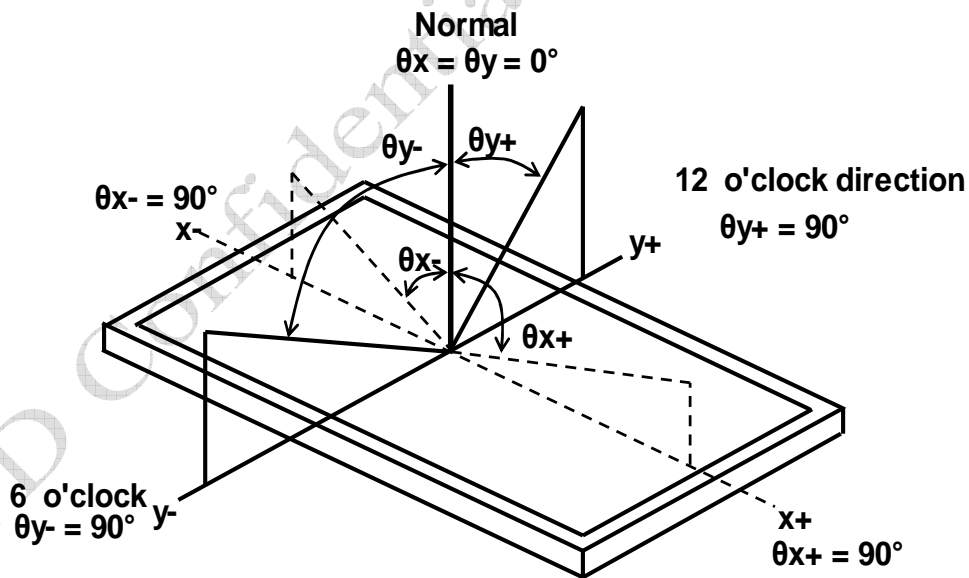
room.

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Figure 3 Measurement Setup

B. Definition of Viewing Angle

Figure 4 Definition of Viewing Angle

C. Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression
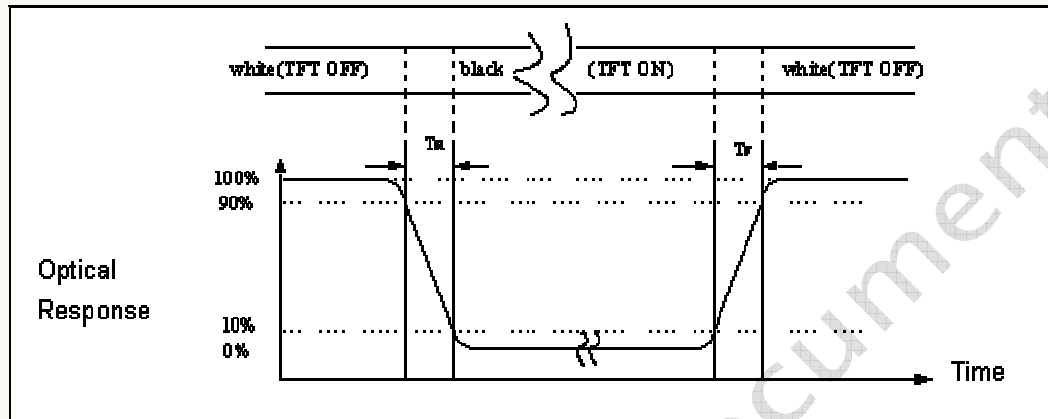
Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

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D. Definition of Response Time (T_R, T_F)

Figure 5 Definition of Response Time

E. Definition of Luminance White

Measure the luminance of gray level 63 at center point and 5 points.

Center of Luminance = Y1

Average Luminance of 5 points = $\dfrac{Y_1 + Y_2 + Y_3 + Y_4 + Y_5}{5}$

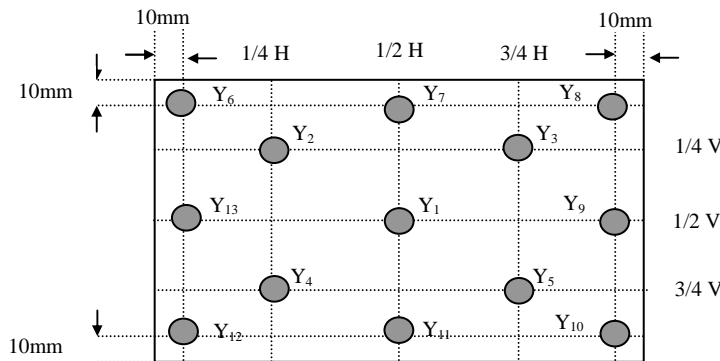F. Definition of Luminance Uniformity(Variation)

Measure the luminance of gray level 63 at 13 points.

Uniformity of 13 points = $\dfrac{\text{Min Luminance of Y1}\sim\text{Y13}}{\text{Max Luminance of Y1}\sim\text{Y13}}$ x 100%

Uniformity of 5 points = $\dfrac{\text{Min Luminance of Y1}\sim\text{Y5}}{\text{Max Luminance of Y1}\sim\text{Y5}}$ x 100%

Figure 6 Measurement Locations of 13 Points

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5.0 Backlight Characteristics
5.1 Parameter Guideline of LED Backlight
Table 3 Parameter Guideline for LED Backlight

Symbol	Parameter		Min.	Typ.	Max.	Units	Condition
VLED	LED input		6	12	21	[V]	Note A
V_F	LED Forward Voltage		2.9	3.3	3.4	[V]	Ta=25
I_F	LED Forward Current			20		[mA]	Ta=25
P_{LED}	LED Power Consumption		-	-	3.0	[W]	Ta=25[deg C] Note B
LT	LED Life Time		10,000	-	-	Hours	Ta=25[deg C] Note C
VPWM_EN	PWM Signal Voltage	High	2.0	3.3	3.6	V	-
		Low	0	-	0.5	V	
FPWM	Output PWM frequency		-	200	1K	Hz	-
VLED_EN	LED enable Voltage	High	2.0	3.3	3.6		-
		Low	0	-	0.5	V	
PWM	PWM Duty ratio		5	-	100	%	-

Note A: A higher LED power supply voltage will result in better power efficiency. Keep the V_{LED} between 12V and 21V is strongly recommended.

Note B: Calculator value for LED chip specification.

Note C: The lifetime of LED is defined as the time when LED packages continue to operate under the conditions at Ta = 25℃ and I_F= 20 mA (per chip) until the brightness becomes ≦50% of its original value.

Note D: All values are measured at condition of V_{LED} =12V、Ta=25℃ and 55%RH.

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6.0 Electrical Characteristics
6.1 Interface Connector

Table 4 Connector Name / Designation

Manufacturer	UJU (or equivalent)
Type / Part Number	IS050-L40B-C10
Mating Receptacle/Part Number	HS050-L40N-N10

Table 5 Signal Pin Assignment

Pin #	Signal Name	Description	Remarks
1	NC	Not connected	
2	VDD	Power supply	3.3V(Typ.)
3	VDD	Power supply	3.3V(Typ.)
4	VEDID	EDID Power	3.3V(Typ.)
5	NC	Not connected(Reserve)	
6	SCLK_EDID	EDID Clock Input	
7	SDAT_EDID	EDID Data Input	
8	Rin0-	$-$LVDS differential data input(R0-R5,G0)	
9	Rin0+	$+$LVDS differential data input(R0-R5,G0)	
10	GND	Ground	
11	Rin1-	$-$LVDS differential data input(G1-G5,B0-B1)	
12	Rin1+	$+$LVDS differential data input(G1-G5,B0-B1)	
13	GND	Ground	
14	Rin2-	$-$LVDS differential data input(B2-B5,HS,VS,DE)	
15	Rin2+	$+$LVDS differential data input(B2-B5,HS,VS,DE)	
16	GND	Ground	
17	RX_OCLK-	$-$LVDS differential clock input	
18	RX_OCLK+	$+$LVDS differential clock input	
19	NC	Not connected(Reserved for Color Engine)	
20	NC	Not connected	
21	NC	Not connected	
22	GND	Ground-Shield	
23	NC	Not connected	
24	NC	Not connected	
25	GND	Ground-Shield	

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26	NC	Not connected	
27	NC	Not connected	
28	GND	Ground-Shield	
29	NC	Not connected	
30	NC	Not connected	
31	VLED_GND	LED Ground	
32	VLED_GND	LED Ground	
33	VLED_GND	LED Ground	
34	NC	Not connected	
35	VPWM_EN	System PWM Logic Input Level	
36	VLED_EN	LED enable Input Level	3.3V(Typ.)
37	NC	Not connected（Reserved for DBC）	
38	VLED	LED Power Supply 6～21V	12V(Typ.)
39	VLED	LED Power Supply 6～21V	12V(Typ.)
40	VLED	LED Power Supply 6～21V	12V(Typ.)

Note: All input signals shall be low or Hi-Z state when VDD is off.

6.2 LVDS Receiver

6.2.1 Signal Electrical Characteristics for LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

Table 6 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Conditions
Differential Input High Threshold	Vth	-	-	+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100	-	-	mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100	-	600	mV	
Common Mode Voltage	Vcm	0.9	1.2	1.5	V	
Common Mode Voltage Offset	ΔVcm	-	-	50	mV	Vcm=+1.2V

Note:

A. Input signals shall be low or Hi-Z state when VDD is off.

B. All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Note: All values are at VDD=3.3V, Ta=25 degree C.

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Figure 7 Voltage Definitions
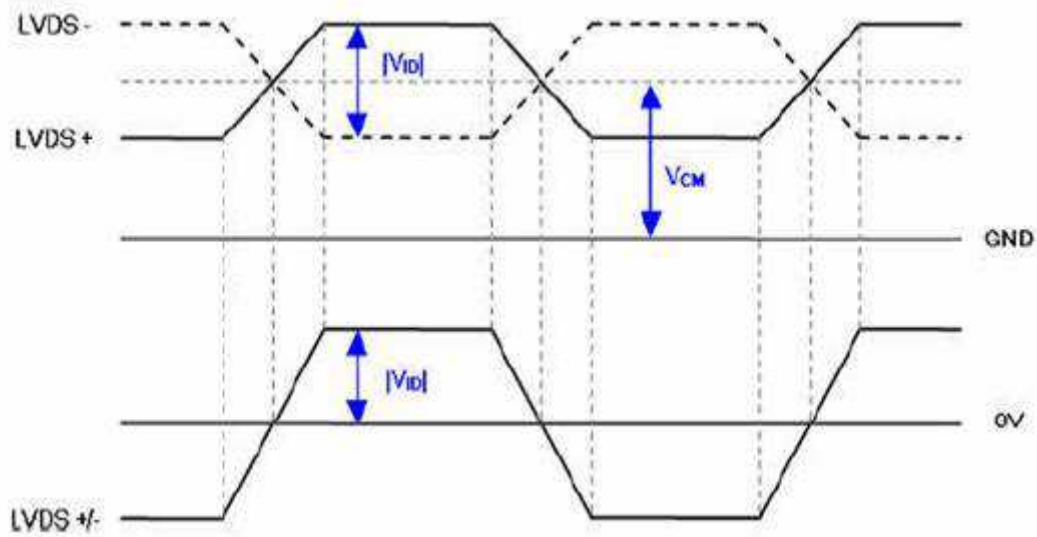
Figure 8 Measurement System

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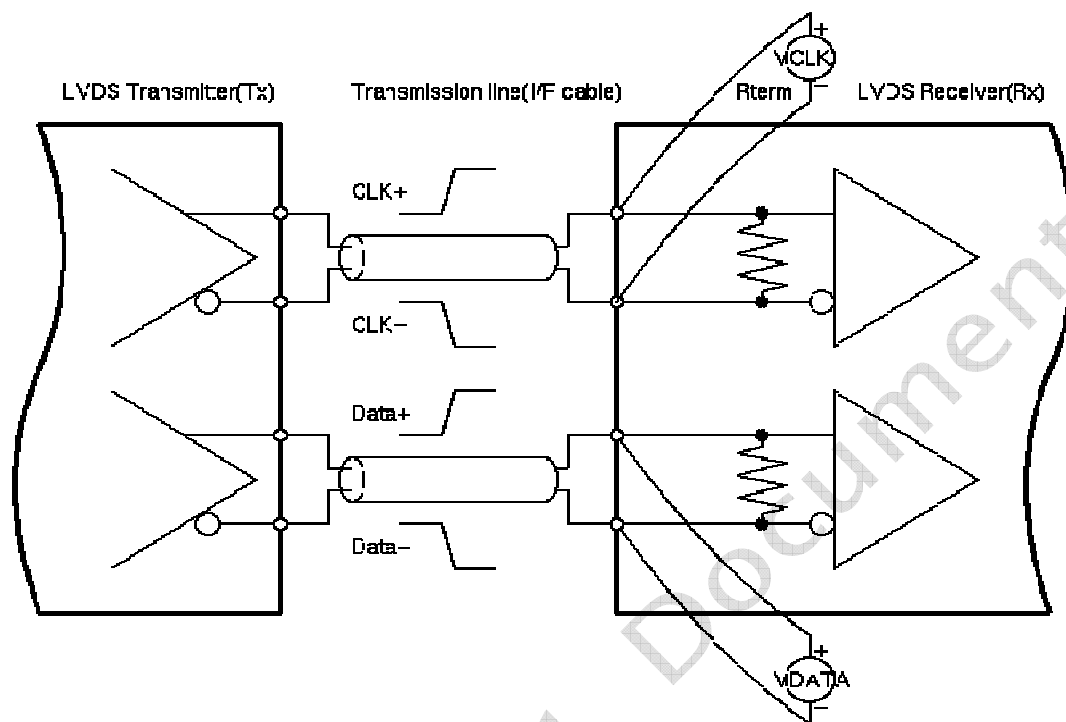
Figure 9 Data mapping
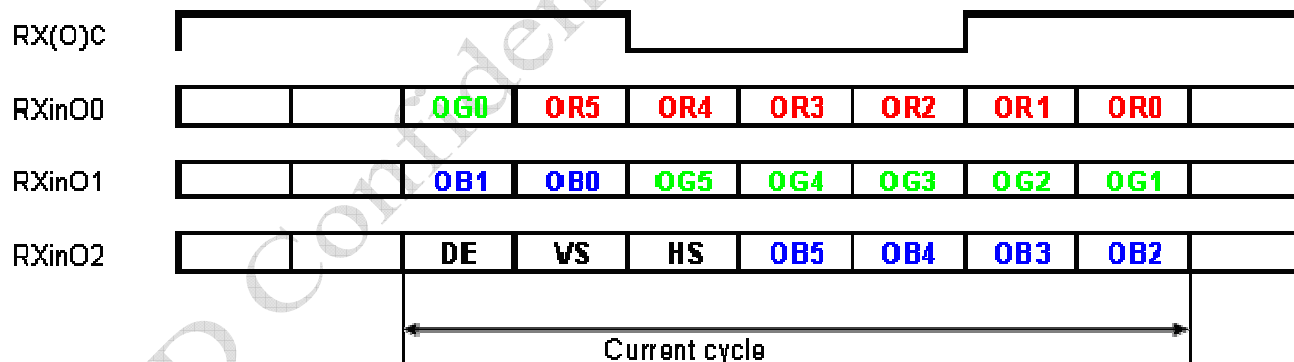
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6.2.2 LVDS Receiver Internal Circuit

Figure 10 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 10 LVDS Receiver Internal Circuit
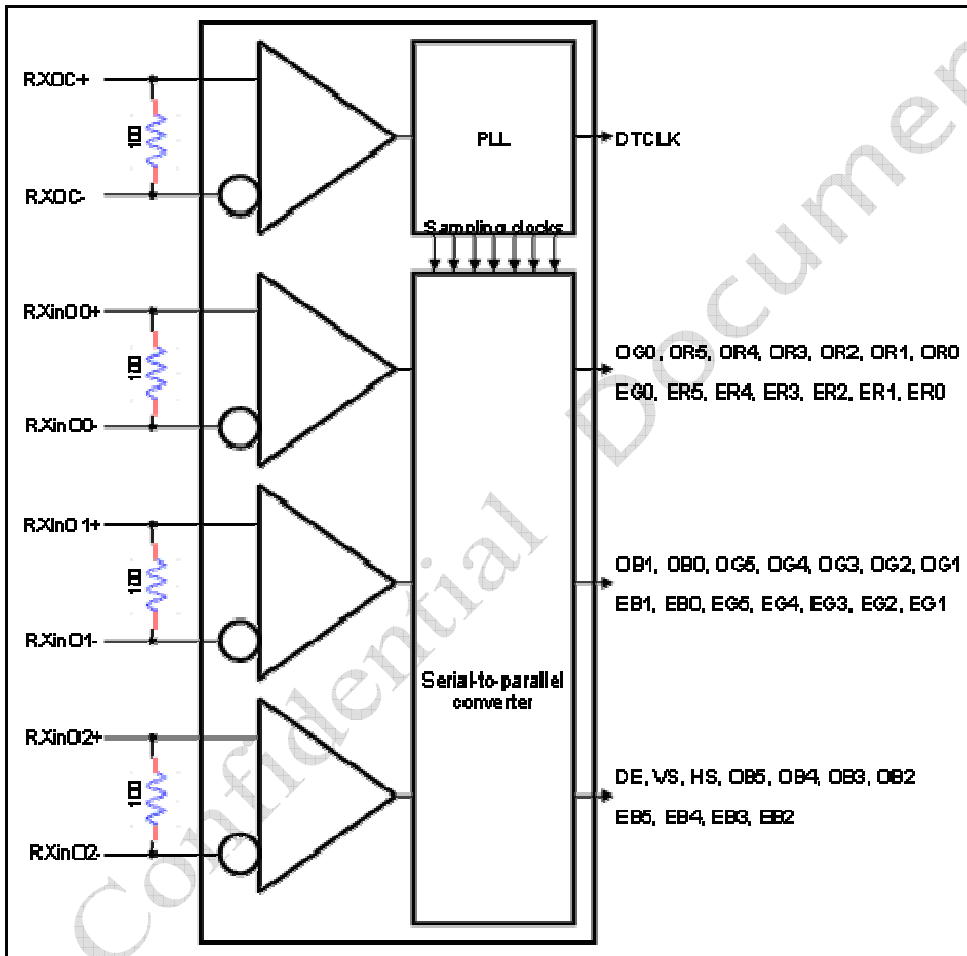
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7.0 Interface Timings

7.1 Timing Characteristics

Table 7 Interface Timings

Parameter	Symbol	Unit	min	Typ.	Max
LVDS Clock Frequency(single)	F_{dck}	MHz	65.88	76.85	82.67
H Total Time	H_{total}	clocks	1520	1560	1690
H Active Time	H_{ac}	clocks	1366	1366	1366
V Total Time	V_{total}	lines	788	821	850
V Active Time	V_{ac}	lines	768	768	768
Frame Rate	V_{sync}	Hz	55	60	65

Figure 11 Timing Characteristics
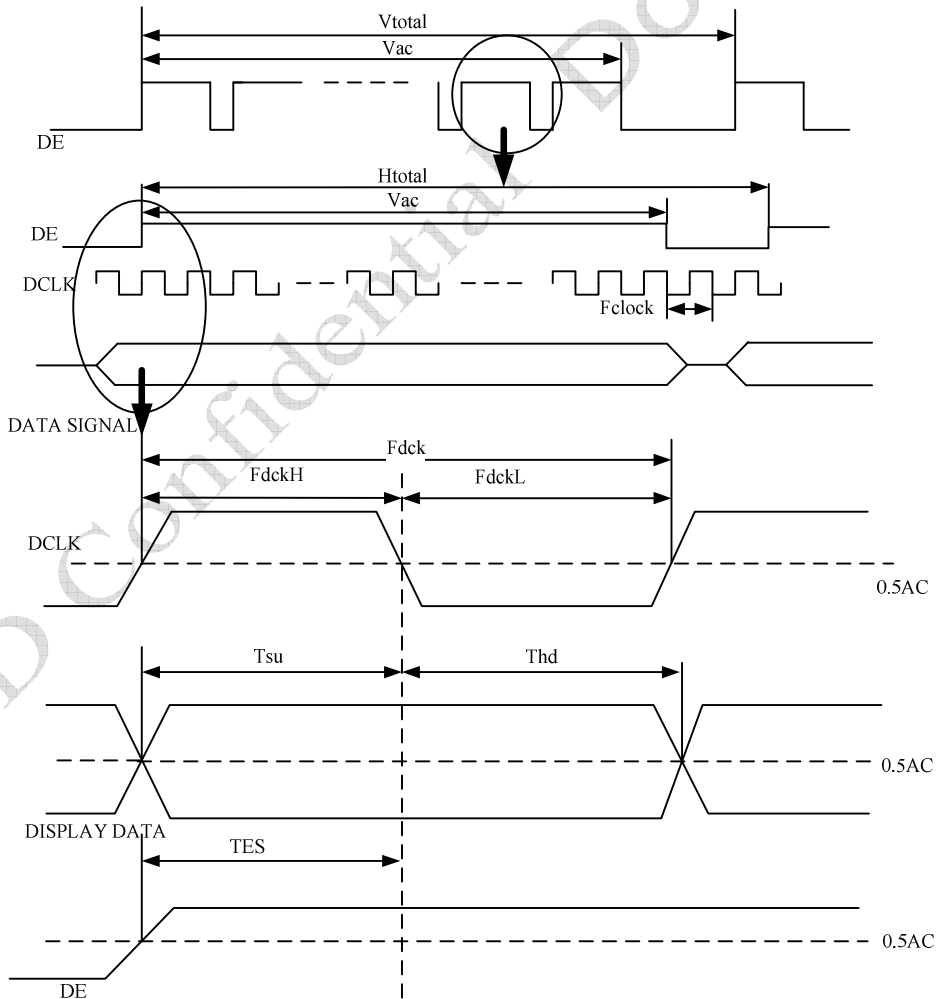
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Note: TES is data enable signal setup time.

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8.0 Power Consumption

Input power specifications are as follows.

Table 8 Power Consumption

Symbol	Parameter	Min	Typ.	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	-
IDD	VDD Current	-	280	340	[mA]	Black pattern, 60Hz
PDD	VDD Power	-	-	1.2	[W]	Black pattern, 60Hz
Irush	Rush Current	-	-	2	[A]	Note A
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	300	[mVp-p]	-

Note: A. Measure Condition

Figure 12   VDD rising time
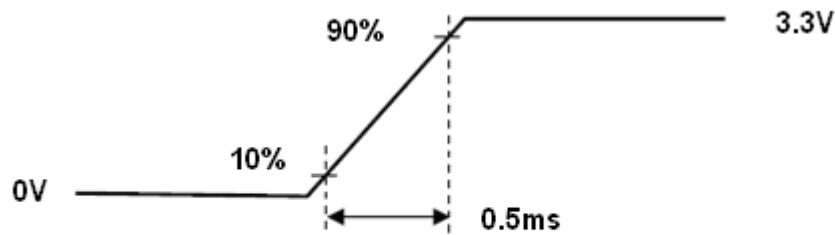
VDD rising time

B.VDD Power Dip Condition

Figure 13   VDD Power Dip
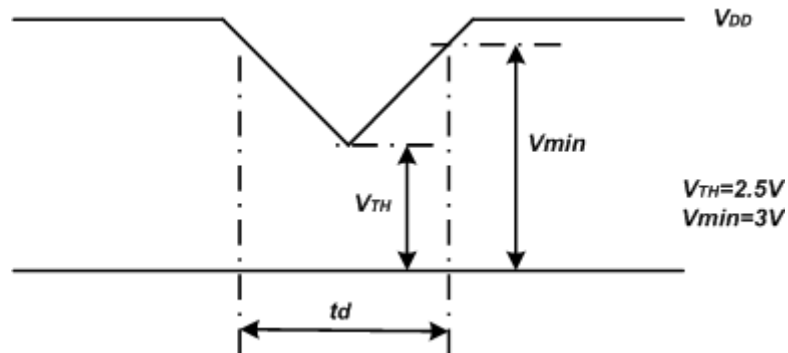
If $V_{TH} < V_{DD} \leq V_{min}$，then $t_d \leq 10ms$；when the voltage return to normal our panel must revive automatically.

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9.0 Power ON/OFF Sequence

VDD power, interface signals, and lamp on/off sequence are shown in

.Signals shall be Hi-Z state or low level when VDD is off.

Table 9 Power Sequencing Requirements
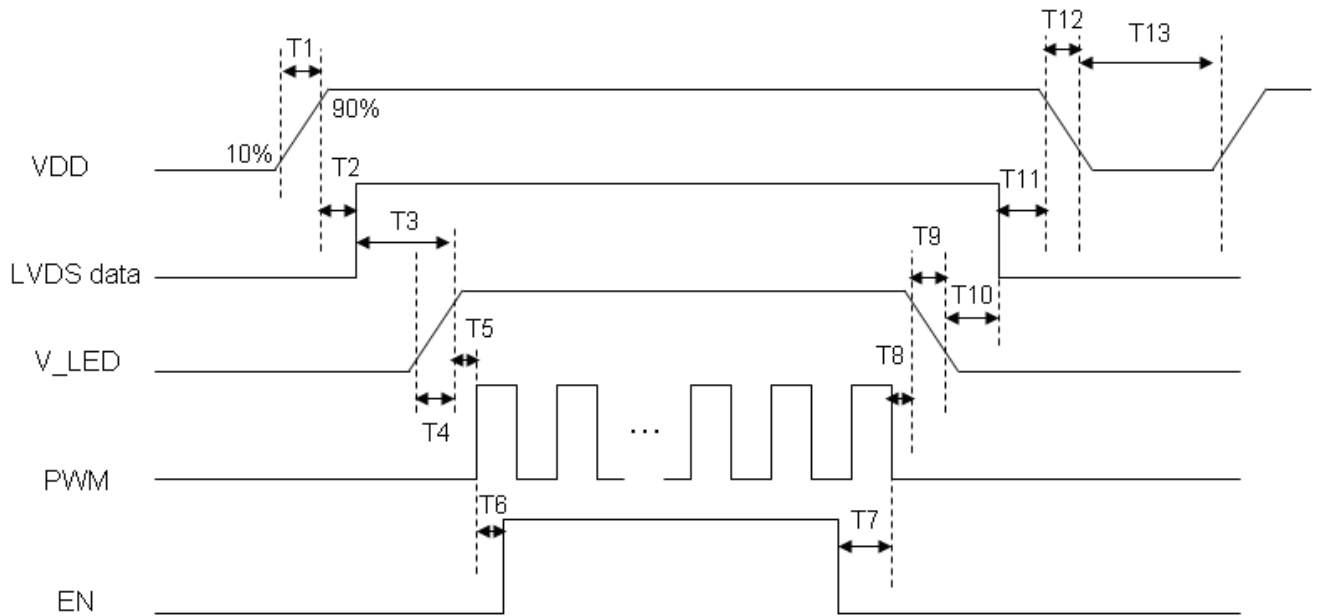
Parameter	Symbol	Unit	min	typ	max
VDD Rise Time	T1	ms	0.5	--	10
VDD Good to Signal Valid	T2	ms	30	--	90
Signal Valid to Backlight On	T3	ms	200	--	--
Backlight Power On Time	T4	ms	0.5	--	--
Backlight VDD Good to System PWM On	T5	ms	10	--	--
System PWM ON to Backlight Enable ON	T6	ms	10	--	--
Backlight Enable Off to System PWM Off	T7	ms	0	--	--
System PWM Off to B/L Power Disable	T8	ms	10	--	--
Backlight Power Off Time	T9	ms	--	10	30
Backlight Off to Signal Disable	T10	ms	200	--	--
Signal Disable to Power Down	T11	ms	0	--	50
VDD Fall Time	T12	ms	--	10	30
Power Off	T13	ms	500	--	--

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10.0 Mechanical Characteristics

Figure 14 Reference Outline Drawing (Front Side)
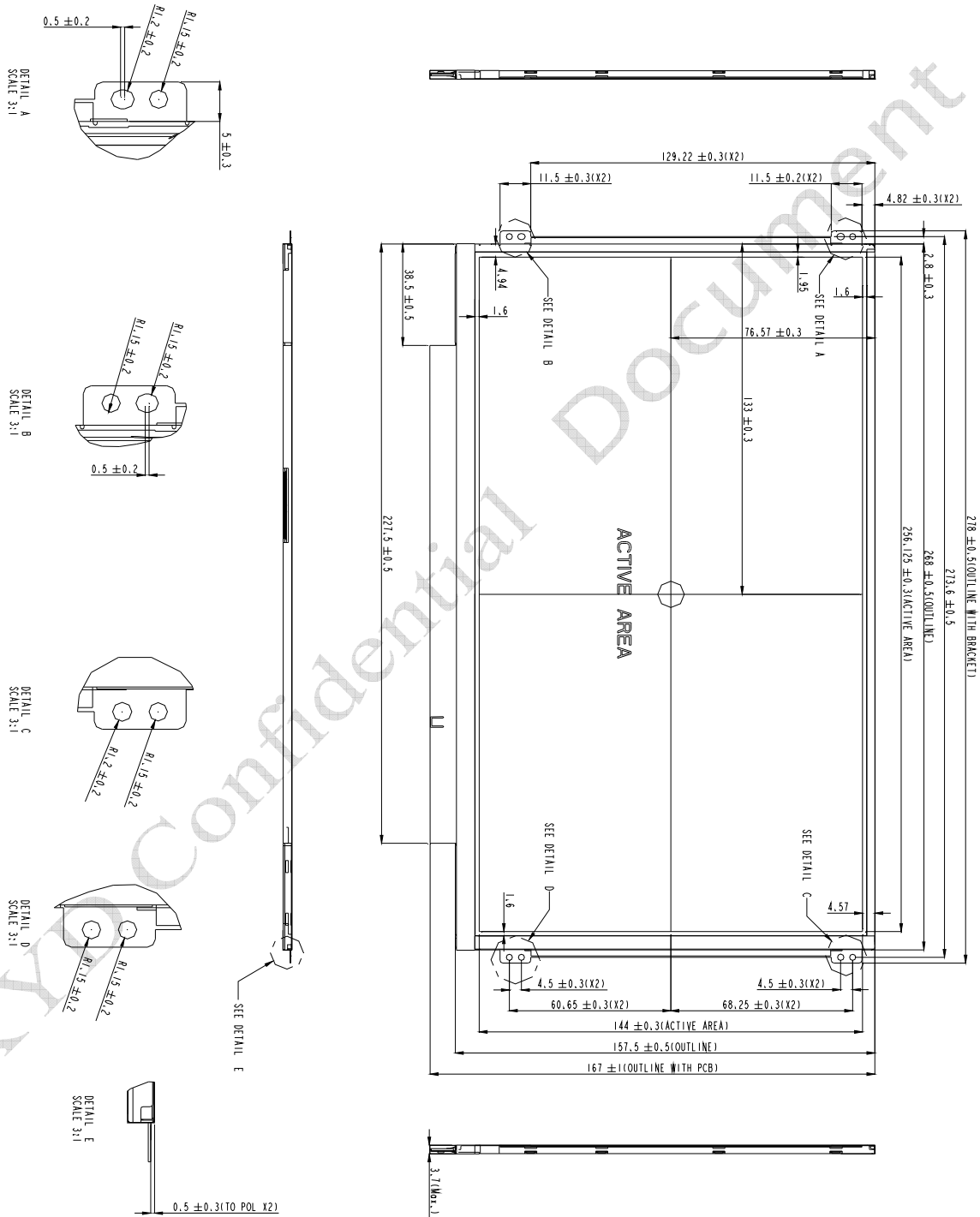
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Figure15 Reference O Outline Drawing (Back Side)
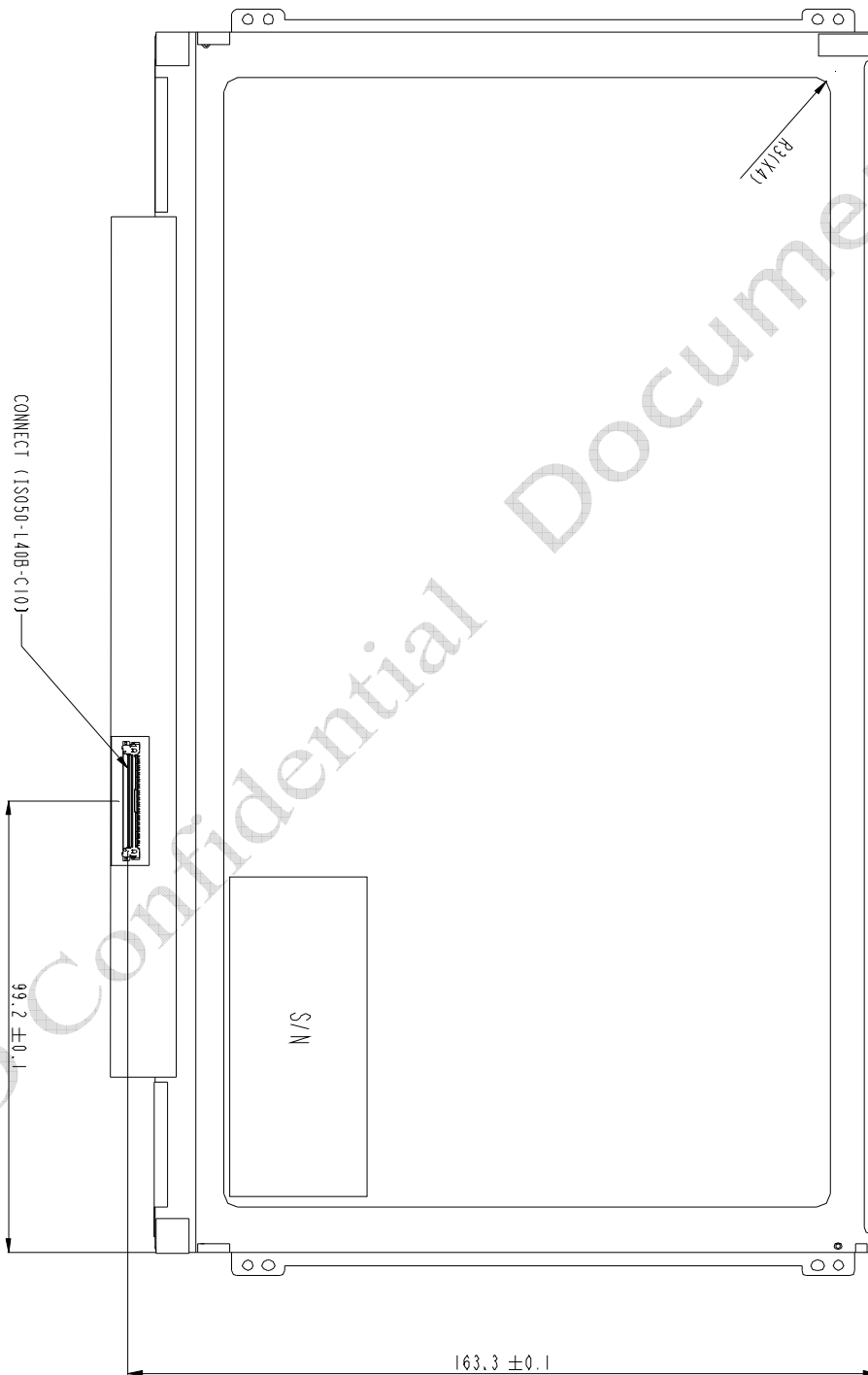
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10.1 Dimension Specifications

Table 10

Width [mm]			278.0±0.5
Height [mm]			167.0±1.0
Thickness [mm]			3.7 (max)
Tape Opening [mm]		X	259.675±0.3
		Y	147.200±0.3
Weight [g]			235 (max)
BM Width [mm]	｜a-b｜ & ｜c-d｜		≤1.0
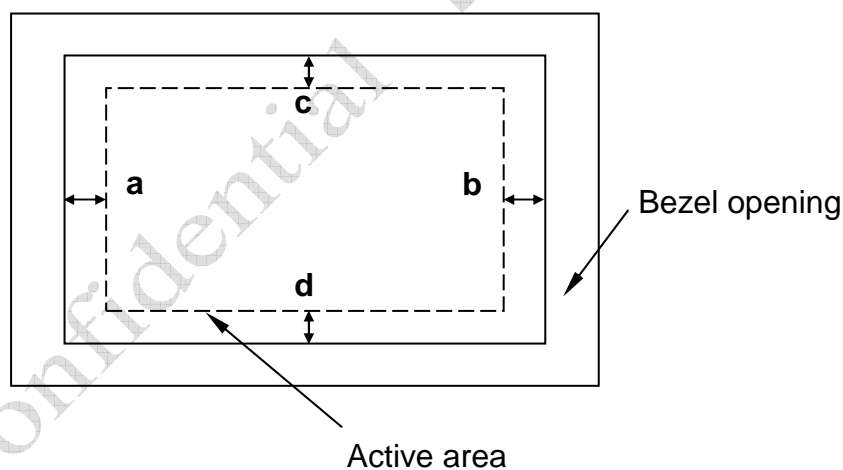
Bezel opening

Active area

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11.0 Package Specification
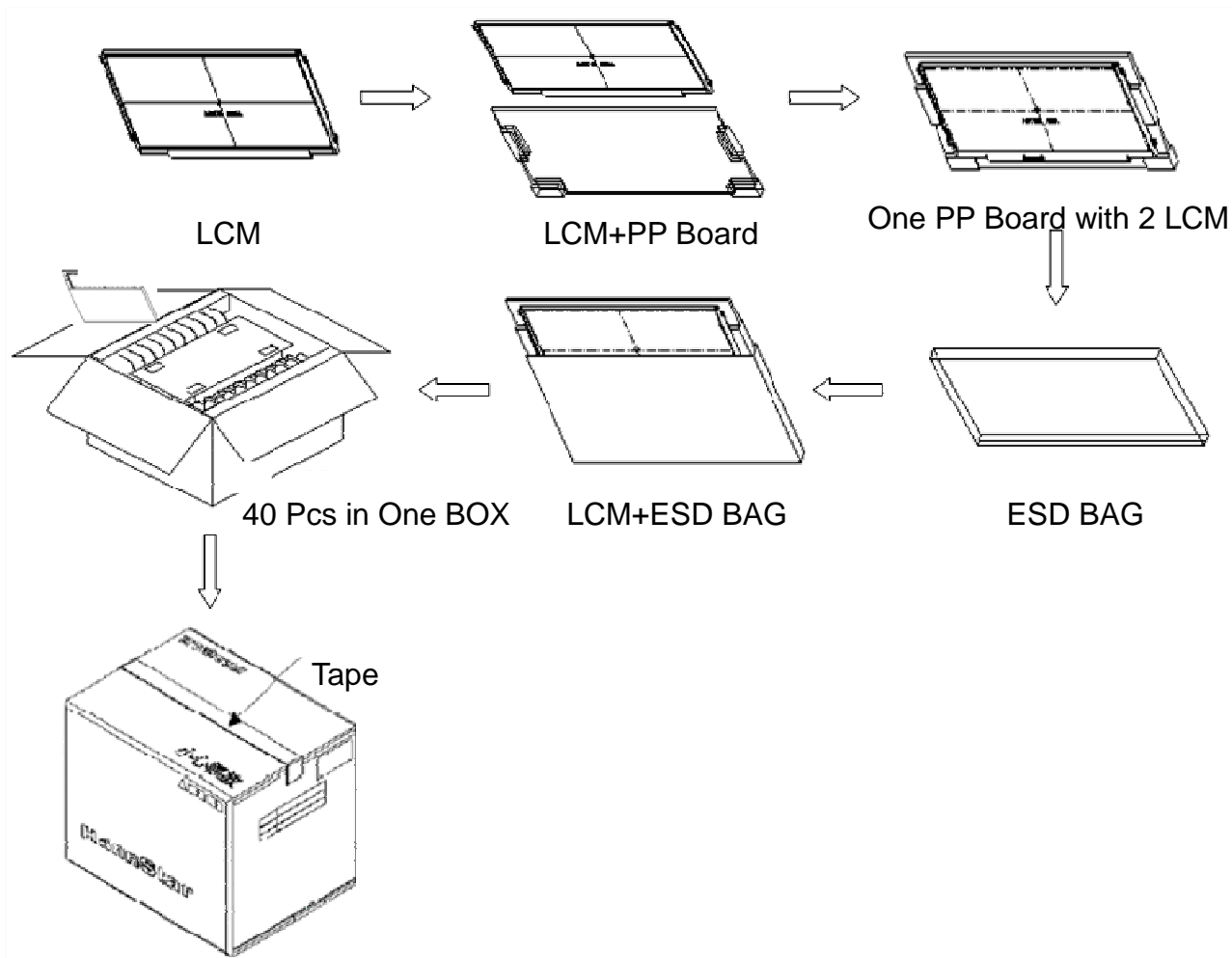
LCM → LCM+PP Board → One PP Board with 2 LCM

40 Pcs in One BOX ← LCM+ESD BAG ← ESD BAG

Tape

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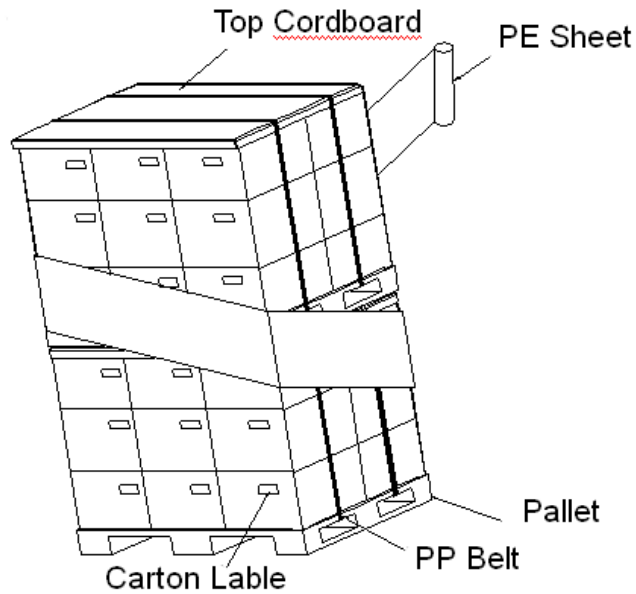
12.0 Lot Mark

12.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

code 1,2,4,5,6,7,8,9,10,11,16: KYOCERA DISPLAY internal flow control code.
code 3: production location.
code 12: production year.
code 13: production month.
code 14,15: production date.

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Code 17,18,19,20: serial number.

Note (1) Production Year

Year	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
Mark	6	7	8	9	A	B	C	D	E	F

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

12.2 23 product barcode

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

code 1,2: MD Module Domain.
code 3,4,5,6,7: KYOCERA DISPLAY internal module name.
code 8,9,10,13,16: KYOCERA DISPLAY internal flow control code.
code 11,12: Cell location Suzhou defined as "SZ".
code 14 ,15: Module line kunshan defined as" KS".
code 17,18,19 : Year, Month, Day Refer to KYOCERA DISPLAY barcode Note(1),Note(2).
code 20~23 : Serial Number.

13.0 General Precaution
13.1 Use Restriction
This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.
13.2 Handling Precaution
1) Please mount LCD module by using mounting holes arranged in four corners tightly.
2) Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. KYOCERA DISPLAY does not warrant the module, if customers disassemble or modify the module.
3) If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid Crystal, and do not contact liquid crystal with skin. If liquid crystal contacts mouth or eyes, rinse

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out with water immediately. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and Rinse thoroughly with water.

4) Disconnect power supply before handling LCD module.

5) Refrain from strong mechanical shock and /or any force to the module.

6) Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature; etc otherwise LCD module may be damaged. It's recommended employing protection circuit for power supply.

7) Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when Persons handle the LCD module for incoming inspection or assembly.

8) When the surface is dusty, please wipe gently with absorbent cotton or other soft Material. When cleaning the adhesives, please use absorbent cotton wetted with a little Petroleum benzene or other adequate solvent.

9) Wipe off saliva or water drops as soon as possible. If saliva or water drops Contact with polarizer for a long time, they may causes deformation or color Fading.

10) Protection film must remove very slowly from the surface of LCD module to
Prevent from electrostatic occurrence.

11) Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is Very weak to electrostatic discharge, Please be careful with electrostatic Discharge .Persons who handle the module should be grounded through adequate methods.

12) Do not adjust the variable resistor located on the module.

13.3 Storage Precaution

1) Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

2) The module shall not be exposed under strong light such as direct sunlight. Otherwise, Display characteristics may be changed.

3) The module should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storage.

13.4 Operation Precaution

1) Do not connect or disconnect the module in the "Power On" condition.

2) Power supply should always be turned on/off by 9.0 "Power on/off sequence".

3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

4) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

13.5 Others

1) Ultra-violet ray filter is necessary for outdoor operation.

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2) Avoid condensation of water which may result in improper operation or disconnection of electrode.

3) If the module keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen.

4) This module has its circuitry PCB's on the down side and should be handled carefully in order not to be stressed.

13.6 Disposal

When disposing LCD module, obey the local environmental regulations.

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14.0 EDID Data Structure

Address	Address	Field Name & Comments	Value	Value	Value
(Decimal)	(HEX)		(HEX)	(BIN)	(DEC)
0	0	Header	00	00000000	0
1	1	Header	FF	11111111	255
2	2	Header	FF	11111111	255
3	3	Header	FF	11111111	255
4	4	Header	FF	11111111	255
5	5	Header	FF	11111111	255
6	6	Header	FF	11111111	255
7	7	Header	00	00000000	0
8	8	manufacture code	26	00100110	38
9	9	manufacture code	CF	11001111	207
10	0A	Product Code	89	10001001	137
11	0B	Product Code	04	00000100	4
12	0C	LCD module Serial No –("0" if not used)	00	00000000	0
13	0D	LCD module Serial No –("0" if not used)	00	00000000	0
14	0E	LCD module Serial No –("0" if not used)	00	00000000	0
15	0F	LCD module Serial No –("0" if not used)	00	00000000	0
16	10	Week of manufacture	1E	00011110	30
17	11	Year of manufacture	14	00010100	20
18	12	EDID Structure Ver # = 1	01	00000001	1
19	13	EDID revision # = 3	03	00000011	3
20	14	Video I/P definition = Digital I/P (80h)	80	10000000	128
21	15	Max H image size = (Rounded to cm)	1A	00011010	26
22	16	Max V image size = (Rounded to cm)	0E	00001110	14
23	17	Display Gamma	78	01111000	120
24	18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A	00001010	10
25	19	Red/Green Low bits (RxRy/GxGy)	BB	10111011	187
26	1A	Blue/White Low bits (BxBy/WxWy)	D0	11010000	208
27	1B	Red X Rx	94	10010100	148
28	1C	Red Y Ry	57	01010111	87
29	1D	Green X Gx	55	01010101	85
30	1E	Green Y Gy	91	10010001	145
31	1F	Blue X Bx	27	00100111	39
32	20	Blue Y By	21	00100001	33
33	21	White X Wx	50	01010000	80
34	22	White Y Wy	54	01010100	84
35	23	Established timings 1 (00h if not used)	00	00000000	0
36	24	Established timing 2 (00h if not used)	00	00000000	0
37	25	Manufacturer's timings (00h if not used)	00	00000000	0
38	26	Standard timing ID1 (01h if not used)	01	00000001	1
39	27	Standard timing ID1 (01h if not used)	01	00000001	1
40	28	Standard timing ID2 (01h if not used)	01	00000001	1

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41	29	Standard timing ID2 (01h if not used)	01	00000001	1
42	2A	Standard timing ID3 (01h if not used)	01	00000001	1
43	2B	Standard timing ID3 (01h if not used)	01	00000001	1
44	2C	Standard timing ID4 (01h if not used)	01	00000001	1
45	2D	Standard timing ID4 (01h if not used)	01	00000001	1
46	2E	Standard timing ID5 (01h if not used)	01	00000001	1
47	2F	Standard timing ID5 (01h if not used)	01	00000001	1
48	30	Standard timing ID6 (01h if not used)	01	00000001	1
49	31	Standard timing ID6 (01h if not used)	01	00000001	1
50	32	Standard timing ID7 (01h if not used)	01	00000001	1
51	33	Standard timing ID7 (01h if not used)	01	00000001	1
52	34	Standard timing ID8 (01h if not used)	01	00000001	1
53	35	Standard timing ID8 (01h if not used)	01	00000001	1
54	36	Pixel Clock LSB	05	00000101	5
55	37	Pixel Clock HSB	1E	00011110	30
56	38	Horizontal Active (lower 8 bits)	56	01010110	86
57	39	Hor blanking (lower 8 bits)	C2	11000010	194
58	3A	Horizontal Active/Horizontal blanking (upper4:4 bits)	50	01010000	80
59	3B	Vertcal active(lower 8 bits)	00	00000000	0
60	3C	Vertical blanking(lower 8 bits)	35	00110101	53
61	3D	Vertical Active : Vertical Blanking (upper4:4 bits)	30	00110000	48
62	3E	Horizontal Sync Offset	30	00110000	48
63	3F	Horizontal Sync Pulse Width	20	00100000	32
64	40	Vertical Sync Offset , Sync Width	3C	00111100	60
65	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
66	42	Horizontal Image Size	00	00000000	0
67	43	Vertical image Size	90	10010000	144
68	44	Horizontal Image Size / Vertical image size	10	00010000	16
69	45	Horizontal Border = (0 for Notebook LCD)	00	00000000	0
70	46	Vertical Border = (0 for Notebook LCD)	00	00000000	0
71	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives,	19	00011001	25
72	48	Timing Descriptor #2	00	00000000	0
73	49		00	00000000	0
74	4A		00	00000000	0
75	4B		00	00000000	0
76	4C		00	00000000	0
77	4D		00	00000000	0
78	4E		00	00000000	0
79	4F		00	00000000	0
80	50		00	00000000	0
81	51		00	00000000	0
82	52		00	00000000	0
83	53		00	00000000	0
84	54		00	00000000	0
85	55		00	00000000	0

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86	56		00	00000000	0
87	57		00	00000000	0
88	58		00	00000000	0
89	59		00	00000000	0
90	5A	Detailed timing/monitor descriptor#3	00	00000000	0
91	5B	Flag	00	00000000	0
92	5C	Flag	00	00000000	0
93	5D	Range limits	FD	11111101	253
94	5E	Flag	00	00000000	0
95	5F	Min. Vertical Freq	37	00110111	55
96	60	Max. Vertical Freq	41	01000001	65
97	61	Min. Horizontal Freq	2B	00101011	43
98	62	Max.Horizontal Freq	31	00110001	49
99	63	Max. Pixel Clock Freq	08	00001000	8
100	64		00	00000000	0
101	65		0A	00001010	10
102	66		20	00100000	32
103	67		20	00100000	32
104	68		20	00100000	32
105	69	New line character indicates end of ASCII string	20	00100000	32
106	6A		20	00100000	32
107	6B		20	00100000	32
108	6C	Detailed timing/monitor descriptor #4	00	00000000	0
109	6D		00	00000000	0
110	6E		00	00000000	0
111	6F	FE (hex) defines ASCII string	FC	11111100	252
112	70	Flag	00	00000000	0
113	71	Manufacture P/N	4D	01001101	77
114	72	Manufacture P/N	31	00110001	49
115	73	Manufacture P/N	31	00110001	49
116	74	Manufacture P/N	36	00110110	54
117	75	Manufacture P/N	4E	01001110	78
118	76	Manufacture P/N	57	01010111	87
119	77	Manufacture P/N	52	01010010	82
120	78	Manufacture P/N	31	00110001	49
121	79	Manufacture P/N	20	00100000	32
122	7A	Manufacture P/N	52	01010010	82
123	7B	Manufacture P/N	31	00110001	49
124	7C	New line character indicates end of ASCII string	20	00100000	32
125	7D		0A	00001010	10
126	7E	Extension Flag = 00	00	00000000	0
127	7F	Checksum	1E	00011110	30