19-3156; Rev 2; 12/04

+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

General Description

The MAX3013 8-channel level translator provides the level shifting necessary to allow 100Mbps data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa.

The MAX3013 features an EN input that, when at logic low, places all inputs/outputs on both sides in tristate and reduces the V_{CC} and V_L supply currents to 0.1µA. This device operates at a guaranteed data rate of 100Mbps for V_L > 1.8V.

The MAX3013 accepts a V_{CC} voltage from +1.65V to +3.6V and a V_L voltage from +1.2V to (V_{CC} - 0.4V), making it ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX3013 is available in 5 x 4 UCSP™, 20-pin 5mm x 5mm QFN, and 20-pin TSSOP packages.

Applications

Low-Voltage ASIC Level Translation

Cell Phones

SPI™, MICROWIRE™ Level Translation

Portable POS Systems

Portable Communication Devices

GPS

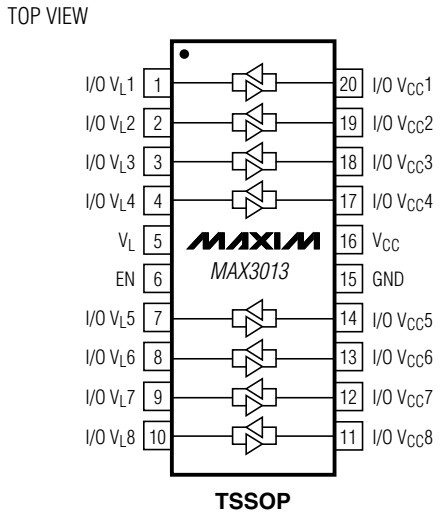
Telecommunications Equipment

UCSP is a trademark of Maxim Integrated Products, Inc.
SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **100Mbps Guaranteed Data Rate**
- **Bidirectional Level Translation**
- **V_L Operation Down to +1.2V**
- **Ultra-Low 0.1µA Supply Current in Shutdown**
- **Low-Quiescent Current (0.1µA)**
- **UCSP, QFN, and TSSOP Packages**

Pin Configurations



Pin Configurations continued at end of data sheet.

Typical Operating Circuit appears at end of data sheet.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	NUMBER OF $V_L \rightarrow V_{CC}$ TRANSLATORS	NUMBER OF $V_L \leftarrow V_{CC}$ TRANSLATORS	DATA RATE (Mbps)
MAX3013EUP	-40°C to +85°C	20 TSSOP	8	8	100
MAX3013EBP-T	-40°C to +85°C	5 x 4 UCSP	8	8	100
MAX3013EGP	-40°C to +85°C	20 QFN-EP*	8	8	100

**EP = Exposed paddle.*

+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} .....-0.3V to +4V
V_L.....-0.3V to +4V
I/O V_{CC} .....-0.3V to (V_{CC} + 0.3V)
I/O V_L.....-0.3V to (V_L + 0.3V)
EN .....-0.3V to (V_L + 0.3V)
Short-Circuit Duration I/O V_L, I/O V_{CC} to GND.....Continuous

Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 11mW/°C above +70°C) 879mW
5 x 4 UCSP (derate 10mW/°C above +70°C) 800mW
20-Pin QFN (derate 20.0mW/°C above +70°C) 1.60W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V) (Note 1), EN = V_L, C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 40pF, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_L Supply Range	V_L		1.2		V_{CC} - 0.4	V
V_{CC} Supply Range	V_{CC}		1.65		3.6	V
Supply Current from V_{CC}	I_{QVCC}	I/O $V_{CC\_}$ = 0, I/O V_L _ = 0 or I/O $V_{CC\_}$ = V_{CC}, I/O V_L _ = V_L		0.1	1	µA
Supply Current from V_L	I_{QVL}	I/O $V_{CC\_}$ = 0, I/O V_L _ = 0 or I/O $V_{CC\_}$ = V_{CC}, I/O V_L _ = V_L		0.1	4	µA
		I/O $V_{CC\_}$ = 0, I/O V_L _ = 0 or I/O $V_{CC\_}$ = V_{CC}, I/O V_L _ = V_L, V_L < V_{CC} - 0.2V		0.1	100	
V_{CC} Tristate Output Mode Supply Current	I_{TS-VCC}	T_A = +25°C, EN = 0		0.03	1	µA
V_L Tristate Output Mode Supply Current	I_{TS-VL}	T_A = +25°C, EN = 0		0.1	0.2	µA
		T_A = +25°C, EN = 0, V_L = V_{CC} - 0.2V		1	2	
I/O Tristate Output Mode Leakage Current		T_A = +25°C, EN = 0,			0.15	µA
		T_A = +25°C, EN = 0, V_L = V_{CC} - 0.2V			30	
LOGIC-LEVEL THRESHOLDS						
I/O $V_{L\_}$ Input-Voltage High	V_{IHL}		2/3 x V_L			V
I/O $V_{L\_}$ Input-Voltage Low	V_{ILL}				1/3 x V_L	V
I/O $V_{CC\_}$ Input-Voltage High	V_{IHC}		2/3 x V_{CC}			V
I/O $V_{CC\_}$ Input-Voltage Low	V_{ILC}				1/3 x V_{CC}	V
EN Input-Voltage High	V_{IH}	T_A = +25°C	2/3 x V_L			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V) (Note 1), EN = V_L, C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 40pF, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Input-Voltage Low	V_{IL}	T_A = +25°C			1/3 x V_L	V
EN Input Current		T_A = +25°C			±5	µA
I/O $V_{L\_}$ Output-Voltage High	V_{OHL}	I/O $V_{L\_}$ source current = 20µA	2/3 x V_L			V
I/O $V_{L\_}$ Output-Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 20µA			1/3 x V_L	V
I/O $V_{CC\_}$ Output-Voltage High	V_{OHC}	I/O $V_{CC\_}$ source current = 20µA	2/3 x V_{CC}			V
I/O $V_{CC\_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$ sink current = 20µA			1/3 x V_{CC}	V

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V) (Note 1), EN = V_L, C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 40pF, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	C_{IOVCC} = 15pF, Figure 1			2.5	ns
		C_{IOVCC} = 20pF, Figure 1			3	
		C_{IOVCC} = 40pF, Figure 1			4	
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	C_{IOVCC} = 15pF, Figure 1			2.5	ns
		C_{IOVCC} = 20pF, Figure 1			3	
		C_{IOVCC} = 40pF, Figure 1			4	
I/O $V_{CC\_}$ One-Shot Output					18.5	Ω
I/O $V_{L\_}$ Rise Time	t_{RVL}	C_{IOVL} = 15pF, Figure 2			2.5	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}	C_{IOVL} = 15pF, Figure 2			2.5	ns
I/O $V_{L\_}$ One-Shot Output Impedance					12.5	Ω
Propagation Delay (Driving I/O $V_{L\_}$)	I/O_{VL-VCC}	C_{IOVCC} = 15pF, Figure 1			6.5	ns

+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

TIMING CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V) (Note 1), EN = V_L, C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 40pF, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay (Driving I/O $V_{CC\_}$)	I/O_{VCC-VL}	C_{IOVL} = 15pF, Figure 2			6	ns
Part-to-Part Skew	t_{PPSKEW}	C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_{CC} = 2.5V, V_L = 1.8V (Note 3)			4	ns
Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ after EN	t_{EN-VCC}	C_{IOVCC} = 15pF, Figure 3			1000	ns
Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ after EN	t_{EN-VL}	C_{IOVL} = 15pF, Figure 4			1000	ns
Maximum Data Rate		C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_L > 1.8V	100			Mbps
		C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_L > 1.2V	80			

Note 1: V_L must be less than or equal to V_{CC} - 0.4V during normal operation. However, V_L can be greater than V_{CC} - 0.4V during starting up and shutting down conditions.

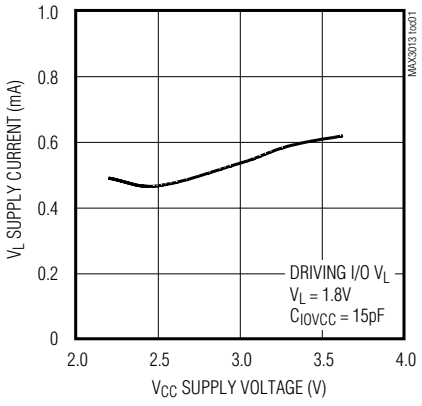
Note 2: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: Not production tested. Guaranteed by design.

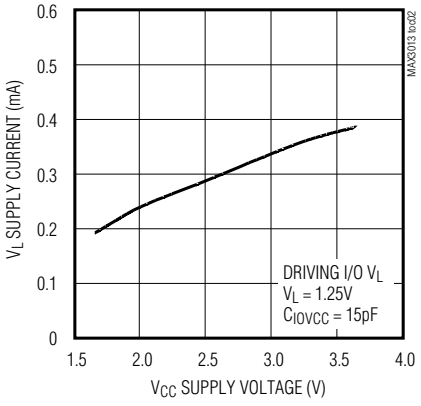
Typical Operating Characteristics

(Data rate = 100Mbps, V_{CC} = 3.3V, V_L = 1.8V, T_A = +25°C, unless otherwise noted.)

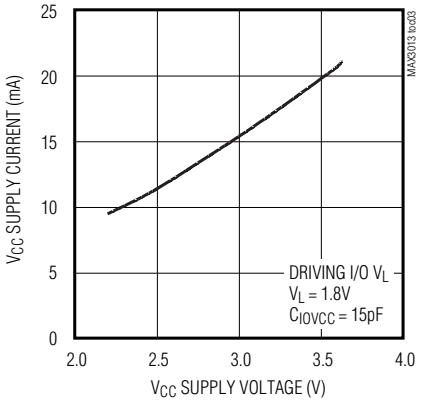
V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE



V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE



V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE

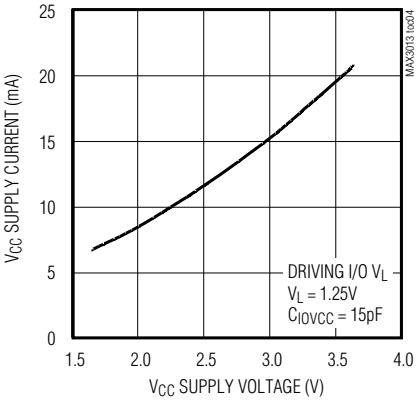


+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

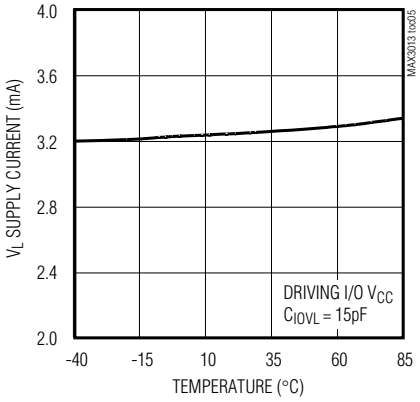
Typical Operating Characteristics (continued)

(Data rate = 100Mbps, V_{CC} = 3.3V, V_L = 1.8V, T_A = +25°C, unless otherwise noted.)

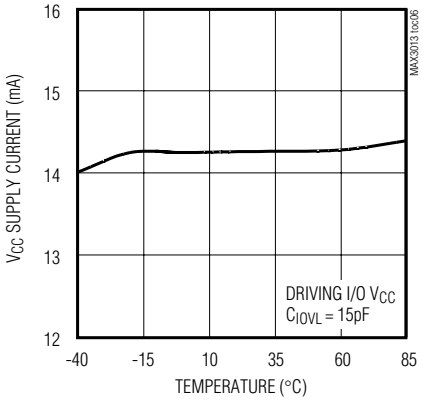
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



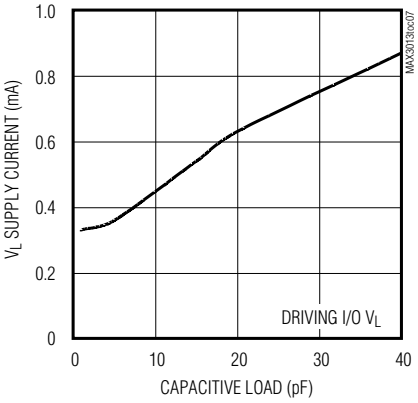
V_L SUPPLY CURRENT vs. TEMPERATURE



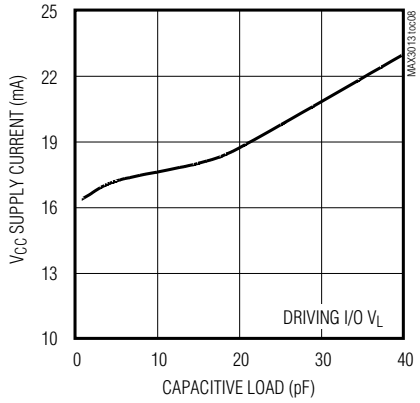
V_{CC} SUPPLY CURRENT vs. TEMPERATURE



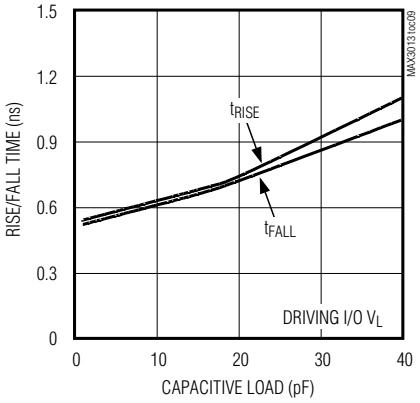
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_{CC}



V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_{CC}



RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_{CC}

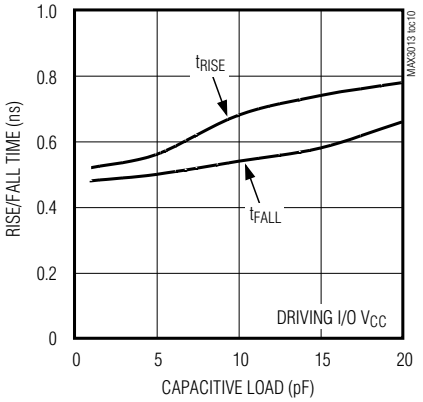


+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

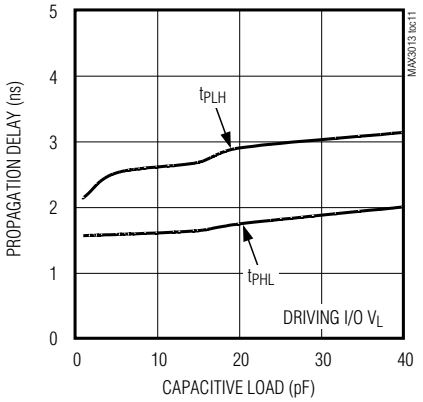
Typical Operating Characteristics (continued)

(Data rate = 100Mbps, V_{CC} = 3.3V, V_L = 1.8V, T_A = +25°C, unless otherwise noted.)

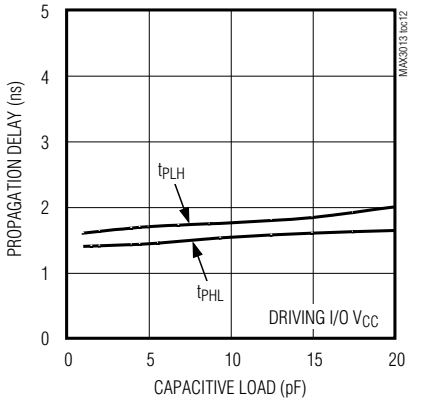
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_L



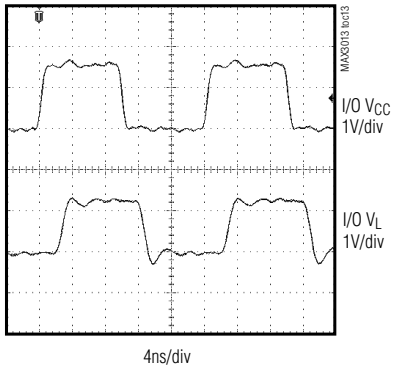
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_{CC}



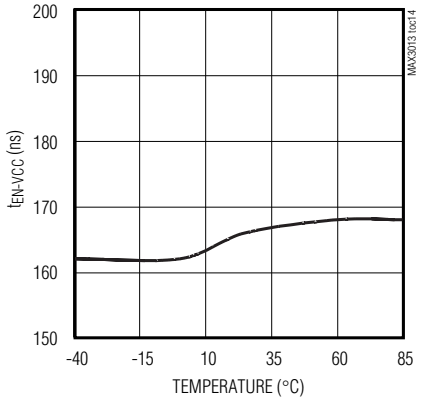
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L



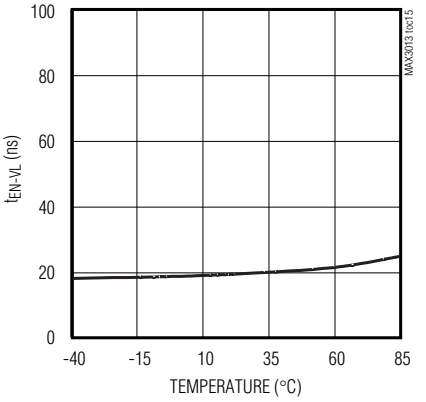
TYPICAL I/O V_{CC} DRIVING



t_{EN-VCC} vs. TEMPERATURE (C_{IOVCC} = 15pF)



t_{EN-VL} vs. TEMPERATURE (C_{IOVL} = 15pF)



Pin Description

PIN		BUMP	NAME	FUNCTION
TSSOP	QFN	UCSP		
1	18	B1	I/O V_L1	Input/Output 1, Referenced to V_L
2	19	A1	I/O V_L2	Input/Output 2, Referenced to V_L
3	20	B2	I/O V_L3	Input/Output 3, Referenced to V_L
4	1	A2	I/O V_L4	Input/Output 4, Referenced to V_L
5	2	A3	V_L	V_L Input Voltage, +1.2V ≤ V_L ≤ (V_{CC} - 0.4V). Bypass V_L to GND with a 0.1µF capacitor.
6	3	A4	EN	Enable Input. If EN is pulled low, all inputs/outputs are in tristate. Drive EN high (V_L) for normal operation.
7	4	B3	I/O V_L5	Input/Output 5, Referenced to V_L
8	5	A5	I/O V_L6	Input/Output 6, Referenced to V_L
9	6	B4	I/O V_L7	Input/Output 7, Referenced to V_L
10	7	B5	I/O V_L8	Input/Output 7, Referenced to V_L
11	8	C5	I/O V_{CC}8	Input/Output 8, Referenced to V_{CC}
12	9	C4	I/O V_{CC}7	Input/Output 7, Referenced to V_{CC}
13	10	D5	I/O V_{CC}6	Input/Output 6, Referenced to V_{CC}
14	11	C3	I/O V_{CC}5	Input/Output 5, Referenced to V_{CC}
15	12	D4	GND	Ground
16	13	D3	V_{CC}	V_{CC} Input Voltage, +1.65V ≤ V_{CC} ≤ +3.6V. Bypass V_{CC} to GND with a 0.1µF capacitor.
17	14	D2	I/O V_{CC}4	Input/Output 4, Referenced to V_{CC}
18	15	C2	I/O V_{CC}3	Input/Output 3, Referenced to V_{CC}
19	16	D1	I/O V_{CC}2	Input/Output 2, Referenced to V_{CC}
20	17	C1	I/O V_{CC}1	Input/Output 1, Referenced to V_{CC}

+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

Test Circuits/Timing Diagrams

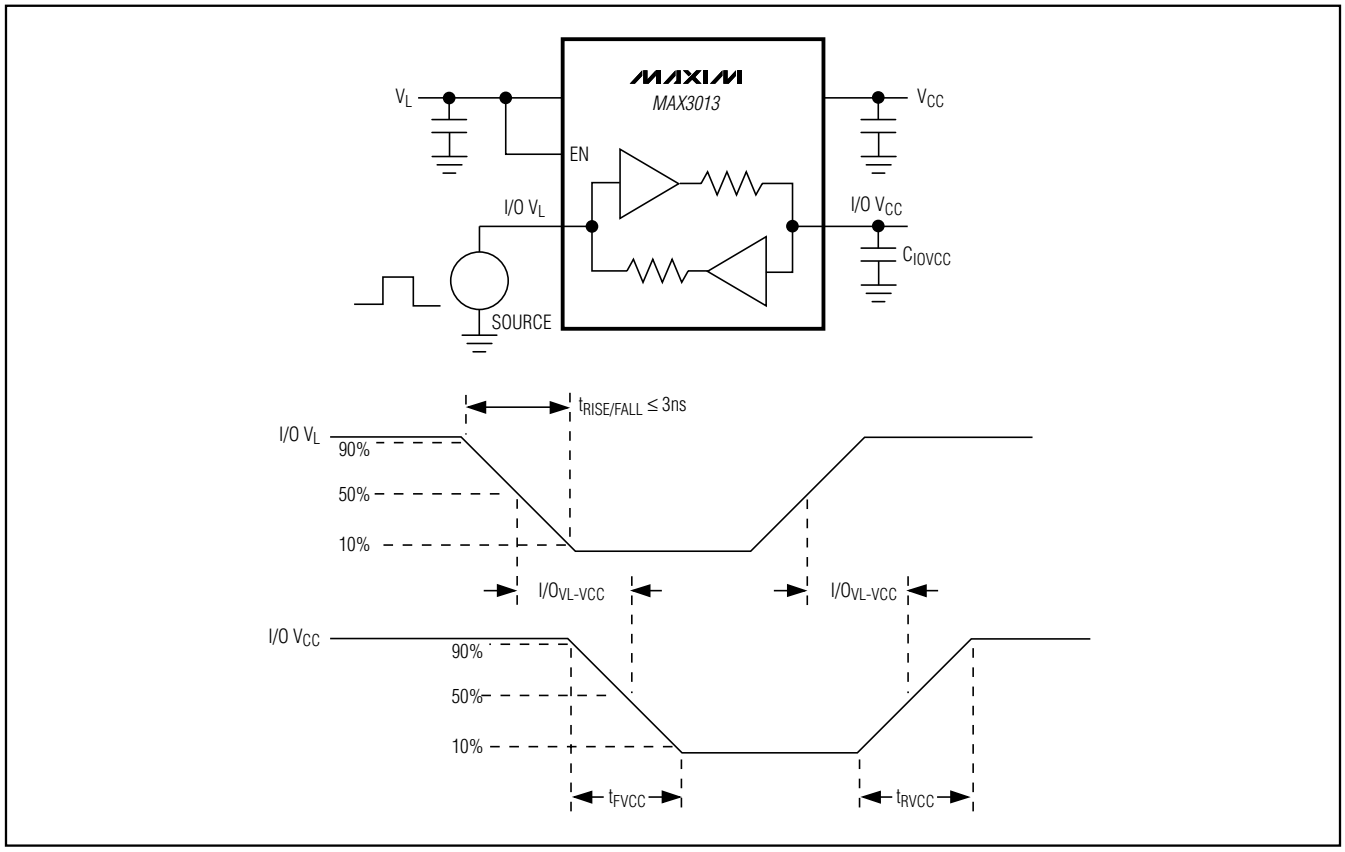


Figure 1. Driving I/O V_L Test Circuit and Timing

Test Circuits/Timing Diagrams (continued)

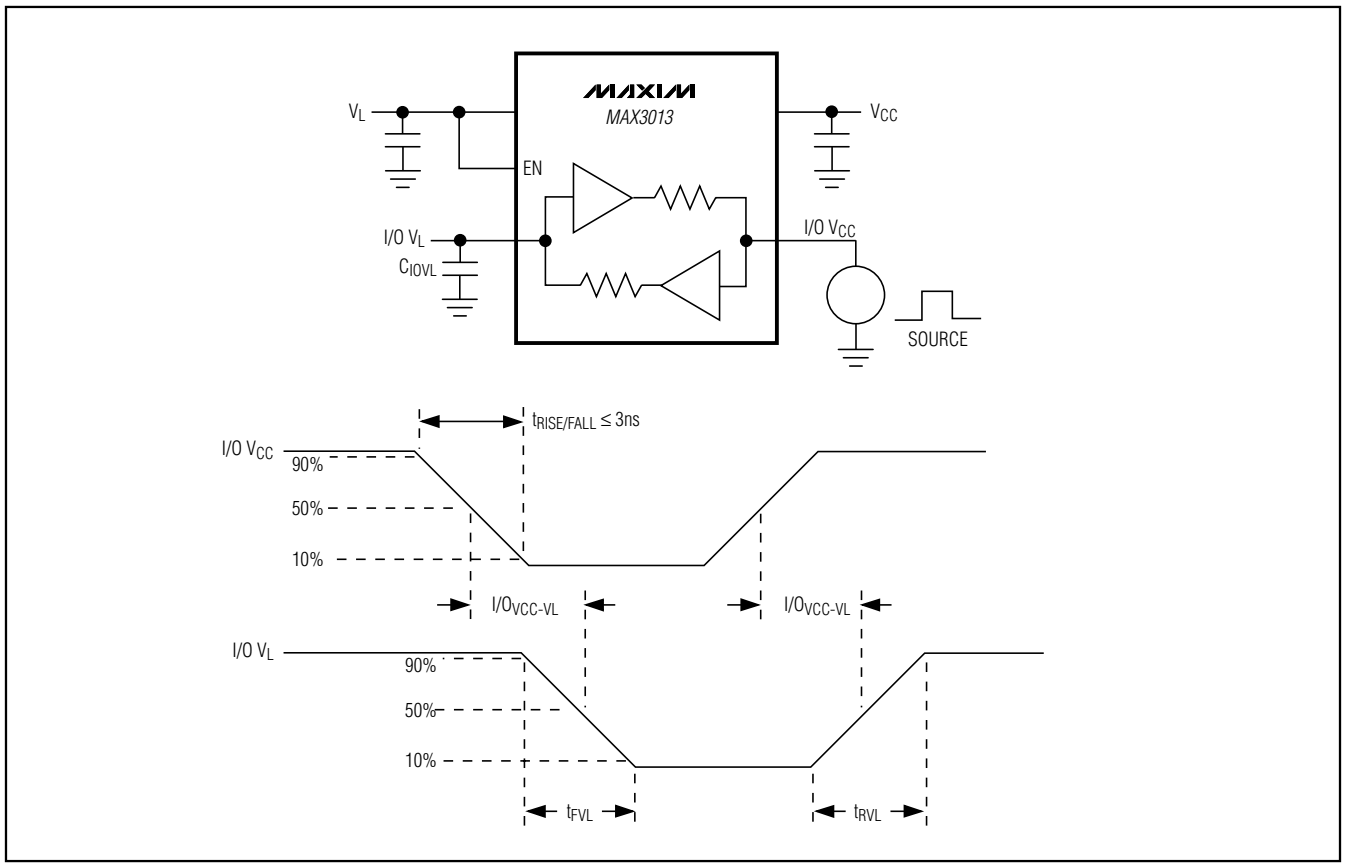


Figure 2. Driving I/O V_{CC} Test Circuit and Timing

+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

Test Circuits/Timing Diagrams (continued)

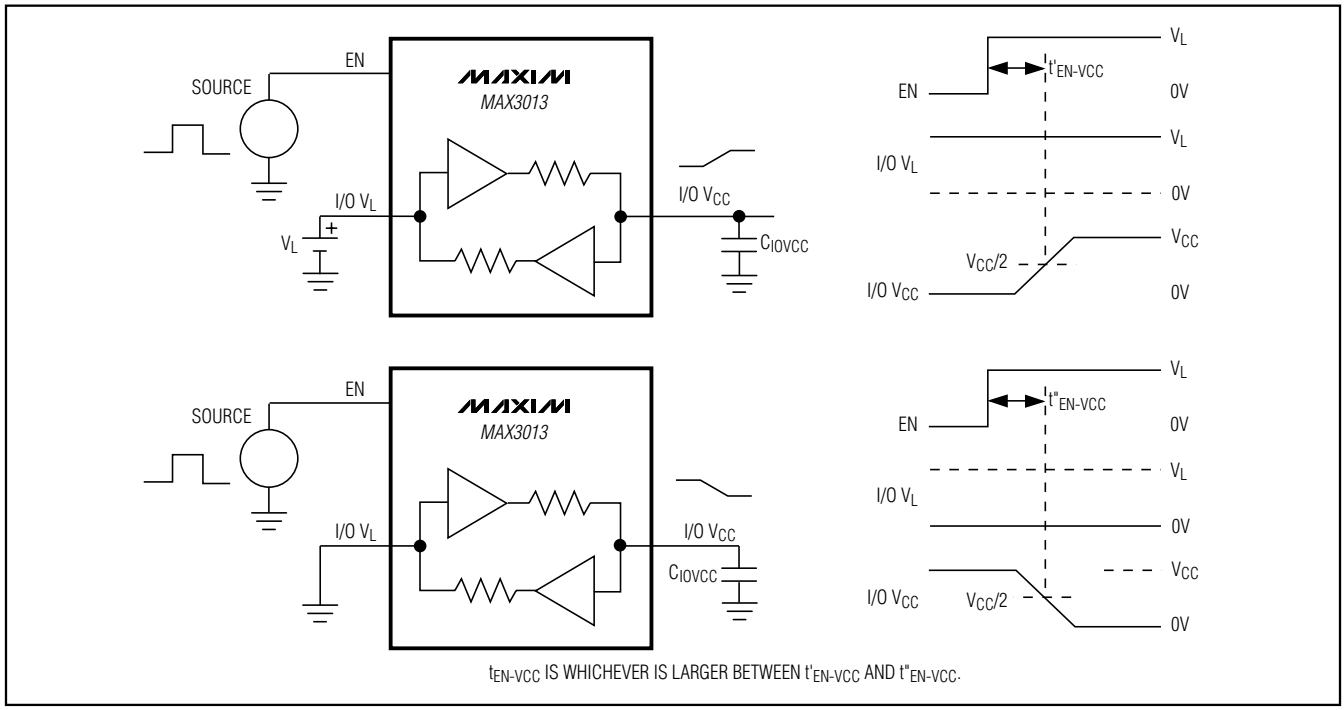


Figure 3. Propagation Delay from I/O V_L to I/O V_{CC} after EN

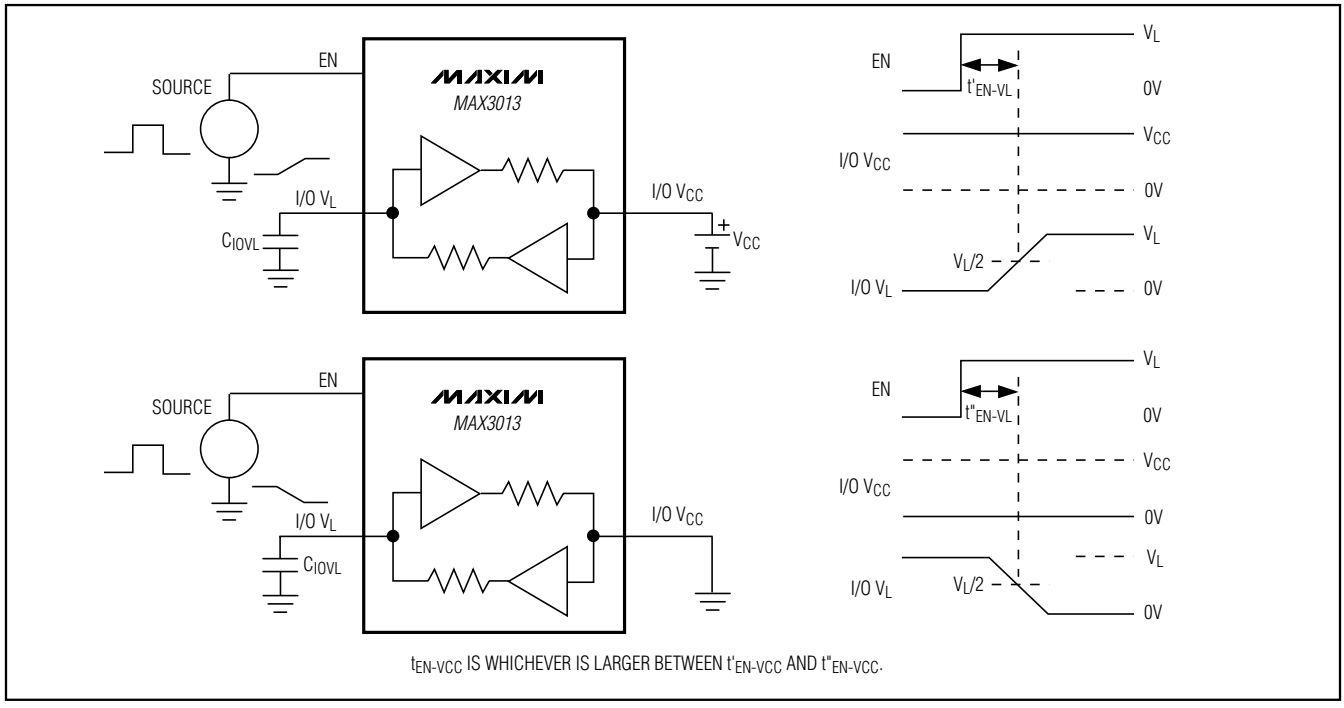


Figure 4. Propagation Delay from I/O V_{CC} to I/O V_L after EN

Detailed Description

The MAX3013 logic-level translator provides the level shifting necessary to allow 100Mbps data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX3013 bidirectional level translator allows data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX3013 accepts V_L from +1.2V to (V_{CC} - 0.4V) and operate with V_{CC} from +1.65V to +3.6V, making it ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX3013 features an input enable mode (EN) that reduces V_{CC} and V_L supply currents to 0.1µA, when in tristate mode. This device operates at a guaranteed data rate of 100Mbps for V_L > +1.8V.

Level Translation

For proper operation, ensure that $+1.65V \le V_{CC} \le +3.6V$, $+1.2V \le V_L \le (V_{CC} - 0.4V)$. During power-up sequencing, $V_L \ge V_{CC}$ does not damage the device. During power-supply sequencing, when V_{CC} is floating and V_L is powering up, up to 40mA current can be sourced to each load on the V_L side, yet the device does not latch up. The maximum data rate depends heavily on the load capacitance (see the *Typical Operating Characteristics*, Rise/Fall Times), output impedance of the driver, and the operating voltage range (see the *Timing Characteristics*).

Input Driver Requirements

The MAX3013 architecture is based on a one-shot accelerator output stage (see Figure 5). Accelerator output stages are always in tristate mode except when there is a transition on any of the translators on the input side, either I/O V_L or I/O V_{CC}. Then, a short pulse is generated during which the accelerator output stages become active and charge/discharge the capacitances at the I/Os. Due to its bidirectional nature, both input stages become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior helps to speed up the transition on the driven side.

For proper operation, the external driver must meet the following conditions: <25Ω output impedance and >20mA output current. Figure 6 shows a graph of Typical Input Current vs. Input Voltage.

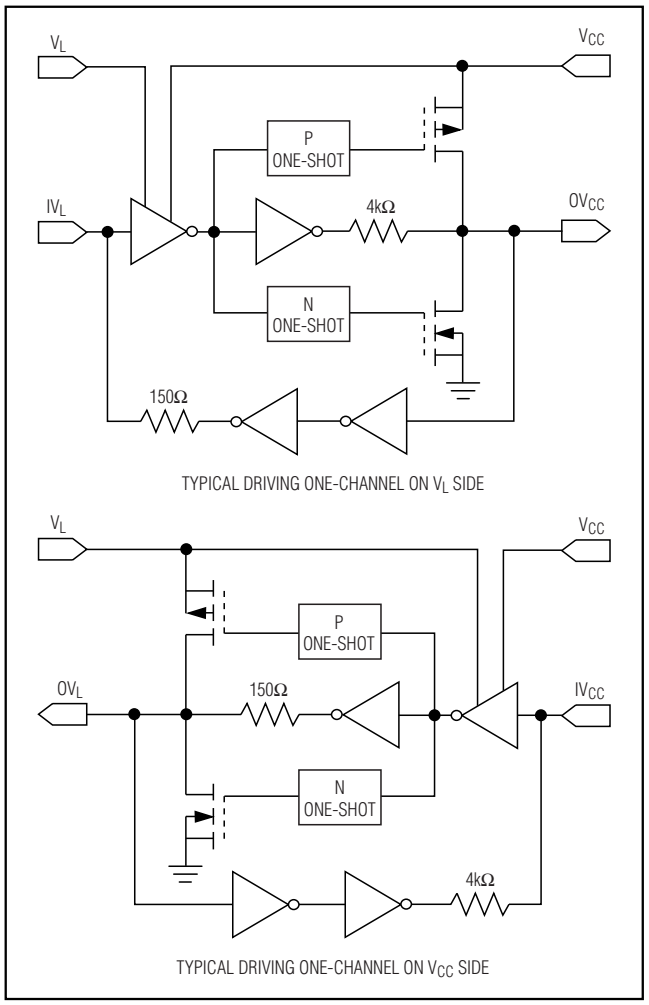


Figure 5. MAX3013 Simplified Diagram (1 I/O line)

Output Load Requirements

The MAX3013 I/O was designed to drive CMOS inputs. Do not load the I/O lines with a resistive load less than 25kΩ. Also, do not place an RC circuit at the input of the MAX3013 to slow down the edges. If a slower data rate is required, please see the MAX3000E/MAX3001E logic-level translator.

For I^2C level translation, please refer to the MAX3372E–MAX3379E/MAX3390E–MAX3393E data sheet.

+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

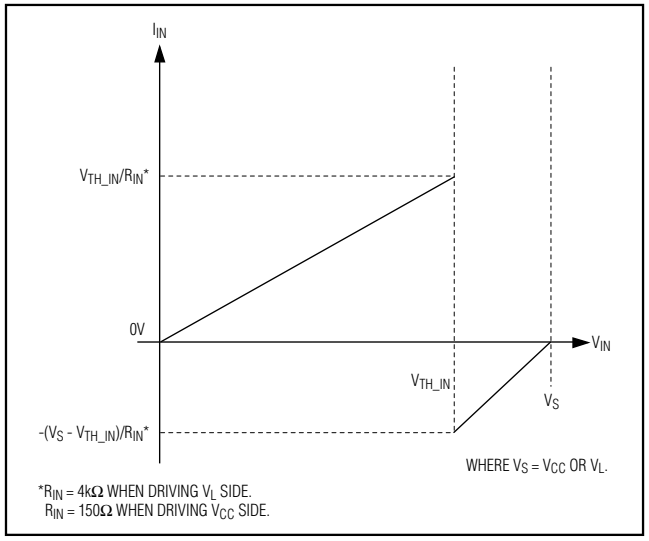


Figure 6. Typical I_{IN} vs. V_{IN}

Enable Input (EN)

The MAX3013 features an EN input. Pull EN low to set the MAX3013 I/O on both sides in tristate output mode. Drive EN to logic high (V_L) for normal operation.

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_L and V_{CC} to ground with a 0.1µF ceramic capacitor. Place the bypass capacitors as close to the power-supply input pins as possible.

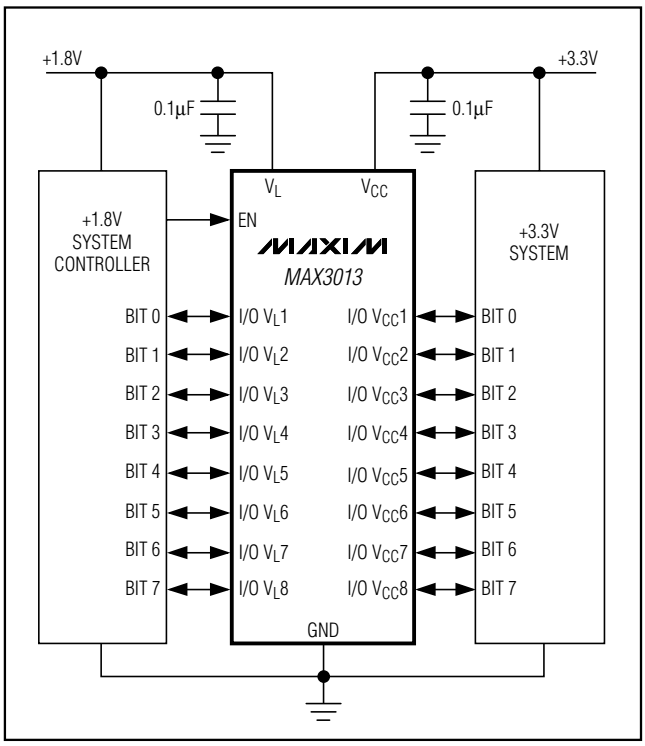
8-Bit Bus Translation

The MAX3013 level-shifts the data present on the I/O line between +1.2V to +3.6V, making it ideal for level translation between a low-voltage ASIC and a higher voltage system. The *Typical Operating Circuit* shows the MAX3013 bidirectional translator in an 8-bit bus level translation from a 1.8V system to a 3.3V system and vice versa.

Unidirectional vs. Bidirectional Level Translator

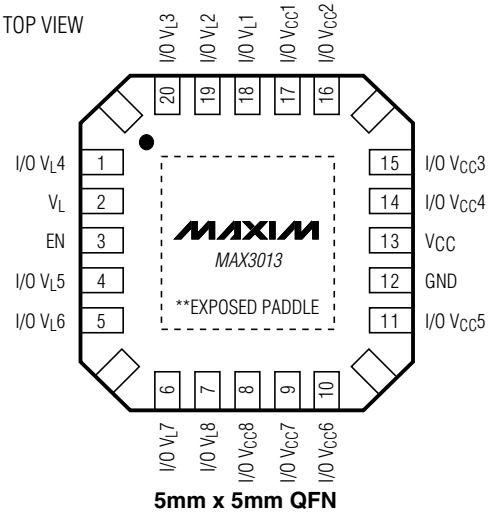
The MAX3013 bidirectional translator can operate as a unidirectional device to translate signals without inversion. This device provides the smallest solution (UCSP package) for unidirectional level translation without inversion.

Typical Operating Circuit

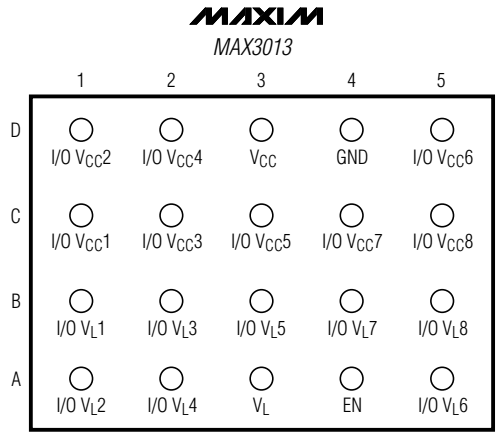


+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

Pin Configurations (continued)



5mm x 5mm QFN



20 UCSP
(BOTTOM VIEW)

Chip Information

TRANSISTOR COUNT: 1447

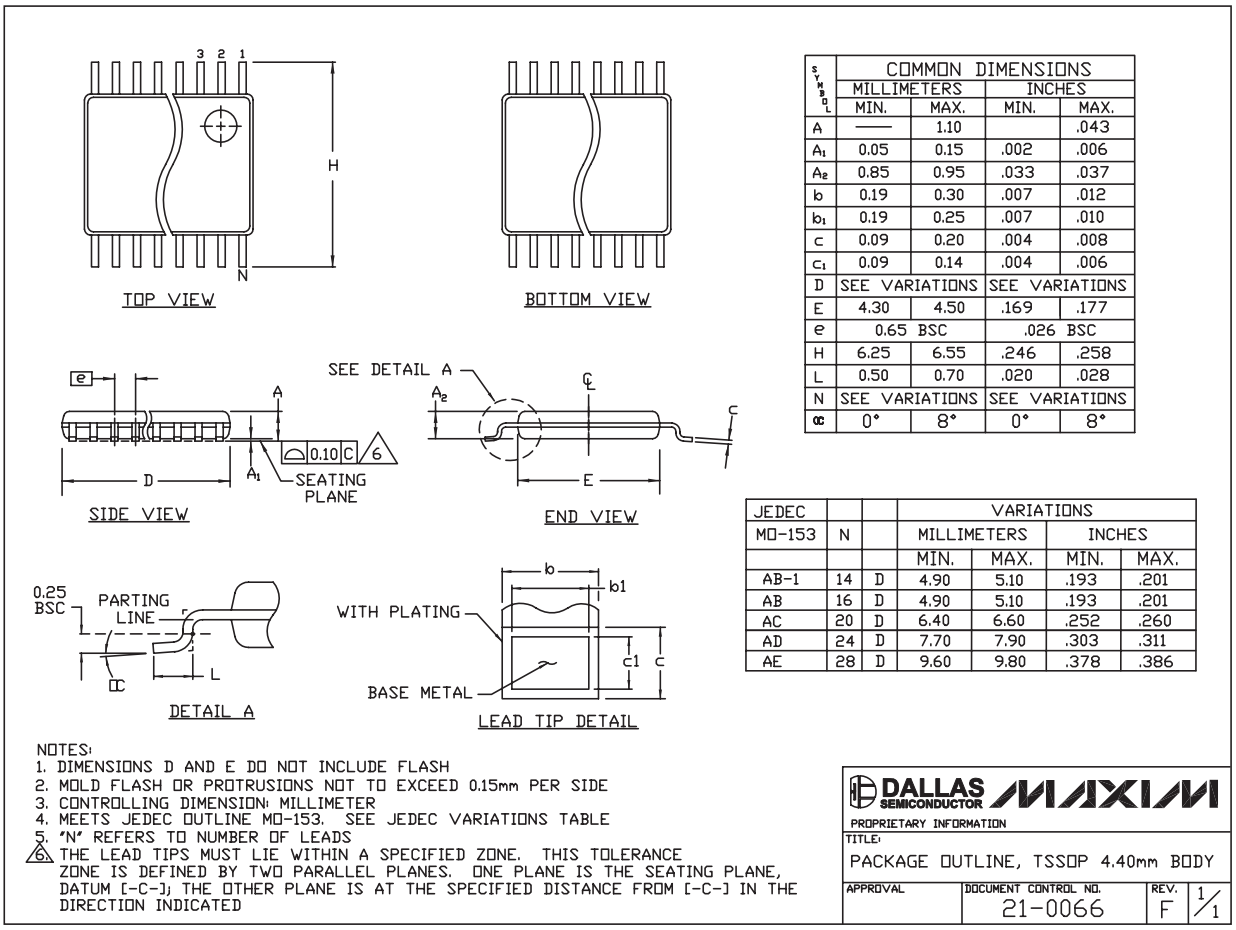
PROCESS: BiCMOS

+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

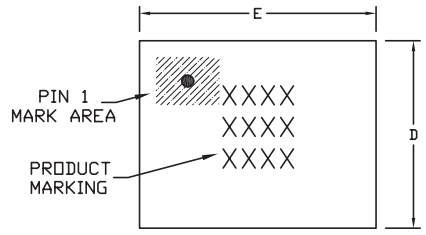
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

5x4 UCSP.EPS

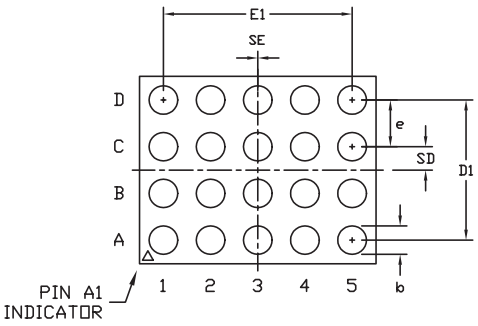


TOP VIEW

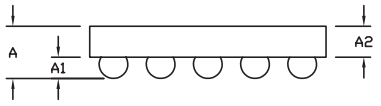
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	2.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B20-1	2.03±0.08	2.54±0.08	NONE
B20-2	2.03±0.08	2.54±0.08	B2, B3, B4
B20-4	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C4
B20-5	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C3, C4
B20-6	2.16±0.08	2.54±0.08	B2, B3, B4

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 5x4 UCSP

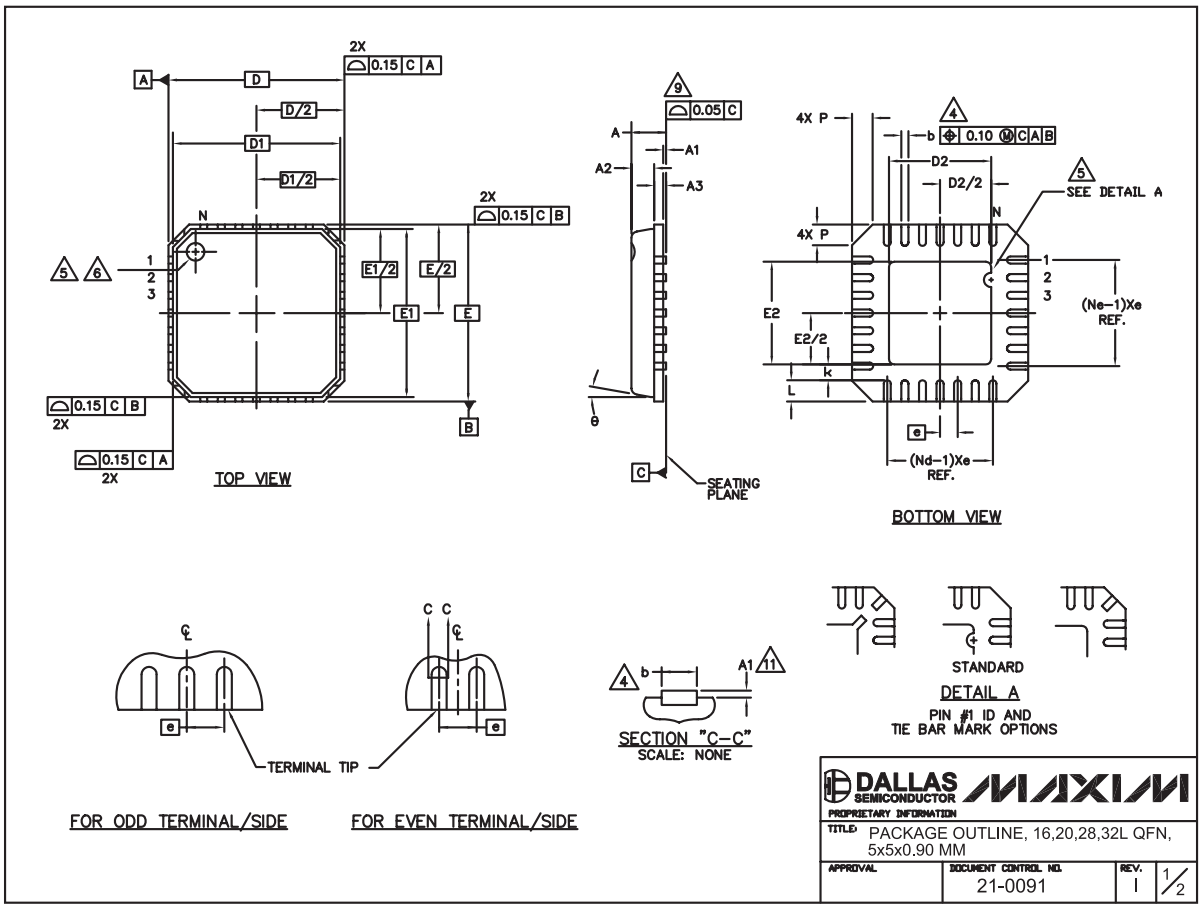
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0095	I	1/1

+1.2V to +3.6V, 0.1µA, 100Mbps, 8-Channel Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32L QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO. 21-0091	REV. I	2/2