MCP6N16

Zero-Drift Instrumentation Amplifier

Features:

- High DC Precision:
  - V_{OS}: ±17 µV (maximum, G_{MIN} = 100)
  - TC_1: ±60 nV/°C (maximum, G_{MIN} = 100)
  - CMRR: 112 dB (minimum, G_{MIN} = 100, V_{DD} = 5.5V)
  - PSRR: 110 dB (minimum, G_{MIN} = 100, V_{DD} = 5.5V)
  - g_E: ±0.15% (maximum, G_{MIN} = 10, 100)
- Flexible:
  - Minimum Gain (G_{MIN}) Options: 1, 10 and 100 V/V
  - Rail-to-Rail Input and Output
  - Gain Set by Two External Resistors
- Bandwidth: 500 kHz (typical, Gain = G_{MIN} = 1, 10)
- Power Supply:
  - V_{DD}: 1.8V to 5.5V
  - I_Q: 1.1 mA (typical)
  - Power Savings (Enable) Pin: EN
- Enhanced EMI Protection:
  - Electromagnetic Interference Rejection Ratio (EMIRR): 111 dB at 2.4 GHz
- Extended Temperature Range: -40°C to +125°C

Typical Applications:

- High-Side Current Sensor
- Wheatstone Bridge Sensors
- Difference Amplifier with Level Shifting
- Power Control Loops

Design Aids:

- SPICE Macro Model
- Microchip Advanced Part Selector (MAPS)
- Application Notes

Description:

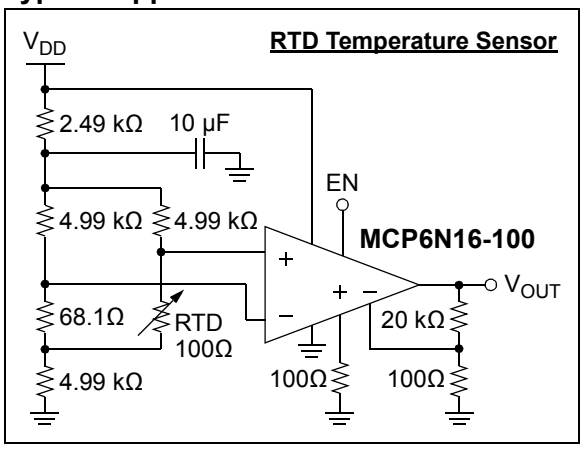
Microchip Technology Inc. offers the single Zero-Drift MCP6N16 instrumentation amplifier (INA) with Enable pin (EN) and three minimum gain options (G_{MIN}). The internal offset correction gives high DC precision: it has very low offset and offset drift, and negligible 1/f noise.

Two external resistors set the gain, minimizing gain error and drift over temperature. The reference voltage (V_{REF}) shifts the output voltage (V_{OUT}).

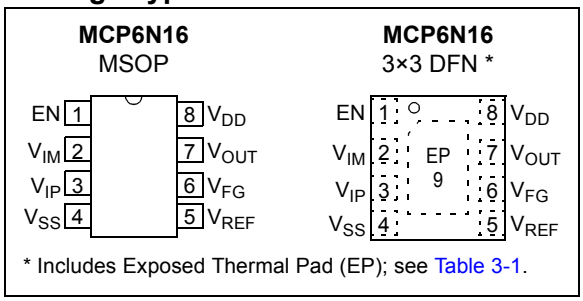
The MCP6N16 is designed for single-supply operation, with rail-to-rail input (no common mode crossover distortion) and output performance. The supply voltage range (1.8V to 5.5V) is low enough to support many portable applications. All devices are fully specified from -40°C to +125°C. Each part has EMI filters at the input pins, for good EMI rejection (EMIRR).

These parts have three minimum gain options (1, 10 and 100 V/V). This allows the user to optimize the input offset voltage and input noise for different applications.

Typical Application Circuit



Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Minimum Gain Options

Table 1 shows key specifications that differentiate between the different minimum gain (G_{MIN}) options. See **Section 1.0 "Electrical Characteristics"**, **Section 6.0 "Packaging Information"** and Product Identification System for further information on G_{MIN}.

TABLE 1: KEY DIFFERENTIATING SPECIFICATIONS

Part No.	G_{MIN} (V/V) Nom.	V_{OS} (±µV) Max.	TC_1 (±nV/°C) Max. T_A = -40 to +125°C	CMRR (dB) Min. V_{DD} = 5.5V	PSRR (dB) Min.	V_{DMH} (V) Min.	GBWP (MHz) Typ.	E_{ni} (μV_{P-P}) Typ. f = 0.1 to 10 Hz	e_{ni} (nV/√Hz) Typ. f < 500 Hz
MCP6N16-001	1	85	1800	89	91	2.7	0.50	19	900
MCP6N16-010	10	22	180	103	104	0.27	5.0	2.2	105
MCP6N16-100	100	17	60	112	110	0.027	35	0.93	45

Note 1: G_{MIN} is the minimum stable gain (G_{DM}), for a given part option. In other words, $G_{DM} \geq G_{MIN}$.

Figures 1 to 3 show input offset voltage versus temperature for the three gain options (G_{MIN} = 1, 10, 100 V/V).

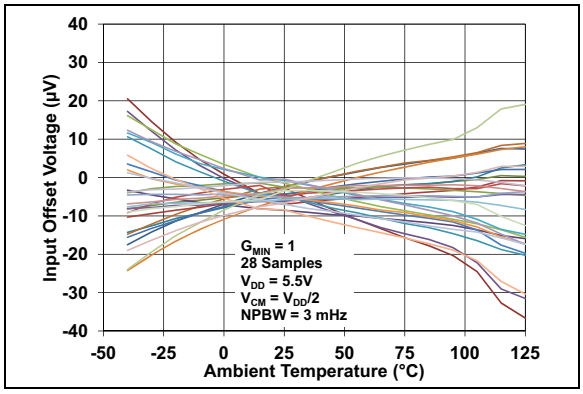


FIGURE 1: *Input Offset Voltage vs. Temperature, with G_{MIN} = 1.*

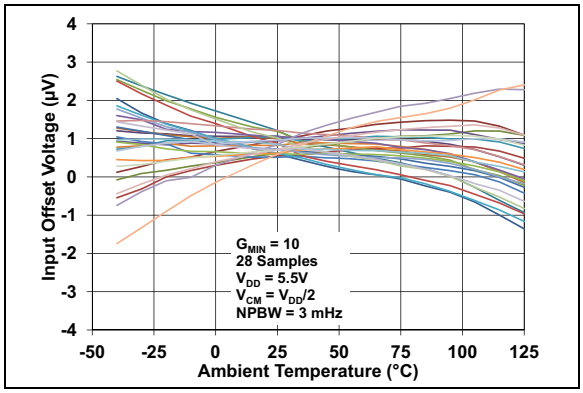


FIGURE 2: *Input Offset Voltage vs. Temperature, with G_{MIN} = 10.*

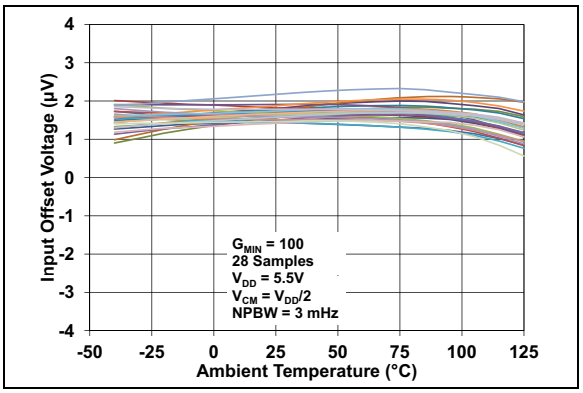


FIGURE 3: *Input Offset Voltage vs. Temperature, with G_{MIN} = 100.*

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 6.5V

Current at Input Pins **(Note 1)** ..... ±2 mA

Analog Inputs (V_{IP} and V_{IM}) **(Note 1)** ..... V_{SS} – 1.0V to V_{DD} + 1.0V

All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V

Difference Input Voltage ..... $|V_{DD} – V_{SS}|$

Output Short-Circuit Current ..... Continuous

Current at Output and Supply Pins ..... ±30 mA

Storage Temperature ..... -65°C to +150°C

Maximum Junction Temperature ..... +150°C

ESD protection on all pins (HBM, MM) ..... ≥ 4 kV, 400V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: See **Section 4.3.1.2 “Input Voltage Limits”** and **Section 4.3.1.3 “Input Current Limits”**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Input Offset							
Input Offset Voltage	V_{OS}	-85	—	+85	µV	1	T_A = +25°C
		-22	—	+22		10	
		-17	—	+17		100	
Input Offset Voltage Drift – Linear Temp. Co.	TC_1	-1800	—	+1800	nV/°C	1	T_A = -40°C to +125°C **(Note 2)**
		-180	—	+180		10	
		-60	—	+60		100	
Input Offset Voltage Drift – Quadratic Temp. Co.	TC_2	—	±560	—	pV/°C^2	1	T_A = -40°C to +125°C
		—	±63	—		10	
		—	±69	—		100	
Input Offset Aging	ΔV_{OS}	—	±1.0	—	µV	1	408 hr Life Test at +150°C, measured at +25°C
		—	±0.8	—		10	
		—	±0.7	—		100	
Power Supply Rejection Ratio	PSRR	91	109	—	dB	1	
		104	122	—		10	
		110	128	—		100	
Output Offset							
Output Offset Voltage	V_{OSO}		0		µV	all	
Input Current and Impedance (Note 3)							
Input Bias Current	I_B	-100	±2	+100	pA	all	
Across Temperature		—	20	—			T_A = +85°C
Across Temperature		0	250	2000			T_A = +125°C

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Input Offset Current	I_{OS}	-800	±300	+800	pA	all	
Across Temperature		—	±320	—			T_A = +85°C
Across Temperature		-1500	±350	+1500			T_A = +125°C
Common Mode Input Impedance	Z_{CM}	—	10^{13}||10	—	Ω||pF		
Differential Input Impedance	Z_{DIFF}	—	10^{13}||4	—			
Input Common Mode Voltage (V_{CM} or V_{REF}) (Note 3)							
Input Voltage Range **(Note 4, Note 5)**	V_{IVL}	—	V_{SS} – 0.25	V_{SS} – 0.15	V	all	
	V_{IVH}	V_{DD} + 0.15	V_{DD} + 0.30	—			
Common Mode Rejection Ratio	CMRR	80	98	—	dB	1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 1.8V
		94	112	—		10	
		103	121	—		100	
		89	107	—		1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 5.5V
		103	121	—		10	
		112	130	—		100	
Common Mode Rejection Ratio at V_{REF}	CMRR2	83	101	—	dB	1	V_{REF} = 0.2V to V_{DD} – 0.2V, V_{DD} = 1.8V
		98	116	—		10	
		102	120	—		100	
		94	112	—		1	V_{REF} = 0.2V to V_{DD} – 0.2V, V_{DD} = 5.5V
		109	127	—		10	
		115	133	—		100	

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 (**Note 1**).

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Common Mode Nonlinearity (**Note 6**)	INL_{CM}	-550	—	+550	ppm	1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 1.8V
		-75	—	+75		10	
		-20	—	+20		100	
		-310	—	+310		1	V_{CM} = V_{IVL} to V_{IVH}, V_{DD} = 5.5V
		-35	—	+35		10	
		-10	—	+10		100	
Input Differential Voltage (V_{DM}) (Note 3)							
Differential Input Voltage Range (**Note 5**)	V_{DML}	—	-3.4/G_{MIN}	-2.7/G_{MIN}	V	all	V_{DD} ≥ 2.9V, V_{REF} = V_{DD}, V_{OUT} within ±0.2%
	V_{DMH}	+2.7/G_{MIN}	+3.4/G_{MIN}	—			V_{DD} ≥ 2.9V, V_{REF} = 0V, V_{OUT} within ±0.2%
Differential Gain Error (**Note 6**)	g_E	—	±0.03	—	%	1	V_{DD} = 1.8V, V_{REF} = V_{DD}/2, V_{DM} = ±(0.7V)/G_{MIN}
		—	±0.02	—	%	10, 100	
		—	±0.03	—		1	V_{DD} = 5.5V, V_{REF} = V_{DD}/2, V_{DM} = ±(2.55V)/G_{MIN}
		—	±0.02	—		10, 100	
		-0.25	±0.04	+0.25	%	1	V_{DD} = 5.5V, V_{REF} = 0.2V, V_{DM} = 0 to (2.7V)/G_{MIN}
		-0.15	±0.02	+0.15	%	10, 100	
		-0.25	±0.04	+0.25	%	1	V_{DD} = 5.5V, V_{REF} = 5.3V, V_{DM} = 0 to (-2.7V)/G_{MIN}
		-0.15	±0.02	+0.15	%	10, 100	

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Differential Gain Drift **(Note 6)**	$\Delta g_E/\Delta T_A$	—	±3	—	ppm/°C	all	V_{DD} = 1.8V, V_{REF} = V_{DD}/2, V_{DM} = ±(0.7V)/G_{MIN}
		—	±4	—			V_{DD} = 5.5V, V_{REF} = V_{DD}/2, V_{DM} = ±(2.55V)/G_{MIN}
		—	±4	—			V_{DD} = 5.5V, V_{REF} = 0.2V, V_{DM} = 0 to (2.7V)/G_{MIN}
		—	±3	—			V_{DD} = 5.5V, V_{REF} = 5.3V, V_{DM} = 0 to (-2.7V)/G_{MIN}
Differential Nonlinearity **(Note 6)**	INL_{DM}	—	±300	—	ppm	all	V_{DD} = 1.8V, V_{REF} = V_{DD}/2, V_{DM} = ±(0.7V)/G_{MIN}
		—	±150	—			V_{DD} = 5.5V, V_{REF} = V_{DD}/2, V_{DM} = ±(2.55V)/G_{MIN}
		—	±300	—			V_{DD} = 5.5V, V_{REF} = 0.2V, V_{DM} = 0 to (2.7V)/G_{MIN}
		—	±300	—			V_{DD} = 5.5V, V_{REF} = 5.3V, V_{DM} = 0 to (-2.7V)/G_{MIN}
DC Open-Loop Gain	A_{OL}	84	102	—	dB	1	V_{DD} = 1.8V, V_{OUT} = 0.2V to 1.6V
		100	118	—		10	
		108	126	—		100	
		95	113	—		1	V_{DD} = 5.5V, V_{OUT} = 0.2V to 5.3V
		111	129	—		10	
		119	137	—		100	

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8 **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Output							
Minimum Output Voltage Swing	V_{OL}	—	V_{SS} + 3	—	mV	all	R_L = 10 kΩ, V_{DD} = 1.8V, V_{DM} = -V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 – 0.9V
		—	V_{SS} + 6	—			R_L = 10 kΩ, V_{DD} = 5.5V, V_{DM} = -V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 – 1V
		—	V_{SS} + 60	V_{SS} + 250			R_L = 1 kΩ, V_{DD} = 5.5V, V_{DM} = -V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 – 1V
Maximum Output Voltage Swing	V_{OH}	—	V_{DD} – 3	—	mV		R_L = 10 kΩ, V_{DD} = 1.8V, V_{DM} = V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 + 0.9V
		—	V_{DD} – 6	—			R_L = 10 kΩ, V_{DD} = 5.5V, V_{DM} = V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 + 1V
		V_{DD} – 250	V_{DD} – 60	—			R_L = 1 kΩ, V_{DD} = 5.5V, V_{DM} = V_{DD}/(2G_{MIN}), V_{REF} = V_{DD}/2 + 1V
Output Short-Circuit Current	I_{SC}	—	±10	—	mA		V_{DD} = 1.8V
		—	±35	—			V_{DD} = 5.5V
Power Supply							
Supply Voltage	V_{DD}	1.8	—	5.5	V	all	
Quiescent Current per Amplifier	I_Q	0.5	1.1	1.6	mA		I_O = 0
POR Trip Voltage	V_{PRL}	0.9	1.27	—	V		
	V_{PRH}	—	1.33	1.6	V		

Note 1: V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM}) and G_{DM} = 1 + R_F/R_G.

2: For Design Guidance only; not tested.

3: These specifications apply to the V_{IP}, V_{IM} input pair (use V_{CM}) and to the V_{REF}, V_{FG} input pair (use V_{REF} instead).

4: This specification applies to the V_{IP}, V_{IM}, V_{REF} and V_{FG} pins individually.

5: Figures 2-52 and 2-53 show the V_{IVL}, V_{IVH}, V_{DML} and V_{DMH} variation over temperature.

6: See **Section 1.5 "Explanation of DC Error Specifications"**.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
AC Response							
Gain-Bandwidth Product	GBWP	—	0.5	—	MHz	1	
		—	5	—		10	
		—	35	—		100	
Phase Margin	PM	—	70	—	°	all	
Open-Loop Output Impedance	R_{OL}	—	1.6	—	kΩ		
Power Supply Rejection Ratio	PSRR	—	80	—	dB	1	f = 1 kHz
		—	98	—		10	
		—	123	—		100	
Common Mode Rejection Ratio at V_{CM} and V_{REF}	CMRR, CMRR2	—	83	—	dB	1	f = 10 kHz
		—	80	—		10	
		—	140	—		100	
Step Response (see **Section 4.1.4 "AC Performance"**)							
Slew Rate	SR	**Note 1**			V/µs	all	
Start-Up Time	t_{STR}	—	2	—	ms	1	G_{DM} = 1000, V_{DD} power up to 0.1% V_{OUT} settling **(Note 3, Note 4)**
		—	0.3	—		10	
		—	0.2	—		100	
Overdrive Recovery, Input Common Mode	t_{IRC}	—	1	—	µs	all	V_{IP} =V_{IM} = V_{IVH} + 0.5V to V_{DD} – 1V (or V_{IVL} – 0.5V to 1V), 90% of V_{OUT} change (I_B ≤ 2 mA) **(Note 4)**
Overdrive Recovery, Input Differential Mode	t_{IRD}	—	10	—			$G_{MIN}V_{DM}$ = $G_{MIN}V_{DMH}$ + 0.5V to 0V (or $G_{MIN}V_{DML}$ – 0.5V to 0V), V_{REF} = 1V (or V_{DD} – 1V), 90% of V_{OUT} change **(Note 4)**
Overdrive Recovery, Output	t_{OR}	—	180	—			$G_{DM}V_{DM}$ = 1.5V to 0V (or -1.5V to 0V), V_{REF} = V_{DD} – 1V (or 1V), 90% of V_{OUT} change **(Note 4)**

Note 1: The slew rate is limited by the GBWP; the large signal step response is dominated by the small signal bandwidth.

2: These parameters were characterized using the circuit in Figure 1-8. In Figures 2-75 and 2-76, there is an IMD tone at DC, a residual tone at 100 Hz and other IMD tones and clock tones.

3: High gains behave differently; see **Section 4.4.4 "Offset at Power-Up"**.

4: t_{STR}, t_{STL}, t_{IRC}, t_{IRD} and t_{OR} include some uncertainty due to clock edge timing.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
Noise							
Input Noise Voltage Density	e_{ni}	—	900	—	nV/√Hz	1	f = 500 Hz
		—	105	—		10	
		—	45	—		100	
Input Noise Voltage	E_{ni}	—	19	—	μV_{P-P}	1	f = 0.1 Hz to 10 Hz
		—	2.2	—		10	
		—	0.93	—		100	
		—	5.9	—		1	f = 0.01 Hz to 1 Hz
		—	0.69	—		10	
		—	0.30	—		100	
Input Current Noise Density	i_{ni}	—	7	—	fA/√Hz	all	f = 1 kHz
Output Noise Voltage Density	e_{no}		0		nV/√Hz		
Output Noise Voltage	E_{no}		0		μV_{P-P}		
Amplifier Distortion (Note 2)							
Intermodulation Distortion (AC)	IMD	—	5	—	μV_{PK}	all	V_{CM} tone = 100 mV_{PK} at 100 Hz
EMI Protection							
EMI Rejection Ratio	EMIRR	—	103	—	dB	all	V_{IN} = 0.1 V_{PK}, f = 400 MHz
		—	106	—			V_{IN} = 0.1 V_{PK}, f = 900 MHz
		—	106	—			V_{IN} = 0.1 V_{PK}, f = 1800 MHz
		—	111	—			V_{IN} = 0.1 V_{PK}, f = 2400 MHz

Note 1: The slew rate is limited by the GBWP; the large signal step response is dominated by the small signal bandwidth.

2: These parameters were characterized using the circuit in Figure 1-8. In Figures 2-75 and 2-76, there is an IMD tone at DC, a residual tone at 100 Hz and other IMD tones and clock tones.

3: High gains behave differently; see **Section 4.4.4 "Offset at Power-Up"**.

4: t_{STR}, t_{STL}, t_{IRC}, t_{IRD} and t_{OR} include some uncertainty due to clock edge timing.

TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

Parameters	Sym.	Min.	Typ.	Max.	Units	G_{MIN}	Conditions
EN Low Specifications							
EN Logic Threshold, Low	V_{IL}	—	—	$0.2V_{DD}$	V	all	
EN Input Current, Low	I_{ENL}	—	-10	—	pA		EN = 0V
GND Current	I_{SS}	-8	-2	—	µA		EN = 0V, V_{DD} = 5.5V
Amplifier Output Leakage	$I_{O(LEAK)}$	—	-1	—	nA		EN = 0V
EN High Specifications							
EN Logic Threshold, High	V_{IH}	$0.8V_{DD}$	—	—	V	all	
EN Input Current, High	I_{ENH}	—	10	—	pA		EN = V_{DD}
EN Dynamic Specifications							
EN Input Hysteresis	V_{HYST}	—	$0.16V_{DD}$	—	V	all	
EN Input Resistance	R_{PD}	—	10^{13}	—	Ω		
EN Low to Amplifier Output High Z Turn-Off Time	t_{OFF}	—	0.1	2	µs		EN = $0.2V_{DD}$ to V_{OUT} = $0.1(V_{DD}/2)$, V_L = 0V
EN High to Amplifier Output On Time	t_{ON}	—	12	100			V_{DD} = 1.8V, EN = $0.8V_{DD}$ to V_{OUT} = $0.9(V_{DD}/2)$, V_L = 0V
		—	30	100			V_{DD} = 5.5V, EN = $0.8V_{DD}$ to V_{OUT} = $0.9(V_{DD}/2)$, V_L = 0V
EN Low to EN High hold time	t_{ENLH}	50	—	—			Minimum time before releasing EN (**Note 1**)
EN High to EN Low setup time	t_{ENHL}	50	—	—			Minimum time before exerting EN (**Note 1**)
POR Dynamic Specifications							
V_{DD} ↓ to Output Off	t_{PHL}	—	10	—	µs	all	V_L = 0V, V_{DD} = 1.8V to V_{PRL} – 0.1V step, 90% of V_{OUT} change
V_{DD} ↑ to Output On	t_{PLH}	—	100	—			V_L = 0V, V_{DD} = 0V to V_{PRH} + 0.1V step, 90% of V_{OUT} change

Note 1: For design guidance only; not tested.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{DD} = 1.8V to 5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125		**Note 1**
Storage Temperature Range	T_A	-65	—	+150		
Thermal Package Resistances						
Thermal Resistance, 8L-DFN (3×3)	θ_{JA}	—	57	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—		

Note 1: Operation must not cause T_J to exceed the Absolute Maximum Junction Temperature specification (+150°C).

1.3 Timing Diagrams

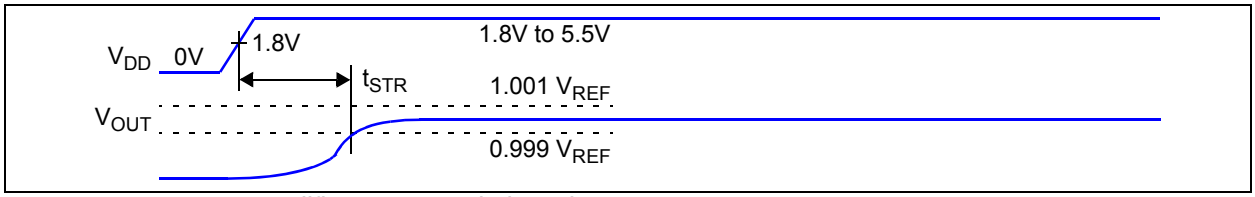


FIGURE 1-1: *Amplifier Start-Up Timing Diagram.*

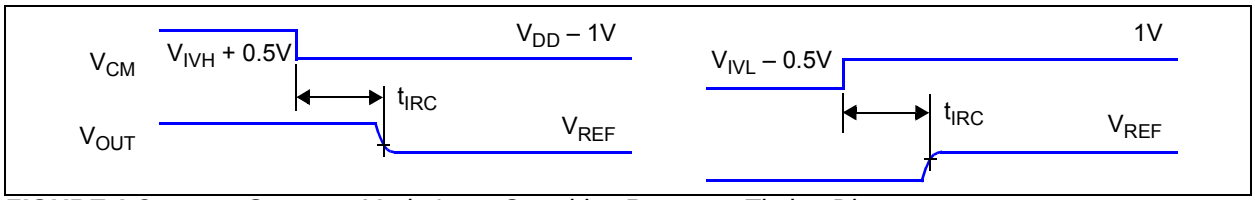


FIGURE 1-2: *Common Mode Input Overdrive Recovery Timing Diagram.*

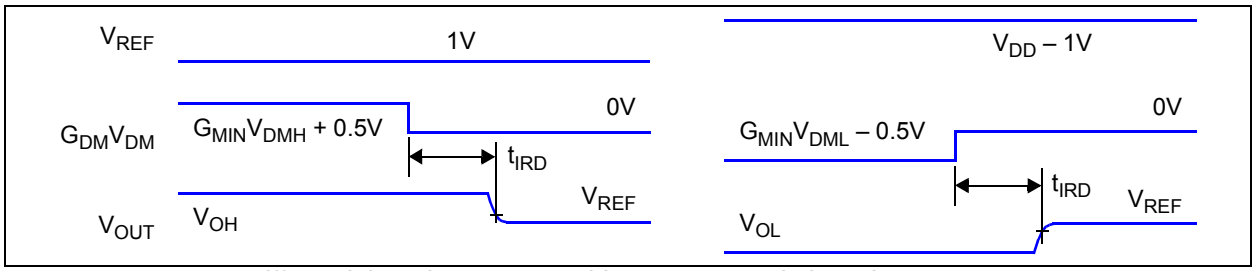


FIGURE 1-3: *Differential Mode Input Overdrive Recovery Timing Diagram.*

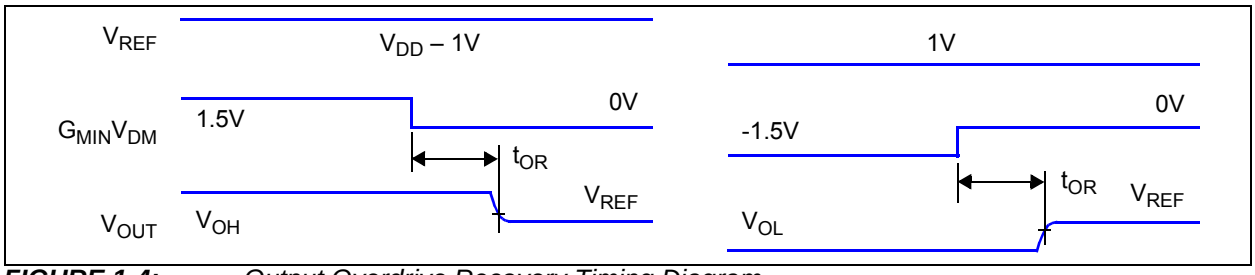


FIGURE 1-4: *Output Overdrive Recovery Timing Diagram.*

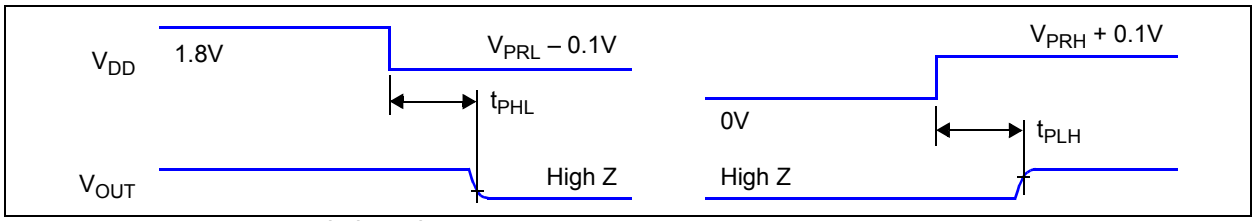


FIGURE 1-5: *POR Timing Diagram.*

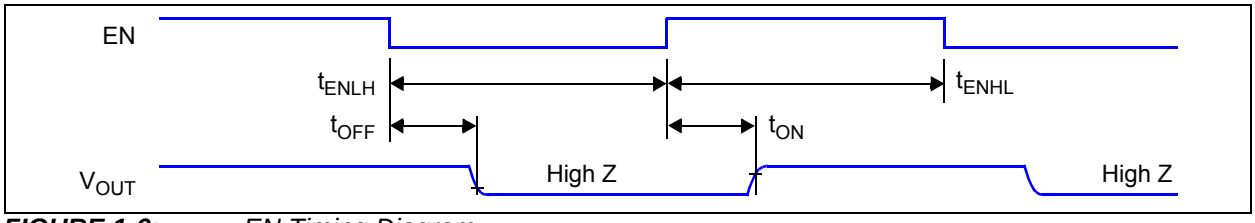


FIGURE 1-6: *EN Timing Diagram.*

1.4 DC Test Circuits

1.4.1 INPUT OFFSET TEST CIRCUIT

Figure 1-7 is a simple circuit that can test the INA's input offset errors and input voltage range (V_E, V_{IVL} and V_{IVH}; see **Section 1.5.1 "Input Offset Related Errors"** and **Section 1.5.2 "Input Offset Common Mode Nonlinearity"**). U_2 is part of a control loop that forces V_{OUT} to equal V_{CNT}; U_1 can be set to any bias point.

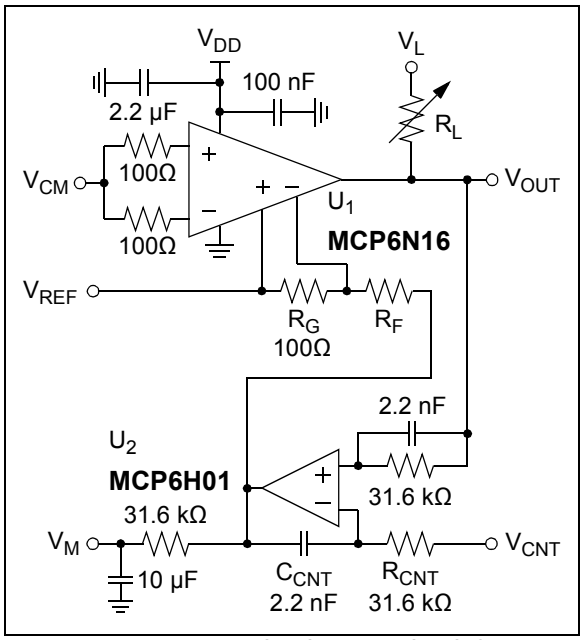


FIGURE 1-7: *Simple Test Circuit for Common Mode (Input Offset).*

When MCP6N16 is in its normal range of operation, the DC output voltages are (where V_E is the sum of input offset errors and g_E is the gain error):

EQUATION 1-1:

$$\begin{aligned} G_{DM} &= 1 + R_F/R_G \\ V_{OUT} &= V_{CNT} \\ V_M &= V_{REF} + G_{DM}(1 + g_E)V_E \end{aligned}$$

Table 1-5 shows the resulting behavior for different G_{MIN} options.

TABLE 1-5: RESULTS

G_{MIN} (V/V) Nom.	R_F (kΩ) Typ.	G_{DM} (kV/V) Typ.	$G_{DM}V_{OS}$ (±mV) Max.	BW (kHz) Typ. at V_{OUT}	BW (Hz) Typ. at V_M
1	100	1.00	85	0.50	0.50
10	402	4.02	88	1.2	
100			68	8.7	

1.4.2 DIFFERENTIAL GAIN TEST CIRCUIT

Figure 1-8 is a simple circuit that can test the INA's differential gain error, nonlinearity and input voltage range (g_E, INL_{DM}, V_{DML} and V_{DMH}; see **Section 1.5.3 "Differential Gain Error and Nonlinearity"**). R_F and R_G are 0.01% for accurate gain error measurements.

The output voltages are (where V_E is the sum of input offset errors and g_E is the gain error):

EQUATION 1-2:

$$\begin{aligned} G_{DM} &= 1 + R_F/R_G \\ V_{OUT} &= V_{REF} + G_{DM}(1 + g_E)(V_{DM} + V_E) \\ V_M &= V_{REF} + G_{DM}(1 + g_E)(V_{DM} + V_E) \end{aligned}$$

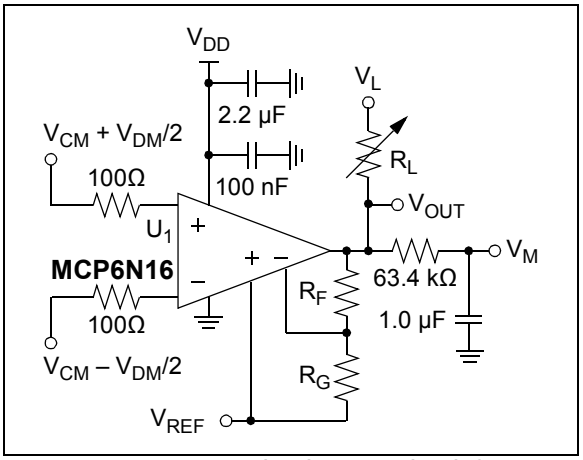


FIGURE 1-8: *Simple Test Circuit for Differential Mode.*

For different values of V_{REF}, V_{DM} sweeps over different ranges to keep V_{REF}, V_{FG} and V_{OUT} within their ranges.

Table 1-6 shows the recommended R_F and R_G; they produce a 10 kΩ load. V_L can usually be left open.

TABLE 1-6: SELECTING R_F AND R_G

G_{MIN} (V/V) Nom.	R_F (kΩ) Nom.	R_G (kΩ) Nom.	G_{DM} (V/V) Nom.
1	0	Open	1.0000
10	10.0 || 90.9	1.00	10.009
100	10.0 || 1000	100	100.01

1.4.3 DYNAMIC TESTING OF INPUT BEHAVIOR

The circuit in Figure 1-8 can test the input's dynamic behavior (i.e., IMD, t_{STR}, t_{STL}, t_{IRC}, t_{IRD} and t_{OR}); measure the output at V_{OUT}, instead of at V_M.

1.5 Explanation of DC Error Specifications

1.5.1 INPUT OFFSET RELATED ERRORS

The input offset error (V_E) is extracted from input offset measurements (see **Section 1.4.1 "Input Offset Test Circuit"**), based on Equation 1-1:

EQUATION 1-3:

$$V_E = (V_M - V_{REF}) / (G_{DM}(1 + g_E))$$

V_E has several terms, which assume a linear response to changes in V_{DD}, V_{SS}, V_{CM}, V_{OUT} and T_A (all of which are in their specified ranges):

EQUATION 1-4:

$$V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{REF}}{CMRR2} + \frac{\Delta V_{OUT}}{A_{OL}} + \Delta T_A \cdot TC_1$$

Where:

PSRR, *CMRR*, CMRR2 and A_{OL} are in units of V/V

ΔT_A is in units of °C

TC_1 is in units of V/°C

V_{DM} = 0

Equation 1-2 shows how V_E affects V_{OUT}.

1.5.2 INPUT OFFSET COMMON MODE NONLINEARITY

The input offset error (V_E) changes nonlinearly with V_{CM}. Figure 1-9 shows V_E vs. V_{CM}, as well as a linear fit line (V_{E_LIN}) based on V_{OS} and CMRR. The INA is in standard conditions (ΔV_{OUT} = 0, V_{DM} = 0, etc.). V_{CM} is swept from V_{IVL} to V_{IVH}. The test circuit is in **Section 1.4.1 "Input Offset Test Circuit"** and V_E is calculated using Equation 1-3.

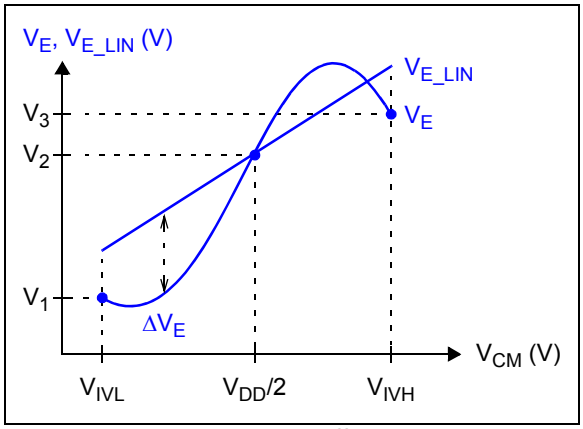


FIGURE 1-9: *Input Offset Error vs. Common Mode Input Voltage.*

Based on the measured V_E data, we obtain the following linear fit:

EQUATION 1-5:

$$V_{E\_LIN} = V_{OS} + (V_{CM} - V_{DD}/2)/CMRR$$

Where:

$$V_{OS} = V_2$$

$$1/CMRR = (V_3 - V_1)/(V_{IVH} - V_{IVL})$$

The remaining error (ΔV_E) is described by the Common Mode Nonlinearity spec:

EQUATION 1-6:

$$INL_{CMH} = max(\Delta V_E)/(V_{IVH} - V_{IVL})$$

$$INL_{CML} = min(\Delta V_E)/(V_{IVH} - V_{IVL})$$

$$INL_{CM} = INL_{CMH}, \quad |INL_{CMH}| \geq |INL_{CML}|$$

$$= INL_{CML}, \quad otherwise$$

Where:

$$\Delta V_E = V_E - V_{E\_LIN}$$

The same common mode behavior applies to V_E when V_{REF} is swept, instead of V_{CM}, since both input stages are designed the same:

EQUATION 1-7:

$$V_{E\_LIN2} = V_{OS} + (V_{REF} - V_{DD}/2)/CMRR2$$

$$INL_{CMH2} = max(\Delta V_{E2})/(V_{IVH} - V_{IVL})$$

$$INL_{CML2} = min(\Delta V_{E2})/(V_{IVH} - V_{IVL})$$

$$INL_{CM2} = INL_{CMH2}, \quad |INL_{CMH2}| \geq |INL_{CML2}|$$

$$= INL_{CML2}, \quad otherwise$$

Where:

$$\Delta V_{E2} = V_E - V_{E\_LIN2}$$

1.5.3 DIFFERENTIAL GAIN ERROR AND NONLINEARITY

The differential errors are extracted from differential gain measurements (see **Section 1.4.2 "Differential Gain Test Circuit"**), based on Equation 1-2. These errors are the differential gain error (g_E) and the input offset error (V_E, which changes nonlinearly with V_{DM}):

EQUATION 1-8:

$$G_{DM} = 1 + R_F/R_G$$
$$V_M = G_{DM}(1 + g_E)(V_{DM} + V_E)$$

These errors are adjusted for the expected output, then referred back to the input, giving the differential input error (V_{ED}) as a function of V_{DM}:

EQUATION 1-9:

$$V_{ED} = V_M/G_{DM} - V_{DM}$$

Figure 1-10 shows V_{ED} vs. V_{DM}, as well as a linear fit line (V_{ED_LIN}) based on V_{ED} and g_E. The INA is in standard conditions (ΔV_{OUT} = 0, etc.). V_{DM} is swept from V_{DML} to V_{DMH}.

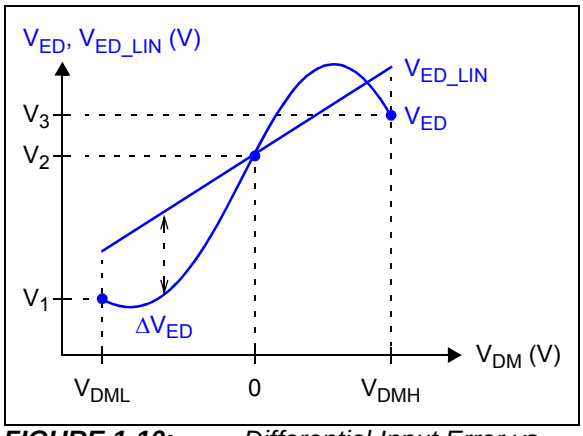


FIGURE 1-10: *Differential Input Error vs. Differential Input Voltage.*

Based on the measured V_{ED} data, we obtain the following linear fit:

EQUATION 1-10:

$$V_{ED\_LIN} = (1 + g_E)V_E + g_E V_{DM}$$
Where:
$$g_E = (V_3 - V_1)/(V_{DMH} - V_{DML}) - 1$$
$$V_E = V_2/(1 + g_E)$$

Note that the V_E value measured here is not as accurate as the one obtained in **Section 1.5.1 "Input Offset Related Errors"**.

The remaining error (ΔV_{ED}) is described by the Differential Nonlinearity spec:

EQUATION 1-11:

$$INL_{DMH} = max(\Delta V_{ED})/(V_{DMH} - V_{DML})$$
$$INL_{DML} = min(\Delta V_{ED})/(V_{DMH} - V_{DML})$$
$$INL_{DM} = INL_{DMH}, \quad |INL_{DMH}| \geq |INL_{DML}|$$
$$= INL_{DML}, \quad \text{otherwise}$$
Where:
$$\Delta V_{ED} = V_{ED} - V_{ED\_LIN}$$

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

2.1 DC Precision

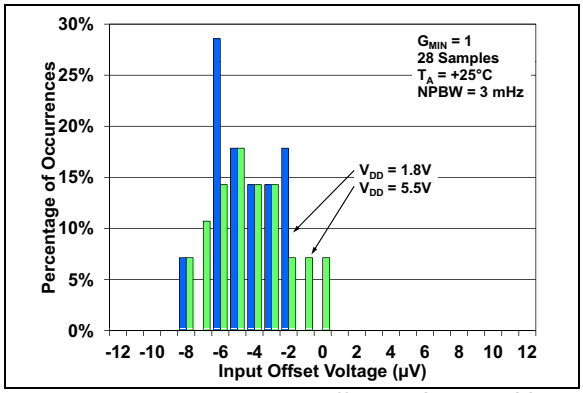


FIGURE 2-1: *Input Offset Voltage, with G_{MIN} = 1.*

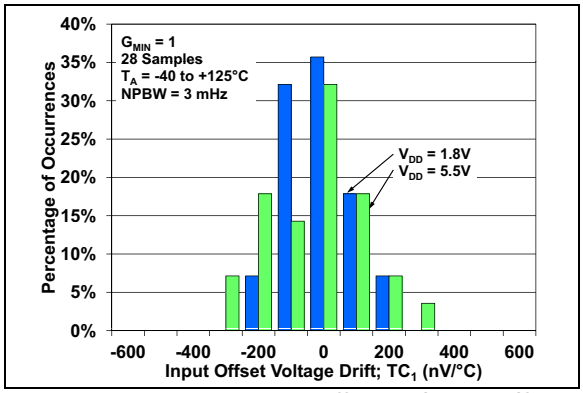


FIGURE 2-4: *Input Offset Voltage Drift, with G_{MIN} = 1.*

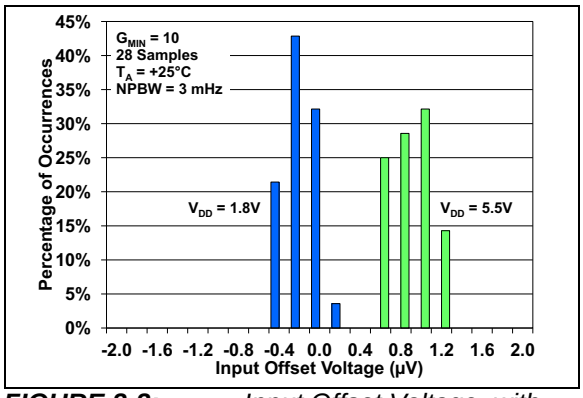


FIGURE 2-2: *Input Offset Voltage, with G_{MIN} = 10.*

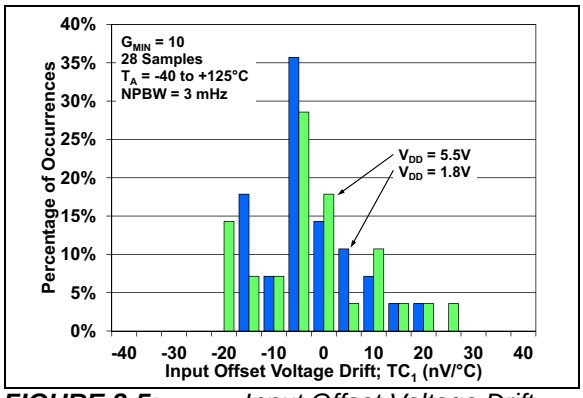


FIGURE 2-5: *Input Offset Voltage Drift, with G_{MIN} = 10.*

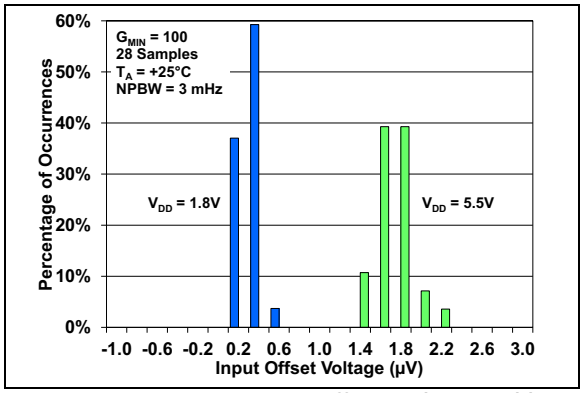


FIGURE 2-3: *Input Offset Voltage, with G_{MIN} = 100.*

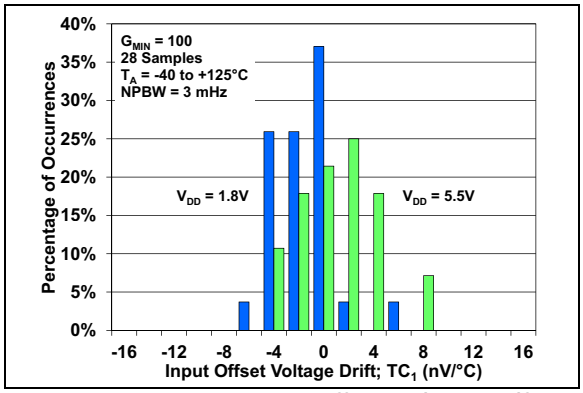


FIGURE 2-6: *Input Offset Voltage Drift, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

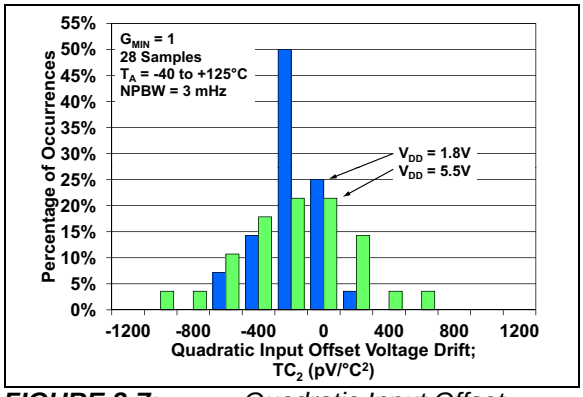


FIGURE 2-7: *Quadratic Input Offset Voltage Drift, with G_{MIN} = 1.*

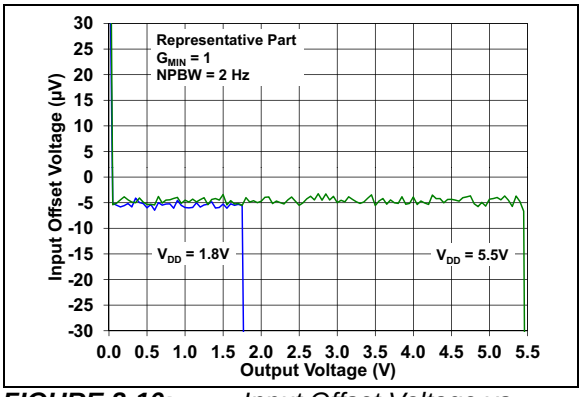


FIGURE 2-10: *Input Offset Voltage vs. Output Voltage, with G_{MIN} = 1.*

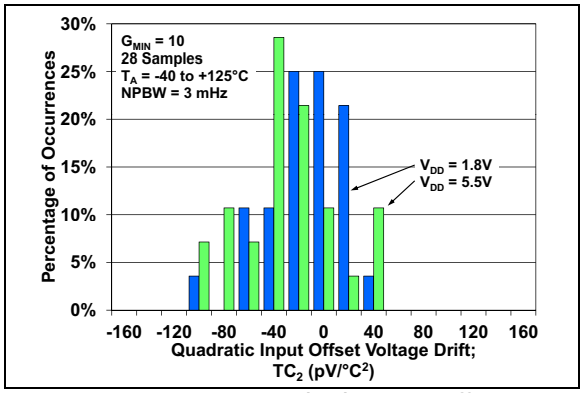


FIGURE 2-8: *Quadratic Input Offset Voltage Drift, with G_{MIN} = 10.*

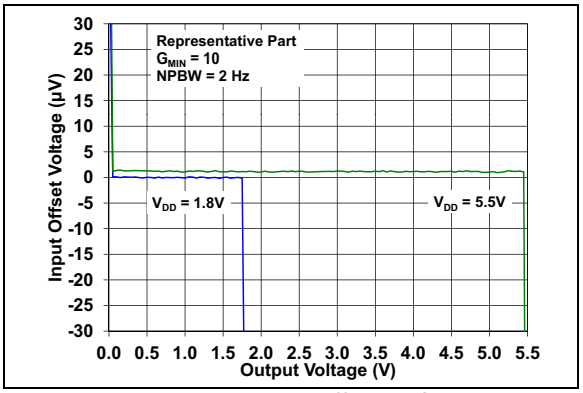


FIGURE 2-11: *Input Offset Voltage vs. Output Voltage, with G_{MIN} = 10.*

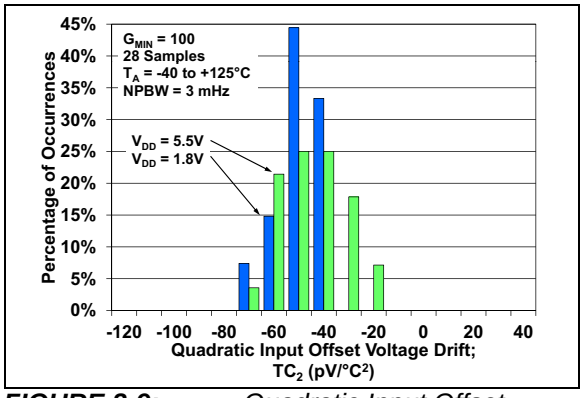


FIGURE 2-9: *Quadratic Input Offset Voltage Drift, with G_{MIN} = 100.*

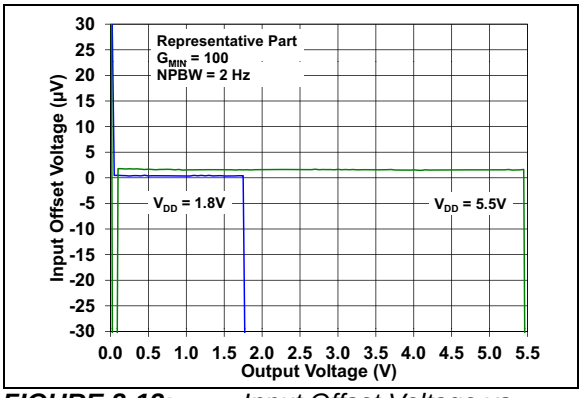


FIGURE 2-12: *Input Offset Voltage vs. Output Voltage, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

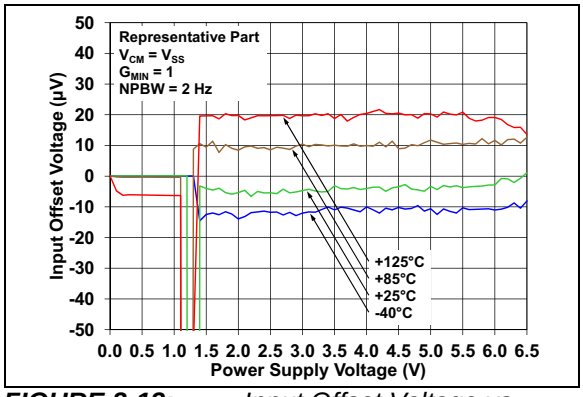


FIGURE 2-13: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0V and G_{MIN} = 1.*

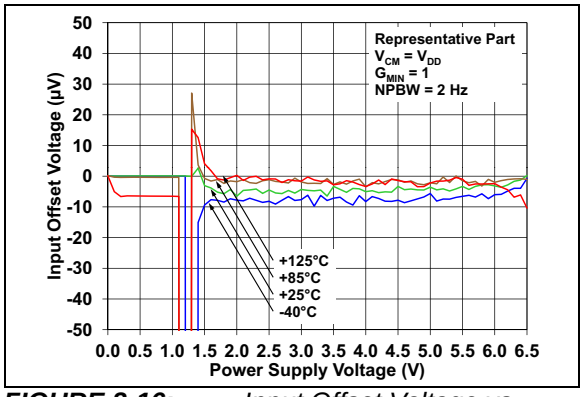


FIGURE 2-16: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} and G_{MIN} = 1.*

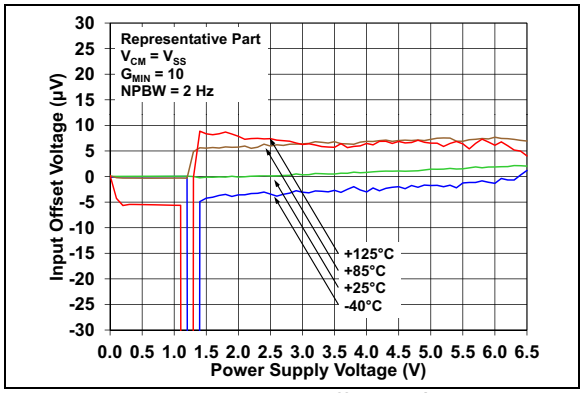


FIGURE 2-14: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0V and G_{MIN} = 10.*

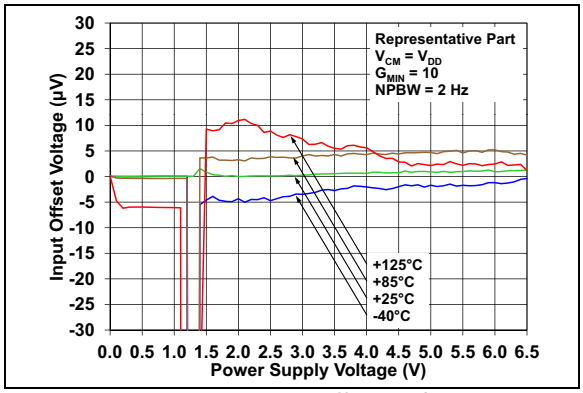


FIGURE 2-17: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} and G_{MIN} = 10.*

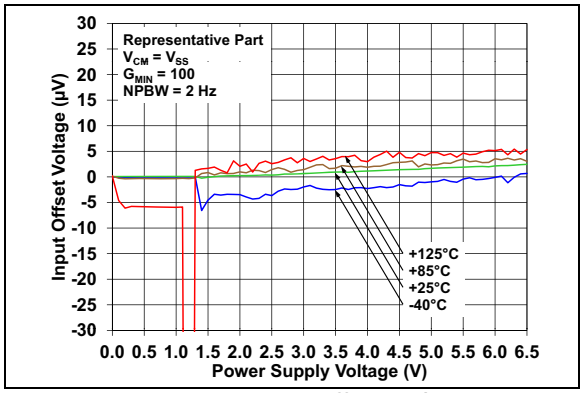


FIGURE 2-15: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = 0V and G_{MIN} = 100.*

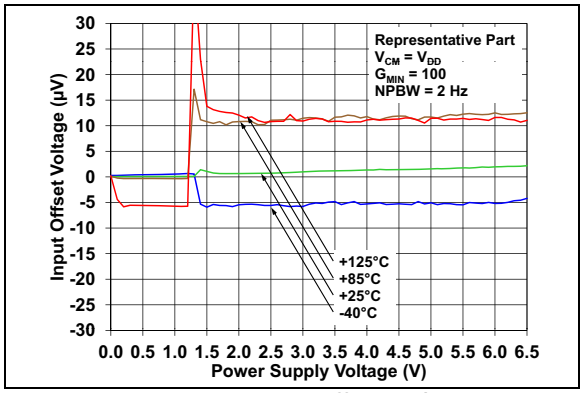


FIGURE 2-18: *Input Offset Voltage vs. Power Supply Voltage, with V_{CM} = V_{DD} and G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

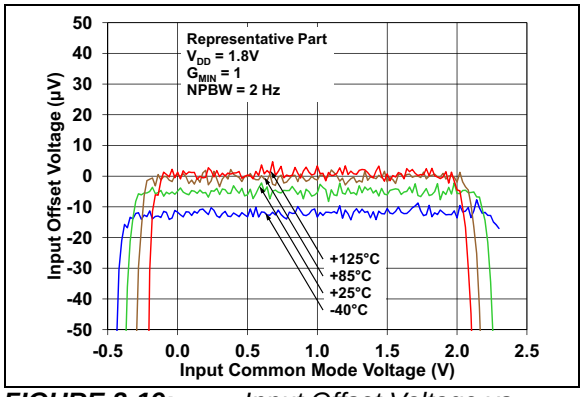


FIGURE 2-19: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 1.8V and G_{MIN} = 1.*

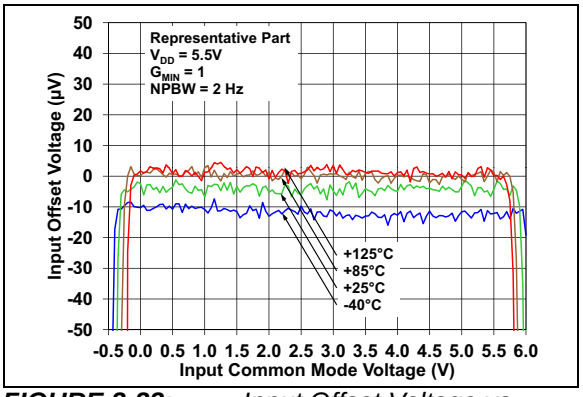


FIGURE 2-22: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 5.5V and G_{MIN} = 1.*

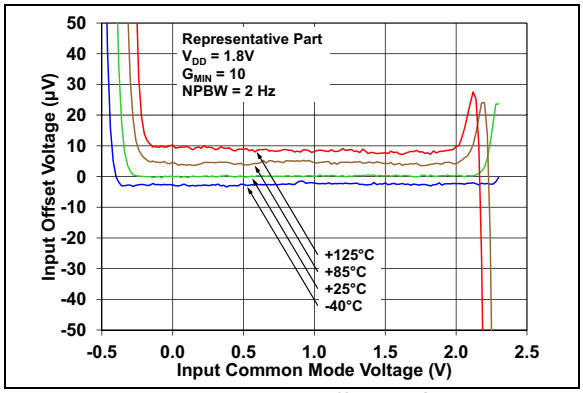


FIGURE 2-20: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 1.8V and G_{MIN} = 10.*

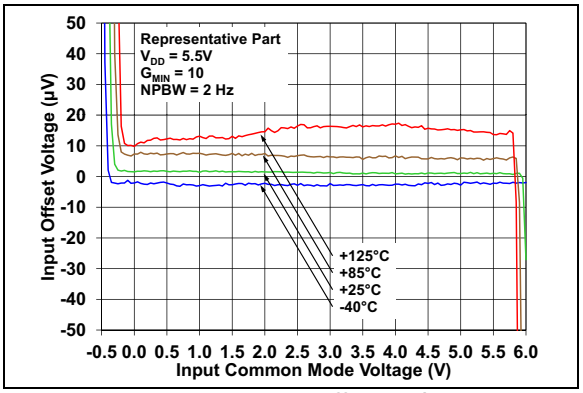


FIGURE 2-23: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 5.5V and G_{MIN} = 10.*

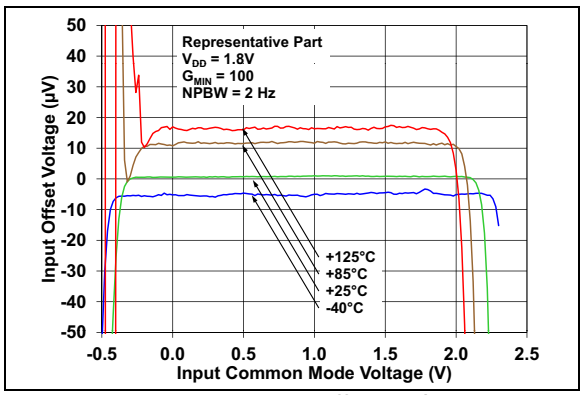


FIGURE 2-21: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 1.8V and G_{MIN} = 100.*

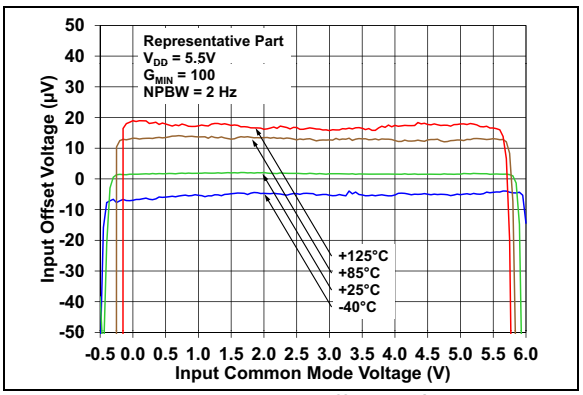


FIGURE 2-24: *Input Offset Voltage vs. Common Mode Voltage, with V_{DD} = 5.5V and G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

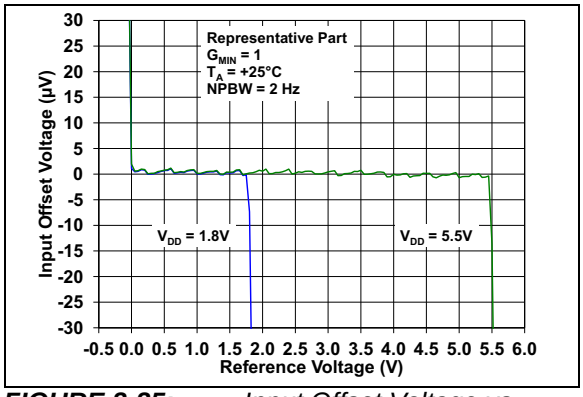


FIGURE 2-25: *Input Offset Voltage vs. Reference Voltage, with G_{MIN} = 1.*

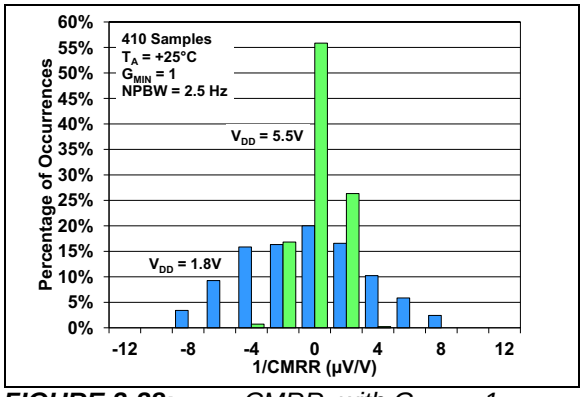


FIGURE 2-28: *CMRR, with G_{MIN} = 1.*

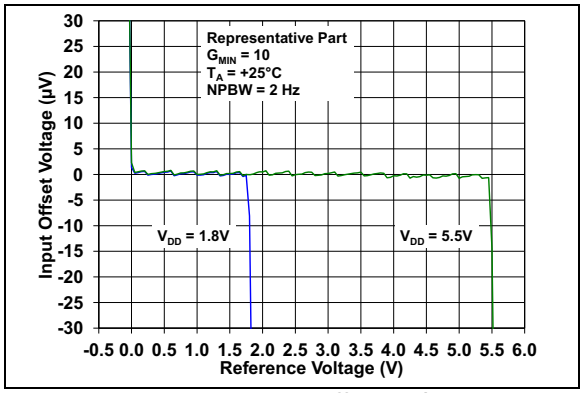


FIGURE 2-26: *Input Offset Voltage vs. Reference Voltage, with G_{MIN} = 10.*

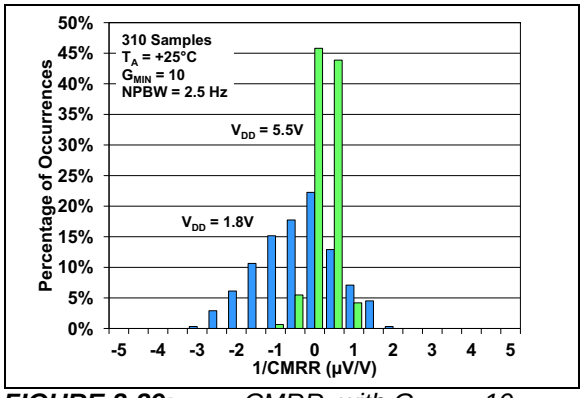


FIGURE 2-29: *CMRR, with G_{MIN} = 10.*

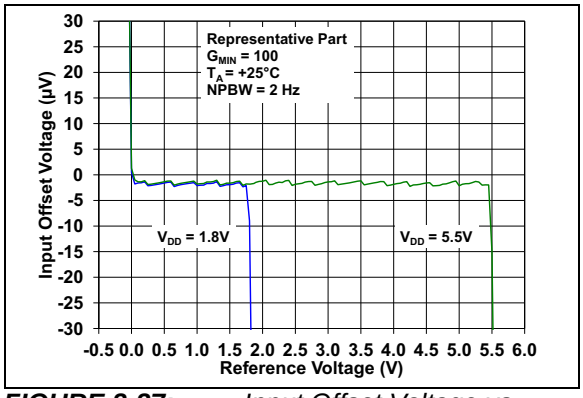


FIGURE 2-27: *Input Offset Voltage vs. Reference Voltage, with G_{MIN} = 100.*

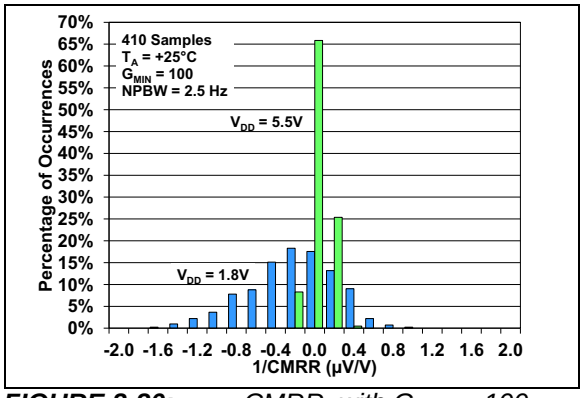


FIGURE 2-30: *CMRR, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

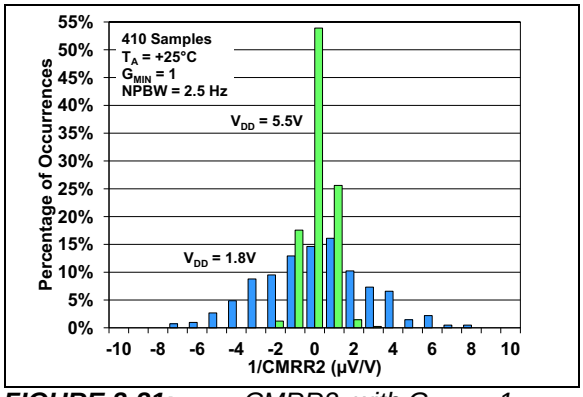


FIGURE 2-31: *CMRR2, with G_{MIN} = 1.*

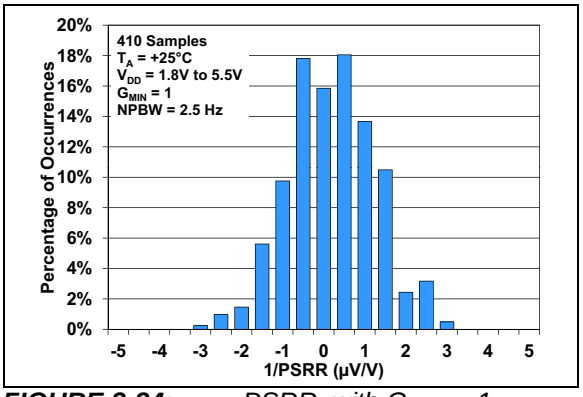


FIGURE 2-34: *PSRR, with G_{MIN} = 1.*

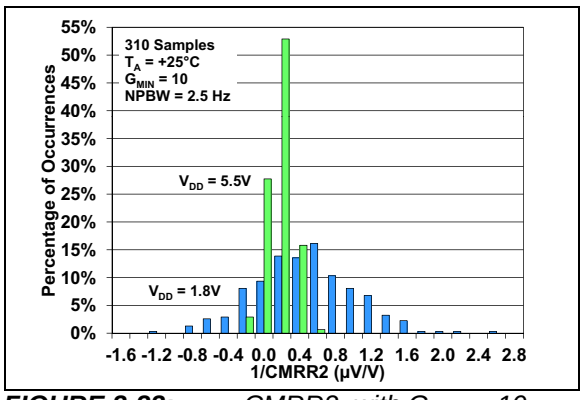


FIGURE 2-32: *CMRR2, with G_{MIN} = 10.*

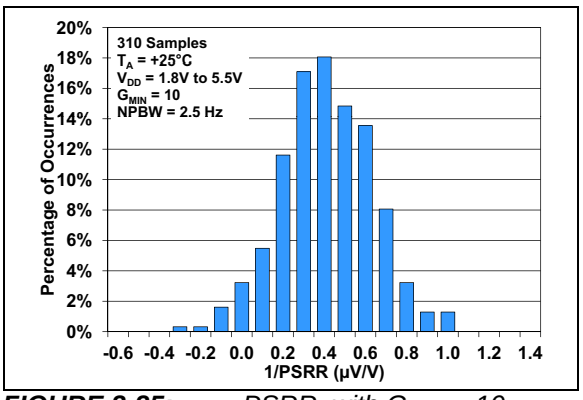


FIGURE 2-35: *PSRR, with G_{MIN} = 10.*

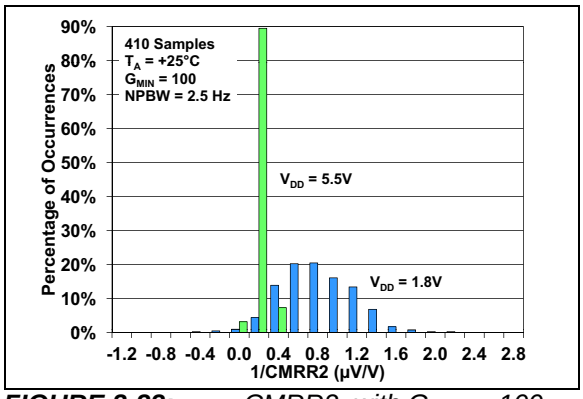


FIGURE 2-33: *CMRR2, with G_{MIN} = 100.*

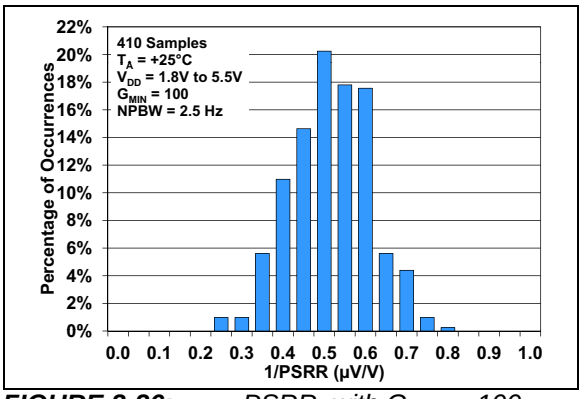


FIGURE 2-36: *PSRR, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

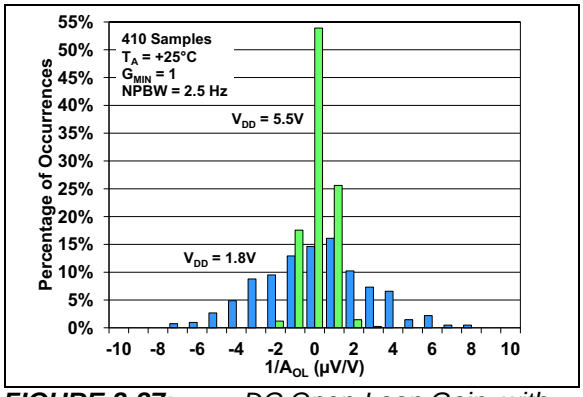


FIGURE 2-37: *DC Open-Loop Gain, with G_{MIN} = 1.*

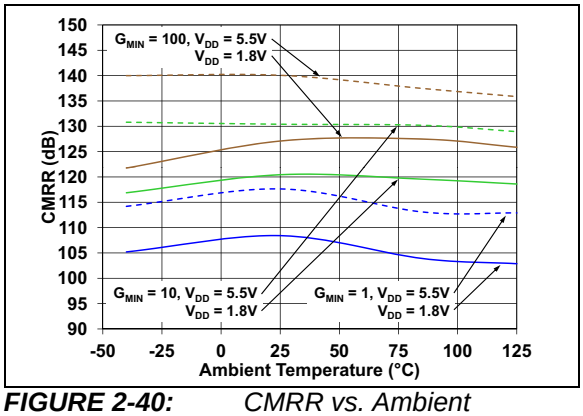


FIGURE 2-40: *CMRR vs. Ambient Temperature.*

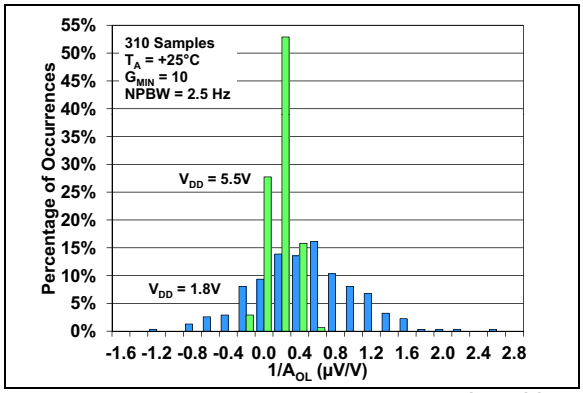


FIGURE 2-38: *DC Open-Loop Gain, with G_{MIN} = 10.*

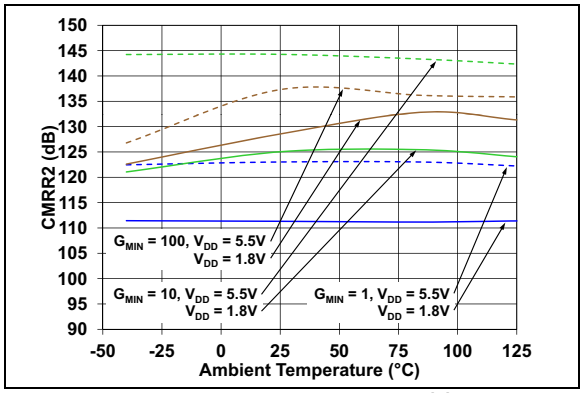


FIGURE 2-41: *CMRR2 vs. Ambient Temperature.*

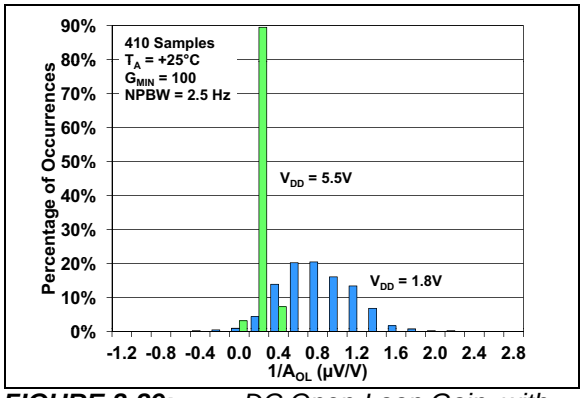


FIGURE 2-39: *DC Open-Loop Gain, with G_{MIN} = 100.*

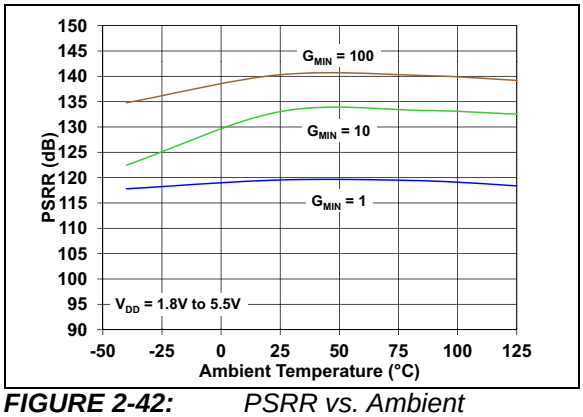


FIGURE 2-42: *PSRR vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

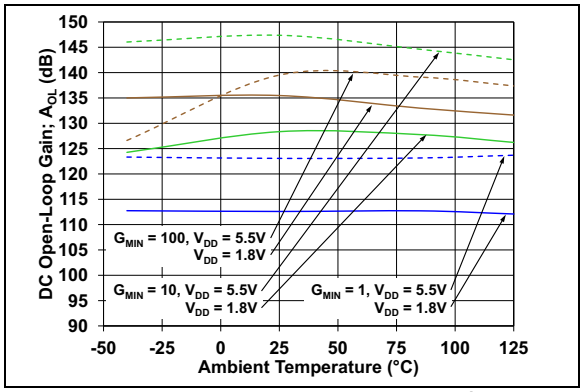


FIGURE 2-43: *DC Open-Loop Gain vs. Ambient Temperature.*

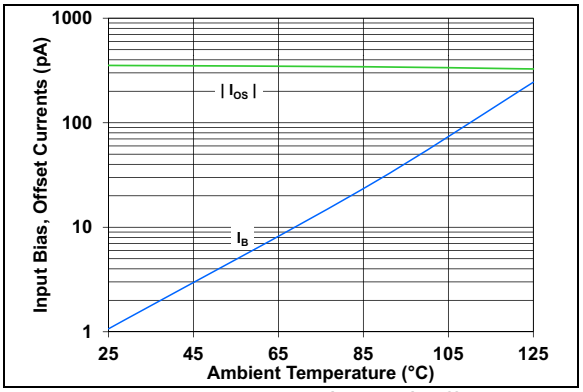


FIGURE 2-46: *Input Bias and Offset Currents vs. Ambient Temperature, with V_{DD} = 5.5V.*

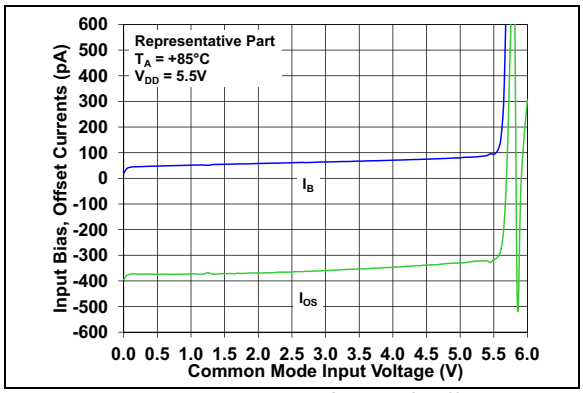


FIGURE 2-44: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +85°C.*

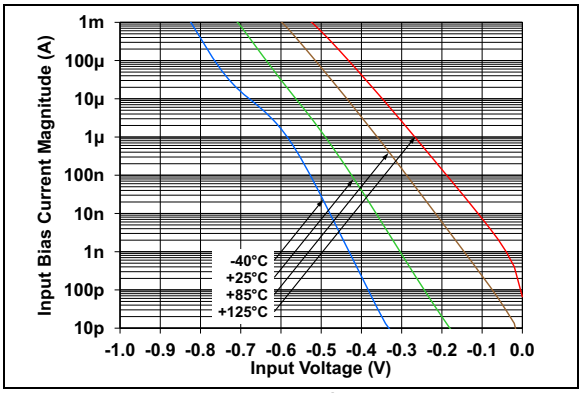


FIGURE 2-47: *Input Bias Current Magnitude vs. Input Voltage (below V_{SS}).*

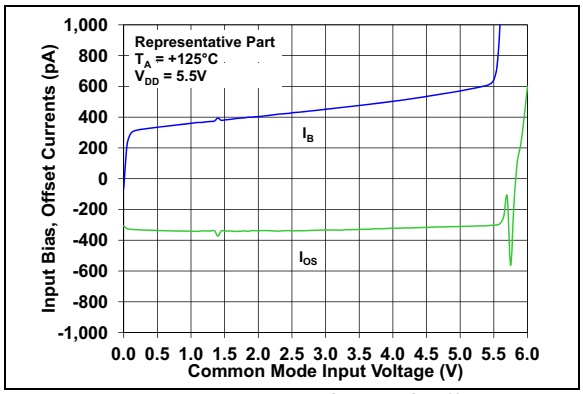


FIGURE 2-45: *Input Bias and Offset Currents vs. Common Mode Input Voltage, with T_A = +125°C.*

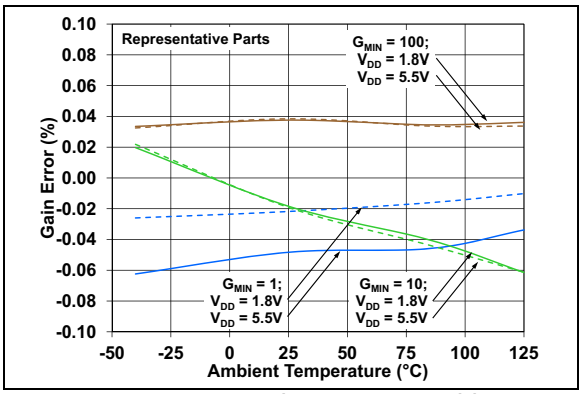


FIGURE 2-48: *Gain Error vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

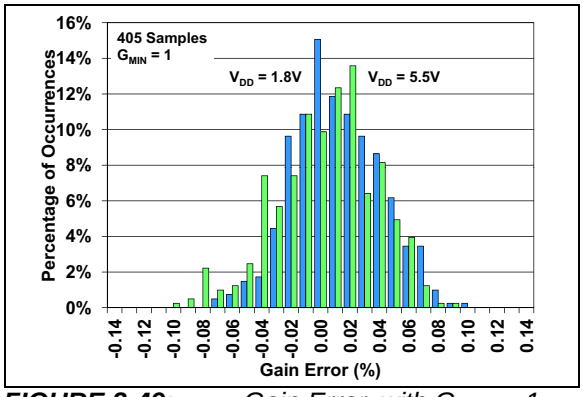


FIGURE 2-49: *Gain Error, with G_{MIN} = 1.*

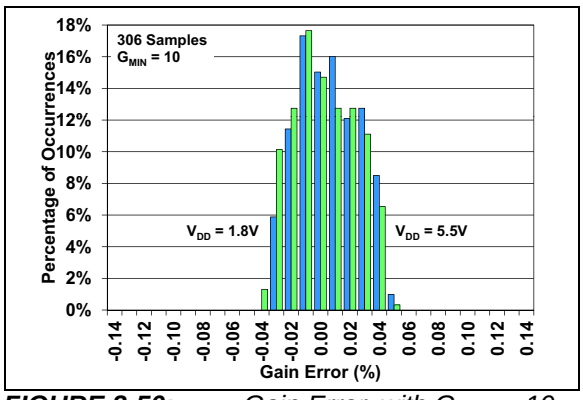


FIGURE 2-50: *Gain Error, with G_{MIN} = 10.*

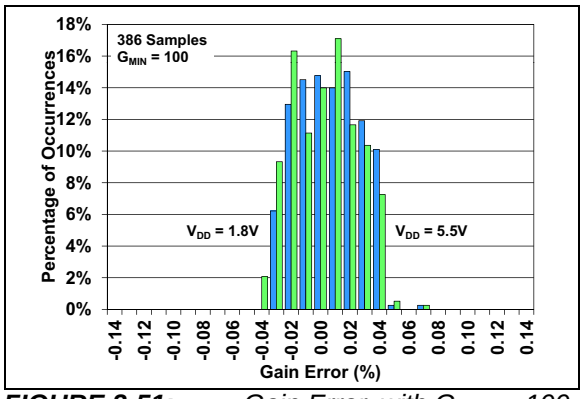


FIGURE 2-51: *Gain Error, with G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

2.2 Other DC Voltages and Currents

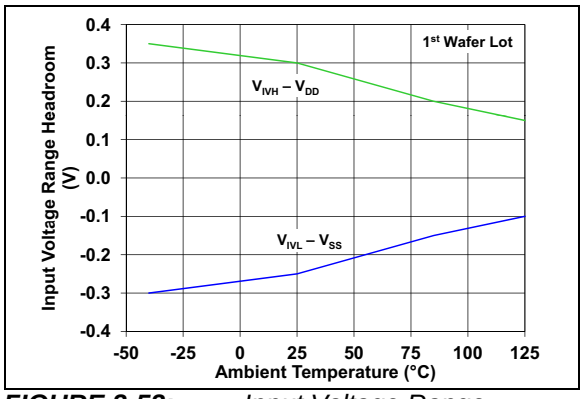


FIGURE 2-52: *Input Voltage Range Headroom vs. Ambient Temperature.*

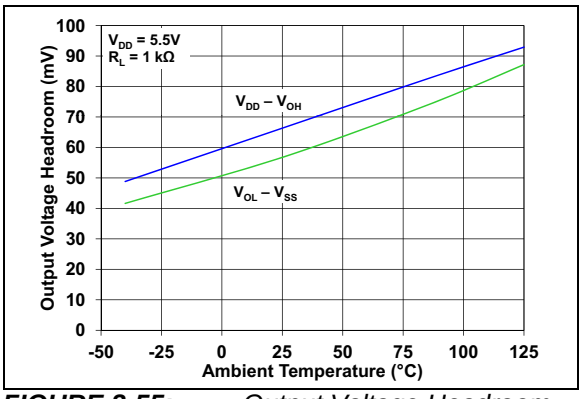


FIGURE 2-55: *Output Voltage Headroom vs. Ambient Temperature.*

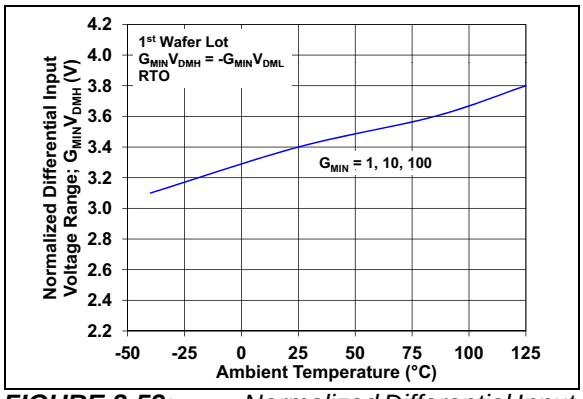


FIGURE 2-53: *Normalized Differential Input Voltage Range vs. Ambient Temperature.*

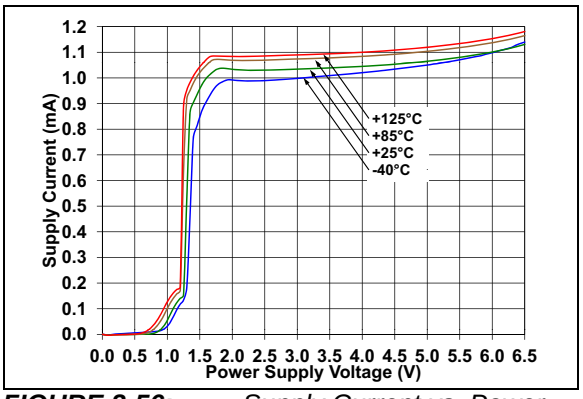


FIGURE 2-56: *Supply Current vs. Power Supply Voltage.*

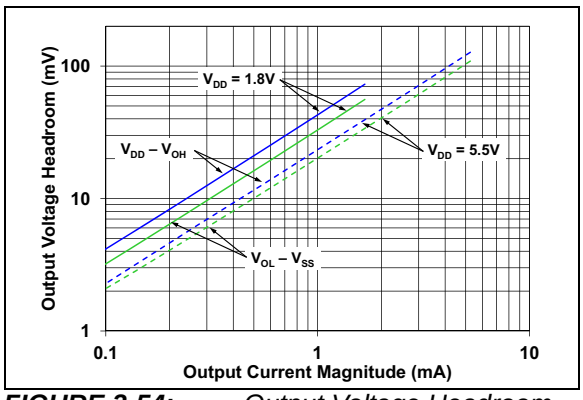


FIGURE 2-54: *Output Voltage Headroom vs. Output Current Magnitude.*

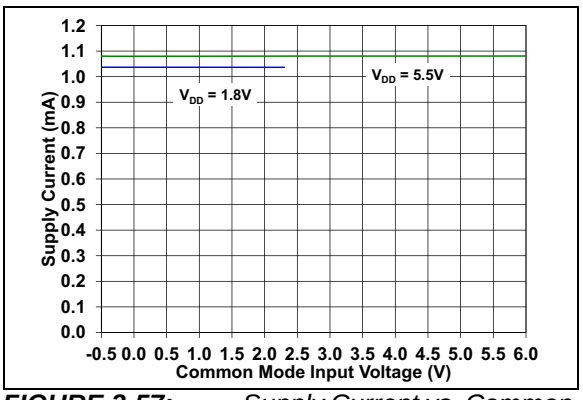


FIGURE 2-57: *Supply Current vs. Common Mode Input Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

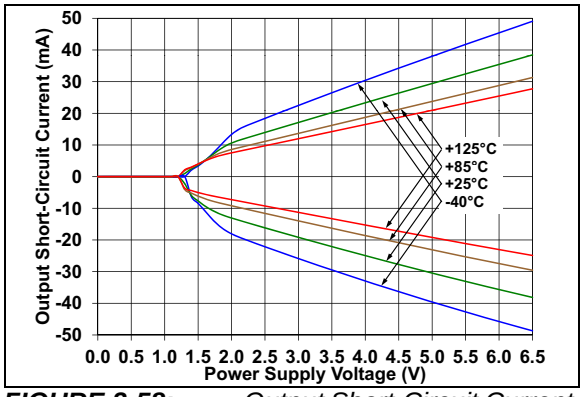


FIGURE 2-58: *Output Short-Circuit Current vs. Power Supply Voltage.*

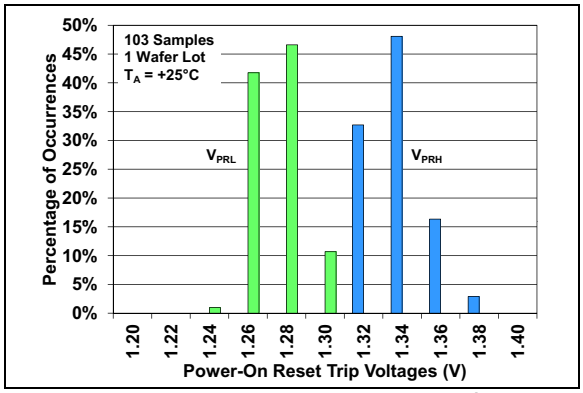


FIGURE 2-59: *Power-On Reset Trip Voltages.*

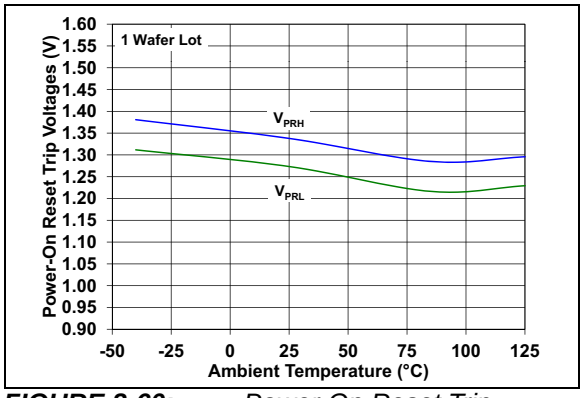


FIGURE 2-60: *Power-On Reset Trip Voltages vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

2.3 Frequency Response

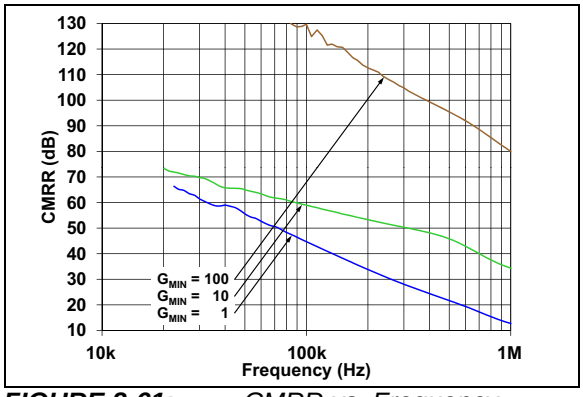


FIGURE 2-61: *CMRR vs. Frequency.*

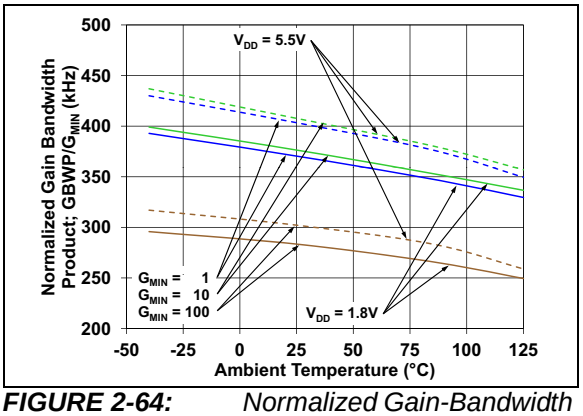


FIGURE 2-64: *Normalized Gain-Bandwidth Product vs. Ambient Temperature.*

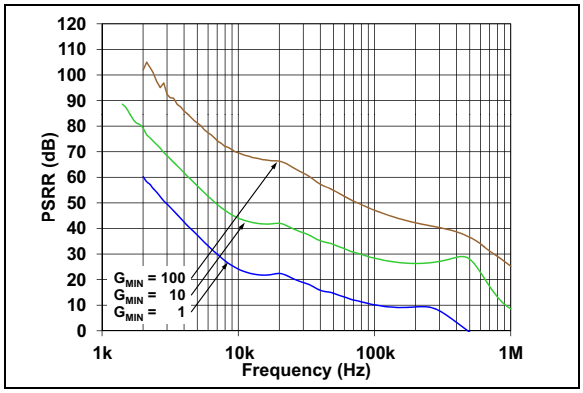


FIGURE 2-62: *PSRR vs. Frequency.*

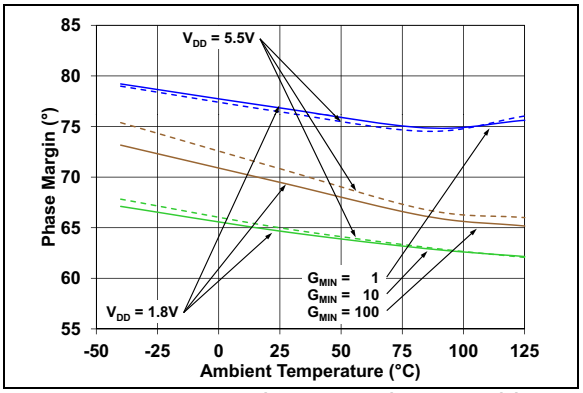


FIGURE 2-65: *Phase Margin vs. Ambient Temperature.*

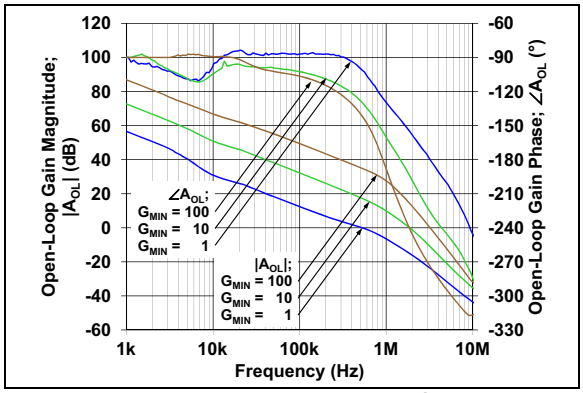


FIGURE 2-63: *Open-Loop Gain vs. Frequency.*

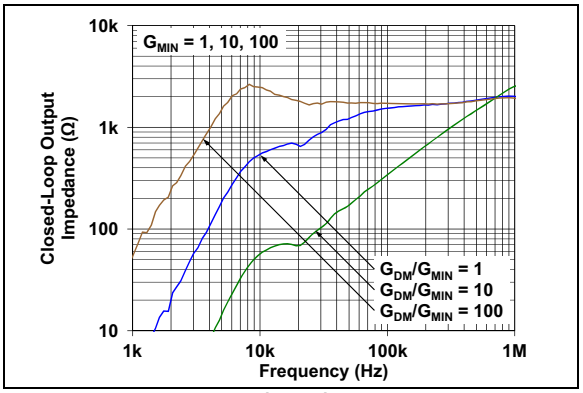


FIGURE 2-66: *Closed-Loop Output Impedance vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

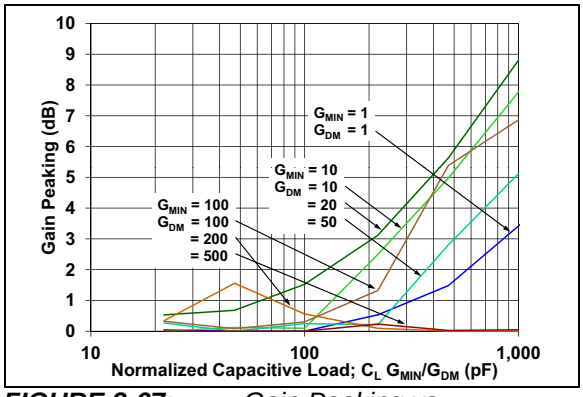


FIGURE 2-67: *Gain Peaking vs. Normalized Capacitive Load.*

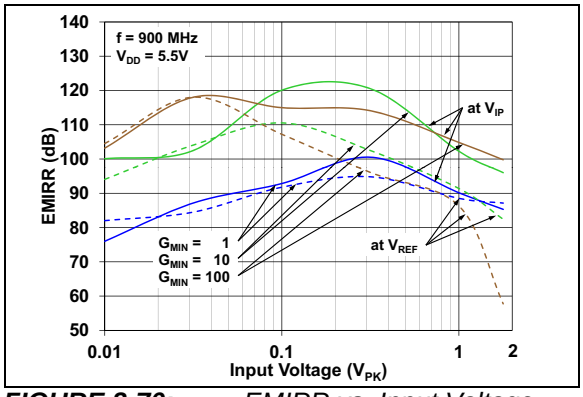


FIGURE 2-70: *EMIRR vs. Input Voltage, with f = 900 MHz.*

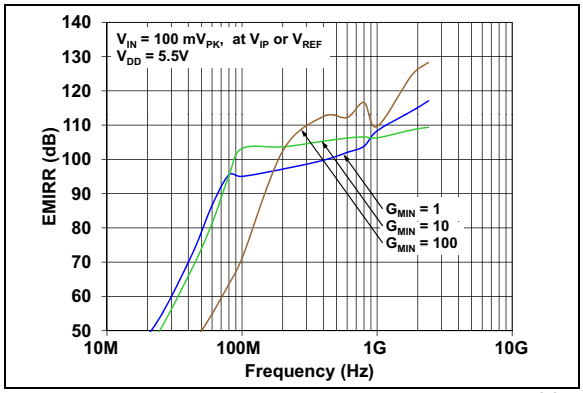


FIGURE 2-68: *EMIRR vs. Frequency, with V_{IN} = 100 mV_{PK}.*

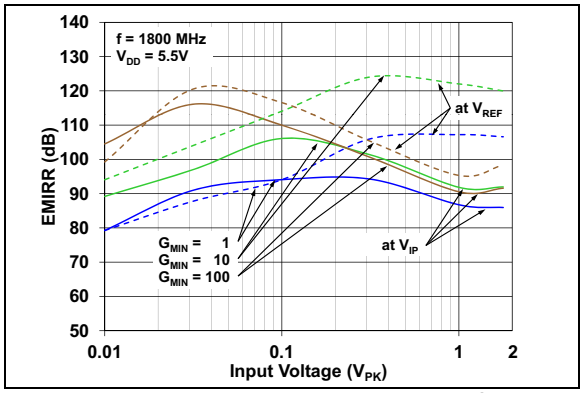


FIGURE 2-71: *EMIRR vs. Input Voltage, with f = 1800 MHz.*

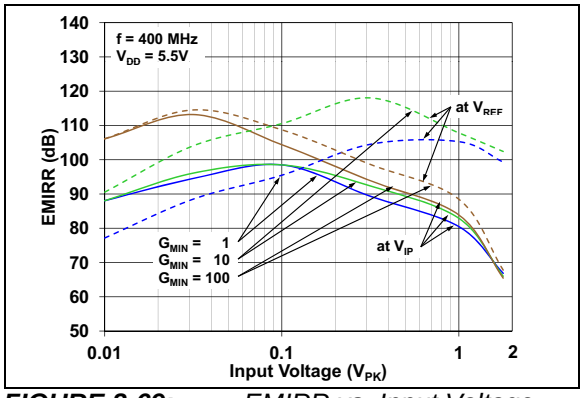


FIGURE 2-69: *EMIRR vs. Input Voltage, with f = 400 MHz.*

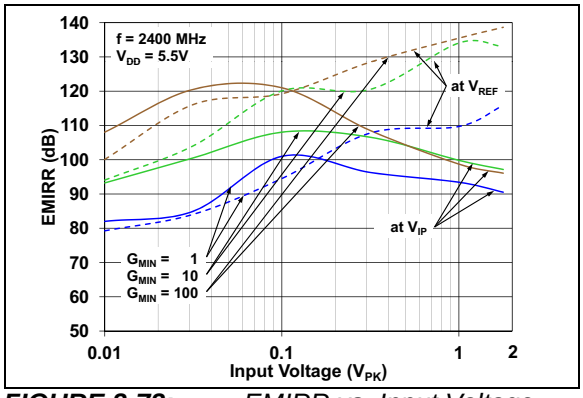


FIGURE 2-72: *EMIRR vs. Input Voltage, with f = 2400 MHz.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

2.4 Noise

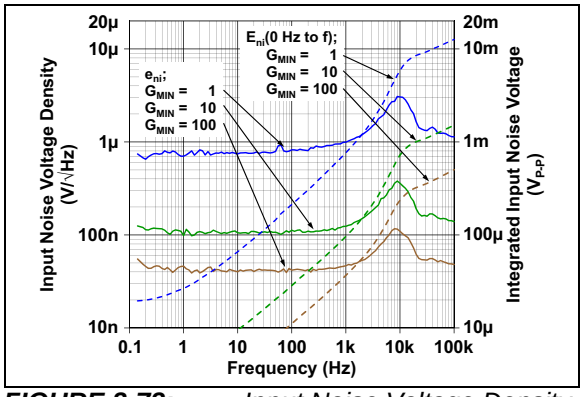


FIGURE 2-73: *Input Noise Voltage Density and Integrated Input Noise Voltage vs. Frequency.*

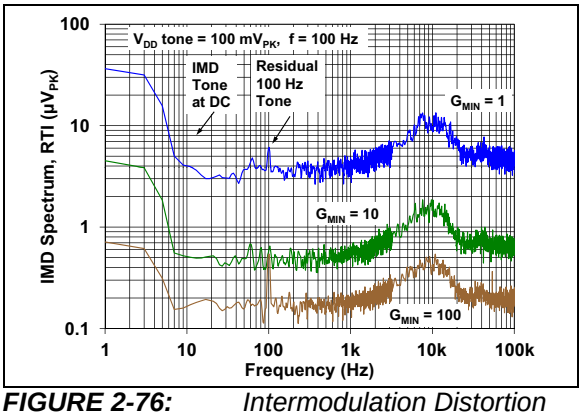


FIGURE 2-76: *Intermodulation Distortion vs. Frequency with V_{DD} Disturbance (see Figure 1-8).*

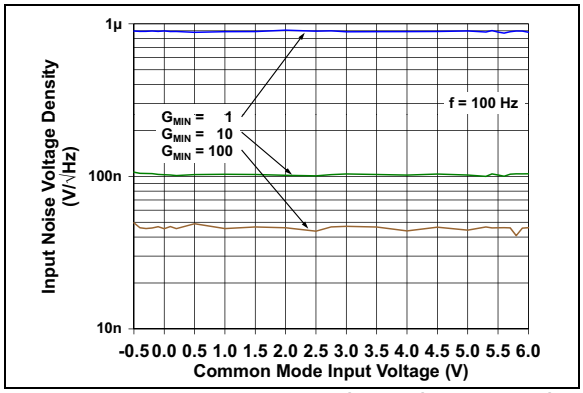


FIGURE 2-74: *Input Noise Voltage Density vs. Input Common Mode Voltage.*

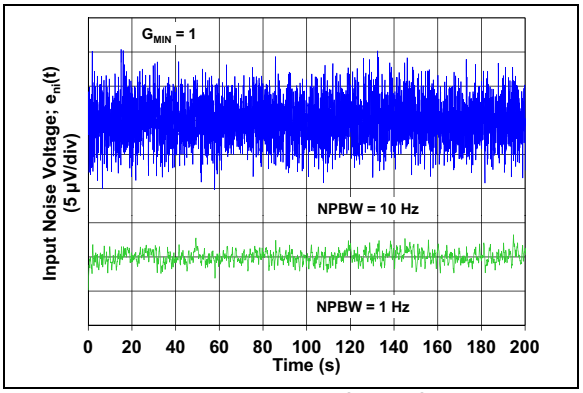


FIGURE 2-77: *Input Noise Voltage vs. Time, with 1 Hz and 10 Hz Filters and G_{MIN} = 1.*

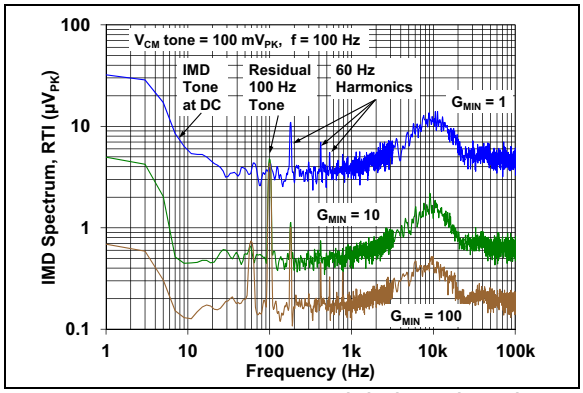


FIGURE 2-75: *Intermodulation Distortion vs. Frequency with V_{CM} Disturbance (see Figure 1-8).*

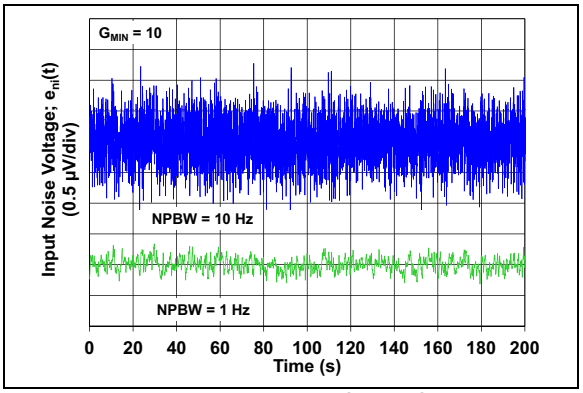


FIGURE 2-78: *Input Noise Voltage vs. Time, with 1 Hz and 10 Hz Filters and G_{MIN} = 10.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

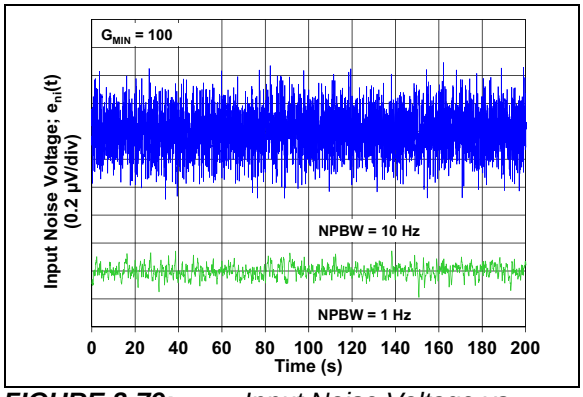


FIGURE 2-79: *Input Noise Voltage vs. Time, with 1 Hz and 10 Hz Filters and G_{MIN} = 100.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

2.5 Time Response

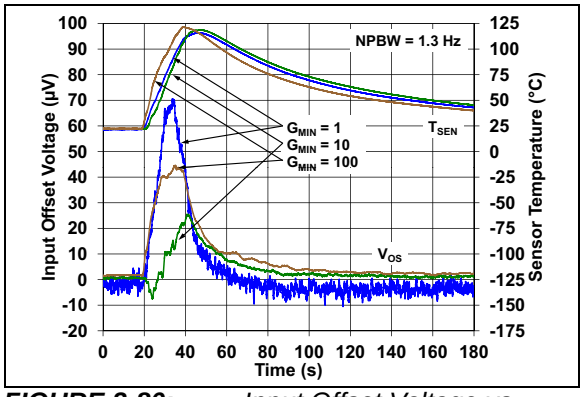


FIGURE 2-80: *Input Offset Voltage vs. Time with Temperature Change.*

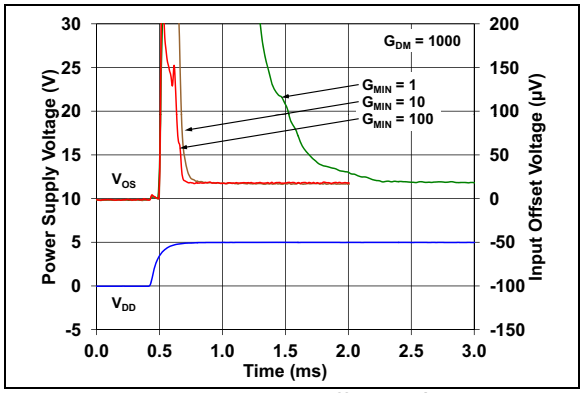


FIGURE 2-81: *Input Offset Voltage vs. Time at Power-Up.*

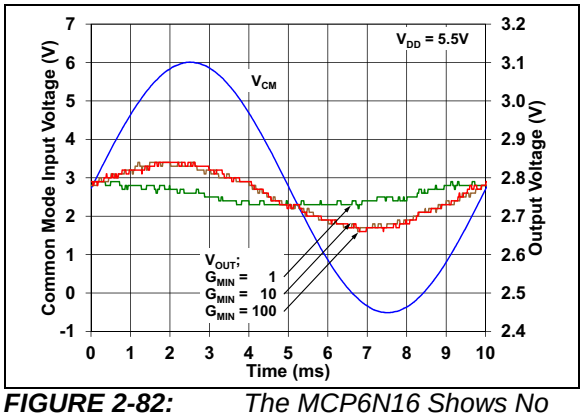


FIGURE 2-82: *The MCP6N16 Shows No Phase Reversal vs. Common Mode Input Overdrive, with V_{DD} = 5.5V.*

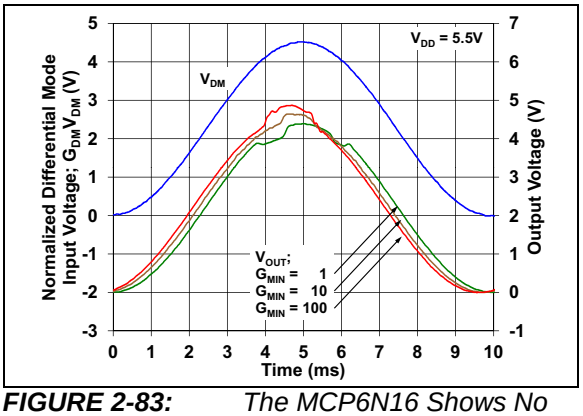


FIGURE 2-83: *The MCP6N16 Shows No Phase Reversal vs. Differential Input Overdrive, with V_{DD} = 5.5V.*

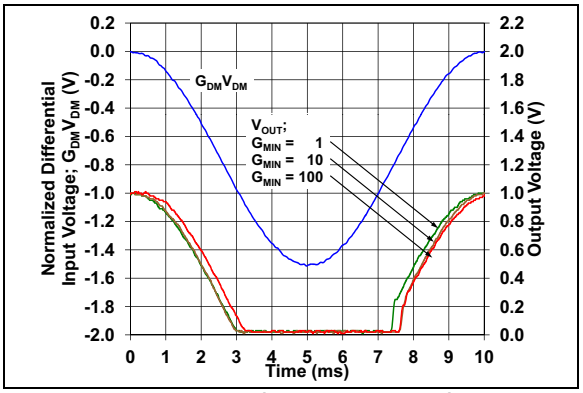


FIGURE 2-84: *The MCP6N16 Shows No Phase Reversal vs. Output Overdrive to V_{SS}.*

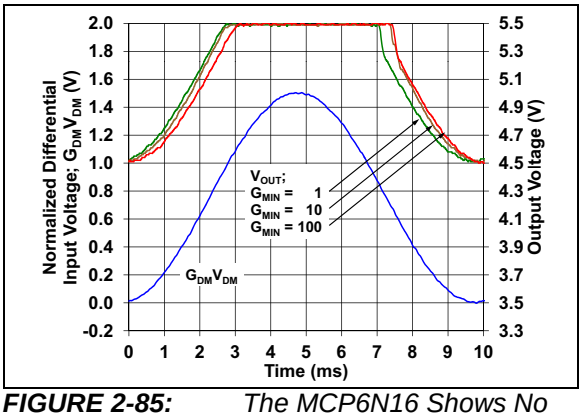


FIGURE 2-85: *The MCP6N16 Shows No Phase Reversal vs. Output Overdrive to V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

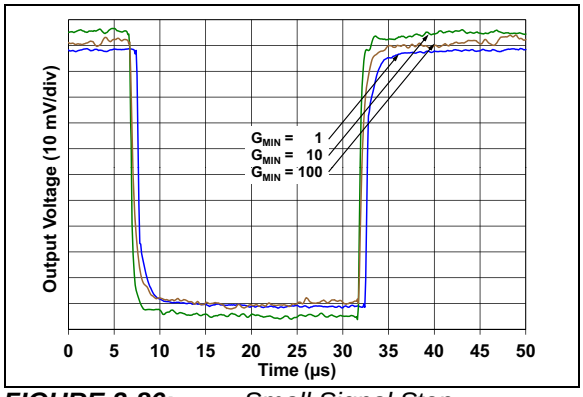


FIGURE 2-86: *Small Signal Step Response.*

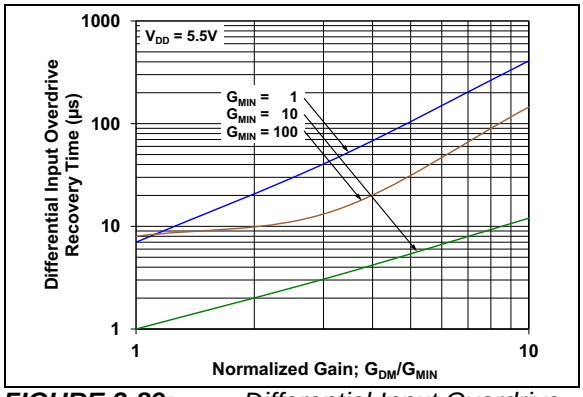


FIGURE 2-89: *Differential Input Overdrive Recovery Time vs. Normalized Gain.*

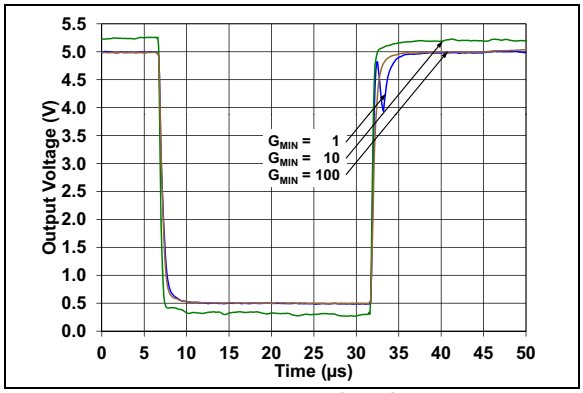


FIGURE 2-87: *Large Signal Step Response.*

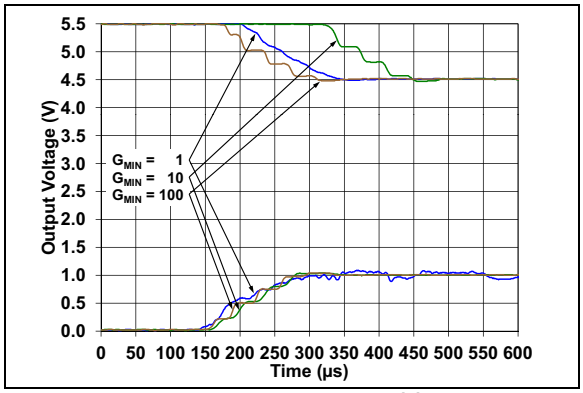


FIGURE 2-90: *Output Overdrive Recovery vs. Time.*

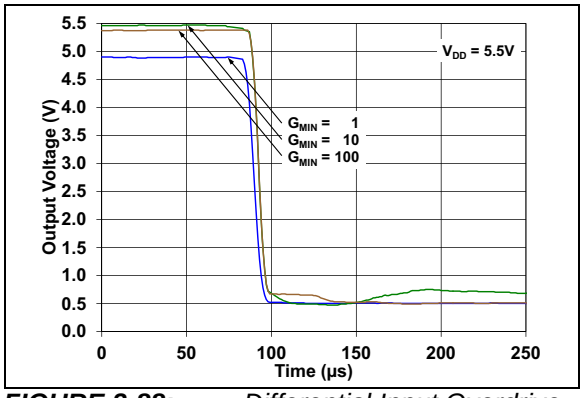


FIGURE 2-88: *Differential Input Overdrive Recovery vs. Time.*

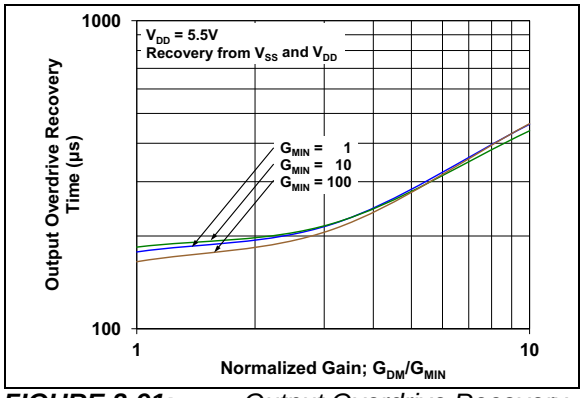


FIGURE 2-91: *Output Overdrive Recovery Time vs. Normalized Gain.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

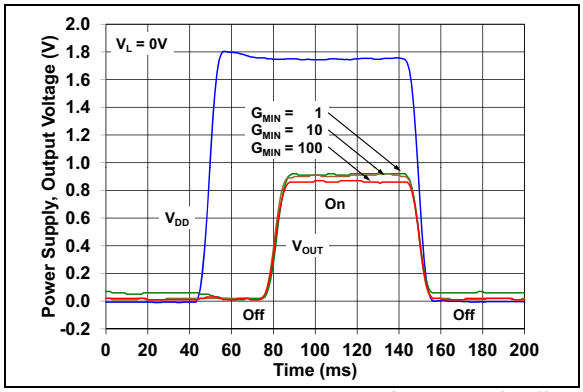


FIGURE 2-92: *Power Supply On and Off and Output Voltage vs. Time.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, C_L = 60 pF, G_{DM} = G_{MIN} and EN = V_{DD}; see Figures 1-7 and 1-8.

2.6 Enable Response

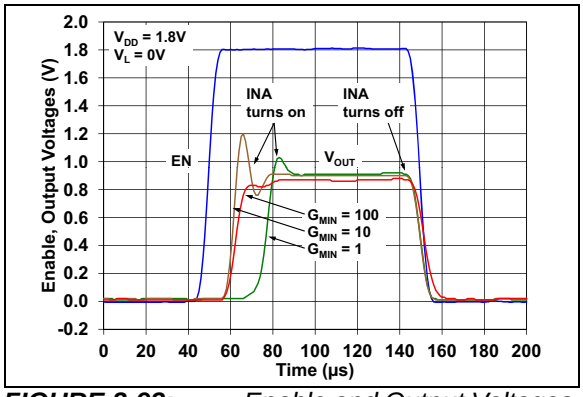


FIGURE 2-93: *Enable and Output Voltages vs. Time, with V_{DD} = 1.8V.*

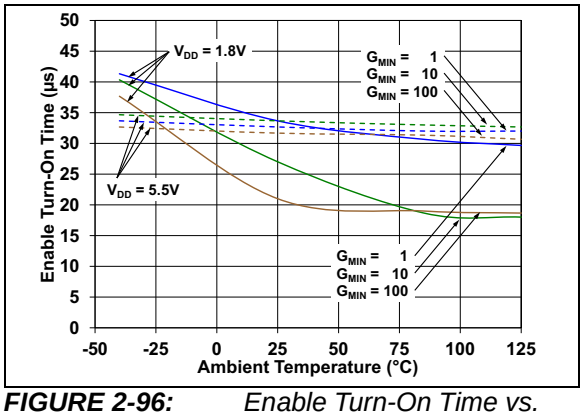


FIGURE 2-96: *Enable Turn-On Time vs. Ambient Temperature.*

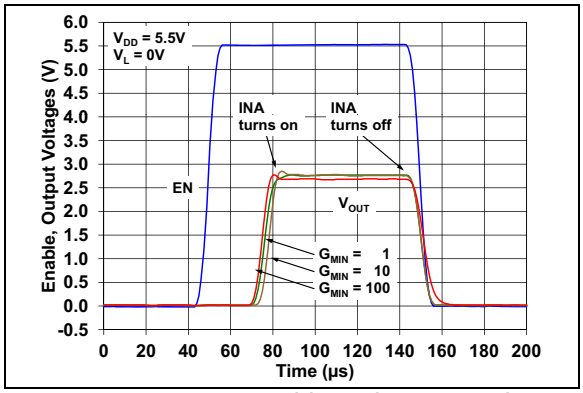


FIGURE 2-94: *Enable and Output Voltages vs. Time, with V_{DD} = 5.5V.*

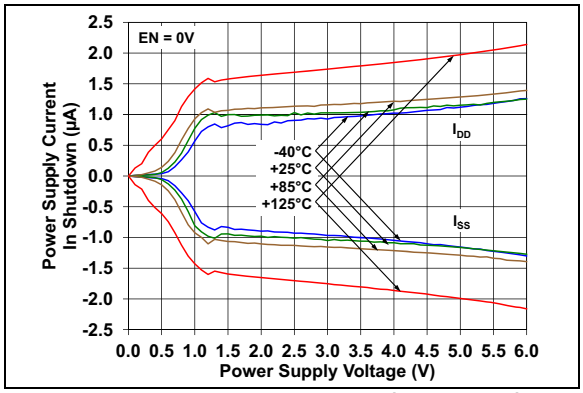


FIGURE 2-97: *Power Supply Current in Shutdown vs. Power Supply Voltage.*

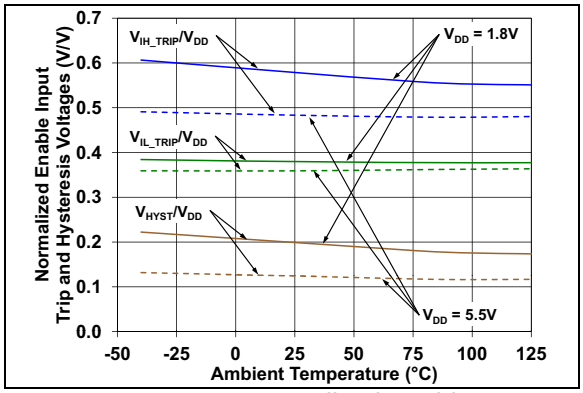


FIGURE 2-95: *Normalized Enable Input Trip and Hysteresis Voltages vs. Ambient Temperature.*

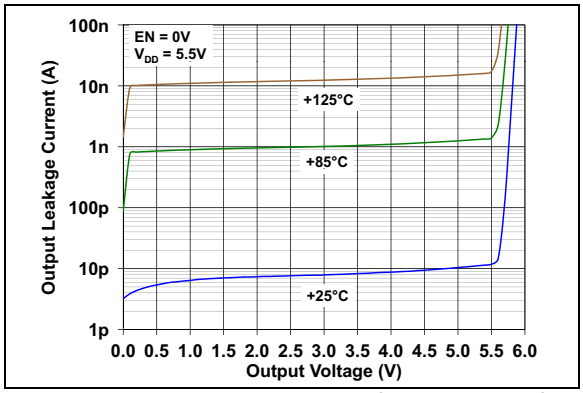


FIGURE 2-98: *Output Leakage Current in Shutdown vs. Output Voltage.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6N16		Symbol	Description
MSOP	DFN		
1	1	EN	Enable Input
2	2	V_{IM}	Inverting Input
3	3	V_{IP}	Non-inverting Input
4	4	V_{SS}	Negative Power Supply
5	5	V_{REF}	Reference Input
6	6	V_{FG}	Feedback Input
7	7	V_{OUT}	Output
8	8	V_{DD}	Positive Power Supply
—	9	EP	Exposed Thermal Pad (EP); must be connected to V_{SS}.

3.1 Digital Enable Input (EN)

This input (EN) is a CMOS, Schmitt-triggered input. When it is low, it puts the part in a low-power state. When high, the part operates normally. The EN pin must not be left floating.

3.2 Analog Signal Inputs (V_{IP}, V_{IM})

The non-inverting and inverting inputs (V_{IP} and V_{IM}) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins (V_{SS}, V_{DD})

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply; V_{DD} will need bypass capacitors.

3.4 Analog Reference Input (V_{REF})

The analog reference input (V_{REF}) is the non-inverting input of the second input stage; it shifts V_{OUT} to its desired range. The external gain resistor (R_G) is connected to this pin. It is a high-impedance CMOS input with low bias current.

3.5 Analog Feedback Input (V_{FG})

The analog feedback input (V_{FG}) is the inverting input of the second input stage. The external feedback components (R_F and R_G) are connected to this pin. It is a high-impedance CMOS input with low bias current.

3.6 Analog Output (V_{OUT})

The analog output (V_{OUT}) is a low impedance voltage output. It represents the differential input voltage ($V_{DM} = V_{IP} – V_{IM}$), with gain G_{DM} and is shifted by V_{REF}. The external feedback resistor (R_F) is connected to this pin.

3.7 Exposed Thermal Pad (EP)

There is an internal connection between the exposed thermal pad (EP) and the V_{SS} pin; they must be connected to the same potential on the printed circuit board (PCB).

This pad can be connected to a PCB ground (V_{SS}) plane region to provide a larger heat sink. This improves the package thermal resistance (θ_{JA}).

4.0 APPLICATIONS

The MCP6N16 instrumentation amplifier (INA) is manufactured using Microchip's state of the art CMOS process. Its low cost, low power and high speed make it ideal for battery-powered applications.

4.1 Basic Performance

4.1.1 STANDARD CIRCUIT

Figure 4-1 shows the standard circuit configuration for these INAs. When the inputs and output are in their specified ranges, the output voltage is approximately:

EQUATION 4-1:

$$V_{OUT} \approx V_{REF} + G_{DM}V_{DM}$$

Where:

$$G_{DM} = 1 + R_F / R_G$$

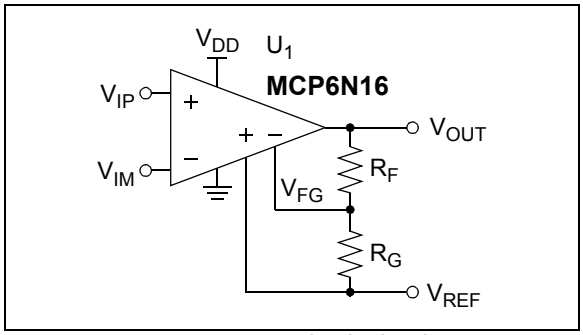


FIGURE 4-1: *Standard Circuit.*

For normal operation, keep:

- V_{IP}, V_{IM}, V_{REF} and V_{FG} between V_{IVL} and V_{IVH}
- $V_{IP} – V_{IM}$ (i.e., V_{DM}) between V_{DML} and V_{DMH}
- V_{OUT} between V_{OL} and V_{OH}

4.1.2 ANALOG ARCHITECTURE

Figure 4-2 shows the block diagram for these INAs, without details on chopper-stabilized operation.

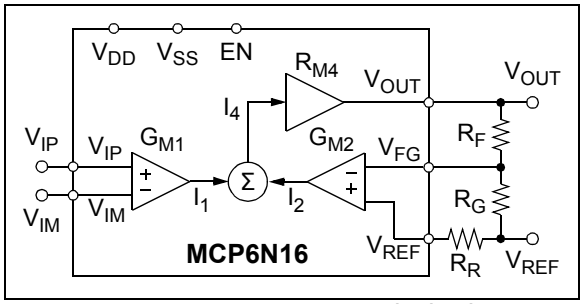


FIGURE 4-2: *MCP6N16 Block Diagram.*

The input signal is applied to G_{M1}. Equation 4-2 shows the relationships between the input voltages (V_{IP} and V_{IM}) and the common mode and differential voltages (V_{CM} and V_{DM}).

EQUATION 4-2:

$$\begin{aligned} V_{IP} &= V_{CM} + V_{DM}/2 \\ V_{IM} &= V_{CM} - V_{DM}/2 \\ V_{CM} &= (V_{IP} + V_{IM})/2 \\ V_{DM} &= V_{IP} - V_{IM} \end{aligned}$$

The negative feedback loop includes G_{M2}, R_{M4}, R_F and R_G. These blocks set the DC open-loop gain (A_{OL}) and the nominal differential gain (G_{DM}):

EQUATION 4-3:

$$\begin{aligned} A_{OL} &= G_{M2}R_{M4} \\ G_{DM} &= 1 + R_F/R_G \end{aligned}$$

A_{OL} is very high, so I_4 is very small and $I_1 + I_2 \approx 0$. This makes the differential inputs to G_{M1} and G_{M2} equal in magnitude and opposite in polarity. Ideally, this gives:

EQUATION 4-4:

$$\begin{aligned} (V_{FG} - V_{REF}) &= V_{DM} \\ V_{OUT} &= V_{DM}G_{DM} + V_{REF} \end{aligned}$$

For an ideal part, changing V_{CM}, V_{SS} or V_{DD} produces no change in V_{OUT}. V_{REF} shifts V_{OUT} as needed.

The different G_{MIN} options change G_{M1}, G_{M2} and the internal compensation capacitor. This results in the performance trade-offs shown in Table 1.

4.1.3 DC ERRORS

Section 1.5 "Explanation of DC Error Specifications" defines some of the DC error specifications. These errors are internal to the INA, and can be summarized as follows:

EQUATION 4-5:

$$\begin{aligned} V_{OUT} &= V_{REF} + G_{DM}(1 + g_E)(V_{DM} + \Delta V_{ED}) \\ &\quad + G_{DM}(1 + g_E)(V_E + \Delta V_E) \end{aligned}$$

Where:

$$V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{REF}}{CMRR2} + \frac{\Delta V_{OUT}}{A_{OL}} + \Delta T_A \cdot TC_1$$

$$|\Delta V_{ED}| \le |INL_{DM}|(V_{DMH} - V_{DML})$$

$$|\Delta V_E| \le |INL_{CM}|(V_{IVH} - V_{IVL})$$

Where:

PSRR, *CMRR*, *CMRR2* and A_{OL} are in units of V/V

ΔT_A is in units of °C

TC_1 is in units of V/°C

V_{DM} = 0

The nonlinearity specifications (INL_{CM} and INL_{DM}) describe errors that are nonlinear functions of V_{CM} and V_{DM}, respectively. They give the maximum excursion from linear response over the entire common mode and differential ranges.

The input bias current and offset current specifications (I_B and I_{OS}), together with a circuit's external input resistances, give an additional DC error. Figure 4-3 shows the resistors that set the DC bias point.

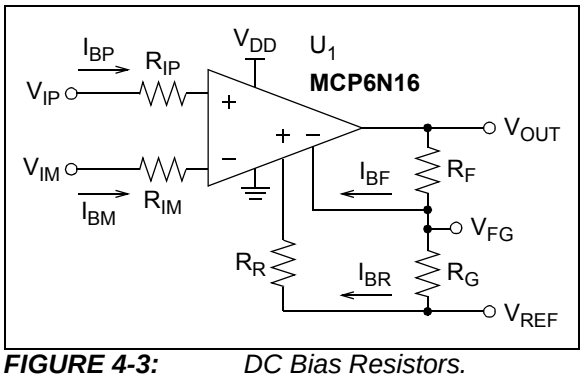


FIGURE 4-3: *DC Bias Resistors.*

The resistors at the main input (R_{IP} and R_{IM}) and its input bias currents (I_{BP} and I_{BM}) give the following changes in the INA's bias voltages:

EQUATION 4-6:

$$\begin{aligned}\Delta V_{IP} &= -I_{BP}R_{IP} = -(I_B + I_{OS}/2)R_{IP}\\ \Delta V_{IM} &= -I_{BM}R_{IM} = -(I_B - I_{OS}/2)R_{IM}\\ \Delta V_{CM} &= (\Delta V_{IP} + \Delta V_{IM})/2\\ &= -I_B(R_{IP} + R_{IM})/2 - I_{OS}(R_{IP} - R_{IM})/4\\ \Delta V_{DM} &= \Delta V_{IP} - \Delta V_{IM}\\ &= -I_B(R_{IP} - R_{IM}) - I_{OS}(R_{IP} + R_{IM})/2\\ \Delta V_{OUT} &= G_{DM}(\Delta V_{DM} + \Delta V_{CM}/CMRR)\end{aligned}$$

Where:

CMRR is in units of V/V

The change in V_{CM} (ΔV_{CM}) can affect the input range, for large R_{IP} or R_{IM}. The best design results when R_{IP} and R_{IM} are equal and small:

EQUATION 4-7:

$$\begin{aligned}\Delta V_{OUT} &\approx G_{DM}\Delta V_{DM}\\ &\approx G_{DM}(\pm 2 I_B \varepsilon_{RTOL} - I_{OS})R_{IP}\end{aligned}$$

Where:

$R_{IP} = R_{IM}$

ε_{RTOL} = tolerance of R_{IP} and R_{IM}

The resistors at the feedback input (R_R, R_F and R_G) and its input bias currents (I_{BR} and I_{BF}) give the following changes in the INA's bias voltages:

EQUATION 4-8:

$$\begin{aligned}\Delta V_{REF} &= -I_{BR}R_R = -(I_{B2} + I_{OS2}/2)R_R\\ \Delta V_{FG} &\approx \Delta V_{REF}, \quad \text{due to high } A_{OL}\\ \Delta V_{OUT} &\approx I_{B2}(R_F - G_{DM}R_R) + I_{OS2}(R_F + G_{DM}R_R)/2\end{aligned}$$

Where:

I_{B2} meets the I_B specification
I_{OS2} meets the I_{OS} specification
$I_{B2} \neq I_B$, in general
$I_{OS2} \neq I_{OS}$, in general

The change in V_{REF} (ΔV_{REF}) can affect the input range, for large R_R or R_F. The best design results when $G_{DM}R_R$ and R_F are equal (i.e., $R_R = R_F||R_G$) and small:

EQUATION 4-9:

$$\Delta V_{OUT} \approx (\pm(2 I_{B2} \varepsilon_{RTOL} + I_{OS2}))R_F$$

Where:

$G_{DM}R_R = R_F$

εR_{TOL} = tolerance of R_R, R_F and R_G

4.1.4 AC PERFORMANCE

The bandwidth of these amplifiers depends on G_{DM} and G_{MIN}:

EQUATION 4-10:

$$\begin{aligned}f_{BW} &\approx f_{GBWP}/G_{DM}\\ &\approx (0.50\ MHz)(G_{MIN}/G_{DM}), \quad G_{MIN} = 1, 10\\ &\approx (0.35\ MHz)(G_{MIN}/G_{DM}), \quad G_{MIN} = 100\end{aligned}$$

Where:

f_{BW} = -3 dB bandwidth

f_{GBWP} = Gain-Bandwidth product

The bandwidth at the maximum output swing is called the Full Power Bandwidth (f_{FPBW}). It is limited by the Slew Rate (SR) for many amplifiers, but is close to f_{BW} for these parts:

EQUATION 4-11:

$$\begin{aligned}f_{FPBW} &\approx SR/(\pi V_O)\\ &\approx f_{BW}, \quad \text{for these parts}\end{aligned}$$

Where:

V_O = Maximum output voltage swing
$\approx V_{OH} - V_{OL}$

4.1.5 NOISE PERFORMANCE

As shown in Figure 2-73, the noise density is white at low frequencies; the 1/f noise is negligible for almost all applications. As a result, the time domain data in Figures 2-77, 2-78 and 2-79 is well behaved.

4.2 Overview of Zero-Drift Operation

Figure 4-4 shows a simplified diagram of the MCP6N16 zero-drift INAs. This diagram will be used to explain how low voltage errors are reduced in this architecture (much better V_{OS}, TC_1 ($\Delta V_{OS}/\Delta T_A$), CMRR, CMRR2, PSRR, A_{OL} and 1/f noise).

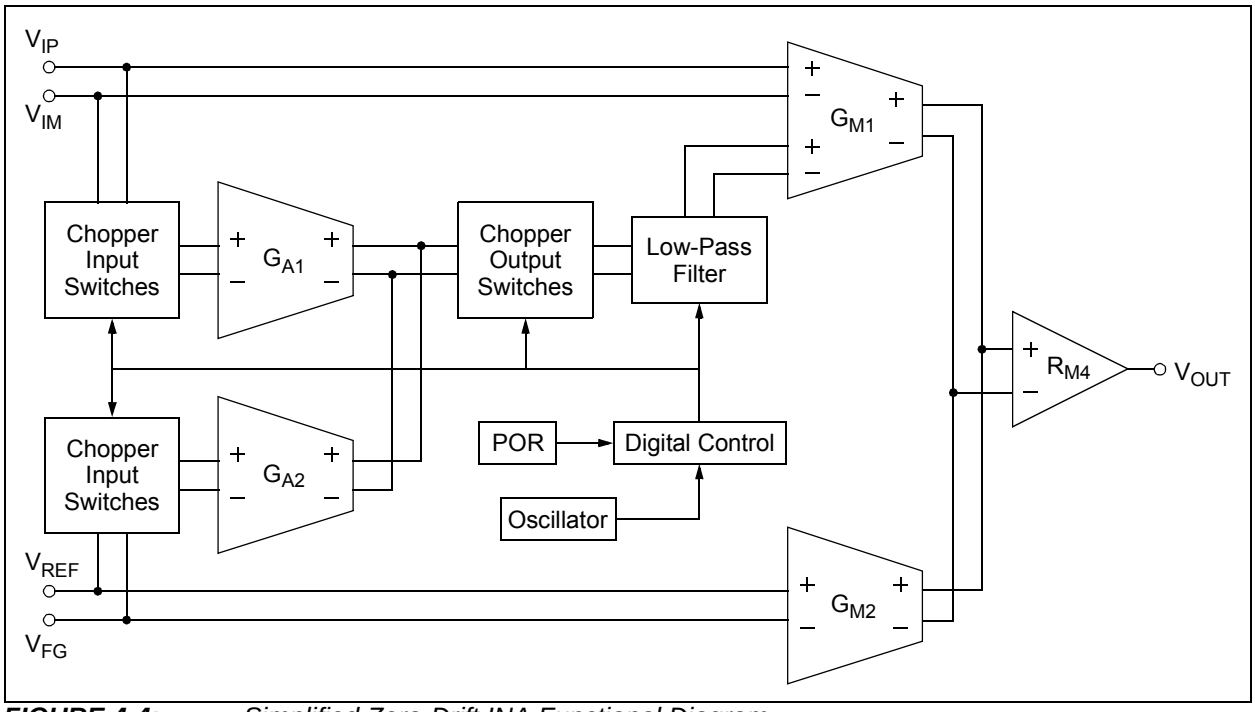


FIGURE 4-4: *Simplified Zero-Drift INA Functional Diagram.*

4.2.1 BUILDING BLOCKS

The Main Amplifiers (G_{M1} and G_{M2}) are designed for high gain and bandwidth, with a differential topology. The main input pairs (+ and - pins at the top left) are for the higher frequency portion of the input signal. The auxiliary input pair (+ and - pins at the bottom left of G_{M1}) is for the low frequency portion of the input signal and corrects the INA's input offset voltage. Both inputs are added together internally.

The Auxiliary Amplifiers (G_{A1} and G_{A2}), the Chopper Input Switches and the Chopper Output Switches provide a high DC gain to the input signal. DC errors are modulated to higher frequencies and white noise to low frequencies.

The Low-Pass Filter reduces high-frequency content, including harmonics of the Chopping Clock.

The Output Buffer (R_{M4}) converts current to voltage and drives external loads at the V_{OUT} pin.

The Oscillator runs at f_{CLK} = 200 kHz. Its output is divided by 8, to produce the Chopping Clock rate of f_{CHOP} = 25 kHz.

The internal POR part starts the part in a known good state, protecting against power supply brown-outs. The Digital Control block outputs clocks and POR events.

4.2.2 CHOPPING ACTION

Figure 4-5 shows the amplifier connections for the first phase of the Chopping Clock and Figure 4-6 shows them for the second phase. The slow voltage errors alternate in polarity, making the average error small.

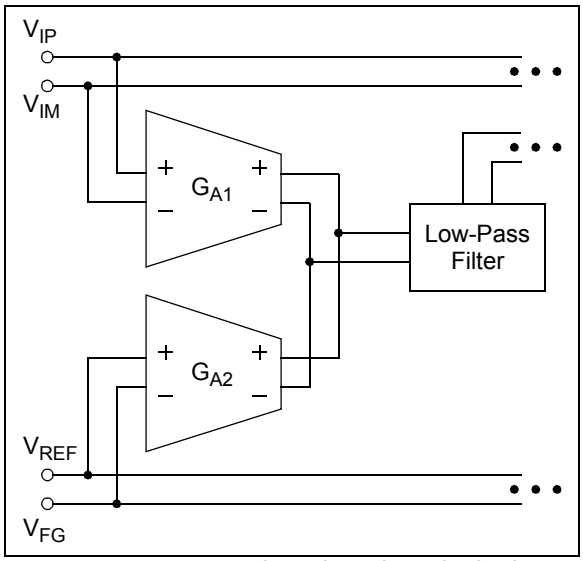


FIGURE 4-5: *First Chopping Clock Phase; Simplified Diagram.*

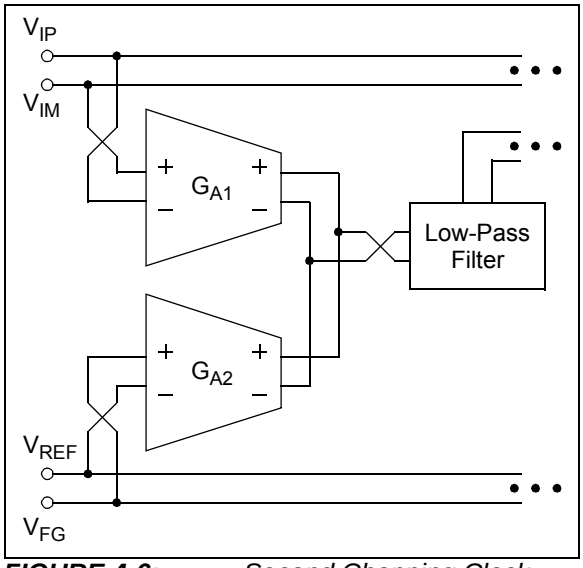


FIGURE 4-6: *Second Chopping Clock Phase; Simplified Diagram.*

4.2.3 INTERMODULATION DISTORTION (IMD)

These INAs will show intermodulation distortion (IMD) products when an AC signal is present.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the zero-drift circuitry's nonlinear response to produce IMD tones at sum and difference frequencies. Each of the square wave clock's harmonics has a series of IMD tones centered on it. See Figures 2-75 and 2-76.

4.3 Other Functional Blocks

4.3.1 RAIL-TO-RAIL INPUTS

Each input stage uses one PMOS differential pair at the input. The output of each differential pair is processed using current mode circuitry. The inputs show no crossover distortion vs. common mode voltage.

With this topology, the inputs (V_{IP} and V_{IM}) operate normally down to V_{SS} – 0.15V and up to V_{DD} + 0.15V at room temperature (see Figure 2-52). The input offset voltage (V_{OS}) is measured at V_{CM} = V_{SS} – 0.15V and V_{DD} + 0.15V (at +25°C) to ensure proper operation.

4.3.1.1 Phase Reversal

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-82 shows an input voltage exceeding both supplies with no phase inversion.

The input devices also do not exhibit phase inversion when the differential input voltage exceeds its limits; see Figure 2-83.

4.3.1.2 Input Voltage Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). This requirement is independent of the current limits discussed later on.

The ESD protection on the inputs can be depicted as shown in Figure 4-7. This structure was chosen to protect the input transistors against many (but not all) overvoltage conditions, and to minimize input bias current (I_B).

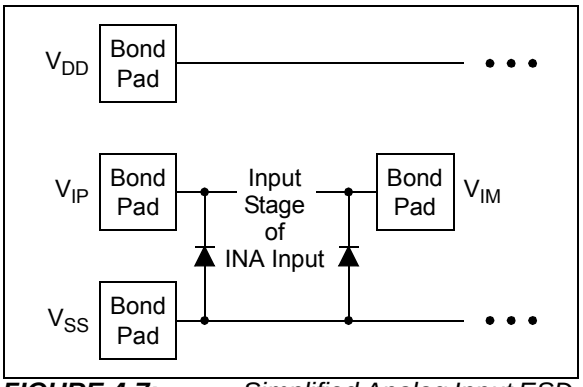


FIGURE 4-7: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow over-voltage (beyond V_{DD}) events. Very fast ESD events (that meet the specification) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the INA inputs. Figure 4-8 shows one approach to protecting these inputs. D_1 and D_2 may be small signal silicon diodes, Schottky diodes for lower clamping voltages or diode-connected FETs for low leakage.

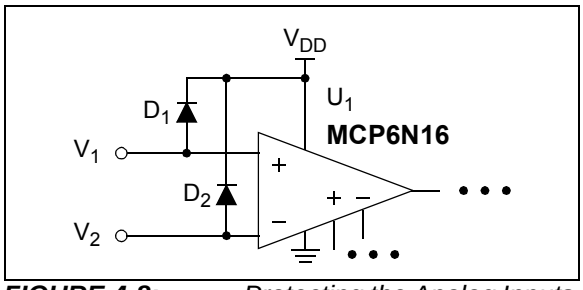
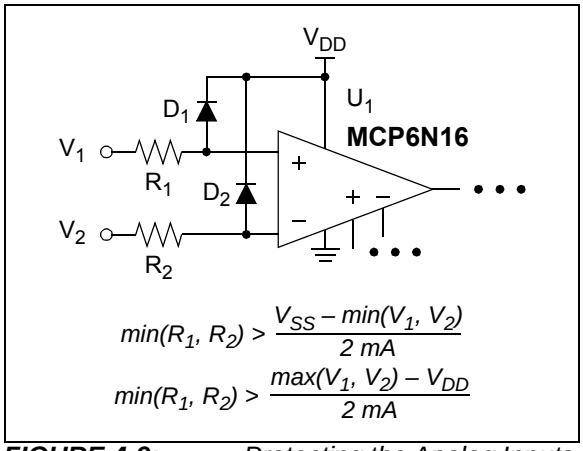


FIGURE 4-8: *Protecting the Analog Inputs Against High Voltages.*

4.3.1.3 Input Current Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see **Section 1.1 "Absolute Maximum Ratings †"**). This requirement is independent of the voltage limits previously discussed.

Figure 4-9 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible current in or out of the input pins (and into D_1 and D_2). The diode currents will dump onto V_{DD}.



$$min(R_1, R_2) > \frac{V_{SS} - min(V_1, V_2)}{2\ mA}$$

$$min(R_1, R_2) > \frac{max(V_1, V_2) - V_{DD}}{2\ mA}$$

FIGURE 4-9: *Protecting the Analog Inputs Against High Currents.*

It is also possible to connect the diodes to the left of the resistor R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IP} and V_{IM}) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-47.

4.3.1.4 Input Voltage Ranges

Figure 4-10 shows possible input voltage values (V_{SS} = 0V). Lines with a slope of +1 have constant V_{DM} (e.g., the V_{DM} = 0 line). Lines with a slope of -1 have constant V_{CM} (e.g., the $V_{CM} = V_{DD}/2$ line).

For normal operation, V_{IP} and V_{IM} must be kept within the region surrounded by the thick blue lines. The horizontal and vertical blue lines show the limits on the individual inputs. The blue lines with a slope of +1 show the limits on V_{DM}; the larger G_{MIN} is, the closer they are to the V_{DM} = 0 line.

The input voltage range specifications (V_{IVL} and V_{IVH}) change with the supply voltages (V_{SS} and V_{DD}, respectively). The differential input range specifications (V_{DML} and V_{DMH}) change with minimum gain (G_{MIN}). Temperature also affects these specifications.

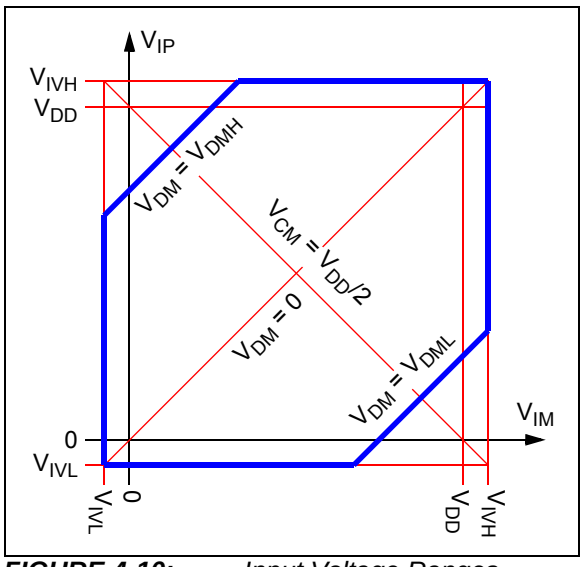


FIGURE 4-10: *Input Voltage Ranges.*

To take full advantage of V_{DML} and V_{DMH}, set V_{REF} (see Figures 1-7 and 1-8) so that the output (V_{OUT}) is centered between the supplies (V_{SS} and V_{DD}). Also set the gain (G_{DM}) to keep V_{OUT} within its range.

4.3.2 ENABLE

This input (EN) is a CMOS, Schmitt-triggered input. When it is low, it puts the part in a low-power state and the output is put into a high-impedance state. When high, the part operates normally.

If the EN pin is left floating, the amplifier will not operate properly.

4.3.3 RAIL-TO-RAIL OUTPUT

The Minimum Output Voltage (V_{OL}) and Maximum Output Voltage (V_{OH}) specifications describe the widest output swing that can be achieved under the specified load conditions.

The output can also be limited when V_{IP} or V_{IM} exceeds V_{IVL} or V_{IVH} or when V_{DM} exceeds V_{DML} or V_{DMH}.

4.4 Applications Tips

4.4.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE

Table 1 gives both the linear and quadratic temperature coefficients (TC_1 and TC_2) of input offset voltage. The input offset voltage can be estimated as follows:

EQUATION 4-12:

$$V_{OS}(T_A) = V_{OS} + TC_1\Delta T + TC_2\Delta T^2$$

Where:

T_A = -40°C to +125°C

ΔT = T_A – 25°C

$V_{OS}(T_A)$ = Input offset voltage at T_A

V_{OS} = Input offset voltage at +25°C

TC_1 = Linear temperature coefficient

TC_2 = Quadratic temperature coefficient

These specifications show these INA's intrinsic performance. The plots of input offset voltage versus temperature on the second page (Figures 1 to 3) show the typical behavior for a few parts from the first wafer lot.

In most designs, other effects will dominate the circuit temperature performance; see **Section 4.4.13 "PCB Design for DC Precision"** for more details.

4.4.2 NOISE EFFECT ON OFFSET VOLTAGE

The input noise (e_{ni}) makes measured offset values (V_{OS}) vary in a random manner. Lower noise requires a lower noise power bandwidth (NPBW; see AN1228, mentioned in **5.3 "Application Notes"**), which increases measurement time. In the offset-related specifications (A_{OL}, CMRR, CMRR2 and PSRR) and plots, the various values of NPBW were chosen to trade off time versus accuracy of results.

4.4.3 DC GAIN PLOTS

Figures 2-28 to 2-39 are histograms of the reciprocals (in units of µV/V) of CMRR, PSRR and A_{OL}, respectively. They represent the change in input offset voltage (V_{OS}) with a change in common mode input voltage (V_{CM}), power supply voltage (V_{DD}) and output voltage (V_{OUT}).

The $1/A_{OL}$ histogram is centered near 0 µV/V because the measurements are dominated by the INA's input noise. The negative values shown represent noise and tester limitations, *not* unstable behavior. Production tests make multiple V_{OS} measurements, which validates an INA's stability; an unstable part would show greater V_{OS} variability, or the output would stick at one of the supply rails.

4.4.4 OFFSET AT POWER-UP

When these parts power up, the input offset (V_{OS}) starts at its uncorrected value (usually less than ±10 mV). Circuits with high DC gain can cause the output to reach one of the two rails. In this case, the time to a valid output is delayed by an output overdrive time (like t_{ODR}), in addition to a start-up time (like t_{STR}).

It can be simple to avoid this extra start-up time. Reducing the gain is one method. Adding a capacitor across the feedback resistor (R_F) is another method.

4.4.5 SOURCE RESISTANCES

The input bias currents have two significant components: switching glitches that dominate at room temperature and below, and input ESD diode leakage currents that dominate at +85°C and above.

Make the resistances seen by the inputs small and equal. This minimizes the output offset caused by the input bias currents.

The inputs should see a resistance on the order of 10Ω to 1 kΩ at high frequencies (i.e., above 1 MHz). This helps minimize the impact of switching glitches, which are very fast, on overall performance. In some cases, it may be necessary to add resistors in series with the inputs to achieve this improvement in performance.

Small input resistances at the inputs may be needed for high gains. Without them, parasitic capacitances might cause positive feedback and instability.

4.4.6 SOURCE CAPACITANCE

The capacitances seen by the inputs should be small. Large input capacitances and source resistances, together with high gain, can lead to positive feedback and instability.

4.4.7 MINIMUM STABLE GAIN

There are three options for different Minimum Stable Gains (1, 10 and 100 V/V; see Table 1). The differential gain (G_{DM}) needs to be greater than or equal to G_{MIN} in order to maintain stability.

Picking a part with higher G_{MIN} has the advantages of lower input noise voltage density (e_{ni}), lower input offset voltage (V_{OS}) and increased gain-bandwidth product (GBWP). The differential input voltage range (V_{DML} and V_{DMH}) is lower for higher G_{MIN}, but supports a reasonable output voltage range.

4.4.8 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage amplifiers. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth reduces. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. Lower gains (G_{DM}) exhibit greater sensitivity to capacitive loads.

When driving large capacitive loads with these instrumentation amps (e.g., > 80 pF), a small series resistor at the output (R_{ISO} in Figure 4-11) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

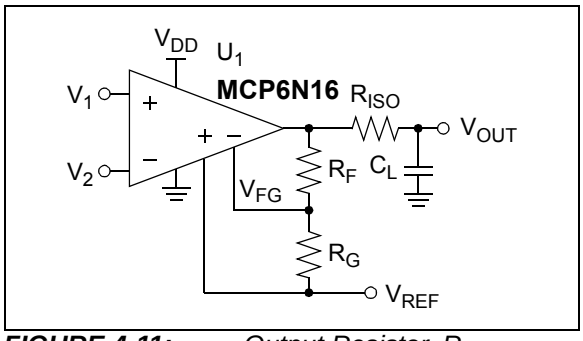


FIGURE 4-11: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-12 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L G_{MIN}/G_{DM}), where G_{DM} is the circuit's differential gain ($1 + R_F/R_G$) and G_{MIN} is the minimum stable gain.

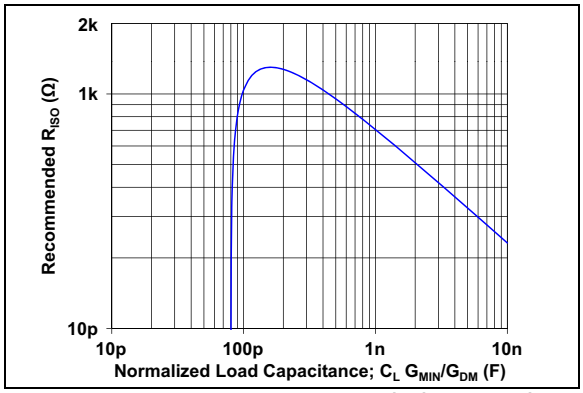


FIGURE 4-12: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for the circuit, double check the resulting frequency response peaking and step response overshoot on the bench. Modify R_{ISO}'s value until the response is reasonable.

4.4.9 GAIN RESISTORS

Figure 4-13 shows a simple gain circuit with the INA's input capacitances at the feedback inputs (V_{REF} and V_{FG}). These capacitances interact with R_G and R_F to modify the gain at high frequencies. The equivalent capacitance acting in parallel to R_G is $C_G = C_{DM} + C_{CM}$ plus any board capacitance in parallel to R_G. C_G will cause an increase in G_{DM} at high frequencies, which reduces the phase margin of the feedback loop (i.e., reduce the feedback loop's stability).

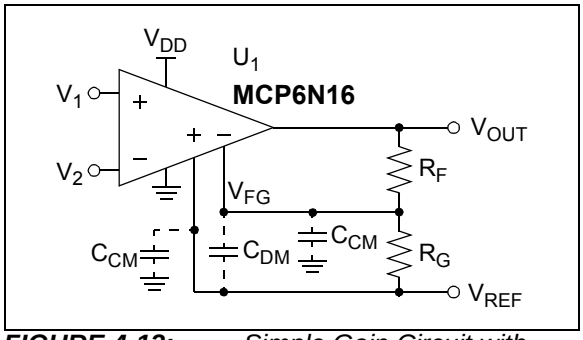


FIGURE 4-13: *Simple Gain Circuit with Parasitic Capacitances.*

In this data sheet, $R_F + R_G = 10\ k\Omega$ for most gains (0Ω for $G_{DM} = 1$); see Table 1-6. This choice gives good phase margin. In general, R_F (Figure 4-13) needs to meet the following limits to maintain stability:

EQUATION 4-13:

For $G_{DM} = 1$:

$$R_F = 0$$

For $G_{DM} > 1$:

$$R_F < \frac{\alpha G_{DM}^2}{2\pi f_{GBWP} C_G}$$

Where:

$\alpha \leq 0.25$

$G_{DM} \geq G_{MIN}$

f_{GBWP} = Gain-Bandwidth Product

$C_G = C_{DM} + C_{CM} + (PCB\ stray\ capacitance)$

4.4.10 EMI REJECTION RATIO (EMIRR)

Electromagnetic interference (EMI) can be coupled to an INA through electromagnetic induction or radiation, or by conduction. INAs are most sensitive to EMI at their input pins.

EMIRR describes an INA's EMI robustness. Internal passive filters in these parts improve the EMIRR, when good PCB layout techniques are used. EMIRR is defined to be:

EQUATION 4-14:

$$EMIRR(dB) = 20 \bullet log\left(\frac{V_{RF}}{\Delta V_{OS}}\right)$$

Where:

V_{RF} = Peak Input Voltage of EMI (V_{PK})

ΔV_{OS} = Input Offset Voltage Shift (V)

4.4.11 REDUCING UNDESIRED NOISE AND SIGNALS

Reduce undesired noise and signals with:

- Low bandwidth signal filters:
  - Minimizes random analog noise
  - Reduces interfering signals
- Good PCB layout techniques:
  - Minimizes crosstalk
  - Minimizes parasitic capacitances and inductances that interact with fast switching edges
- Good power supply design:
  - Isolation from other parts
  - Filtering of interference on supply line(s)

4.4.12 SUPPLY BYPASS

With these INAs, the Power Supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. Surface mount, multilayer ceramic capacitors, or their equivalent, should be used.

These INAs require a bulk capacitor (i.e., 1.0 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other nearby analog parts as long as crosstalk through the supplies does not prove to be a problem.

4.4.13 PCB DESIGN FOR DC PRECISION

In order to achieve DC precision on the order of ±1 µV, many physical errors need to be minimized. The design of the printed circuit board (PCB), the wiring, and the thermal environment have a strong impact on the precision achieved. A poor PCB design can easily be more than 100 times worse than the MCP6N16 op amps' minimum and maximum specifications.

4.4.13.1 PCB Layout

Any time two dissimilar metals are joined together, a temperature dependent voltage appears across the junction (the Seebeck or thermojunction effect). This effect is used in thermocouples to measure temperature. The following are examples of thermojunctions on a PCB:

- Components (resistors, INAs, …) soldered to a copper pad
- Wires mechanically attached to the PCB
- Jumpers
- Solder joints
- PCB vias

Typical thermojunctions have temperature to voltage conversion coefficients of 1 to 100 µV/°C (sometimes higher).

Microchip's AN1258 ("*Op Amp Precision Design: PCB Layout Techniques*" – DS01258) contains in-depth information on PCB layout techniques that minimize thermojunction effects. It also discusses other effects, such as crosstalk, impedances, mechanical stresses and humidity.

4.4.13.2 Crosstalk

DC crosstalk causes offsets that appear as a larger input offset voltage. Common causes include:

- Common mode noise (remote sensors)
- Ground loops (current return paths)
- Power supply coupling

Interference from the mains (usually 50 Hz or 60 Hz), and other AC sources, can also affect the DC performance. Nonlinear distortion can convert these signals to multiple tones, including a DC shift in voltage.

When the signal is sampled by an ADC, these AC signals can also be aliased to DC, causing an apparent shift in offset.

To reduce interference:

- Keep traces and wires as short as possible
- Use shielding
- Use ground plane (at least a star ground)
- Place the input signal source near to the DUT
- Use good PCB layout techniques
- Use a separate power supply filter (bypass capacitors) for these zero-drift INAs

4.4.13.3 Miscellaneous Effects

Keep the resistances seen by the input pins as small and as near to equal as possible, to minimize bias current-related offsets.

Make the (trace) capacitances seen by the input pins small and equal. This is helpful in minimizing switching glitch-induced offset voltages.

Bending a coax cable with a radius that is too small causes a small voltage drop to appear on the center conductor (the triboelectric effect). Make sure the bending radius is large enough to keep the conductors and insulation in full contact.

Mechanical stresses can make some capacitor types (such as some ceramics) output small voltages. Use more appropriate capacitor types in the signal path and minimize mechanical stresses and vibration.

Humidity can cause electrochemical potential voltages to appear in a circuit. Proper PCB cleaning helps, as does the use of encapsulants.

4.5 Typical Applications

4.5.1 HIGH INPUT IMPEDANCE DIFFERENCE AMPLIFIER

Figure 4-14 shows the MCP6N16 used as a difference amplifier. The inputs are high-impedance and give good CMRR performance.

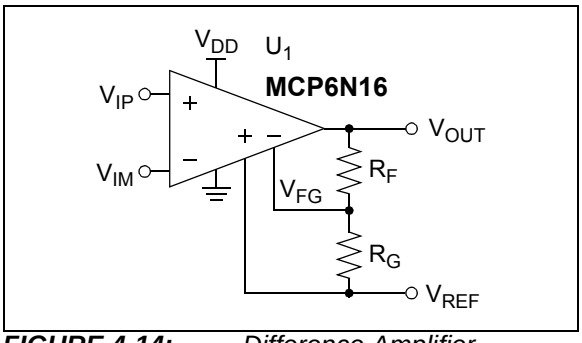


FIGURE 4-14: *Difference Amplifier.*

4.5.2 DIFFERENCE AMPLIFIER FOR VERY LARGE COMMON MODE SIGNALS

Figure 4-15 uses the MCP6N16 INA as a difference amplifier for signals with a very large common mode component. The input resistor dividers (R_1 and R_2) ensure that the INA's inputs are within their normal range of operation. The capacitors (C_1 and C_2) set the same voltage division ratio for high-frequency signals (e.g., a voltage step). C_2 includes the INA's C_{CM}. R_1 and R_2's tolerances affect CMRR.

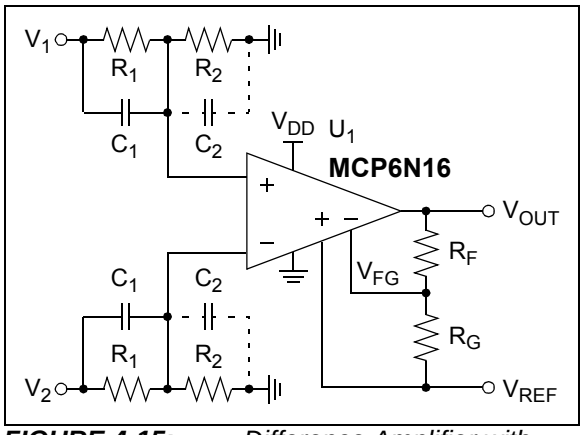


FIGURE 4-15: *Difference Amplifier with Very Large Common Mode Component.*

4.5.3 RTD TEMPERATURE SENSOR

Figure 4-16 shows an RTD temperature sensor circuit, which measures over the -55°C to +155°C range. The sensor chosen changes from 78Ω to 159Ω over this range. The 2.49 kΩ and 4.99 kΩ resistors set the current through the RTD and 68.1Ω resistor. The INA provides a high-differential gain. The 10 µF capacitor filters common mode interference on the bridge.

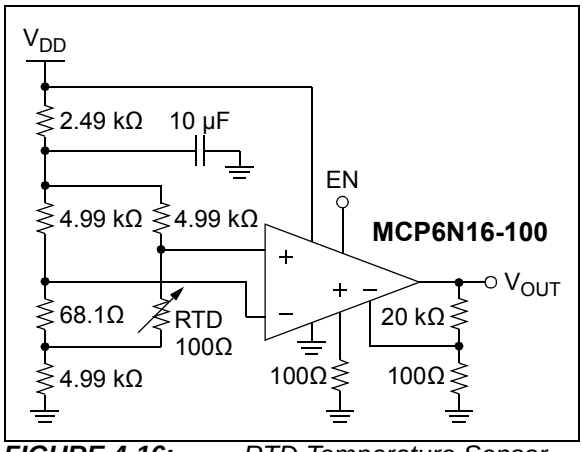


FIGURE 4-16: *RTD Temperature Sensor.*

4.5.4 WHEATSTONE BRIDGE

Figure 4-17 shows the MCP6N16 INA used to condition the signal from a Wheatstone bridge (e.g., strain gage). The overall INA gain is set at 1001 V/V. The best G_{MIN} option to pick, for this gain, is 100 V/V (MCP6N16-100).

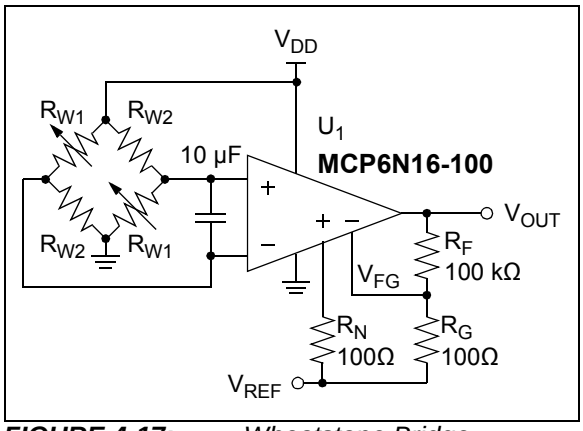


FIGURE 4-17: *Wheatstone Bridge Amplifier.*

4.5.5 HIGH SIDE CURRENT DETECTOR

Figure 4-18 shows the MCP6N16 INA used to detect and amplify the high side current in a power supply design. U_1's low offset voltage makes it possible to reduce R_{SH}, which saves power and minimizes temperature effects. U_1's supply current is included in the measurement. The INA's gain is set at 101 V/V, so V_{OUT} changes 1.01V for every 1A change in I_{DD}.

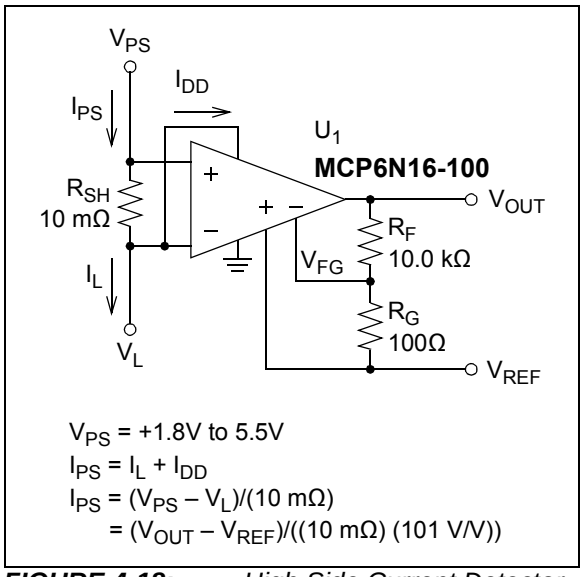


FIGURE 4-18: *High Side Current Detector.*

5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6N16 instrumentation amplifiers.

5.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase and Sampling of Microchip parts.

5.2 Analog Demonstration Board

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analog tools.

5.3 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- **AN884:** *"Driving Capacitive Loads With Op Amps"*, DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview"*, DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors"*, DS01177
- **AN1228:** *"Op Amp Precision Design: Random Noise"*, DS01228
- **AN1258:** *"Op Amp Precision Design: PCB Layout Techniques"*, DS01258

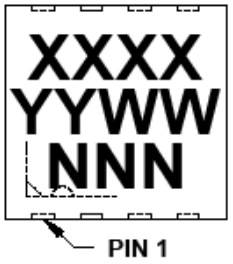
Some of these application notes, and others, are listed in the design guide:

- *"Signal Chain Design Guide"*, DS21825

6.0 PACKAGING INFORMATION

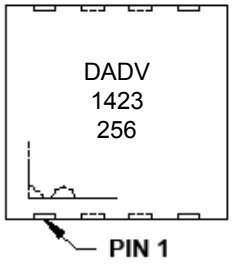
6.1 Package Marking Information

8-Lead DFN (3x3 mm)

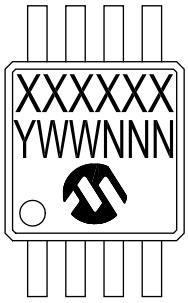


Product Number	Code
MCP6N16-001E/MF	DADV
MCP6N16T-001E/MF	DADV
MCP6N16-010E/MF	DADW
MCP6N16T-010E/MF	DADW
MCP6N16-100E/MF	DADX
MCP6N16T-100E/MF	DADX

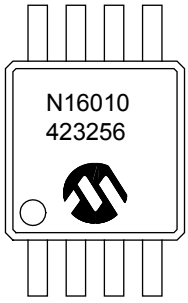
Example



8-Lead MSOP (3x3 mm)



Example

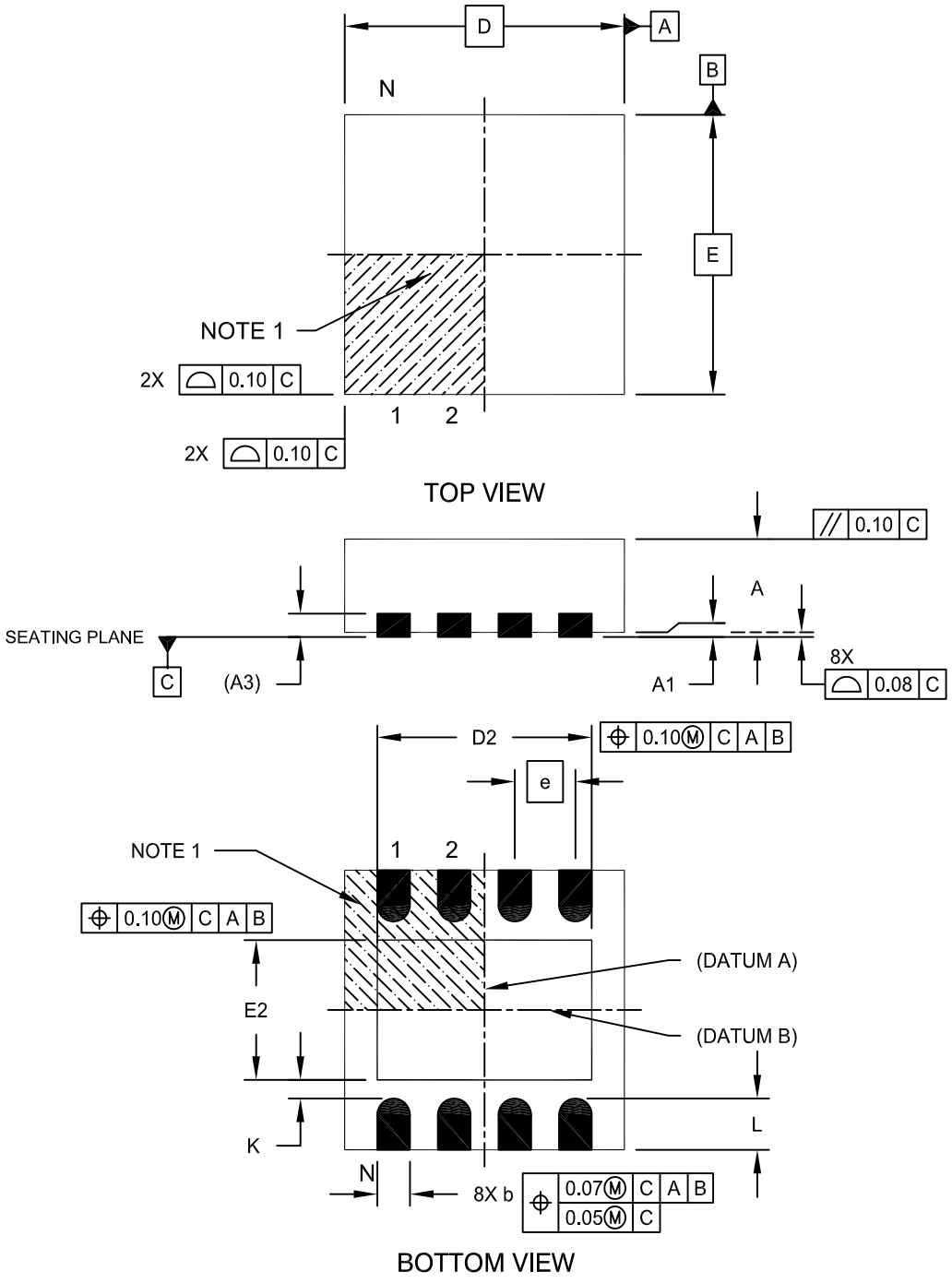


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

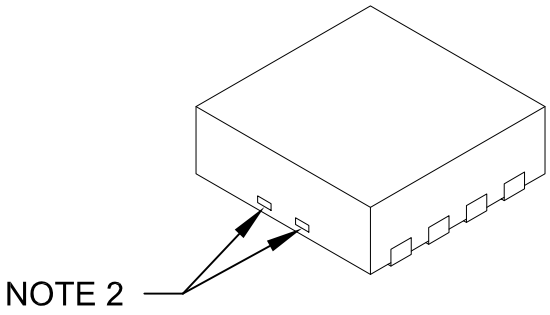
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-062C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.34	-	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.60	-	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

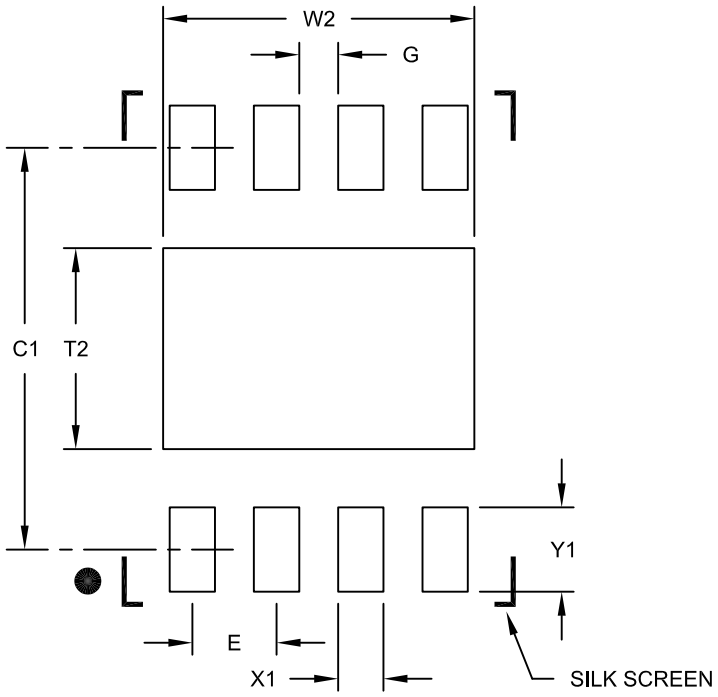
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

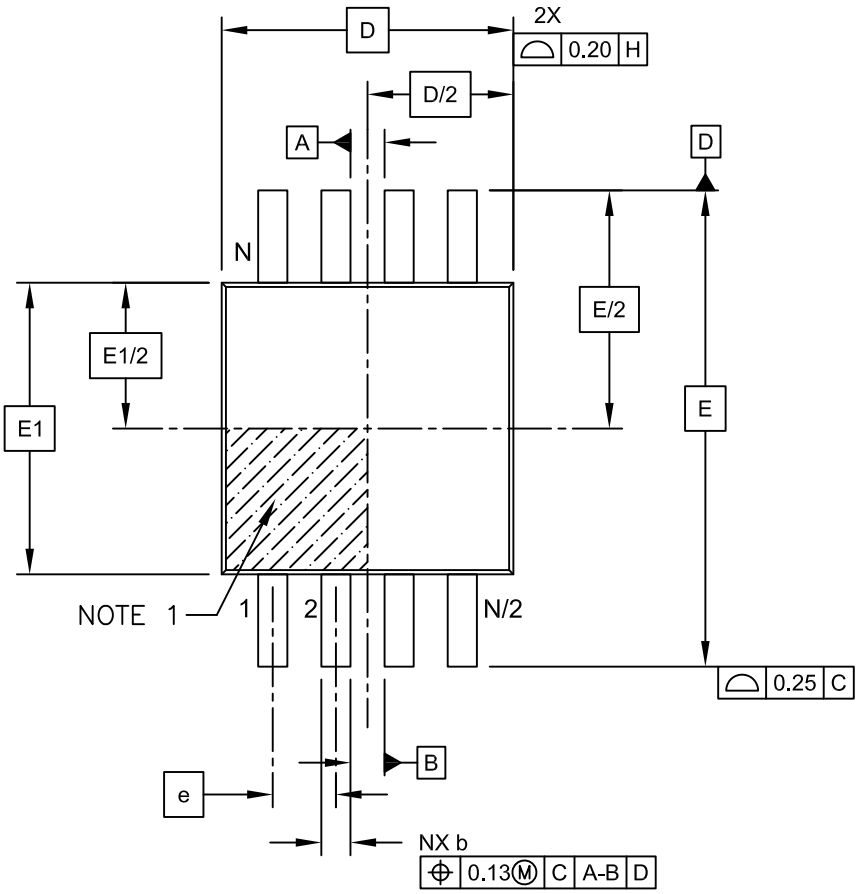
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

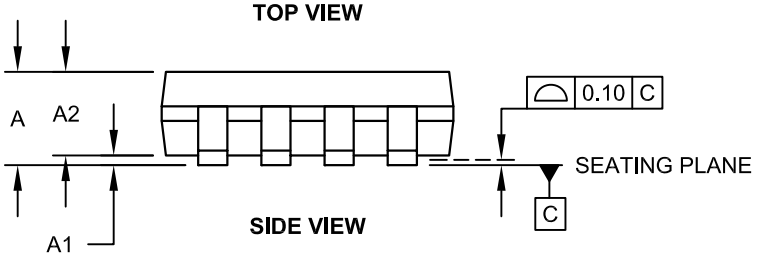
Microchip Technology Drawing No. C04-2062B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

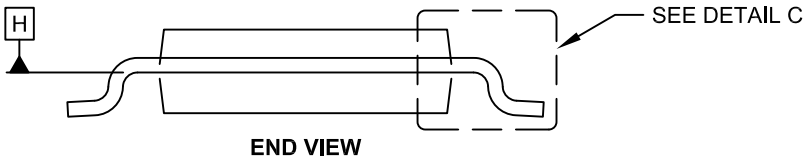
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

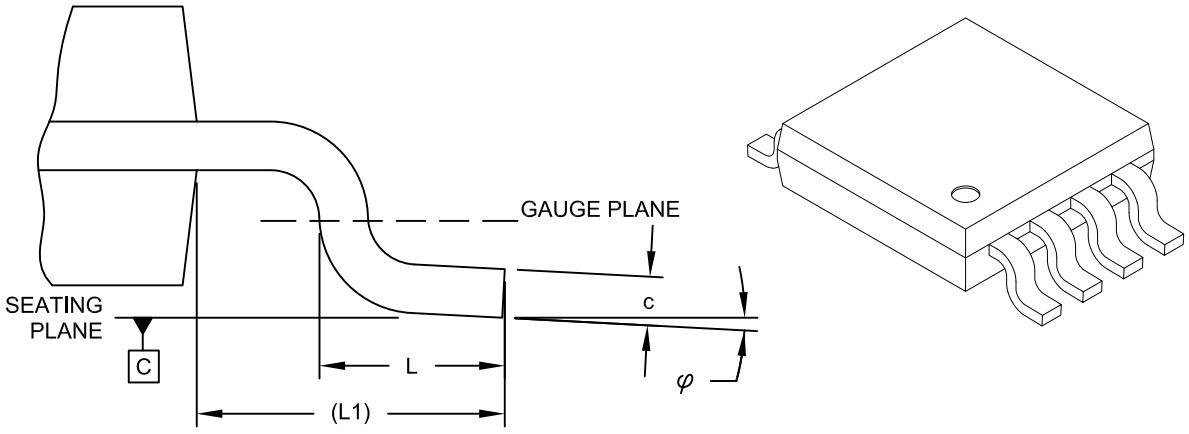


END VIEW

Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

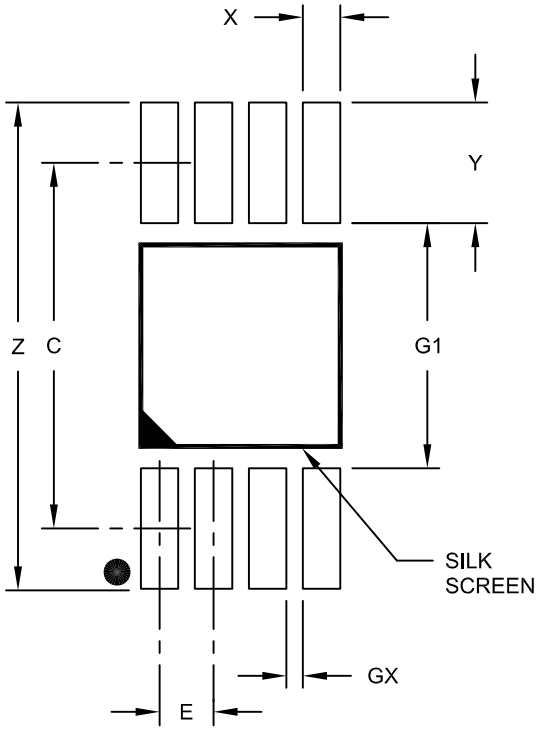
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

APPENDIX A: REVISION HISTORY

Revision A (July 2014)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-XXX	X	/XX
Device	Tape and Reel Option	Gain Option	Temperature Range	Package

Device:	MCP6N16	Single Instrumentation Amplifier
	MCP6N16T	Single Instrumentation Amplifier (Tape and Reel)
Gain Option:	001 =	Minimum gain of 1 V/V
	010 =	Minimum gain of 10 V/V
	100 =	Minimum gain of 100 V/V
Temperature Range:	E =	-40°C to +125°C
Package:	MF =	Plastic Dual Flat, no lead Package - 3×3x0.9 mm Body, 8-lead (DFN)
	MS =	Plastic Micro Small Outline Package, 8-lead (MSOP)

Examples:

a) MCP6N16T-001E/MF: Tape and Reel, Minimum gain = 1, Extended temperature, 8LD 3×3 DFN

b) MCP6N16-010E/MS: Minimum gain = 10, Extended temperature, 8LD MSOP

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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