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	MOBILE LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION **SPECIFICATION**	MOBILE LIQUID CRYSTAL DISPLAY DIVISION II

DEVICE SPECIFICATION FOR

Control IC of TFT-LCD

Type No. LQ0DZC2291

CUSTOMER'S APPROVAL

DATE

BY

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RECORDS OF REVISION

Type No : LQ0DZC2291

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LCY-09033A	2009. 06.05		-	-	1st Issue
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Note: In this ASIC Specification, binary notation, decimal notation and hexadecimal notation are described according to the rules below.

Binary notation: Double quotation marks are used, e.g., “111000” or “1001”. Otherwise, ‘b’ is appended, e.g., 111000b.

Hexadecimal notation: ‘0x’ is used, e.g., 0x3F or 0x2D. Otherwise, ‘H’ is appended, e.g., 20H or 1000H.

Decimal notation: Unless binary notation and hexadecimal notation are used, decimal notation is used.

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1. Overview and Features of Product

1.1. Product Overview

This product is a timing controller for liquid crystal module to display four kinds of resolutions, i.e., WVGA (800RGB[H] × 480[V], WQVGA (400RGB[H] × 240[V]), WEGA1 (480RGB[H] × 272[V]) and WEGA2 (480RGB[H] × 240[V]). Moreover, RGB independent gamma can be controlled by adding external EEPROM. This controller has an auto-loading function. After resetting, the controller reads the register set values/independent gamma parameters from the external EEPROM and works according to the set values.

1.2. Main Features

a) Timing controller (for WVGA, WQVGA, WEGA1 and WEGA2) contained
b) ROMOFF setting (It can be specified whether external EEPROM should be disabled or enabled.)
c) HSY/VSY input monitoring function. (“Free Run” is shown when HSY/VSY has not yet been input and when an error has been occurred in input.)
d) Free Run Display (Blue background screen 1H = 1200 clk or more/1V = 700 Lines or more）
e) Horizontal/vertical reverse display available.
f) Independent gamma setting (supported only for ROMOFF = 0)
g) External D/A Converter 8ch control output supported (only for ROMOFF = 0)
h) External A/D Converter 2ch control output supported (only for ROMOFF = 0)
i) Internal register control with I2C (only for ROMOFF = 0)

1.3. Block diagram

Figure 1-1 shows a simplified block diagram of LQ0DZC2291.

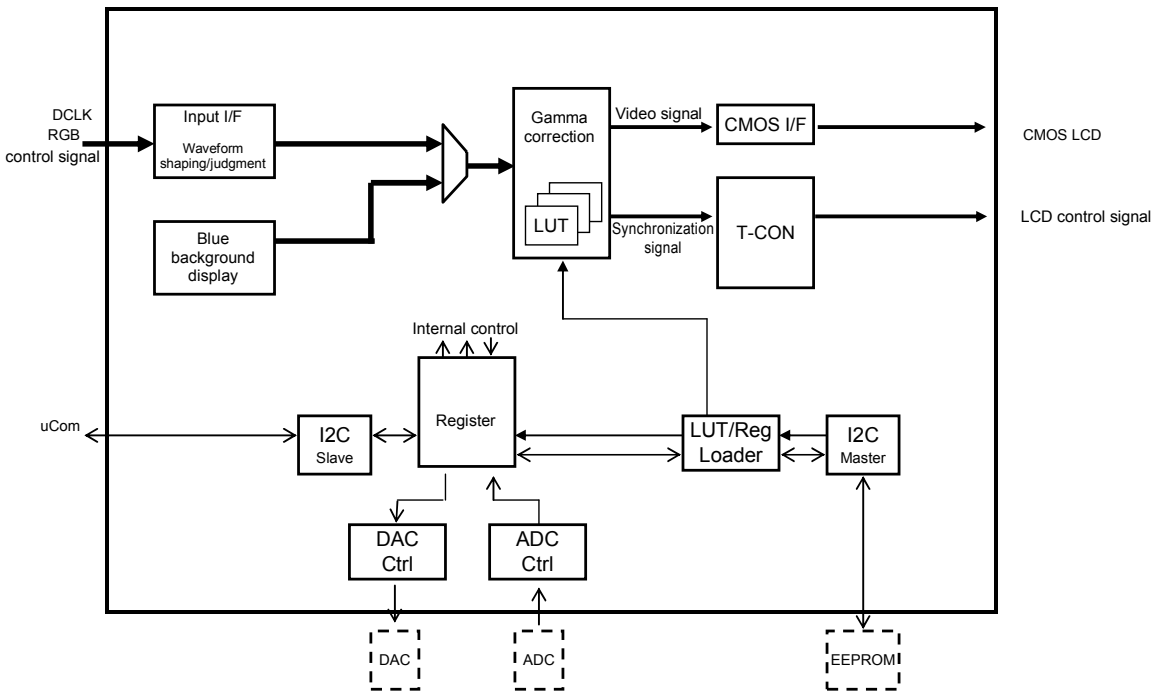


Figure 1-1: Simplified Block Diagram of LQ0DZC2291

Overview of block diagram is described below.

(1) Input I/F

Receives 18-bit parallel data input externally and passes it to the image processing block stated below. Waveform shaping (Hsy/Vsy phase difference absorption), pulse noise elimination (pulse of 2 clk or less) from control signal and synchronization signal input judgment are performed here.

(2) Blue background display

A block to generate the blue background display when Input I/F of (1) has judged that there is no synchronization signal input.

(3) Gamma correction

The gamma correction function allows to process input video data per RGB data and adjust the gamma curve per R, G and B. (This is available only for ROMOFF = '0'.)

(4) T-CON

A block of timing controller to drive a panel of four kinds of resolutions, i.e., WVGA, WQVGA, WEGA1 and /WEGA2.

(5) LUT/Reg_Loader

A block to read a data from the external EEPROM, which is connected to have an initial value of an ASIC's internal register and internal LUT, and to update the data for the register and LUT.

(6) DAC Ctrl

External D/C converter can be connected and controlled to set up the liquid crystal display gradation and specify the COM signal. In this block, a control signal to DAC is generated to control DAC.

(7) ADC Ctrl

External A/D converter can be connected and controlled. This block receives a signal from ADC and stores a data in the internal register of ASIC. Thermistor and photo sensor can be connected and monitored, by way of example.

2. Pin Description

2.1. Pin Layout

Table 2-1 describes all the pins.

Table 2-1: Pin Description

PIN No.	I/O Attribute	Pin Name	Drive Power	Description of Function	Operation when it is not be used
1	–	VDD			
2	I	IG0		Green data input pin (LSB)	
3	I	IG1		Green data input pin	
4	I	IG2		Green data input pin	
5	I	IG3		Green data input pin	
6	I	IG4		Green data input pin	
7	I	IG5		Green data input pin (MSB)	
8	I	IB0		Blue data input pin (LSB)	
9	I	IB1		Blue data input pin	
10	I	IB2		Blue data input pin	
11	I	IB3		Blue data input pin	
12	I	IB4		Blue data input pin	
13	I	IB5		Blue data input pin (MSB)	
14	Id	ROMOFF		Setting whether external EEPROM should be disabled or enabled	
15	Iu	VRVC		Vertical scan reversal	
16	Iu	HRVC		Horizontal scan reversal	
17	Id	SMC		ASIC test pin	OPEN/GND
18	Id	GMDSEL		Gate start pulse output setting	
19	O	SOUT		ASIC test pin	OPEN
20	I	TMC		ASIC test pin	OPEN/GND
21	Id	AMC		ASIC test pin	OPEN/GND
22	Iu	VSY		Vertical synchronization signal input pin	
23	Id	HENAB		Horizontal data enable input pin	
24	Iu	HSY		Horizontal synchronization signal input pin	
25	–	VDD			
26	–	GND			
27	I	DCLK		Clock input pin	
28	–	GND			
29	Isu	FRESET		ASIC reset pin	
30	–	VDD			
31	Id	S_SEL		Source driver setting pin	
32	Id	G_SEL		Gate driver setting pin	
33	Id	DSEL1		Resolution setting pin 1	
34	Id	DSEL2		Resolution setting pin 2	
35	Id	TEST1		ASIC test pin	GND
36	–	GND			
37	Iou	SERDIO	3mA	Serial data I/O pin	OPEN
38	Iu	SERCK		Serial clock input pin	OPEN/VDD
39	O	ADCCK	3mA	ADC clock output pin	OPEN
40	O	ADCCS	3mA	ADC chip select output pin	OPEN
41	O	ADCDI	3mA	ADC control data output pin	OPEN
42	–	ADCDO		ADC data input pin	OPEN/VDD
43	O	DACDI	3mA	DAC data output pin	OPEN
44	O	DACLD	3mA	DAC load output pin	OPEN
45	IOu	DACCK	3mA	DAC clock output pin	OPEN
46	–	GND			
47	O	ROMCK	3mA	EEPROM clock output pin	OPEN
48	O	ROMWC	3mA	EEPROM write protect output pin	OPEN
49	IOu	ROMDIO	3mA	EEPROM data I/O pin	OPEN
50	–	GND			

PIN No.	I/O Attribute	Pin Name	Drive Power	Description of Function	Operation when it is not be used
51	–	VDD			
52	O	OR0	6mA	Red data output pin (LSB)	
53	O	OR1	6mA	Red data output pin	
54	O	OR2	6mA	Red data output pin	
55	O	OR3	6mA	Red data output pin	
56	O	OR4	6mA	Red data output pin	
57	O	OR5	6mA	Red data output pin (MSB)	
58	–	GND			
59	O	OG0	6mA	Green data output pin (LSB)	
60	O	OG1	6mA	Green data output pin	
61	O	OG2	6mA	Green data output pin	
62	O	OG3	6mA	Green data output pin	
63	O	OG4	6mA	Green data output pin	
64	O	OG5	6mA	Green data output pin (MSB)	
65	–	VDD			
66	O	OB0	6mA	Blue data output pin (LSB)	
67	O	OB1	6mA	Blue data output pin	
68	O	OB2	6mA	Blue data output pin	
69	O	OB3	6mA	Blue data output pin	
70	O	OB4	6mA	Blue data output pin	
71	O	OB5	6mA	Blue data output pin (MSB)	
72	–	GND			
73	IO	STHR	6mA	* [1]Start pulse I/O signal	
74	IO	STHL	6mA	* [1]Start pulse I/O signal	
75	–	VDD			
76	–	GND			
77	O	CLK	12mA	Source driver sampling clock	
78	–	GND			
79	O	STB	6mA	Source driver latch pulse output	
80	O	REV	6mA	Source driver polarity reversal control output	
81	O	FS / REVC	6mA	* Offset cancel / COM polarity reversal signal output	
82	O	LBR	3mA	Source driver horizontal reversal control output	
83	IO	GSPOI / MODE2	3mA	* Gate start pulse / Gate mode setting pin	
84	O	R/L	3mA	Gate driver vertical reversal control output	
85	IO	GSPIO / SPS	3mA	* Gate start pulse	
86	O	GOE / MODE1	3mA	* Gate driver control output	
87	O	GCK / CLS	3mA	* Gate driver shift clock	
88	I	TEB		ASIC test pin	VDD
89	Id	TEST2		ASIC test pin	GND
90	O	ALLON	3mA	Full gate output ON setting output	OPEN
91	O	DCON	3mA	Power supply circuit control output	
92	O	G_SLP	3mA	Gate slope control pin	OPEN
93	–	VDD			
94	I	IR0		Red data input pin (LSB)	
95	I	IR1		Red data input pin	
96	I	IR2		Red data input pin	
97	I	IR3		Red data input pin	
98	I	IR4		Red data input pin	
99	I	IR5		Red data input pin (MSB)	
100	–	GND			

I: Input pin O: Output pin IO: I/O pin d: Pull-down for input pin u: Pull-up for input pin su: Schmitt input pin

* [1] Table 12-3 on page 22.

*[2] Refer to Table 2-2 on page 10.

2.2. Pin Settings

Table 2-2 describes the pin settings.

Table 2-2: Pin Settings

<table>
<tr><th>Pin name</th><th>Function</th></tr>
<tr><td>S_SEL (*)</td><td>Source setting pin
For how to set this pin, ask the person in charge of Sharp Corporation.</td></tr>
<tr><td>G_SEL (*)</td><td>Gate setting pin
For how to set this pin, ask the person in charge of Sharp Corporation.</td></tr>
<tr><td>VRVC</td><td>Gate driver scan direction setting
Refer to Chapter 11 “Horizontal/Vertical Reverse Display”.</td></tr>
<tr><td>HRVC</td><td>Source driver scan direction setting
Refer to Chapter 11 “Horizontal/Vertical Reverse Display”.</td></tr>
<tr><td>GMDSEL</td><td>Gate start pulse output setting
Lo: Normal mode
Hi: Interlacing two-pulse mode</td></tr>
<tr><td>D_SEL1 (*)
D_SEL2 (*)</td><td>Input resolution switch setting pin
<table>
<tr><th>Resolution</th><th>D_SEL1</th><th>D_SEL2</th></tr>
<tr><td>WVGA</td><td>0</td><td>0</td></tr>
<tr><td>WQVGA</td><td>1</td><td>0</td></tr>
<tr><td>WEGA1</td><td>0</td><td>1</td></tr>
<tr><td>WEGA2</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>ROMOFF (*)</td><td>EEPROM setting pin
Lo: EEPEOM is enabled.
Hi: EEPEOM is disabled.

If ROMOFF is set to ‘1’, this ASIC is used as a timing controller. Therefore, register control, DAC control, etc. cannot be performed.</td></tr>
<tr><td>FRESET</td><td>Reset pin (Lo-Active)
* Time constant shall be 10 ms or less. Refer Figure 2-1.</td></tr>
</table>

Do not change any setting of pins marked with *, after the ASIC power supply turns ON.

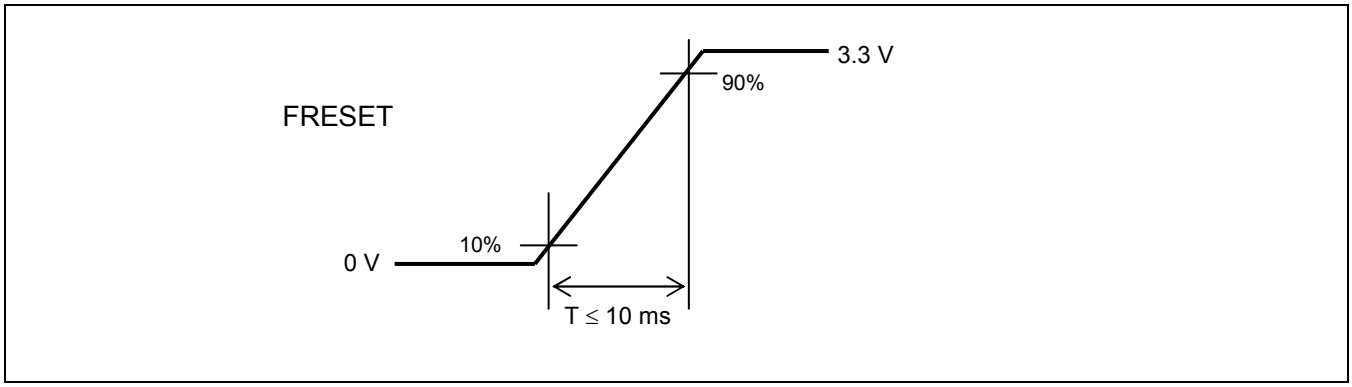


Figure 2-1 FREST Time Constant

3. Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.5 to +4.6	V
Input voltage	V_I	-0.5 to +4.6	V
Output voltage	V_O	-0.5 to +4.6	V
Operating temperature	T_A	-40 to +85	℃
Storage temperature	T_{stg}	-65 to +150	℃

4. Electrical Specification

4.1. Recommended Operating Range

Table 4-1: Recommended Operating Range

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage*[1]	V_{DD}		2.7	3.15	3.6	V
Ambient temperature	T_A		-40		85	℃
Input voltage, high*[1]	V_{IH}		2.00		V_{DD}	V
Input voltage, low*[1]	V_{IL}		0		0.8	V
Positive trigger voltage	V_P	Schmitt Buffer	1.4		2.4	V
Negative trigger voltage	V_N		0.8		1.6	V
Hysteresis voltage	V_H		0.3		1.5	V
Input rise time	t_{ri}		0		200	ns
Input fall time	t_{fi}		0		200	ns
Input rise time	t_{ri}	Schmitt Buffer	0		10	ms
Input fall time	t_{fi}		0		10	ms

* The following Supply voltage conditions operate.

Condition1

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.0		3.6	V
Input voltage, high	V_{IH}	$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	0		$0.3V_{DD}$	V

Condition2

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	2.7		3.0	V
Input voltage, high	V_{IH}	$0.75V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	0		$0.25V_{DD}$	V

4.2. DC Electrical Specification

Table 4-2: DC Electrical Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Static current consumption	I_{DDS}	V_I=V_{DD} or GND			300	μA
Off-state output current	I_{OZ}	V_0=V_{DD} or GND			±10	μA
Output short-circuit current	I_{OS}	V_0=GND			-250	mA
Input leakage current	I_I	V_I=V_{DD} or GND			±1.0	μA
	I_I	V_I=GND (pull-up 50kΩ)	-28	-83	-190	μA
	I_I	V_I=V_{DD} (pull-down 50kΩ)	28	83	190	μA
Pull-up resistor (50kΩ)	R_{PU}	V_I=GND	18.9	39.8	107.1	kΩ
Pull-down resistor (50kΩ)	R_{PD}	V_I=V_{DD}	18.9	39.8	107.1	kΩ
Output current,low	I_{OL}	V_{OL}=0.4V (I_{OL}=3mA type)	3.0			mA
		V_{OL}=0.4V (I_{OL}=6mA type)	6.0			mA
		V_{OL}=0.4V (I_{OL}=12mA type)	12.0			mA
Output current,high	I_{OH}	V_{OH}=2.4V (I_{OL}=3mA type)	-3.0			mA
		V_{OH}=2.4V (I_{OL}=6mA type)	-6.0			mA
		V_{OH}=2.4V (I_{OL}=12mA type)	-12.0			mA

4.3. AC Electrical Specification

Table 4-3: AC Electrical Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rise time	t_r	Output buffer C_L=15pF	2		10	ps
Output fall time	t_r	Output buffer C_L=15pF	2		10	ps

5. Register Map

Table 5-1 shows the register map list of LQ0DZC2291.

Table 5-1: Register Map List

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	00h	da_0ch[7:0]								0000_0000b
★	01h	da_1ch[7:0]								0000_0000b
★	02h	da_2ch[7:0]								0000_0000b
★	03h	da_3ch[7:0]								0000_0000b
★	04h	da_4ch[7:0]								0000_0000b
★	05h	da_5ch[7:0]								1111_1111b
★	06h	da_6ch[7:0]								0111_1000b
★	07h	da_7ch[7:0]								0000_0000b
★	08h	henab[7:0]								1100_0010b
★	09h	-		venab[7:0]						0010_0011b
★	0Ah	-					rsel	vrvc	hrvc	0000_0000b
★	0Bh		stb_hl[6:0]							0100_0101b
★	0Ch	gck_hl[7:0]								1010_1010b
★	0Dh	-	slp_ctrl[6:0]							0100_0011b
★	0Eh	gamma_enb	-							0000_0000b
★	0Fh	test								0000_0000b
★	10h	test								0000_0000b
○	20h	rom_adrs[7:0]								
○	21h	rom_data[7:0]								
○	22h	-						r_read	r_write	
○	23h	test								
○	24h	test								
○	25h	test								
△	30h	-							allon	
△	31h	-							als	
◇	32h	ready	-					jinput	jenable	
△	33h	test								
◇	34h	adc_data1								
◇	35h	adc_data2								

★: Register for auto-loading

als register value 0: Inaccessible.

als register value 1: Write/Read can be done from a host.

○: Register not for auto-loading

als register value 0: Inaccessible

als register value 1: Write/Read can be done from a host.

△: Register not for auto-loading

Regardless of the als register value, Write/Read can be done.

◇: Read-Only register

Regardless of the als register value, Read only can be done.

6. Conditions for Input Signal

6.1. Conditions for Image Signal Input

Table 6-1 to Table 6-4 and Figure 6-1 to Figure 6-4 show the input range specifications for the WVGA, WQVGA, WEGA1 and WEGA2 modes. Also, Table 6-5 shows the horizontal/vertical display data capture position list in the WVGA, WQVGA, WEGA1 and WEGA2 display modes.

Table 6-1: WVGA Input Timing Specifications

WVGA [D_SEL1=0, D_SEL2=0]

ITEM		Symbol	Min.	Typ.	Max.	UNIT	Remark
DCLK	Frequency	tCLK	26.62	33.26	34.60	MHz	Frequency:1/(tV/tH(clk))
	Hi Time	tWCH	5	-	-	ns	
	Low Width	tWCL	5	-	-	ns	
Data[I* 0-5]	Setup time	tDS	5	-	-	ns	
	Hold time	tDH	5	-	-	ns	
Hsy	Cycle	tH(t)	31.45	31.75	38.46	µs	
		tH(clk)	1024	1056	1088	ck	
	Pulse Width	tHPW	5	-	tH-5	ck	
Vsy	Cycle	tV	520	525	635	line	
	Pulse Width	tVPW	2	-	TV-2	line	
frame rate		fV	50	60	60	Hz	
Horizontal display period		tHA	-	800	-	ck	
Hsy_DCLK phase defference		tHC	A-8	A	A+8	ns	A=tWCH(1/2(DCLK))
Hsy_Vsy phase defference		tVH	-10	0	10	ck	
Vertical fromt porch		tVFP	5	-	-	line	
Vertical back porch		tVBP	-	35	-	line	In case ROMOFF='1'
			10	28	35	line	In case ROMOFF='0'
Vertical display porch		tVA	-	480	-	line	
Enable signal[HENAB]	Setup time	tES	5	-	-	ns	
	Hold time	tEH	5	-	-	ns	
	Pulse Width	tEP	-	800	-	ck	
Horizontal front porch		tHFP	2	-	-		
Horizontal display starting position		tHBP	-	194	-		*1
		tHBP	20	-	222	ck	*2

*1: This spec is appied for HENAB Lo mode and W/O EEPROM mode

*2: This spec is applied for HENAB active mode or W/EEPROM mode

Table 6-2: WQVGA Input Timing Specifications

WQVGA [D_SEL1=1, D_SEL2=0]

ITEM		Symbol	Min.	Typ.	Max.	UNIT	Remark
DCLK	Frequency	tCLK	6.96	7.99	9.19	MHz	Frequency:1/(tV/tH(clk))
	Hi Time	tWCH	5	-	-	ns	
	Low Width	tWCL	5	-	-	ns	
Data[I* 0-5]	Setup time	tDS	5	-	-	ns	
	Hold time	tDH	5	-	-	ns	
Hsy	Cycle	tH(t)	61.3	63.6	70.5	µs	
		tH(clk)	491	508	563	ck	
	Pulse Width	tHPW	5	-	TH-5	ck	
Vsy	Cycle	tV	258	262	284	line	
	Pulse Width	tVPW	2	-	TV-2	line	
frame rate		fV	50	60	60	Hz	
Horizontal display period		tHA	-	400	-	ck	
Hsy_DCLK phase defference		tHC	A-8	A	A+8	ns	A=tWCH(1/2(DCLK))
Hsy_Vsy phase defference		tVH	-10	0	10	ck	
Vertical fromt porch		tVFP	5	-	-	line	
Vertical back porch		tVBP	-	20	-	line	In case ROMOFF='1'
			9	-	20	line	In case ROMOFF='0'
Vertical display porch		tVA	-	240	-	line	
Enable signal[HENAB]	Setup time	tES	5	-	-	ns	
	Hold time	tEH	5	-	-	ns	
	Pulse Width	tEP	-	400	-	ck	
Horizontal front porch		tHFP	2	-	-		
Horizontal display starting position		tHBP	-	87	-		*1
		tHBP	20	-	126	ck	*2

*1: This spec is appied for HENAB Lo mode and W/O EEPROM mode

*2: This spec is applied for HENAB active mode or W/EEPROM mode

Table 6-3: WEGA1 Input Timing Specifications

WEGA1 [D_SEL1=0, D_SEL2=1]

ITEM		Symbol	Min.	Typ.	Max.	UNIT	Remark
DCLK	Frequency	tCLK	8.58	9.70	10.99	MHz	Frequency:1/(tV/tH(clk))
	Hi Time	tWCH	5	-	-	ns	
	Low Width	tWCL	5	-	-	ns	
Data[I* 0-5]	Setup time	tDS	5	-	-	ns	
	Hold time	tDH	5	-	-	ns	
Hsy	Cycle	tH(t)	58.8	64.1	66.5	µs	
		tH(clk)	571	622	646	ck	
	Pulse Width	tHPW	5	-	tH-5	ck	
Vsy	Cycle	tV	283	312	344	line	
	Pulse Width	tVPW	2	-	TV-2	line	
frame rate		fV	50	50	60	Hz	
Horizontal display period		tHA	-	480	-	ck	
Hsy_DCLK phase defference		tHC	A-8	A	A+8	ns	A=tWCH(1/2(DCLK))
Hsy_Vsy phase defference		tVH	-10	0	10	ck	
Vertical fromt porch		tVFP	2	-	-	line	
Vertical back porch		tVBP	-	31	-	line	In case ROMOFF='1'
			9	-	41	line	In case ROMOFF='0'
Vertical display porch		tVA	-	272	-	line	
Enable signal[HENAB]	Setup time	tES	5	-	-	ns	
	Hold time	tEH	5	-	-	ns	
	Pulse Width	tEP	-	480	-	ck	
Horizontal front porch		tHFP	2	-	-		
Horizontal display starting position		tHBP	-	116	-		*1
		tHBP	20	-	164	ck	*2

*1: This spec is appied for HENAB Lo mode and W/O EEPROM mode

*2: This spec is applied for HENAB active mode or W/EEPROM mode

Table 6-4: WEGA2 Input Timing Specifications

WEGA2 [D_SEL1=1, D_SEL2=1]

ITEM		Symbol	Min.	Typ.	Max.	UNIT	Remark
DCLK	Frequency	tCLK	8.35	9.59	11.17	MHz	Frequency:1/(tV/tH(clk))
	Hi Time	tWCH	5	-	-	ns	
	Low Width	tWCL	5	-	-	ns	
Data[I* 0-5]	Setup time	tDS	5	-	-	ns	
	Hold time	tDH	5	-	-	ns	
Hsy	Cycle	tH(t)	61.3	63.6	70.5	µs	
		tH(clk)	589	610	685	ck	
	Pulse Width	tHPW	5	-	TH-5	ck	
Vsy	Cycle	tV	258	262	284	line	
	Pulse Width	tVPW	2	-	TV-2	line	
frame rate		fV	50	60	60	Hz	
Horizontal display period		tHA	-	480	-	ck	
Hsy_DCLK phase defference		tHC	A-8	A	A+8	ns	A=tWCH(1/2(DCLK))
Hsy_Vsy phase defference		tVH	-10	0	10	ck	
Vertical fromt porch		tVFP	2	-	-	line	
Vertical back porch		tVBP	-	20	-	line	In case ROMOFF='1'
			9	-	20	line	In case ROMOFF='0'
Vertical display porch		tVA	-	240	-	line	
Enable signal[HENAB]	Setup time	tES	5	-	-	ns	
	Hold time	tEH	5	-	-	ns	
	Pulse Width	tEP	-	480	-	ck	
Horizontal front porch		tHFP	2	-	-		
Horizontal display starting position		tHBP	-	104	-		*1
		tHBP	20	-	152	ck	*2

*1: This spec is appied for HENAB Lo mode and W/O EEPROM mode

*2: This spec is applied for HENAB active mode or W/EEPROM mode

6.2. Horizontal timing 1 HENAB = Active input

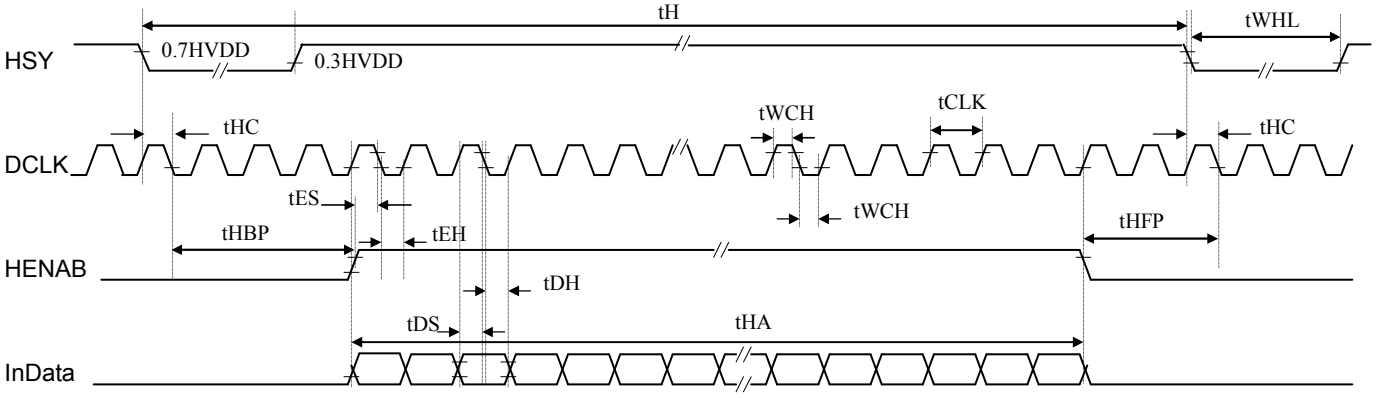


Figure 6-1: WVGA/WQVGA/WEGA1/WEGA2 Input Data Format (HENAB active/horizontal timing)

“InData” above shows the image signal bus of IR0-5, IG0-5 and IB0-5 collectively. This applies to any “InData” after this.

6.3. Horizontal timing 2 HENAB = Fixed to Lo

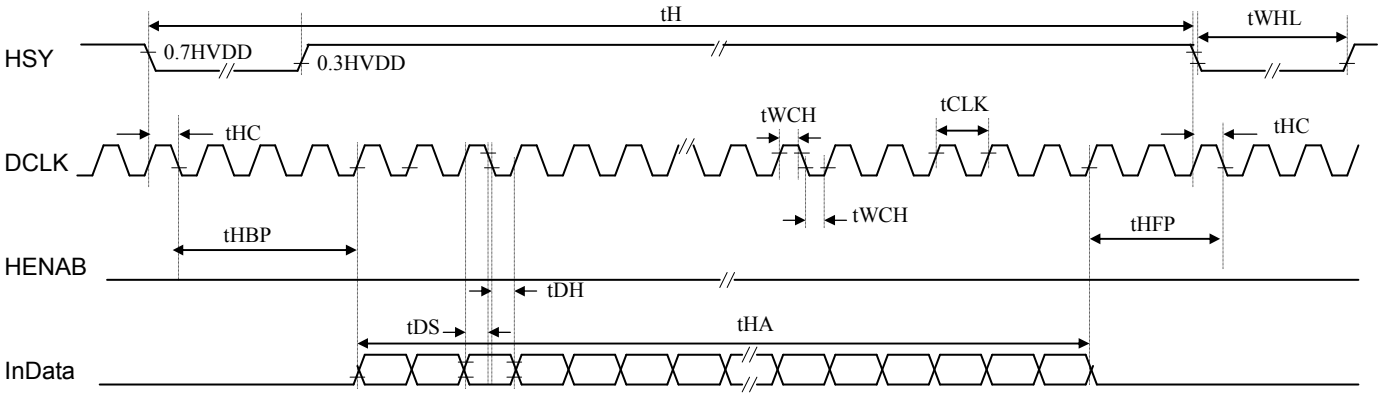


Figure 6-2: WVGA/WQVGA/WEGA1/WEGA2 Input Data Format (HENAB_Lo fixed/horizontal timing)

6.4. Vertical timing 1 HENAB = Active input

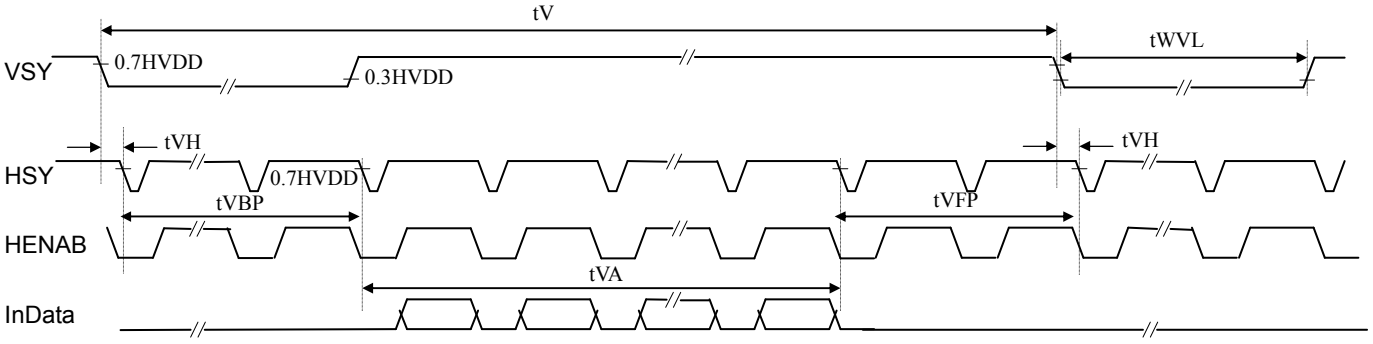


Figure 6-3: WVGA/WQVGA/WEGA1/WEGA2 Input Data Format (HENAB active/vertical timing)

6.5. Vertical timing 2 HENAB = Fixed to Lo

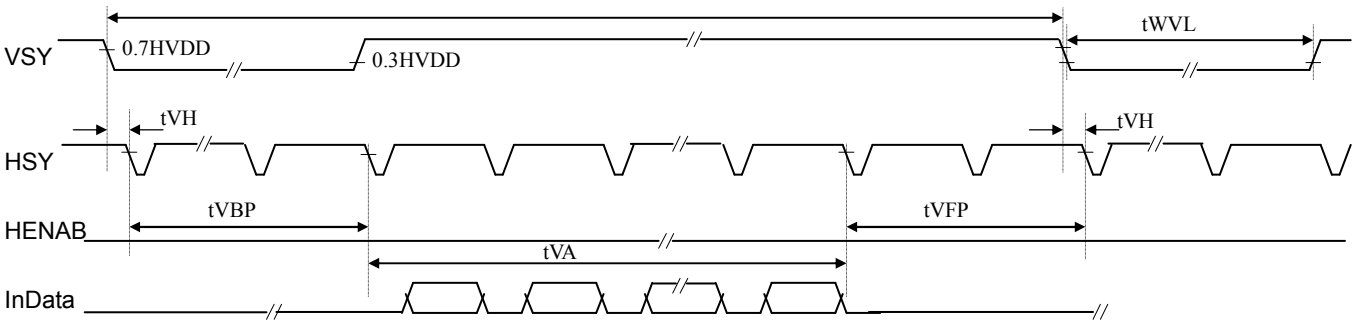


Figure 6-4: WVGA/WQVGA/WEGA1/WEGA2 Input Data Format (HENAB_Lo fixed/vertical timing)

6.6. Horizontal/Vertical Data Capture Position

Table 6-5: Horizontal/Vertical Data Capture Position in WVGA/WQVGA/WEGA1/WEGA2 Display Mode

HENAB input type	ROMOFF setting	tHBP	tVBP
Fixed to Lo	0	A	B
	1	Each condition for input signal tHBP	Each condition for input signal tVBP
Active input	0	DENAB ↑	B
	1	DENAB ↑	Each condition for input signal tVBP

A: Decided according to a henab register set value.

B: Decided according to a venab register set value.

7. Serial Input Conditions (I2C)

7.1. Protocol

Figure 7-1 shows the protocol for I2C used for LQ0DZC2291.

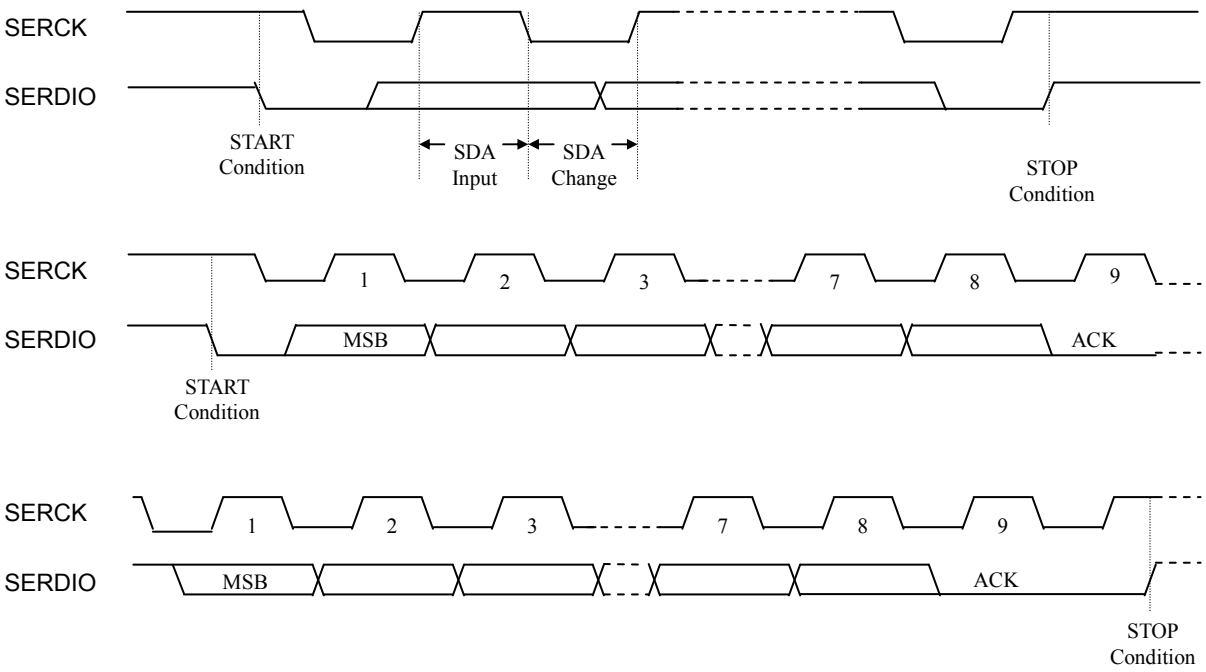


Figure 7-1: I2C Protocol

7.2. Serial Interface AC Characteristics

Figure 7-2 and Table 5-1 show the specifications for AC characteristics of I2C serial I/F.

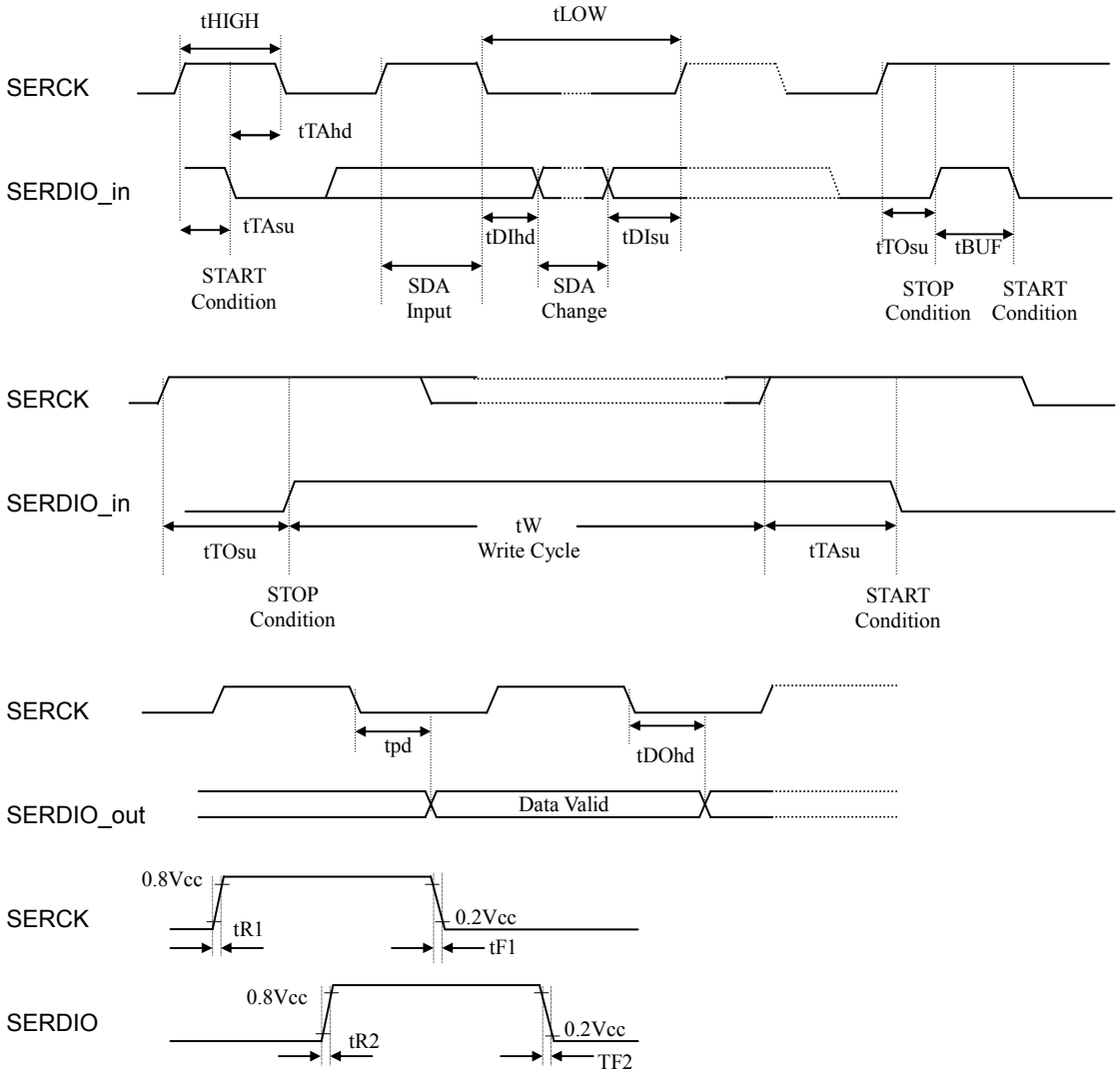


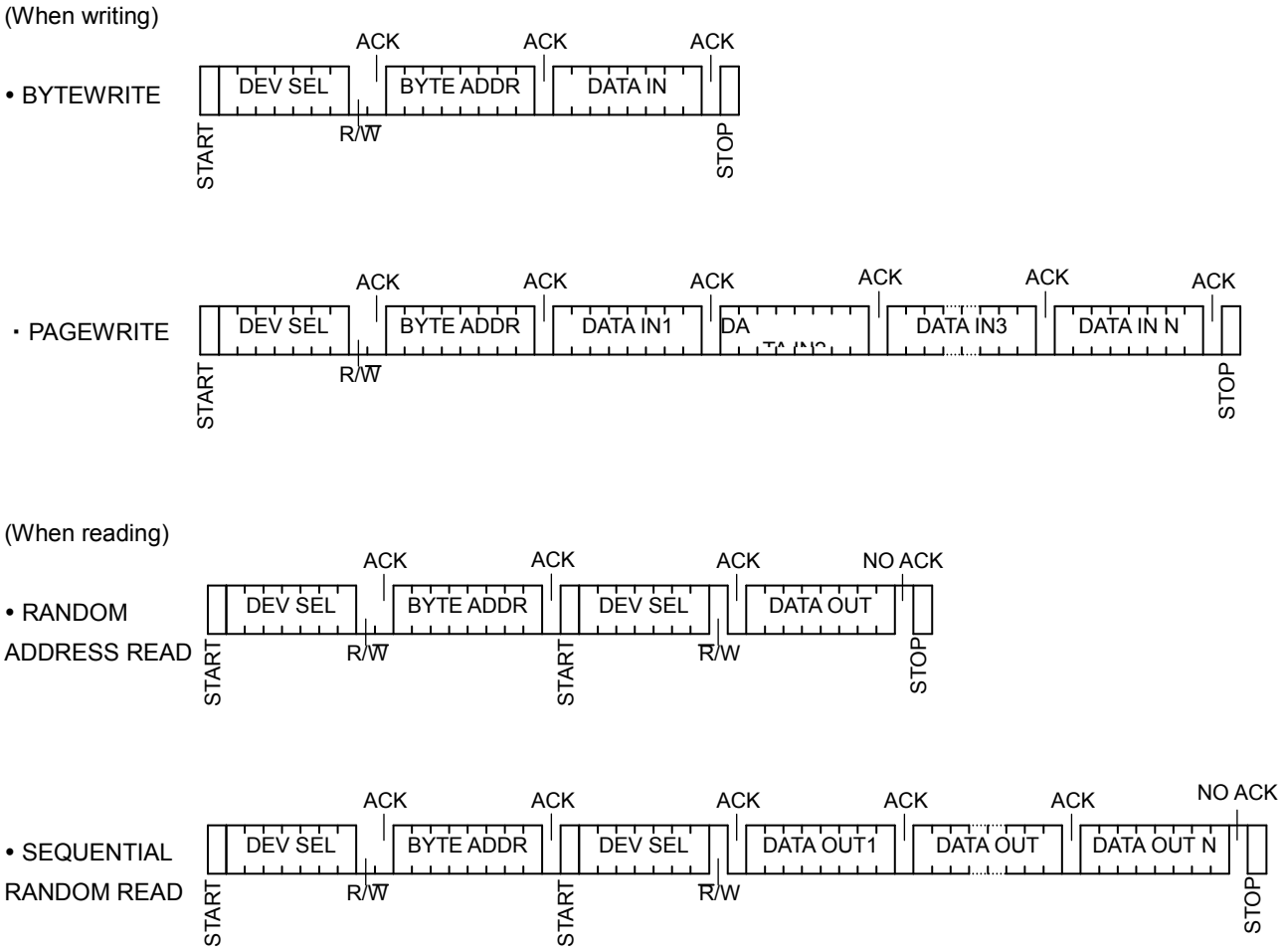
Figure 7-2: AC Specifications for Serial I/F

Table 7-1: AC Specifications for Serial I/F

Item	Symbol	Min.	Max.	Unit
Clock frequency	fSCK		400	kHz
Data clock “Hi” time	tHIGH	600		ns
Data clock “Lo” time	tLOW	1200		ns
Clock rise time	tR1		40	ns
Clock fall time	tF1		40	ns
Data rise time	tR2		40	ns
Data fall time	tF2		40	ns
Input data setup time	tDIsu	100		ns
Input data hold time	tDIhd	0		ns
Output data hold time	tDOhd	200		ns
Output data delay time	tpd	200	900	ns
Start condition setup time	tTAsu	600		ns
Start condition hold time	tTAhd	600		ns
Stop condition setup time	tTOsu	600		ns
Bus release time before transfer start	tBUF	1300		ns
Writing time	tW		10	ms

7.3. Instruction to Write/Read to/from ASIC

Figure 7-3 shows how to Write/Read to/from ASIC with I2C of LQ0DZC2291.



* DEV_SEL of this ASIC is “1000111”.

Figure 7-3: How to Write/Read with I2C

8. Description of Function and Supported Register

8.1. Outline of Loading

This ASIC can transfer the initial values of ASIC's internal register and the parameters for gamma correction, which are stored in EEPROM, to ASIC, when external EEPROM is connected and the ROMOFF pin is set to "0". Transfer EEPROM data from EEPROM into ASIC's internal register and LUT is referred to as "loading" in this document. There are two types of loading in this ASIC, as described below.

(1) Initial loading

This refers to transferring a data in EEPROM as ASIC's initial value into the internal register and LUT after canceling ASIC reset (FREST). This allows to fix an initial operation of ASIC.

(2) Auto-loading

For address 0x31[0]:als = '0', this ASIC transfers a data in EEPROM into ASIC's internal register and LUT once a 64V period.

For the ASIC's internal register, all the registers are not always loaded from EEPROM. Refer to the register map of Table 5-1 and Table 8-1 below and check whether the register should be loaded or not.

Table 8-1: Enabling/Disabling Loading and Access from Host

	ALS="0"	ALS="1"
Register to be loaded (Marked with ★ in the register map)	Access prohibited	Write/Read can be done
Register not to be loaded (Marked with ○ in the register map)	Access prohibited	Write/Read can be done
Register not to be loaded (Marked with △ in the register map)	Write/Read can be done	Write/Read can be done
Read-Only register (Marked with ◇ in the register map)	Read can be done	Read can be done

8.2. Description of Register Regarding Loading

Table 8-2 shows the registers regarding loading.

Table 8-2: Registers Regarding Loading

address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
31h	-							als	xxxx_xxx0b

als=0 Auto-loading enabled: Any access from I2C to a register area to be loaded is prohibited.
als=1 Auto-loading disabled: Register access functions completely.

32h	ready						jinput	jenable	

ready Hi: Initial EEPROM loading completed.
Lo: Initial EEPROM loading in process.

jinput Hi: When HSY/VSY has not yet been input
Lo: At a normal input operation

jenable Hi: When Henable has been input
Lo: when Henable has not yet been input

9. Power ON Sequence

Figure 9-1 below shows the power ON sequence.

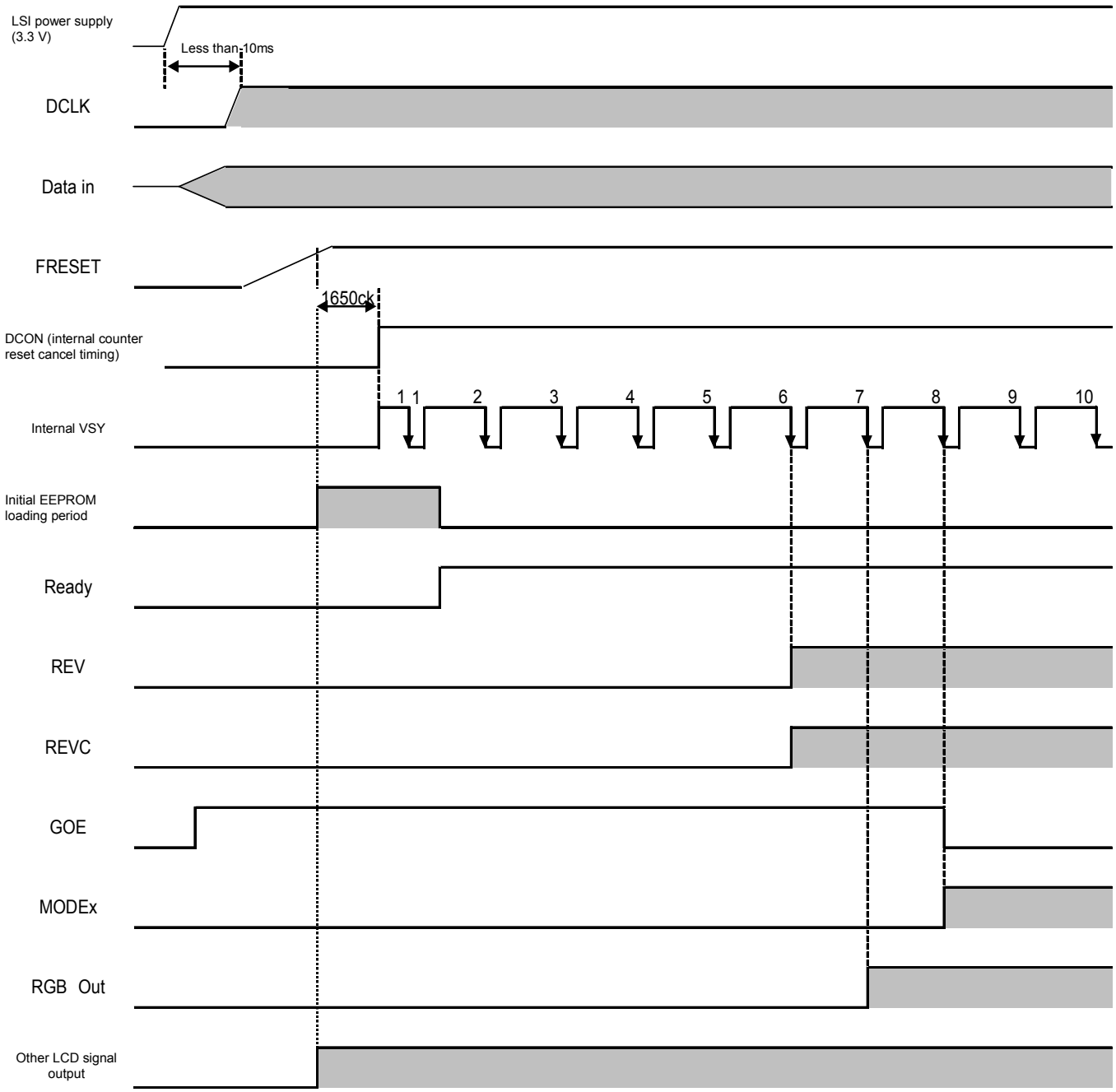


Figure 9-1: Power ON Sequence

Procedure:

(1) When ASIC has turned on, change the reset pin (FRESET) of this ASIC from “Lo” to “Hi” and cancel the reset.

(2) When the reset has been cancelled, ASIC loads the initial values of internal register and LUT from EEPROM (for a maximum period of approximately 2 V).

* In this period, access with I2C from an external CPU to a register to be loaded is prohibited. When making access, check that the ready register is “1” (i.e., initial loading has been completed).

(3) Power ON sequence starts with VsyActive immediately after DCON has become “Hi”.

(4) REV reversal starts according to the Vsy(6) timing. (Polarity reversal starts.)

(5) Data output starts according to the Vsy(7) timing.

(6) The liquid crystal display enters a normal operation state at Vsy(8).

10. I/O Format

Table 10-1 below describes the registers regarding I/O of timing controller (T-CON).

Table 10-1: Registers for I/O format

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	08h	henab[7:0]								0010_0011b
★	09h	-	venab[5:0]							0010_0011b

henab — Horizontal display start position specified when the HENABLE signal is fixed to Lo.
venab — Vertical display start position specified.
* Available only when ROMOFF = '0' is set.

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	0Ah	-					rsel	vrvc	hrvc	0000_0000b

rsel, vrvc ,hrvc — Scan direction change setting
* Refer to "Chapter 12: Horizontal/Vertical Reverse Display".

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	0Bh	-	stb_hl[6:0]							0100_0101b

stb_l — Adjustment of STB in Hi period. Pulse width of STB is adjusted and charge share time is adjusted.
* Refer to the set values listed in Table 10-2.

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	0Ch	gck_hl[7:0]								1010_1010b

gck_hl — Adjustment of CLS in Hi period.
* Refer to the set values listed in Table 10-2.

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	0Dh	-	slp_ctrl[6:0]							0100_0011b

slp_ctrl — Adjustment of G_SLP in Lo period.
* Refer to the set values listed in Table 10-2.

★: Auto-loading register

For the initial setting of stb_hl / gck_hl / slp_ctrl when ROMOFF = '0' has been specified, refer to Table 10-2.

Table 10-2: Setting for stb_hl / gckhl / slp_ctrl

	stb_hl	gck_hl	slp_ctrl
WVGA	69	70	67
WQVGA	16	40	16
WEGA1	20	49	19
WEGA2	20	49	19

Perform the gate driver pulse output setting through the GMDSEL pin. Refer to Table 10-3.

Table 10-3: Gate Start Pulse Output Setting

GMDSEL Pin	Gate start pulse output setting
0	Normal mode
1	Interlacing two-pulse mode

11. FreeRun Display

11.1. Overview of FreeRun Display

This ASIC shows the blue background stored internally when a synchronization signal (Hsy/Vsy) input externally has been disappeared.

11.2. Conditions for Transition to FreeRun

This ASIC counts Hsy/Vsy input externally. If the conditions below are met, this ASIC shows the blue background judging that there is no external input or an input error has occurred.

A value of clk of 1H ≥ 1200 clk
A value of clk of 1H ≤ tHA

The number of lines of 1V ≥ 700 lines
The number of lines of 1V ≤ tVA

11.3. Conditions for Recovery from FreeRun

The ASIC counts Hsy/Vsy input externally in the FreeRun state. When the conditions below have been met and the same count value is obtained twice continuously, the ASIC shows the external input signal display judging that there is an external input.

(tHA < a value of clk of 1H < 1200 clk) & the same count value obtained twice continuously
(tVA < the number of lines of 1V < 700 line) & the same count value obtained twice continuously

12. Horizontal/Vertical Reverse Display

This ASIC can reverse the display horizontally/vertically. The source/gate driver scan direction is set through an input pin, i.e., the HRCV pin/VRVC pin, or a register. The settings are described below.

Table 12-1: Horizontal/Vertical Reverse Display Settings

With or without ROM	ROMOFF='0'		ROMOFF='1'
EEPROM setting 0x0a rsel value	rsel='0'	rsel='1'	
Gate/source scan direction setting	15 pin VRVC/ 16 pin HRVC	0x0a vrvc/hrvc register value	15pin VRVC/ 16pin HRVC

Table 10-2: Register Regarding Horizontal/Vertical Reverse Display

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	0Ah	-					rsel	vrvc	hrvc	0000_0000b

rsel	For 0' setting, the vertical/horizontal reverse display is set by the input pins VRVC and HRVC. For 1' setting, the vertical/horizontal reverse display is set by the register values vrvc and hrvc.
vrvc	If the rsel register value is '1', the vertical reverse display is set.
hrvc	If the rsel register value is '1', the horizontal reverse display is set.

The HRVC pin/hrvc register setting and the I/O of LBR/STHR/STHL are shown below.

Table 12-3: I/O Related to Horizontal Reverse Display

HRVC pin/ hrvc register	LBR	STHR	STHL
0	0	Input	Output
1	1	Output	Input

※Please confirm the I/O relation described in specifications of LCD, and connect it with LQ0DZC2291.

The VRVC pin/vrvc register setting and the I/O of RL/GSPOI_MODE2/GSPIO_SPS are shown below.

Table 12-4: I/O Related to Vertical Reverse Display

	G_SEL='0'			G_SEL='1'		
VRVC/ vrvc register	R/L	GSPOI_ MODE2	GSPIO_ SPS	R/L	GSPOI_ MODE2	GSPIO_ SPS
0	0	Output (GSPOI)	Input (GSPIO)	1	Output (MODE2)	Output (SPS)
1	1	Input (GSPOI)	Output (GSPIO)	0	Output (MODE2)	Output (SPS)

13. RGB Independent Gamma Correction

13.1. Overview of RGB Independent Gamma Correction

By mapping an input 6-bit data to a 8-bit signal based on the parameter stored in EEPROM, the 6-bit data is converted into 8-bit data in ASIC. This allows to control the gamma characteristics of input data per R, G and B independently. This ASIC is for 6-bit liquid crystal panel. So, the data is converted into 8-bit data in a pseudo way by the FRC technology and is displayed on the 6-bit panel. For turning ON/OFF the independent gamma conversion, refer to the register Map. (This is available only for ROMOFF = '0'.)

13.2. Description of Register Regarding RGB Independent Gamma Correction

Table 13-1 shows the register regarding RGB independent gamma correction.

Table 13-1: Register Regarding RGB Independent Gamma Correction

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	0Eh	gamma_en	-							0***_****b

gamma_en: Setting to turn ON/OFF RGB independent gamma
gamma_en='0': Independent gamma correction is disabled. (The gamma correction is omitted.)
gamma_en='1': Independent gamma correction is enabled.

13.3. Flow of Use of Independent Gamma Function

As described above, the independent gamma parameters are loaded from EEPROM. Those independent gamma parameters are stored in the 192 addresses from 0x40 to 0xFF in EEPROM. Therefore, to use the independent gamma function, (1) write the set values corresponding to input gradations in advance and (2) store the data of 0x80 in the address 0x0E (gamma_enb) where is an auto-loading area in EEPROM.

14. EEPROM

14.1. EEPROM

When using this ASIC, “256word×8bitEEPROM” can be connected externally. Connect it to Pin (47: ROMCK, 48: ROMWC, 49: ROMDIO) of ASIC. This allows to load the ASIC register set values and independent gamma parameters from EEPROM. EEPROM is controlled by ASIC. So, any access from an external CPU to EEPROM must be performed through ASIC’s internal register.

14.2. Recommended EEPROM

Rohm “BR24L02-W” can be recommended as EEPROM that connection verification was executed.
* Slave address “1010_000”

14.3. Description of Register Regarding EEPROM

Table 14-1 shows the register regarding EEPROM.

Table 14-1: Description of Register Regarding EEPROM

address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
20h	rom_adrs[7:0]								0000_0000b

rom_adrs: An address to access EEPROM is specified.

21h	rom_data[7:0]								0000_0000b

rom_data: To write a data into EEPROM, specify an target address (in which the data is written) in the rom_adrs register and the target data (to be written) in this register and write the data into EEPROM through the rom_write register.

To read a data from EEPROM, specify an target address (which stores the data to be read) in the rom_adrs and read the data from EEPROM through rom_read register. Then, the data stored in the specified address is stored in this register.
When reading this register, confirm rom_head = 0 in advance.

22h	-						rom_read	rom_write	xxxx_xx00b

rom_read ='0': -
rom_read ='1': The contents of EEPROM address specified in the rom_adrs register are read and then stored in the rom_data register. During reading from EEPROM, this register remains “1”. When reading has been completed and the values have been stored in the rom_data register, this register becomes “0”.

rom_write ='0': -
rom_write ='1': A value of the rom_data register is written into an address in EEPROM, which is specified in the rom_adrs register. During writing into EEPROM, this register remains “1”. When writing has been completed, this register becomes “0”.

You can not set both of rom_read = ‘1’ and rom_write = ‘1’ simultaneously. Your operation is ignored.

14.4. How to Write/Read to/from EEPROM

(How to write)

(1) Read the address 0x22 to check that it is 0x00. (If the Read data in this address is 0x01or0x02, any instruction from an external CPU is ignored because access to EEPROM is in process.)
(2) Specify an EEPROM address to be written into the 0x20 address.
(3) Write a data to be written into the address specified in step (2) in the address 0x21.
(4) When 0x01 has been written into the address 0x22, the data specified in the step (3) is written into the EEPROM address specified in the step (2). (When the operation has been completed, ASIC changes the address 0x22 to 0x00 automatically.)
(5) Unless the address 0x22 changes to 0x00 as stated in the step (1), any more writing/reading to/from EEPROM cannot be executed.

(How to read)

(1) Read the address 0x22 to check that it is 0x00. (If the Read data in this address is 0x01or0x02, any instruction from an external CPU is ignored because access to EEPROM is in process.)
(2) Specify an EEPROM address to be read out to the 0x20 address.
(3) When 0x02 has been written into the address 0x22, reading out from EEPROM to the address specified in the step (2) starts and the read data is written into the address 0x21. (When the operation has been completed, ASIC changes the address 0x22 to 0x00 automatically.)
(4) Check that a data in the address 0x22 is 0x00 and then read out the data written into the address 0x21.

14.5. ROM_Map of EEPROM

Table 14-2 shows mapping in EEPROM of this ASIC. Technique to storage in EEPROM is described below individually in detail.

Table 14-2: ROM_Map of EEPROM

ADRS	Content	ADRS	Content	ADRS	Content	ADRS	Content
0x00	dac_0ch	0x40	Independent gamma (R)_00	0x80	Independent gamma (G)_00	0xC0	Independent gamma (B)_00
0x01	dac_1ch	0x41	Independent gamma (R)_01	0x81	Independent gamma (G)_01	0xC1	Independent gamma (B)_01
0x02	dac_2ch	0x42	Independent gamma (R)_02	0x82	Independent gamma (G)_02	0xC2	Independent gamma (B)_02
0x03	dac_3ch	0x43	Independent gamma (R)_03	0x83	Independent gamma (G)_03	0xC3	Independent gamma (B)_03
0x04	dac_4ch	0x44	Independent gamma (R)_04	0x84	Independent gamma (G)_04	0xC4	Independent gamma (B)_04
0x05	dac_5ch	0x45	Independent gamma (R)_05	0x85	Independent gamma (G)_05	0xC5	Independent gamma (B)_05
0x06	dac_6ch	0x46	Independent gamma (R)_06	0x86	Independent gamma (G)_06	0xC6	Independent gamma (B)_06
0x07	dac_7ch	0x47	Independent gamma (R)_07	0x87	Independent gamma (G)_07	0xC7	Independent gamma (B)_07
0x08	Horizontal display start position adjustment	0x48	Independent gamma (R)_08	0x88	Independent gamma (G)_08	0xC8	Independent gamma (B)_08
0x09	Vertical display start position adjustment	0x49	Independent gamma (R)_09	0x89	Independent gamma (G)_09	0xC9	Independent gamma (B)_09
0x0A	Scan direction change setting	0x4A	Independent gamma (R)_10	0x8A	Independent gamma (G)_10	0xCA	Independent gamma (B)_10
0x0B	Charge share adjustment	0x4B	Independent gamma (R)_11	0x8B	Independent gamma (G)_11	0xCB	Independent gamma (B)_11
0x0C	CLS_Hi period adjustment	0x4C	Independent gamma (R)_12	0x8C	Independent gamma (G)_12	0xCC	Independent gamma (B)_12
0x0D	Gate slope adjustment	0x4D	Independent gamma (R)_13	0x8D	Independent gamma (G)_13	0xCD	Independent gamma (B)_13
0x0E	Gamma control	0x4E	Independent gamma (R)_14	0x8E	Independent gamma (G)_14	0xCE	Independent gamma (B)_14
0x0F	Test register	0x4F	Independent gamma (R)_15	0x8F	Independent gamma (G)_15	0xCF	Independent gamma (B)_15
0x10	Test register	0x50	Independent gamma (R)_16	0x90	Independent gamma (G)_16	0xD0	Independent gamma (B)_16
0x11	Gate output mode setting	0x51	Independent gamma (R)_17	0x91	Independent gamma (G)_17	0xD1	Independent gamma (B)_17
0x12		0x52	Independent gamma (R)_18	0x92	Independent gamma (G)_18	0xD2	Independent gamma (B)_18
0x13		0x53	Independent gamma (R)_19	0x93	Independent gamma (G)_19	0xD3	Independent gamma (B)_19
0x14		0x54	Independent gamma (R)_20	0x94	Independent gamma (G)_20	0xD4	Independent gamma (B)_20
0x15		0x55	Independent gamma (R)_21	0x95	Independent gamma (G)_21	0xD5	Independent gamma (B)_21
0x16		0x56	Independent gamma (R)_22	0x96	Independent gamma (G)_22	0xD6	Independent gamma (B)_22
0x17		0x57	Independent gamma (R)_23	0x97	Independent gamma (G)_23	0xD7	Independent gamma (B)_23
0x18		0x58	Independent gamma (R)_24	0x98	Independent gamma (G)_24	0xD8	Independent gamma (B)_24
0x19		0x59	Independent gamma (R)_25	0x99	Independent gamma (G)_25	0xD9	Independent gamma (B)_25
0x1A		0x5A	Independent gamma (R)_26	0x9A	Independent gamma (G)_26	0xDA	Independent gamma (B)_26
0x1B		0x5B	Independent gamma (R)_27	0x9B	Independent gamma (G)_27	0xDB	Independent gamma (B)_27
0x1C		0x5C	Independent gamma (R)_28	0x9C	Independent gamma (G)_28	0xDC	Independent gamma (B)_28
0x1D		0x5D	Independent gamma (R)_29	0x9D	Independent gamma (G)_29	0xDD	Independent gamma (B)_29
0x1E		0x5E	Independent gamma (R)_30	0x9E	Independent gamma (G)_30	0xDE	Independent gamma (B)_30
0x1F		0x5F	Independent gamma (R)_31	0x9F	Independent gamma (G)_31	0xDF	Independent gamma (B)_31
0x20		0x60	Independent gamma (R)_32	0xA0	Independent gamma (G)_32	0xE0	Independent gamma (B)_32
0x21		0x61	Independent gamma (R)_33	0xA1	Independent gamma (G)_33	0xE1	Independent gamma (B)_33
0x22		0x62	Independent gamma (R)_34	0xA2	Independent gamma (G)_34	0xE2	Independent gamma (B)_34
0x23		0x63	Independent gamma (R)_35	0xA3	Independent gamma (G)_35	0xE3	Independent gamma (B)_35
0x24		0x64	Independent gamma (R)_36	0xA4	Independent gamma (G)_36	0xE4	Independent gamma (B)_36
0x25		0x65	Independent gamma (R)_37	0xA5	Independent gamma (G)_37	0xE5	Independent gamma (B)_37
0x26		0x66	Independent gamma (R)_38	0xA6	Independent gamma (G)_38	0xE6	Independent gamma (B)_38
0x27		0x67	Independent gamma (R)_39	0xA7	Independent gamma (G)_39	0xE7	Independent gamma (B)_39
0x28		0x68	Independent gamma (R)_40	0xA8	Independent gamma (G)_40	0xE8	Independent gamma (B)_40
0x29		0x69	Independent gamma (R)_41	0xA9	Independent gamma (G)_41	0xE9	Independent gamma (B)_41
0x2A		0x6A	Independent gamma (R)_42	0xAA	Independent gamma (G)_42	0xEA	Independent gamma (B)_42
0x2B		0x6B	Independent gamma (R)_43	0xAB	Independent gamma (G)_43	0xEB	Independent gamma (B)_43
0x2C		0x6C	Independent gamma (R)_44	0xAC	Independent gamma (G)_44	0xEC	Independent gamma (B)_44
0x2D		0x6D	Independent gamma (R)_45	0xAD	Independent gamma (G)_45	0xED	Independent gamma (B)_45
0x2E		0x6E	Independent gamma (R)_46	0xAE	Independent gamma (G)_46	0xEE	Independent gamma (B)_46
0x2F		0x6F	Independent gamma (R)_47	0xAF	Independent gamma (G)_47	0xEF	Independent gamma (B)_47
0x30		0x70	Independent gamma (R)_48	0xB0	Independent gamma (G)_48	0xF0	Independent gamma (B)_48
0x31		0x71	Independent gamma (R)_49	0xB1	Independent gamma (G)_49	0xF1	Independent gamma (B)_49
0x32		0x72	Independent gamma (R)_50	0xB2	Independent gamma (G)_50	0xF2	Independent gamma (B)_50
0x33		0x73	Independent gamma (R)_51	0xB3	Independent gamma (G)_51	0xF3	Independent gamma (B)_51
0x34		0x74	Independent gamma (R)_52	0xB4	Independent gamma (G)_52	0xF4	Independent gamma (B)_52
0x35		0x75	Independent gamma (R)_53	0xB5	Independent gamma (G)_53	0xF5	Independent gamma (B)_53
0x36		0x76	Independent gamma (R)_54	0xB6	Independent gamma (G)_54	0xF6	Independent gamma (B)_54
0x37		0x77	Independent gamma (R)_55	0xB7	Independent gamma (G)_55	0xF7	Independent gamma (B)_55
0x38		0x78	Independent gamma (R)_56	0xB8	Independent gamma (G)_56	0xF8	Independent gamma (B)_56
0x39		0x79	Independent gamma (R)_57	0xB9	Independent gamma (G)_57	0xF9	Independent gamma (B)_57
0x3A		0x7A	Independent gamma (R)_58	0xBA	Independent gamma (G)_58	0xFA	Independent gamma (B)_58
0x3B		0x7B	Independent gamma (R)_59	0xBB	Independent gamma (G)_59	0xFB	Independent gamma (B)_59
0x3C		0x7C	Independent gamma (R)_60	0xBC	Independent gamma (G)_60	0xFC	Independent gamma (B)_60
0x3D		0x7D	Independent gamma (R)_61	0xBD	Independent gamma (G)_61	0xFD	Independent gamma (B)_61
0x3E		0x7E	Independent gamma (R)_62	0xBE	Independent gamma (G)_62	0xFE	Independent gamma (B)_62
0x3F		0x7F	Independent gamma (R)_63	0xBF	Independent gamma (G)_63	0xFF	Independent gamma (B)_63

(1) 00h to 3Fh (Basic register setting part)
For the register (marked with ★) for auto-loading in the register Map, be sure to store an initial setting data in this area. For an area not for auto-loading, even if any data is stored in EEPROM, it is not stored in the internal register.

(2) 40h to FFh (Area to store independent gamma parameter)
Independent gamma LUT in ASIC is available for 129 addresses (64 x RGB) x 8 bits. To use the independent gamma function, store the values in 0x40 to 0xFF.

15. Control of D/A Converter (hereinafter referred to as “DAC”)

15.1. Overview of DAC Control

When the external DAC is connected to this ASIC, the ASIC can decide (1) the amplitude value and center voltage value of signal for the opposite electrode (COM electrode) of liquid display and (2) the gradation setting voltage values etc. of the source driver according to the ASIC’s internal register settings. It is assumed that the DAC control is used for the two ways below.

(1) Use in a fixed set value for mass production

(2) Adjustment of opposite electrode center value in a process/source driver gradation setting voltage value

15.2. Recommended Component for DAC

Fujitsu 8chDAC “MB88347” can be recommended as DAC that connection verification was executed.

15.3. Description of Register Regarding DAC Control

Table 15-1 describes the register regarding DAC control

Table 15-1: Description of Register Regarding DAC Control

DAC control

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	initial value
★	00h	dac_0ch[7:0]								0000_0000b
	dac_0ch	DAC 0ch setting register								
★	01h	dac_1ch[7:0]								0000_0000b
	dac_1ch	DAC 1ch setting register								
★	02h	dac_2ch[7:0]								0000_0000b
	dac_2ch	DAC 2ch setting register								
★	03h	dac_3ch[7:0]								0000_0000b
	dac_3ch	DAC 3ch setting register								
★	04h	dac_4ch[7:0]								0000_0000b
	dac_4ch	DAC 4ch setting register								
★	05h	dac_5ch[7:0]								1111_1111b
	dac_5ch	DAC 5ch setting register								
★	06h	dac_6ch[7:0]								0111_1000b
	dac_6ch	DAC 6ch setting register								
★	07h	dac_7ch								0000_0000b
	dac_7ch	DAC 7ch setting register								

15.4. Actual Usage

(1) Use in a fixed set value for mass production

For the use in mass production (normal), store a voltage value to be set in EEPROM in advance. Then, ASIC stores a setting data in the ASIC's register at the initial loading after FRESET and, based on that, a control instruction to DAC is transferred.

(2) Adjustment of opposite electrode center value in a process/source driver gradation setting voltage value

This register is for auto-loading. To adjust in a process, follow the flow below. (How to adjust the amplitude of opposite electrode signal of address is described below. This applies also to any other set values.)

1. Set the ASIC register address 0x31[0]: als ＝ '1' and stop loading from EEPROM.
2. Change the ASIC register address DAC set value to find the most suitable value. (If the amplitude of opposite electrode signal is adjusting, a point that a flicker of liquid crystal minimizes is the most suitable value.)
   *) As described above, when als = '1', transfer to DAC is performed at every 1V. Even if a register is rewritten at a frequency of 1V or less, nothing is reflected in the display. Pay great attention to a change speed of register value.
3. Write the most suitable value confirmed in the step 2 into EEPROM. For how to write it, refer to "14.4. How to Write/Read to/from EEPROM".
4. Here, an initial value has been stored in EEPROM. From now on, ASIC recognizes this initial value whenever the power supply turns on.

16. Control of A/D Converter (hereinafter referred to as “ADC”)

16.1. Overview of ADC Control

When the external ADC is connected to this ASIC, the ASIC can read a value from a photo sensor or thermistor connected to the liquid crystal module and can store it in the ASIC’s internal register. The ASIC can read a data from ADC by reading an applicable register.

16.2. Recommended Component for ADC

National Semiconductor 2chADC “ADCVO8832” can be recommended ADC that connection verification was executed.

Table 16-1: Description of Register Regarding ADC Control

ADC control

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	initial value
◇	34h	adc_data1								0000_0000b
◇	35h	adc_data2								0000_0000b

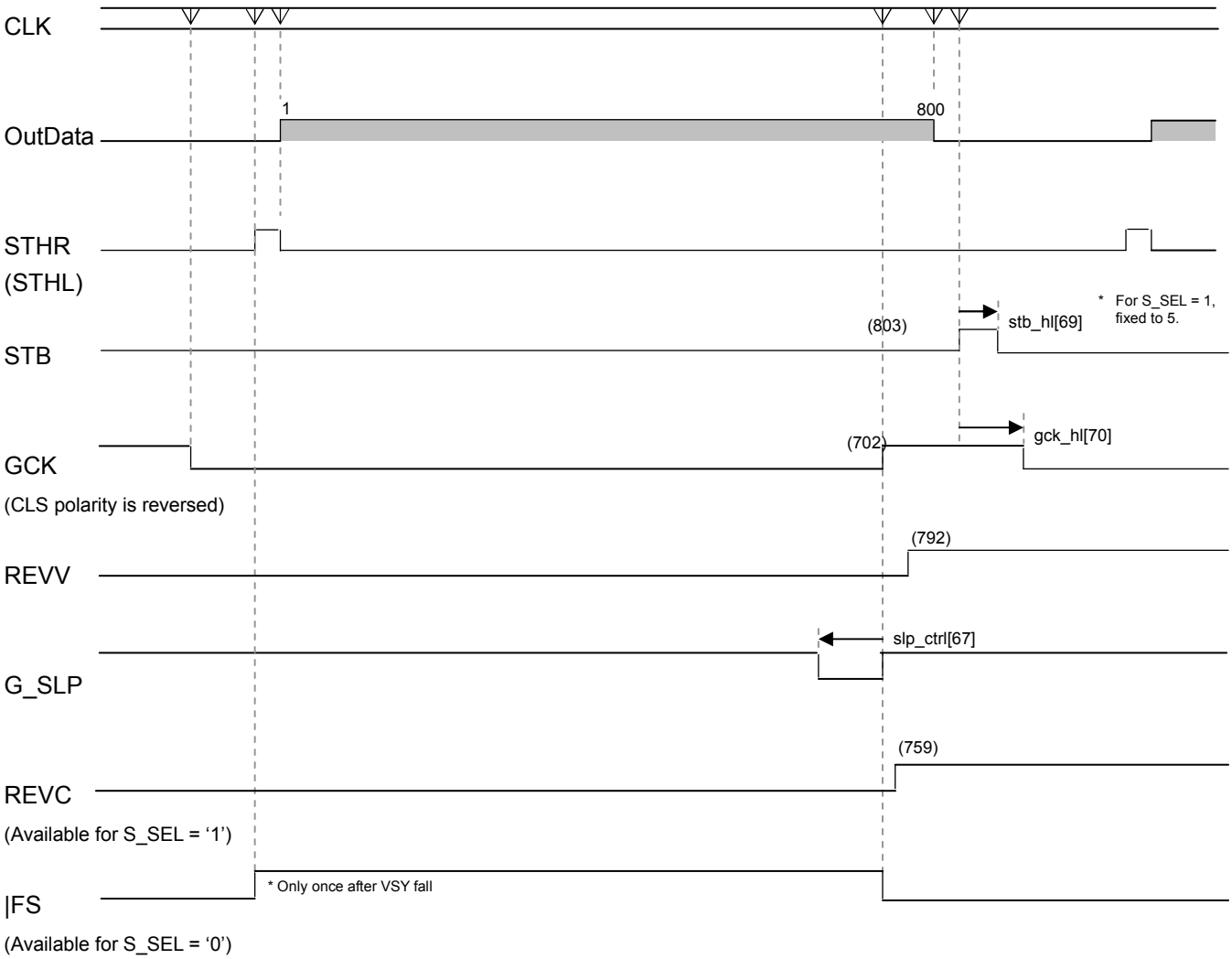
adc_data1 ADC 1ch Register
adc_data2 ADC 2ch Register

17. Output I/F to LCD

Output timing in WVGA,WQVGA,WEGA1 and WEGA2 is shown below.

17.1. Example of Horizontal Timing

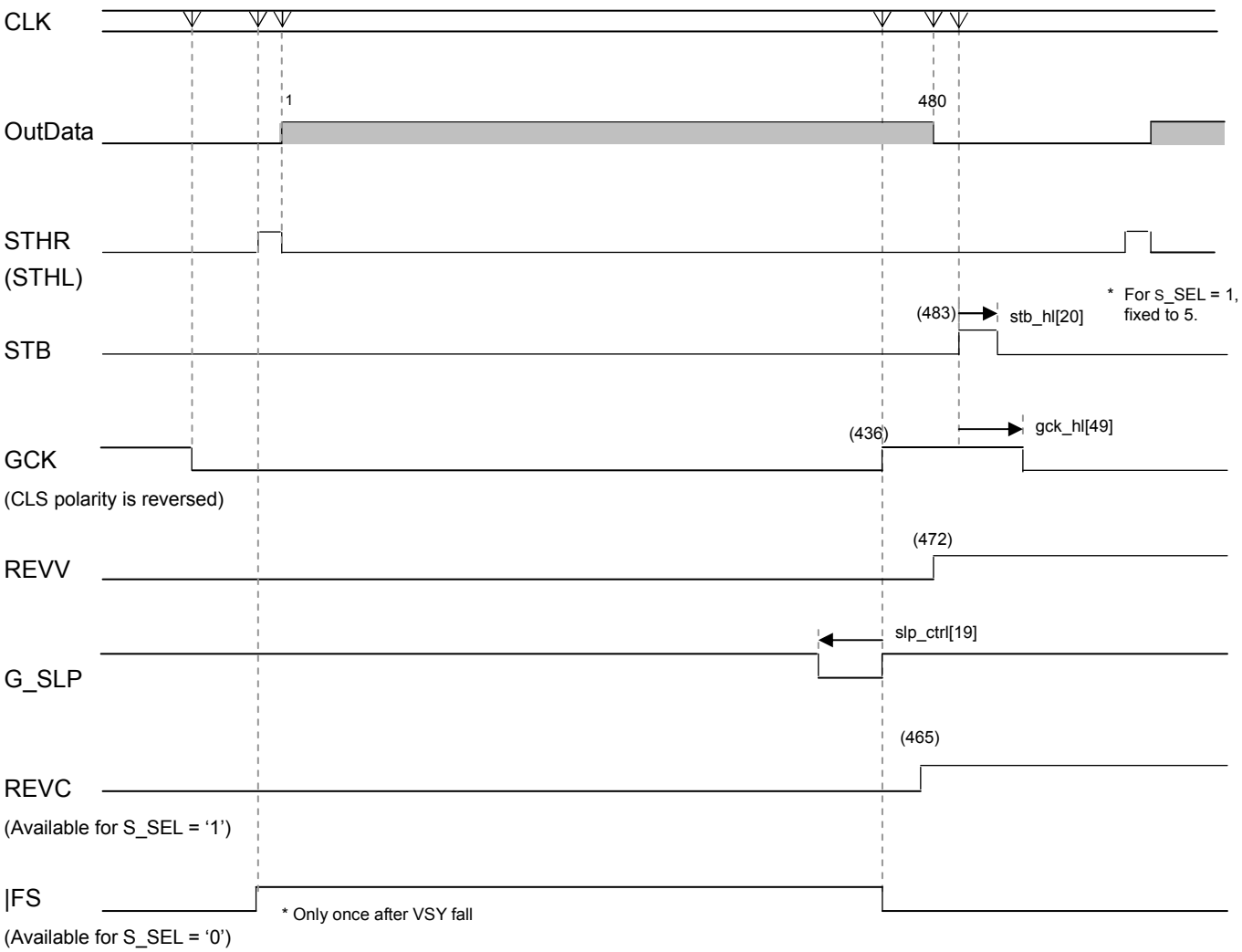
17.1.1. Horizontal Timing for Horizontal Resolution 800 Dots (WVGA)



- Figure in [ ] is a value for ROMOFF = '1'.
- Figure in ( ) is a standard value.

Figure 17-1: Horizontal Timing Chart for Horizontal Resolution 800 Dots (WVGA)

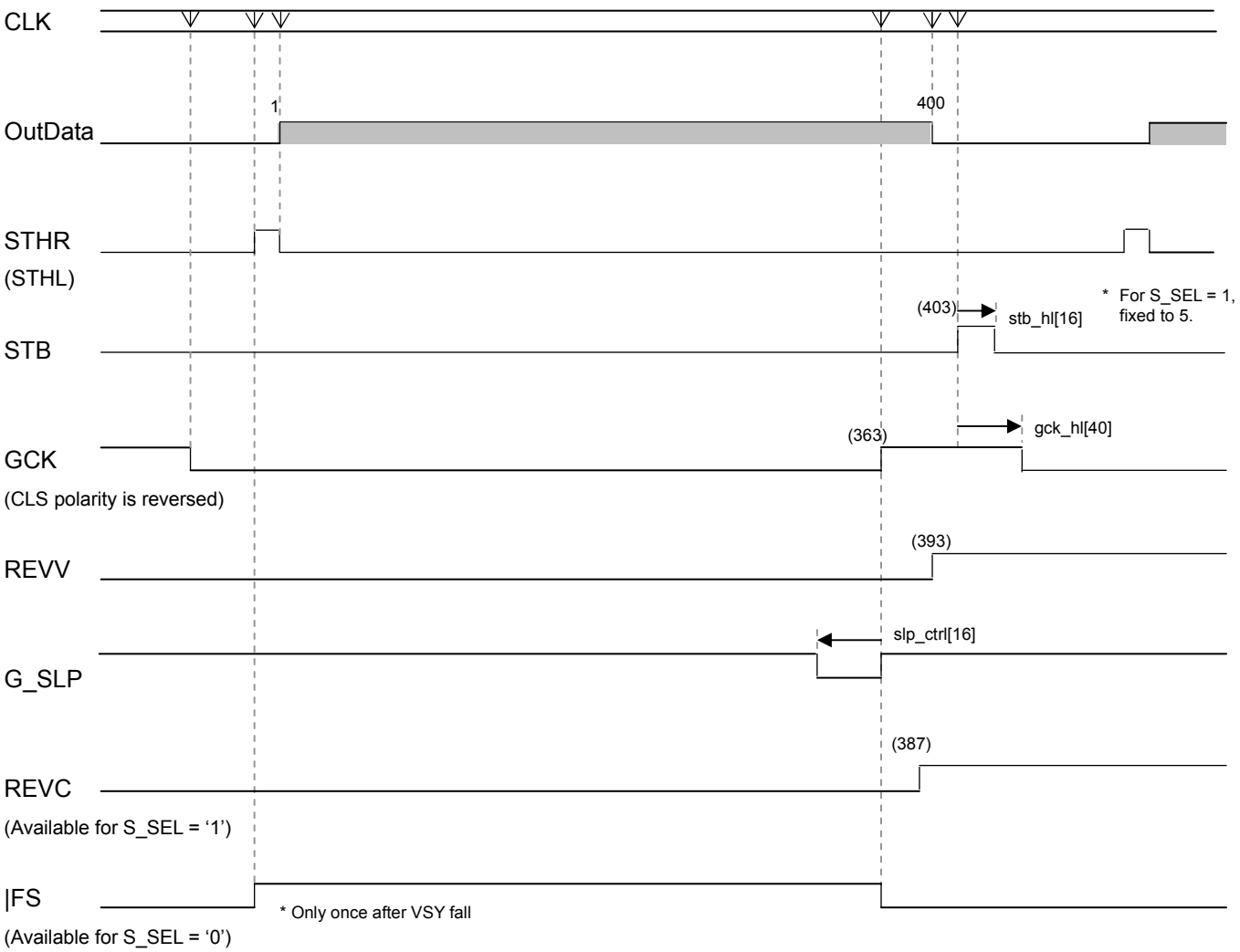
17.1.2. Horizontal Timing for Horizontal Resolution 480 Dots (WEGA1/WEGA2)



- Figure in [ ] is a value for ROMOFF = '1'. [V = for 240 lines: V = for 272 lines]
- Figure in ( ) is a standard value.

Figure 17-2: Horizontal Timing Chart for Horizontal Resolution 480 Dots (WEGA1/WEGA2)

17.1.3. Horizontal Timing for Horizontal Resolution 400 Dots (WQVGA)



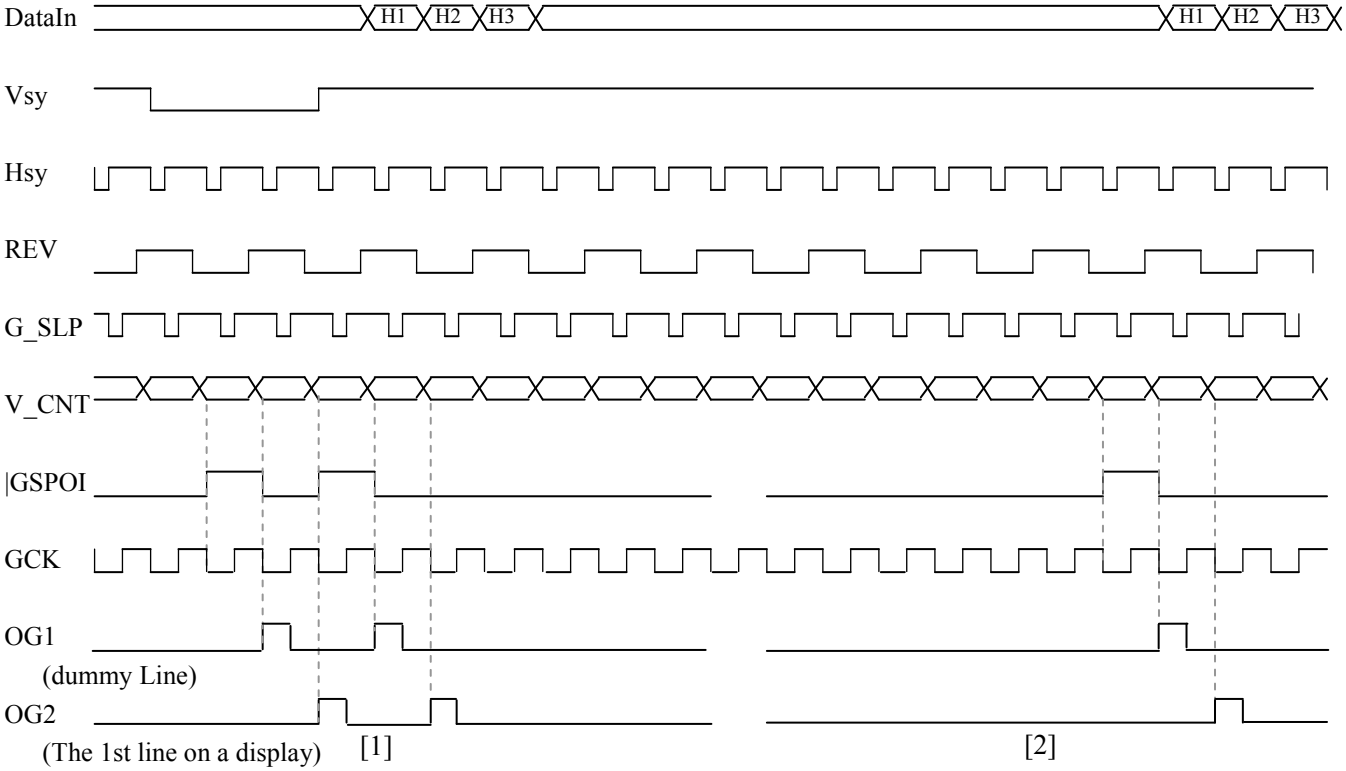
- Figure in [ ] is a value for ROMOFF = '1'.
- Figure in ( ) is a standard value.

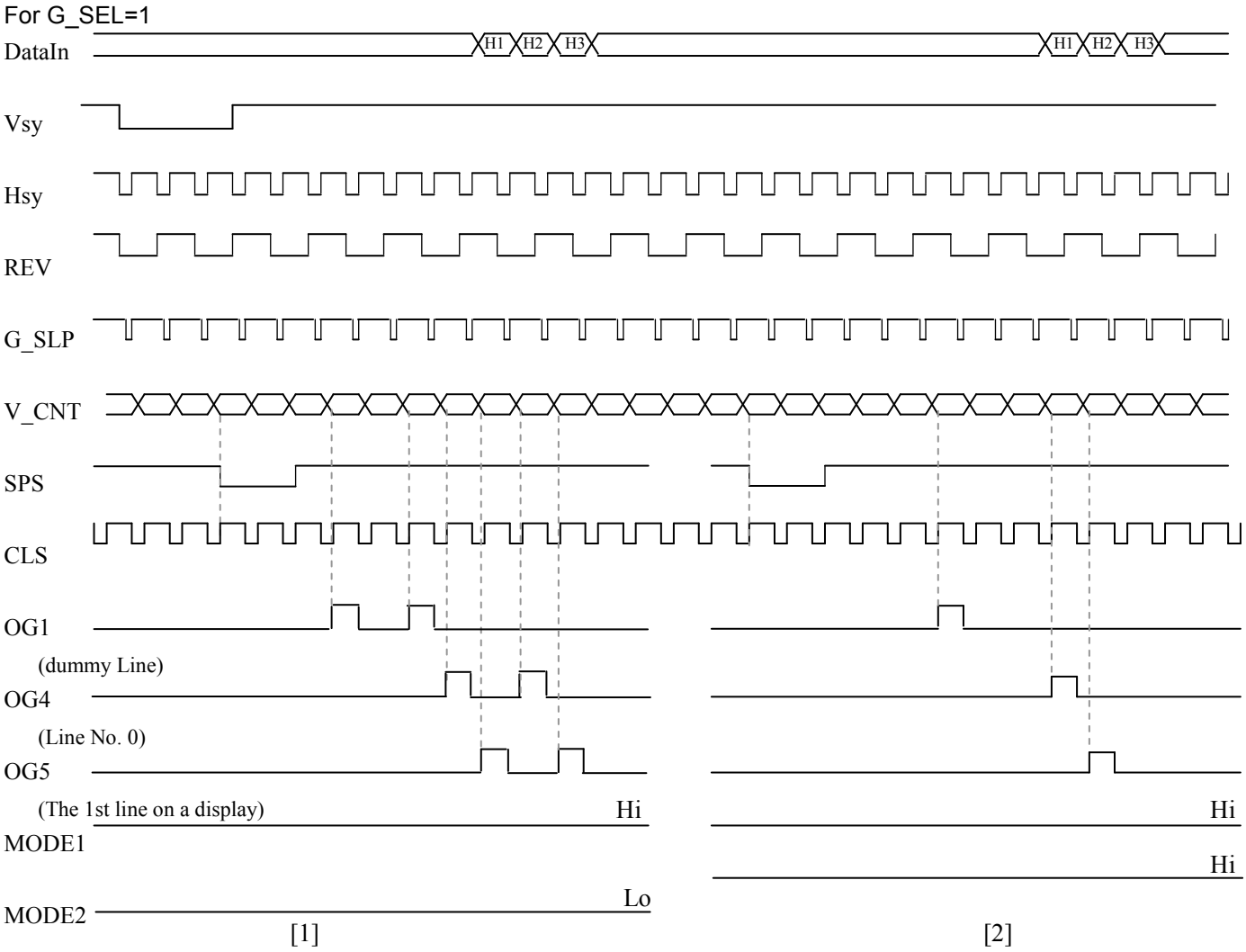
Figure 17-3: Horizontal Timing Chart for Horizontal Resolution 400 Dots (WQVGA)

17.2. Example of Vertical Timing

17.2.1. Vertical Timing for Vertical Resolution 480 Lines (WVGA)

For G_SEL = 0



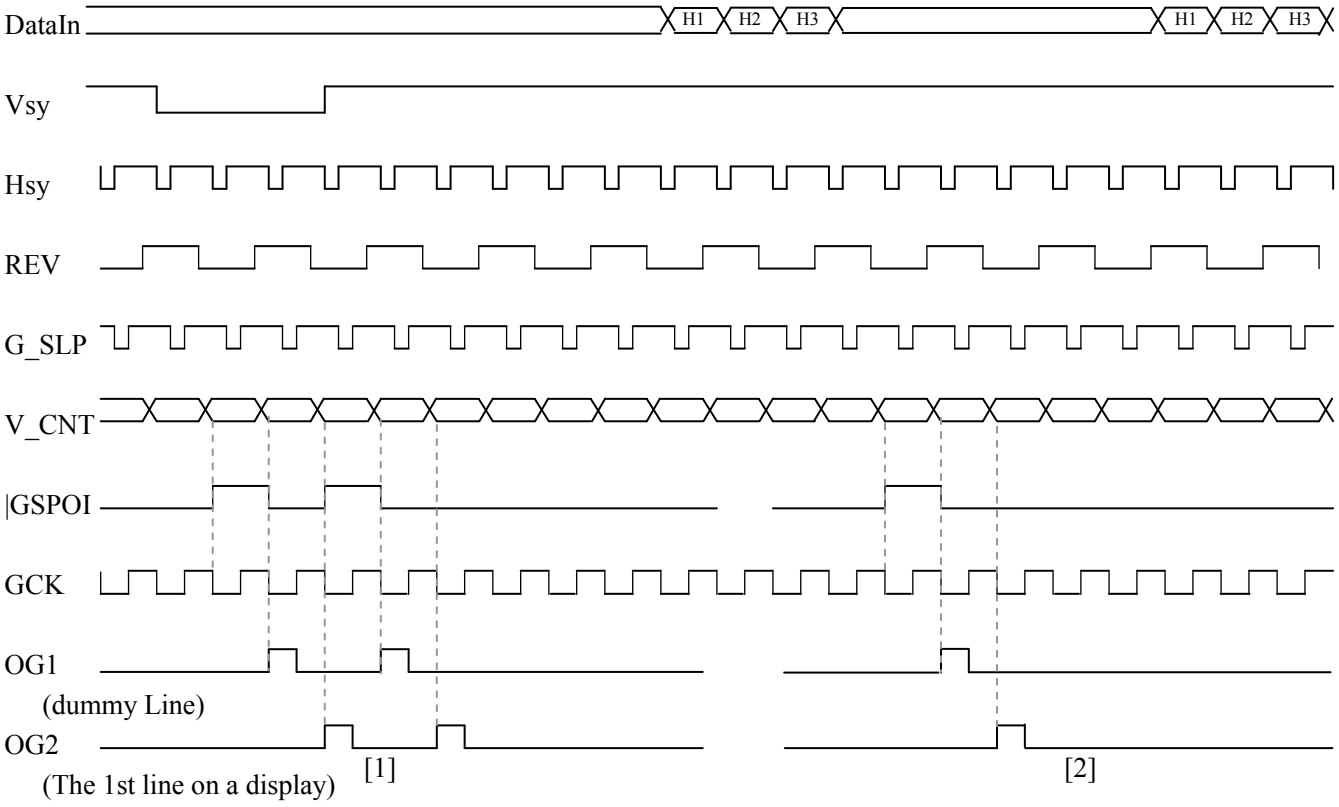


* In the chart above, [1] and [2] refer to the interlacing two-pulse mode and normal mode, respectively.

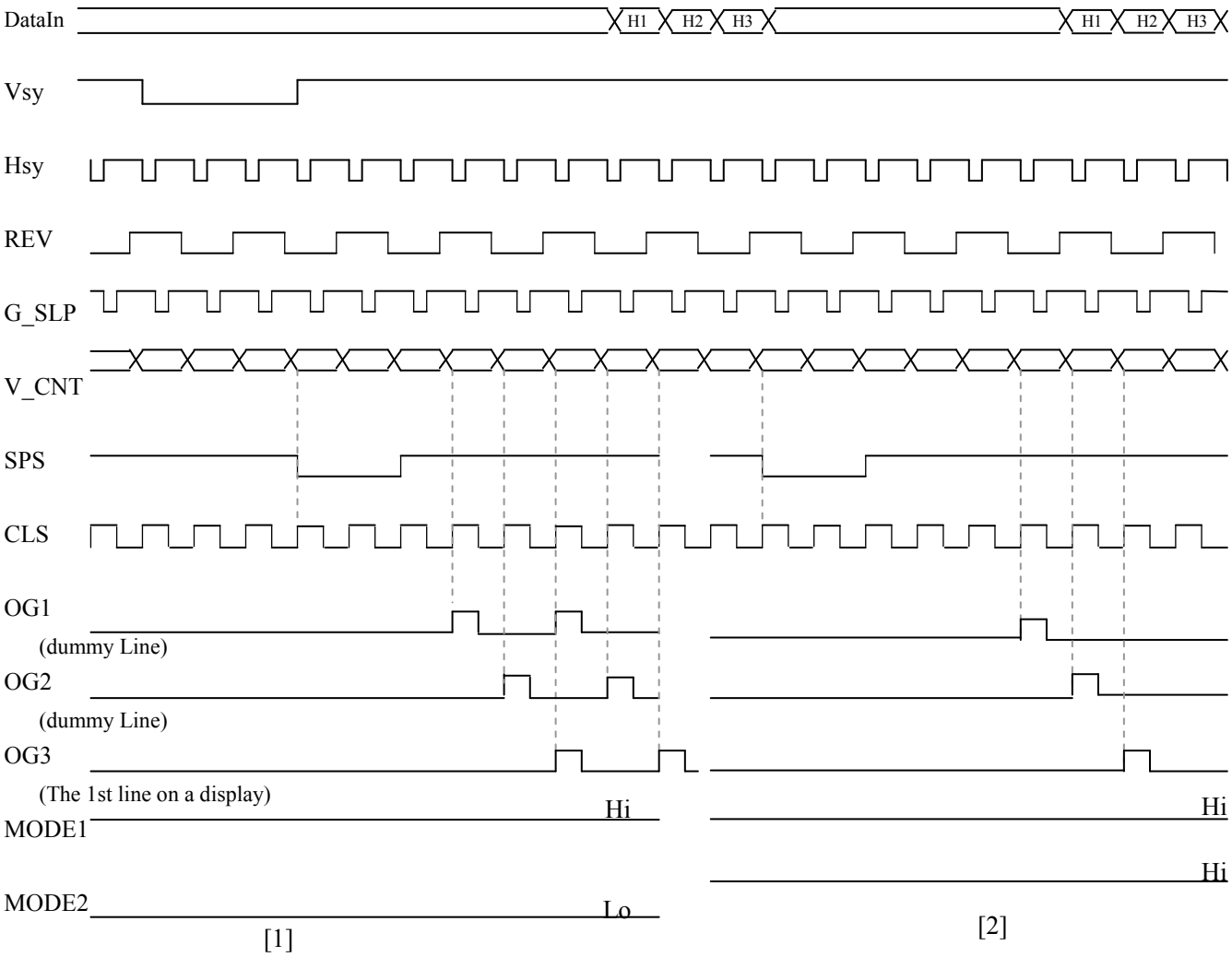
Figure 15-4: Vertical Timing Chart for Vertical Resolution 480 Lines (WVGA)

17.2.2. Vertical Timing for Vertical Resolution 240 Lines (WQVGA/WEGA2)

• For G_SEL = 0



• For G_SEL=1

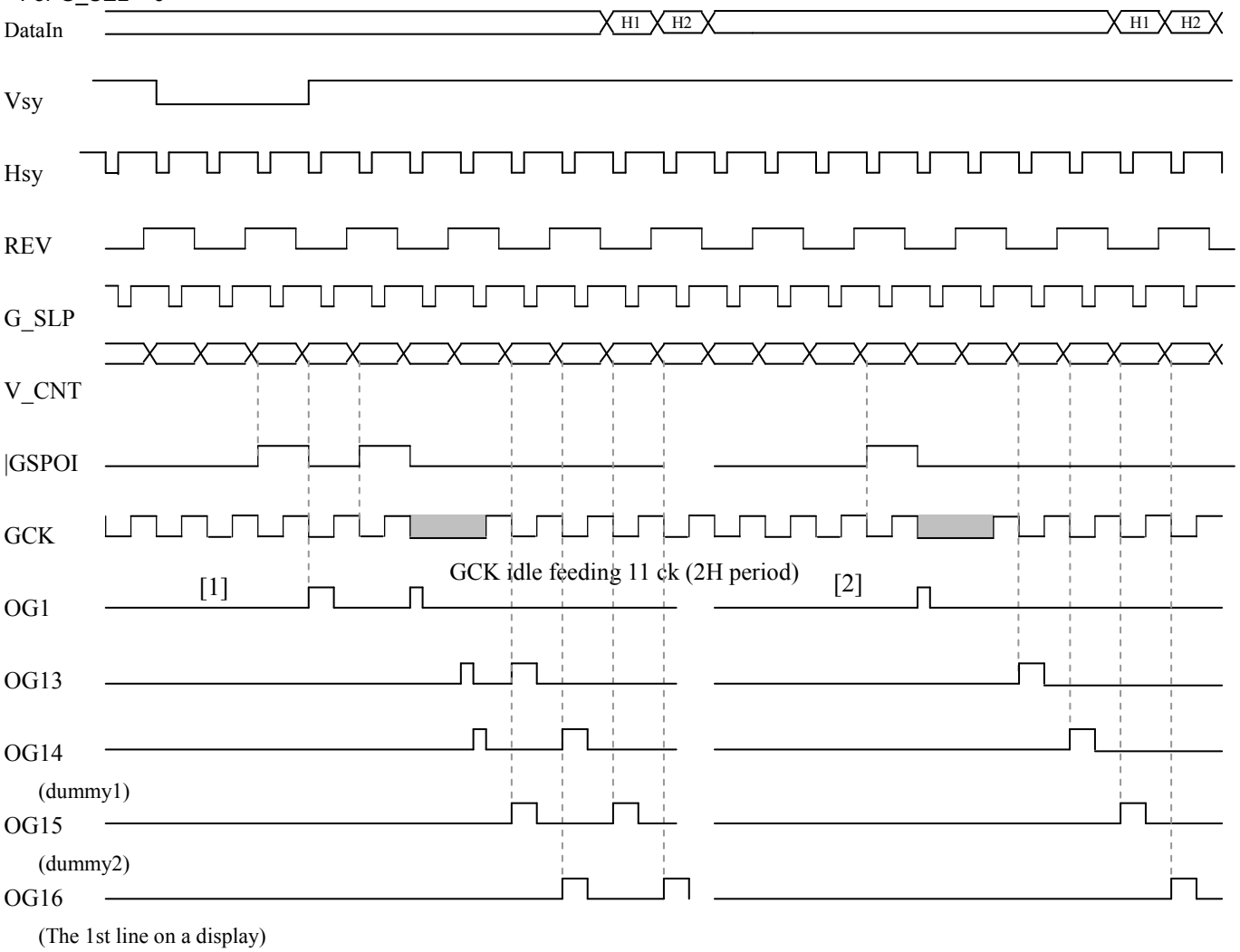


* In the chart above, [1] and [2] refer to the interlacing two-pulse mode and normal mode, respectively.

Figure 17-5: Vertical Timing Chart for Vertical Resolution 240 Lines (WQVGA/WEGA2)

17.2.3. Vertical Timing for Vertical Resolution 272 Lines (WEGA1)

• For G_SEL = 0



* In the chart above, [1] and [2] refer to the interlacing two-pulse mode and normal mode, respectively.

Figure 17-6: Vertical Timing Chart for Vertical Resolution 272 Lines (WEGA1)

18. Cautions on storage

18.1. Storage environment

To maintain the quality of semiconductor devices in storage, the storage environment must be controlled in terms of temperature and humidity and the presence of hazards such as corrosive gas,radioactive rays,and static electricity.

<1> Maintasin the storage site's temperature (Ta) within 5 to 30℃ and the humidity (RH) within 20 to 70%.
Also note the following points.
- •Use a humidifier in dry regions. In this case, use demineralized water of distilled water for humidifyin.
- •Avoid storing semiconductor devices in an overheated area, such as an area exposed to direct sunlight or near a heater, since overheated conditions may result in warping of product containers (magazines, etc).

<2> Store semiconductor devices in areas where temperatures do not fluctuate widely (such as in direct sunlight areas or dark areas), since rapid changes in temperature can cause moisture condensation on the devices.

<3> Store semiconductor devices in an area where the air is clean and free of excess salt, dust, or corrosive gases (such as exhaust gas, smoke, nitrous oxides, sulfur oxides, etc.).

<4> Store semiconductor devices in an area that where they will not undergo mechanical stresses such as vibration or shock.

<5> Store semiconductor devices in an area that where they will not be exposed to radioactive rays, static electricity, or strong magnetic fields.

<6> Points to check after opening a complete dry pack.
A humidity indicator card is included in dry pack packages. When moisture has been absorbed, the color of the card changes from blue to pink. If the card has changed to pink, the product may have absorbed moisture.So bake them before mounting.

18.2. Storage methods

Note the following cautions on semiconductor device storage methods in order to maintain the quality of semiconductor devices.

<1> Avoid stacking heavy items on top semiconductor device boxes since the devices may become damaged (cracks, bent leads, etc.). Since stacking boxes adds an undetermined amount of weight, avoid stacking heavy boxes on top of lighter boxes.

<2> Do not allow any vibration or shock that is strong enough to dent the exterior boxes.

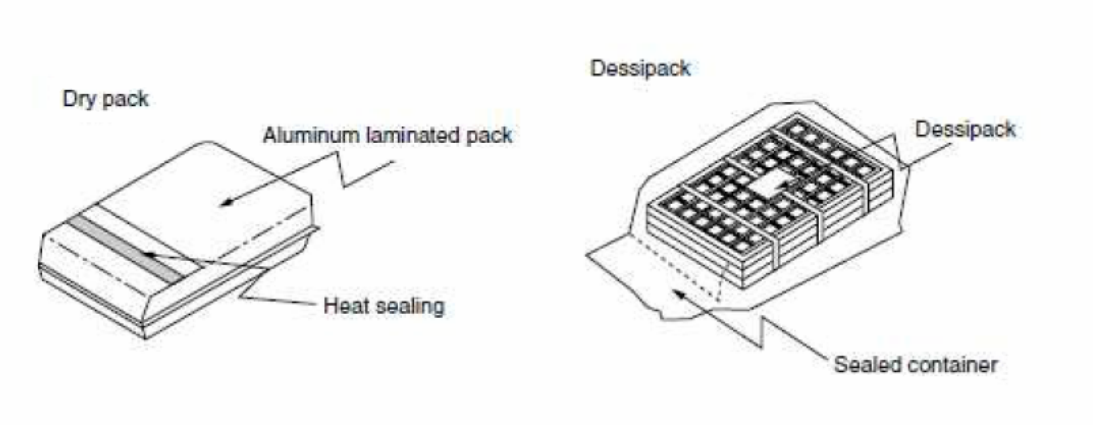
<3> Leave lead ends on external pins of semiconductor devices unprocessed to avoid defects that can occur during solder mounting due to rust, etc.

18.3. Long-term storage

When storing semiconductor devices for a long period (two years or longer), the following cautions should be noted in addition to the caution points mentioned for "18.1. Storage environment" and"18.2. Storage methods" above.

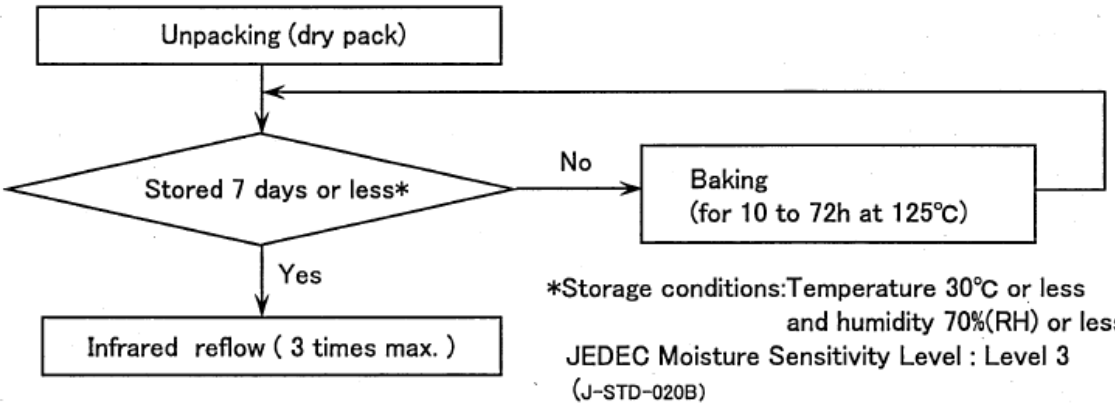
<1> If long-term storage is expected from the start, use either dry pack or a sealed container that also contains silica gel desiccant. After opening a dry pack package, put the contents back into a dry pack to ensure a long shelf life.

<2> If a long period (two years or longer) has elapsed for semiconductor devices that have been stored under in a normal storage environment and using normal storage methods, we recommend checking for solderability and rust on pins before using the semiconductor devices.



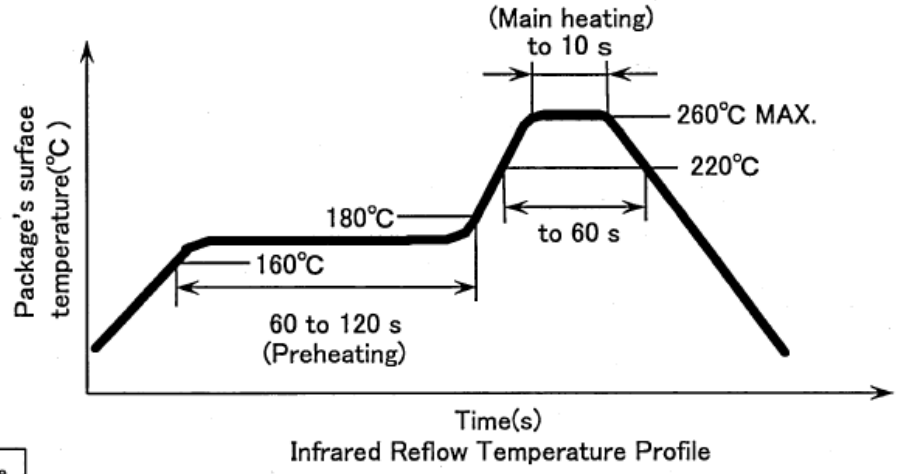
19. Recommended soldering condition of infrared reflow

The following is recommended soldering conditions of infrared reflow.



*Storage conditions:Temperature 30℃ or less
and humidity 70%(RH) or less
JEDEC Moisture Sensitivity Level : Level 3
(J-STD-020B)

Maximum temperature (Package's surface temperature)	: 260℃ or below
Time at maximum temperature	: 10s or less
Time of temperature higher than 220℃	: 60s or less
Preheating time at 160 to 180℃	: 60 to 120s
Maximum number of reflow processes	: 3 times
Maximum chlorine content of rosin flux (percentage mass)	: 0.2 % or less
Exposure limit (Store until the final reflow process starts)	: 7 days or less



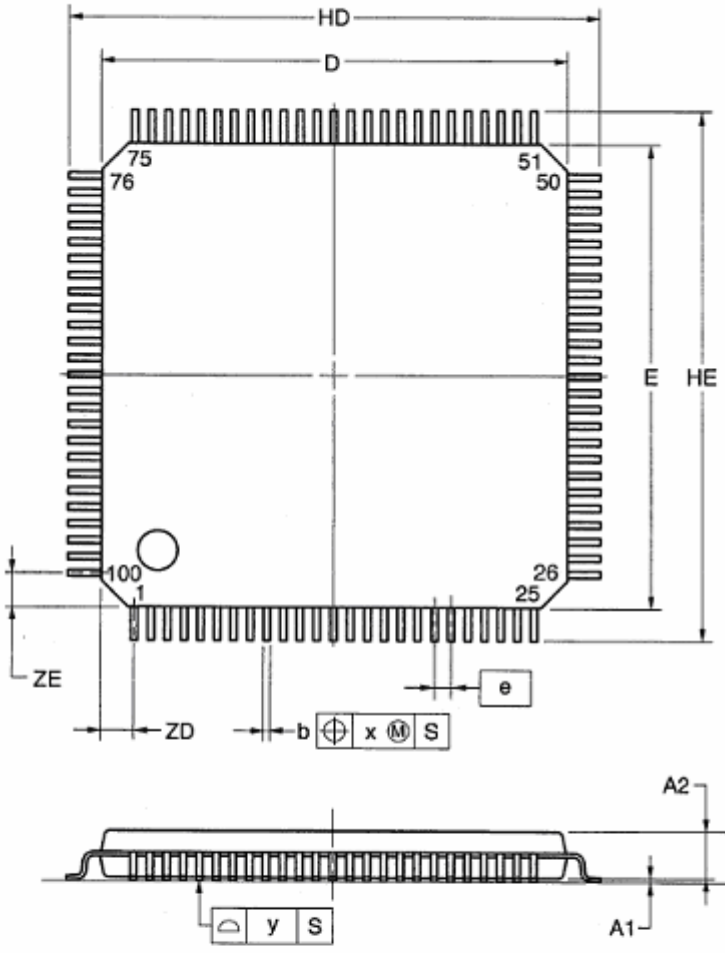
Infrared Reflow Temperature Profile

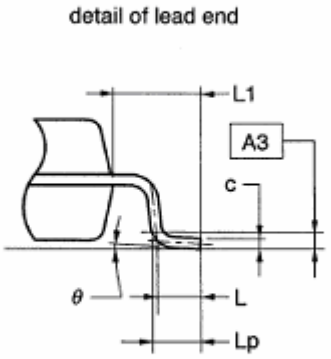
Notice

For baking components, it is necessary to use heatproof type container. Plastic magazines, emboss tape/reels and some of trays are not heatproof type, so if the packing container is not heatproof type, please transfer them to a heatproof type container.

20. Outline drawings

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)





(UNIT:mm)

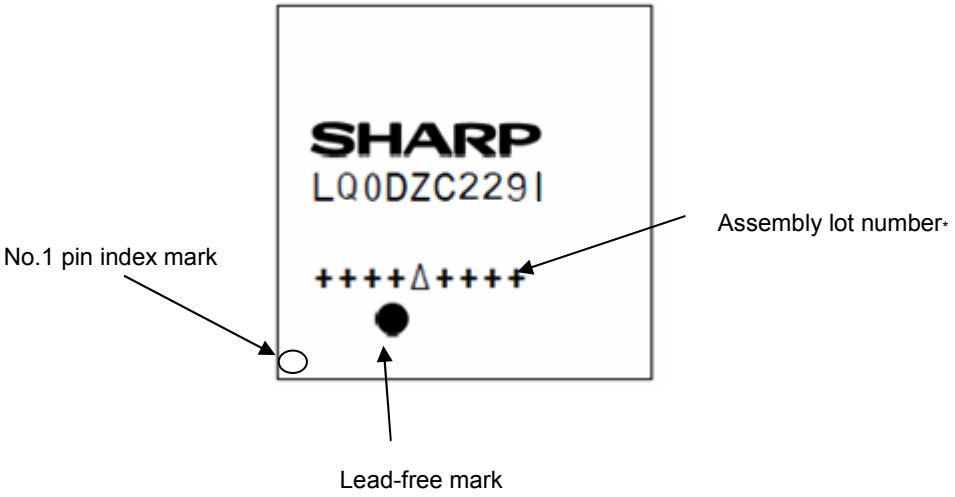
ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

P100GC-50-UEU-1

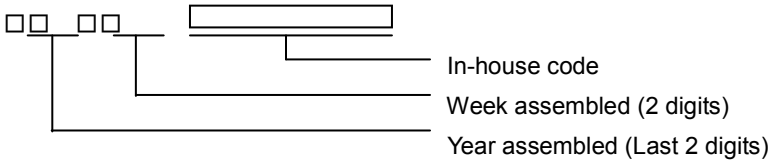
Outer Lead Plating: Ni-Pd-Au Plating

21. Marking

This marking drawing shows the marking items and layout of the contents, and does not specify the typeface size of precise position.

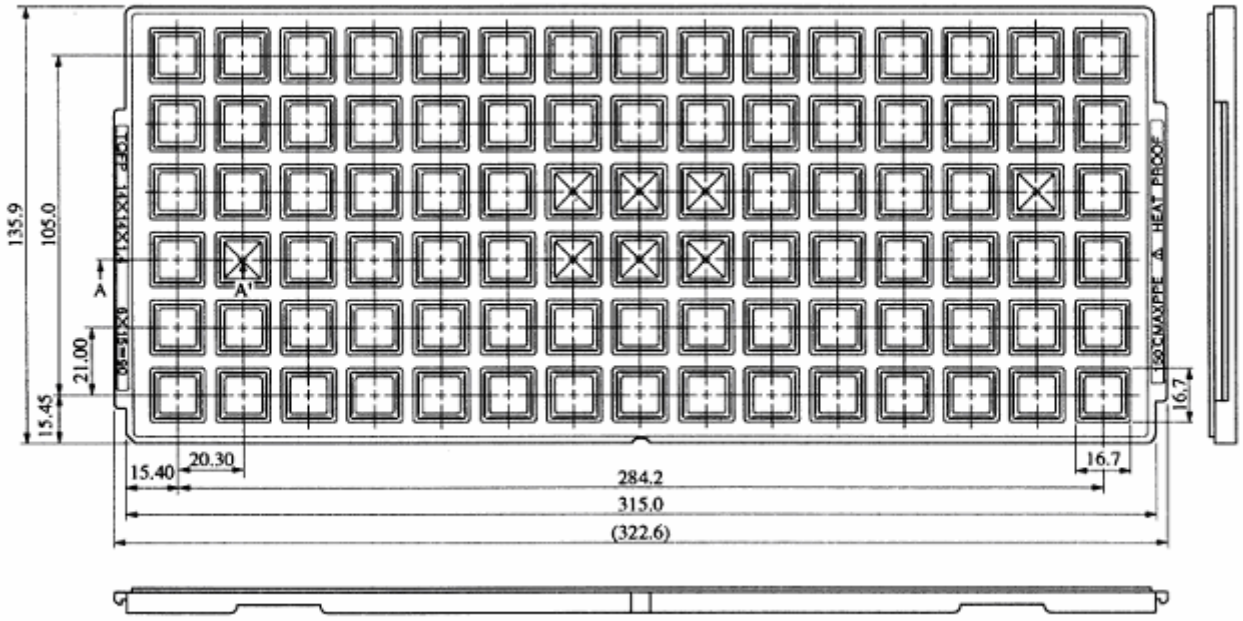


* Construction of lot number

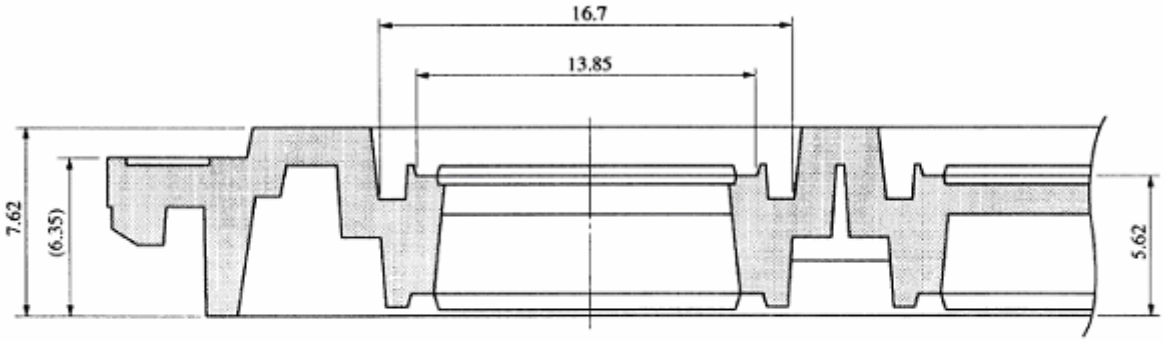


22. Tray container

Unit mm



SectionA - A'



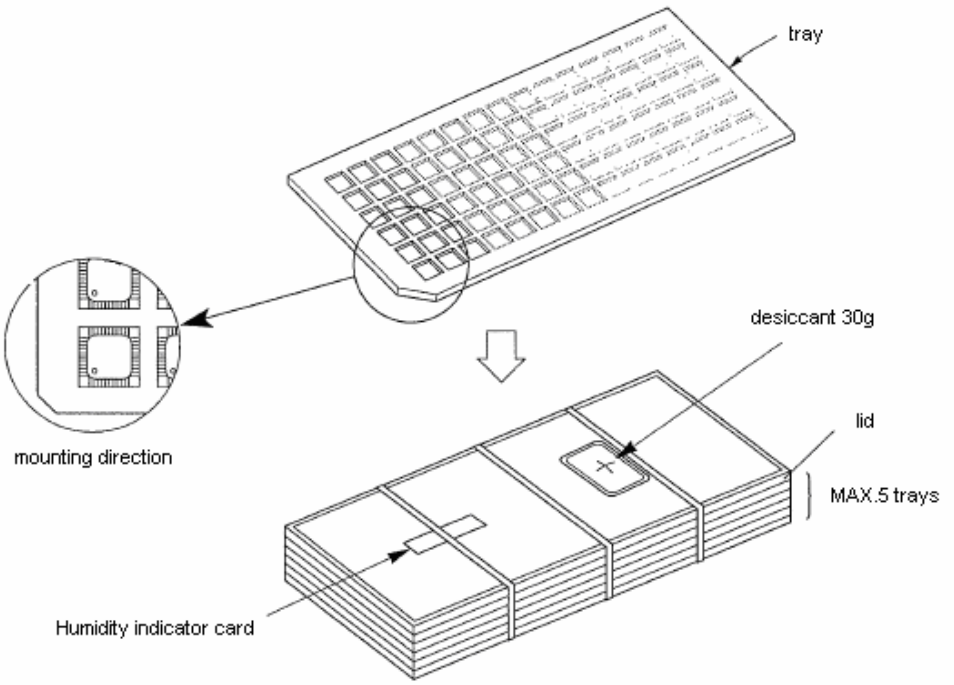
Applied Package	Quantity(pcs)
100-pin Plastic LQFP (1.4mm thick)	90 MAX

Tray	LQFP14 × 14 × 1.4
Material.	Carbon PPE
Heat Proof Temp	135℃ MAX.
Surface Resistance	Less than $1 \times 10^{13}\Omega$ /□

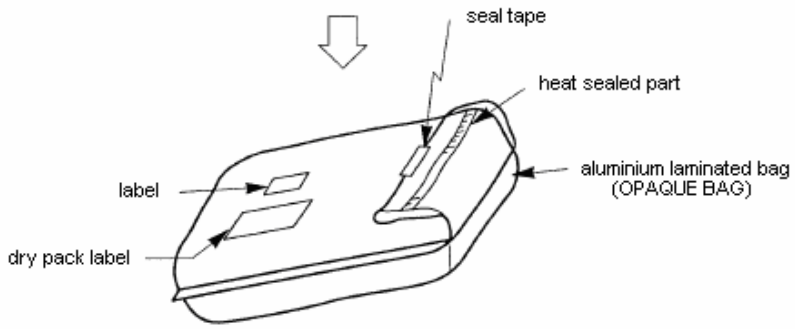
The tolerance of tray's dimensions are based on JEDEC STANDARD.

23.Packing outline drawing

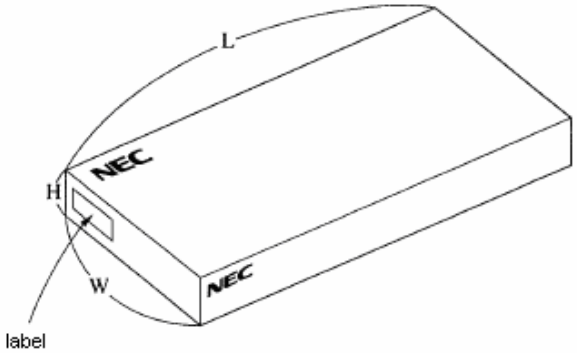
- Container



- Dry pack

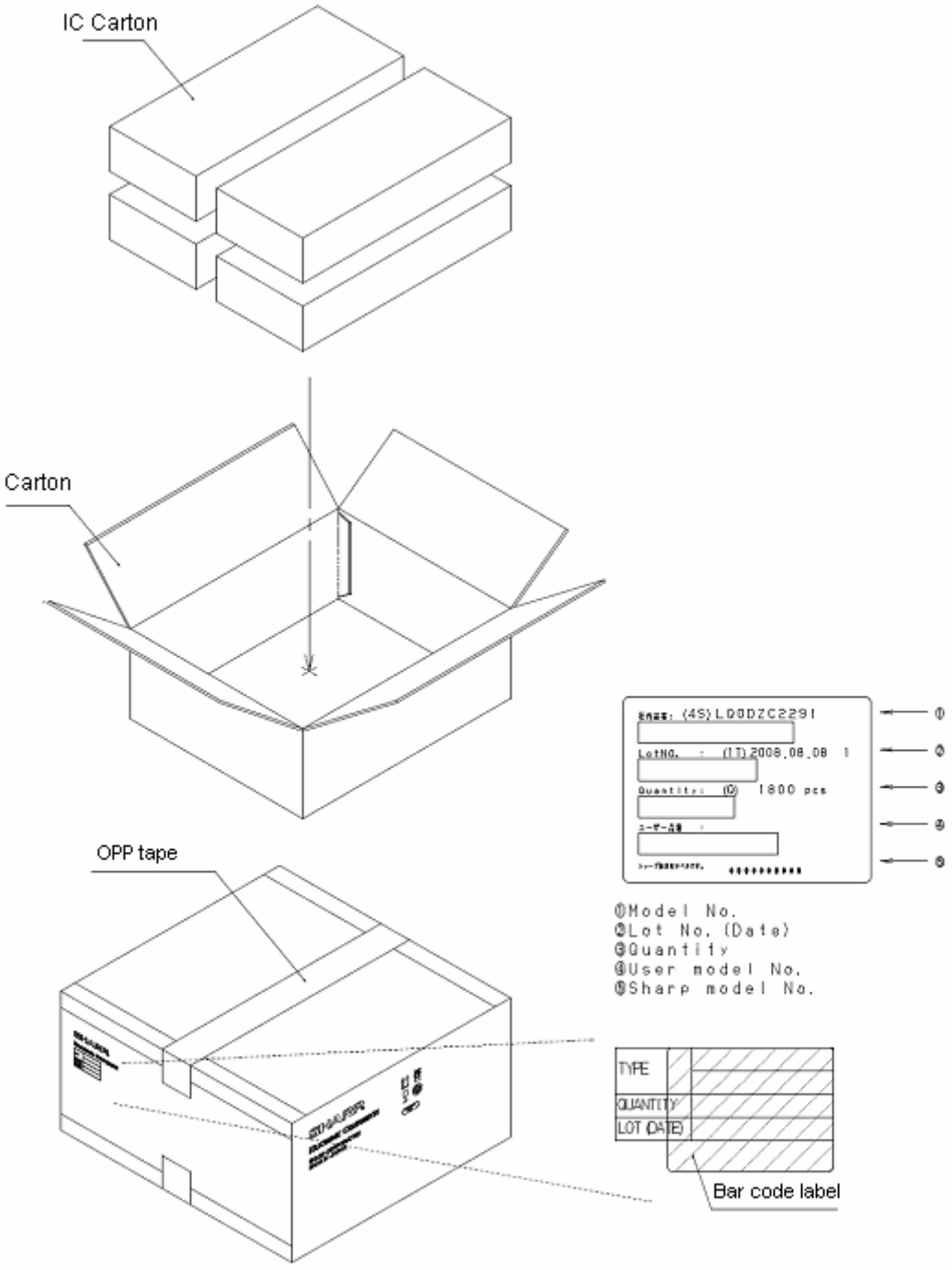


- Inner box



Label position	Side of box
Label	Product name, Quantity, Lot number, Class
Inner box	Dimension (W × L × H) 175 × 375 × 75 (mm)

24. Carton


IC Carton
Carton
OPP tape
①Model No.
②Lot No. (Date)
③Quantity
④User model No.
⑤Sharp model No.
TYPE
QUANTITY
LOT (DATE)
Bar code label