SC202A

3.5MHz, 500mA Step-down Regulator With Integrated Inductor and Digital Programmable Output

POWER MANAGEMENT

Features

- Input Voltage — 2.9V to 5.5V
- Output Voltage — 0.8V to 3.3V
- Output current capability — 500mA
- Internal inductor
- Programmable output voltages — 15
- High light-load efficiency via automatic PSAVE mode
- Fast transient response
- Temperature range — -40 to +85°C
- Oscillator frequency — 3.5MHz
- 100% duty cycle capability
- Quiescent current — 38µA typical
- Shutdown current — 0.1µA typical
- Internal soft-start
- Over-voltage protection
- Current limit and short circuit protection
- Over-temperature protection
- Under-voltage lockout
- Floating control pin protection
- MLPQ-13 — 2.5 x 3.0 x 1.0 (mm) package
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Point of load regulation
- Smart phones and cellular phones
- MP3/personal media players
- Personal navigation devices
- Digital cameras
- Single Li-ion cell or 3 NiMH/NiCd cell devices
- Devices with 3.3V or 5V internal power rails

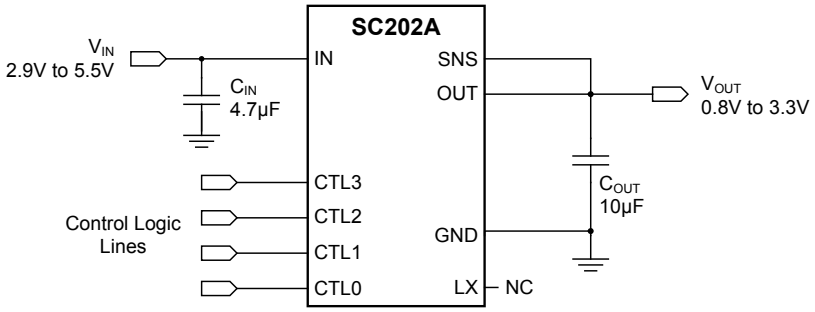
Description

The SC202A is a high efficiency 500mA step-down regulator that includes an integrated inductor inside the package. The input voltage range makes it ideal for battery operated applications with space limitations. The SC202A also includes 15 programmable output voltage settings that can be selected using the four control pins, eliminating the need for external feedback resistors. The output voltage can be fixed to a single setting or dynamically switched between different levels. Pulling all four control pins low disables the output.

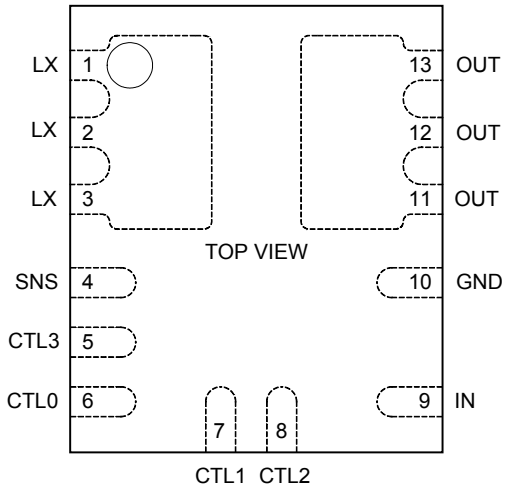
The SC202A operates at a fixed 3.5MHz switching frequency in normal PWM (Pulse-Width Modulation) mode. A variable frequency PSAVE (power-save) mode is used to optimize efficiency at light loads for each output setting. Built-in hysteresis prevents chattering between the two modes.

The SC202A provides several protection features. These include short circuit protection, over-temperature protection, under-voltage lockout, and soft-start to control in-rush current. These features, coupled with the small 2.5 x 3.0 x 1.0 (mm) package, make the SC202A a versatile device ideal for step-down regulation in products needing high efficiency and a small PCB footprint.

Typical Application Circuit



Pin Configuration



MLPQ-13; 2.5 x 3.0, 13 LEAD

θ_{JA} = 58°C/W

Ordering Information

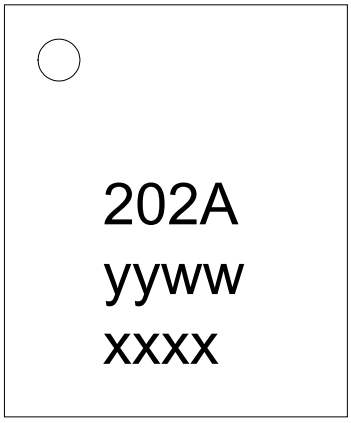
Device	Package
SC202AMLTRT(1)(2)	MLPQ-13 — 2.5 x 3.0
SC202AEVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



yyww = Date Code

xxxx = Semtech Lot Number

Table 1 – Output Voltage Settings

CTL3	CTL2	CTL1	CTL0	Vout
0	0	0	0	Shutdown
0	0	0	1	0.80
0	0	1	0	1.00
0	0	1	1	1.20
0	1	0	0	1.40
0	1	0	1	1.50
0	1	1	0	1.60
0	1	1	1	1.80
1	0	0	0	1.85
1	0	0	1	1.90
1	0	1	0	2.00
1	0	1	1	2.20
1	1	0	0	2.50
1	1	0	1	2.80
1	1	1	0	3.00
1	1	1	1	3.30

Absolute Maximum Ratings

IN (V) ..... -0.3 to +6.0
LX Voltage (V) ..... -1.0 to V_{IN} + 0.5
Other Pins (V) ..... -0.3 to V_{IN} + 0.3
Output Short Circuit to GND ..... Continuous
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Input Voltage Range (V) ..... +2.9 to +5.5
Operating Temperature Range (°C) ..... -40 to +85

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) 58
Junction Temperature Range (°C) ..... -40 to +150
Storage Temperature Range (°C) ..... -65 to +150

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB per JESD51 standards.

Electrical Characteristics

Unless otherwise specified: V_{IN}= 3.6V, C_{IN}=4.7µF, C_{OUT}=10µF, V_{OUT}=1.8V, $T_{J(MAX)}$=125°C, T_A= -40 to +85 °C. Typical values are T_A=+25 °C

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage Range	V_{OUT}		0.8		3.3 (1)	V
Output Voltage Tolerance	V_{OUT_TOL}	I_{OUT} = 200mA	-2.0		2.0	%
		PSAVE mode		1.5		
Line Regulation	$\Delta V_{LINEREG}$	2.9 ≤ V_{IN} ≤ 5.5V, I_{OUT} = 200mA		0.3		%/V
Load Regulation	$\Delta V_{LOADREG}$	200mA ≤ I_{OUT} ≤ 500mA		-1		%/A
Output Current Capability	I_{OUT}		500			mA
Current Limit Threshold	I_{LIMIT}		800		1300	mA
Foldback Current Limit	I_{FB_LIM}	I_{LOAD} > I_{LIMIT}		150		mA
Under-Voltage Lockout	V_{UVLO}	Rising V_{IN}			2.9	V
		Hysteresis		200		mV
Quiescent Current	I_Q	No switching, I_{OUT} = 0mA		38	60	µA
Shutdown Current	I_{SD}	$V_{CTL\ 0\text{-}3}$= 0V		0.1	1.0	µA
Output Leakage Current	I_{OUT}	Into OUT pin		0.1	1.0	µA
High Side Switch Resistance[2]	R_{DSON_P}	I_{OUT}= 100mA		250		mΩ
Low Side Switch Resistance[3]	R_{DSON_N}	I_{OUT}= 100mA		350		

Electrical Characteristics (continued)

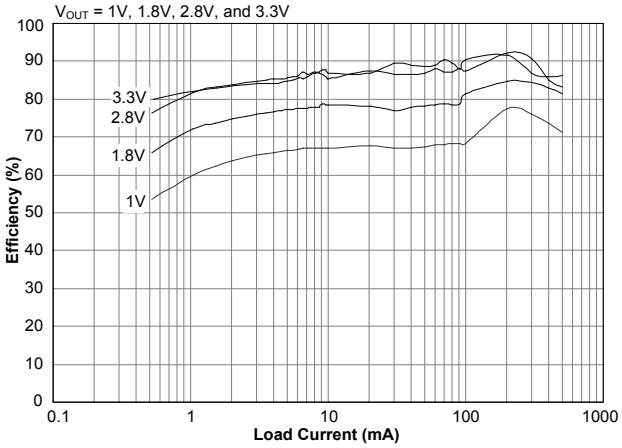
Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Frequency	f_{SW}		2.8	3.5	4.2	MHz
Soft-Start	t_{SS}	V_{OUT} = 90% of final value		100	500	µs
Thermal Shutdown	T_{OT}	Rising temperature		160		°C
Thermal Shutdown Hysteresis	T_{HYST}			20		°C
Logic Inputs - CTL0, CTL1, CTL2, and CTL3						
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.4	V
Input High Current	I_{IH}	$V_{CTL\ 0\text{-}3}$= V_{IN}	-2.0		5.0	µA
Input Low Current	I_{IL}	$V_{CTL\ 0\text{-}3}$= GND	-2.0		2.0	µA

Notes
(1) Maximum output voltage is limited to VIN if the input is less than 3.3V.
(2) Measured from IN to LX
(3) Measured from LX to GND

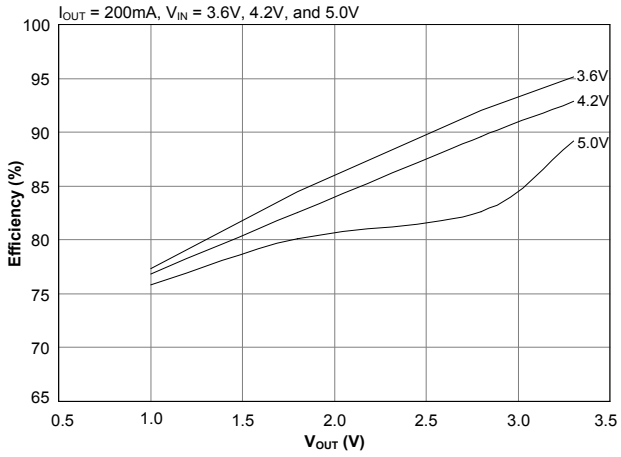
Typical Characteristics

V_{IN} = 4.0V for V_{OUT} = 3.3V, V_{IN} = 3.6V for all others. C_{IN} = 4.7µF, C_{OUT} = 10µF, T_A = 25°C unless otherwise noted.

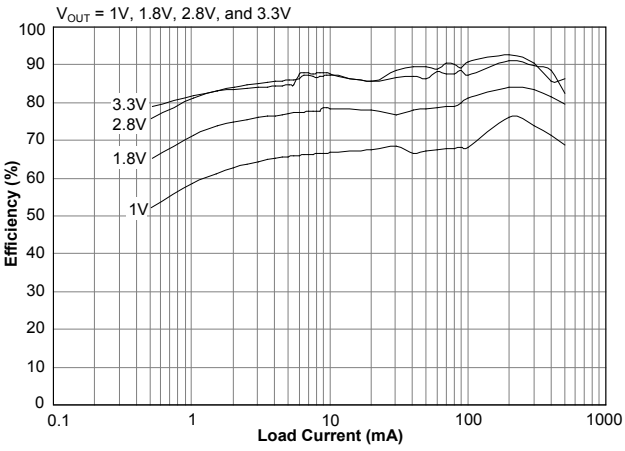
Efficiency vs. I_{OUT} (T_A = -40°C)



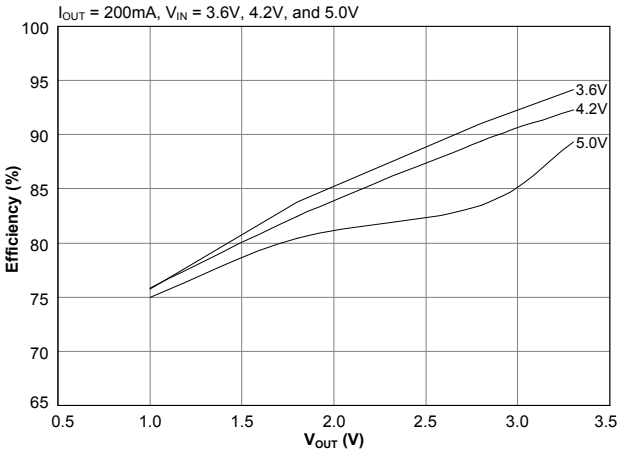
Efficiency vs. V_{OUT} (T_A = -40°C)



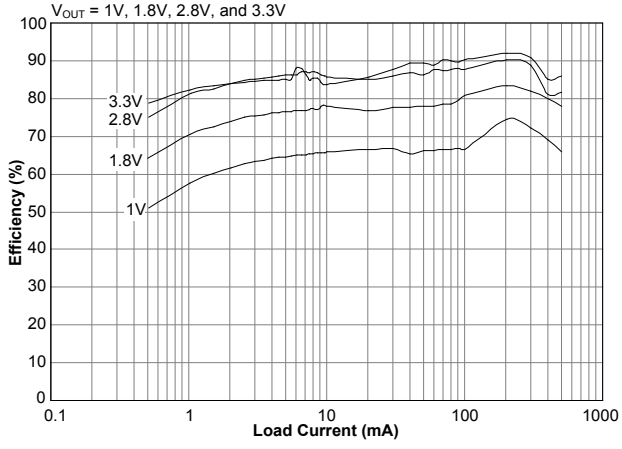
Efficiency vs. I_{OUT} (T_A = 25°C)



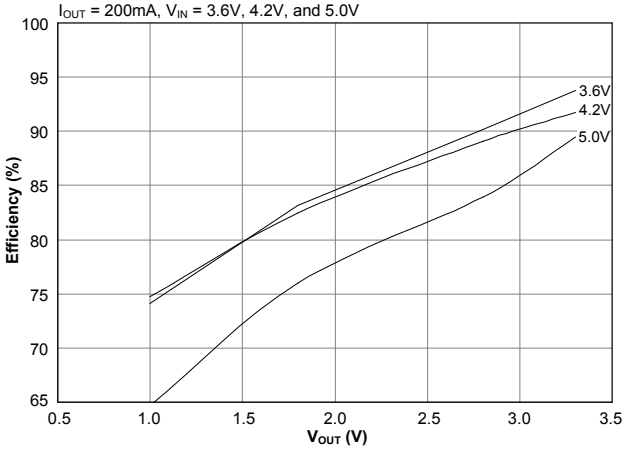
Efficiency vs. V_{OUT} (T_A = 25°C)



Efficiency vs. I_{OUT} (T_A = 85°C)



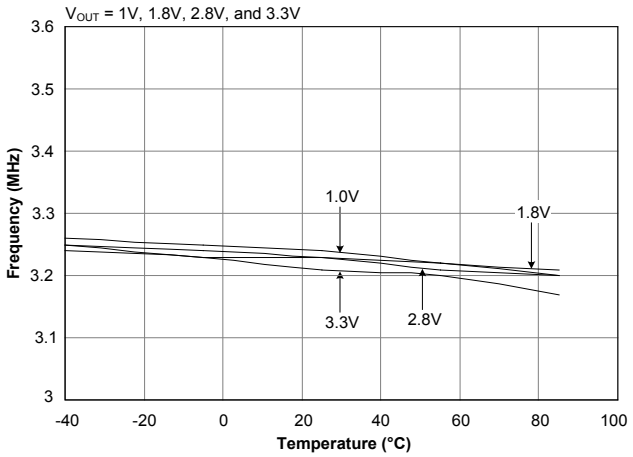
Efficiency vs. V_{OUT} (T_A = 85°C)



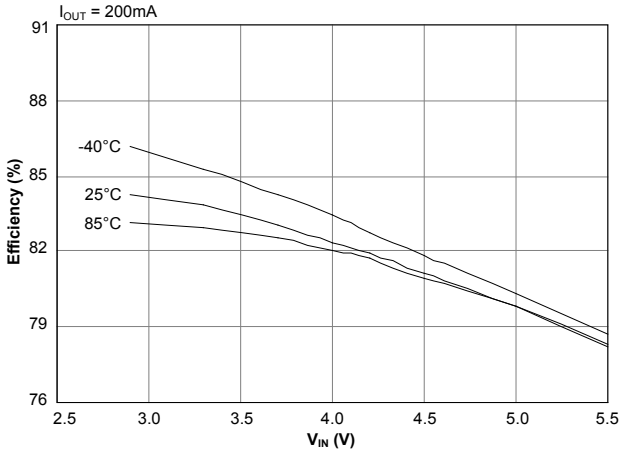
Typical Characteristics (continued)

V_{IN} = 4.0V for V_{OUT} = 3.3V, V_{IN} = 3.6V for all others. C_{IN} = 4.7µF, C_{OUT} = 10µF, T_A = 25°C unless otherwise noted.

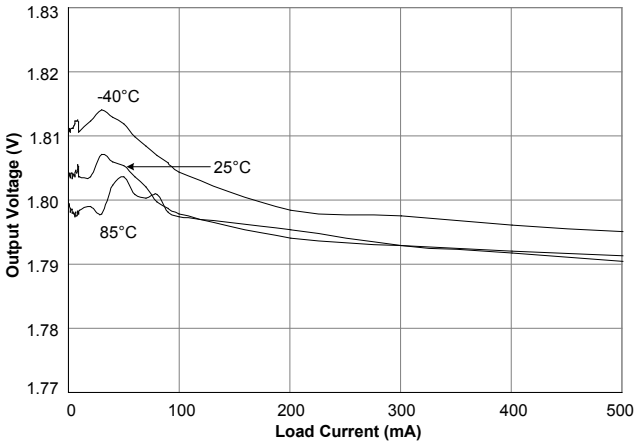
Frequency vs. Temperature



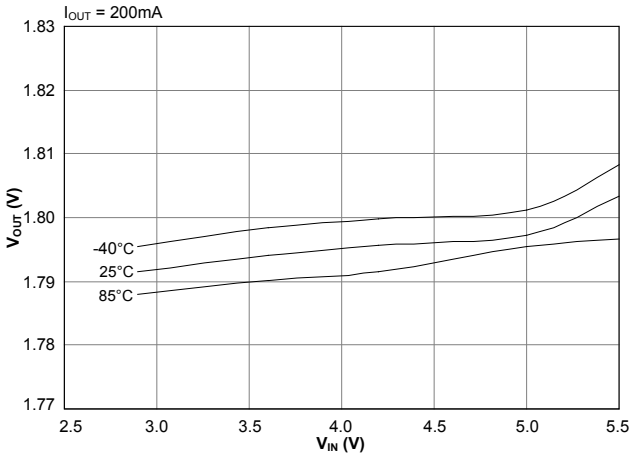
Efficiency vs. V_{IN} (V_{OUT}=1.8V)



Load Regulation (V_{OUT} = 1.8V)

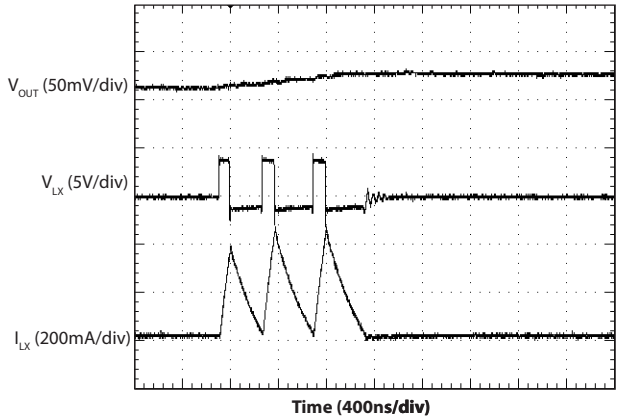


Line Regulation (V_{OUT}=1.8V)

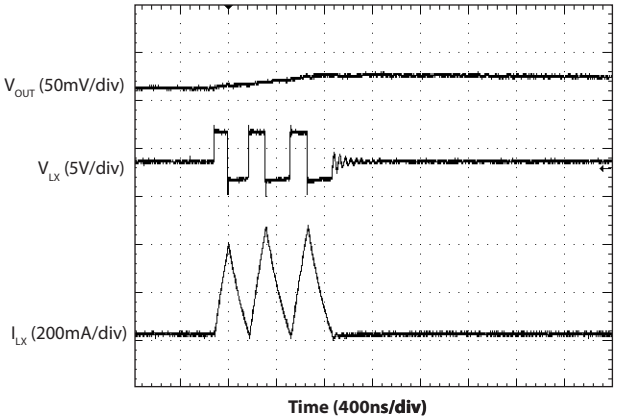


Typical Characteristics (continued)

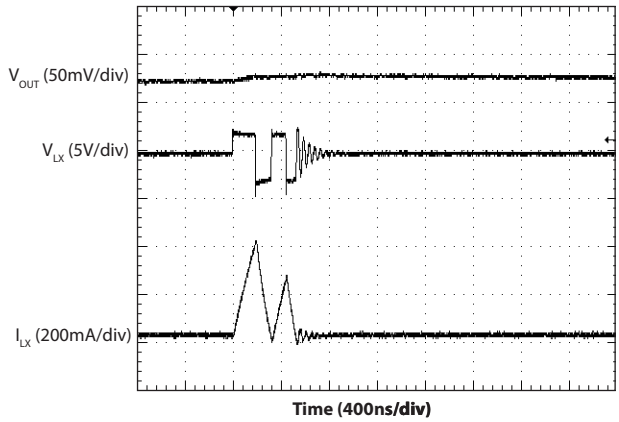
Light Load Switching — V_{OUT} = 1.0V



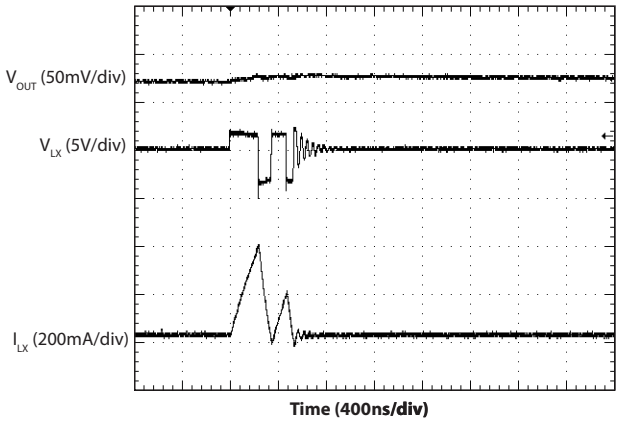
Light Load Switching — V_{OUT} = 1.8V



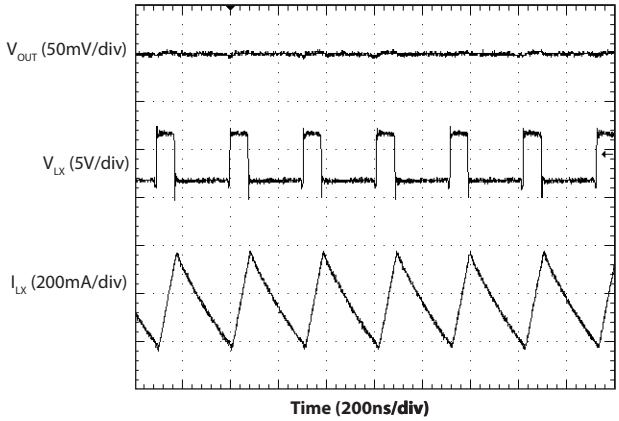
Light Load Switching — V_{OUT} = 2.8V



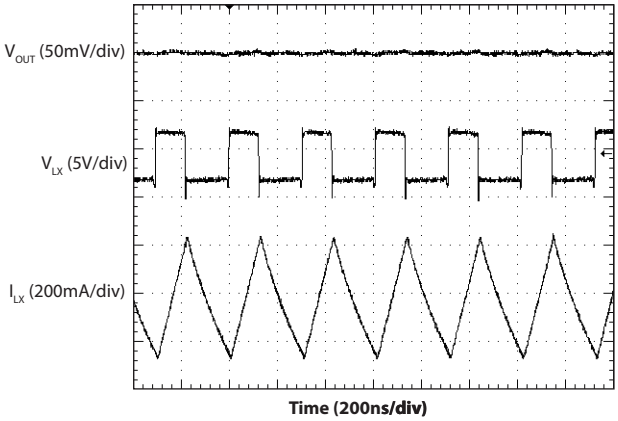
Light Load Switching — V_{OUT} = 3.3V



Heavy Load Switching — V_{OUT} = 1.0V

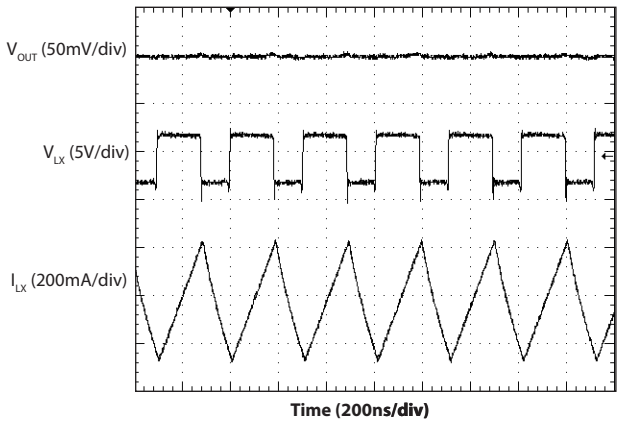


Heavy Load Switching — V_{OUT} = 1.8V

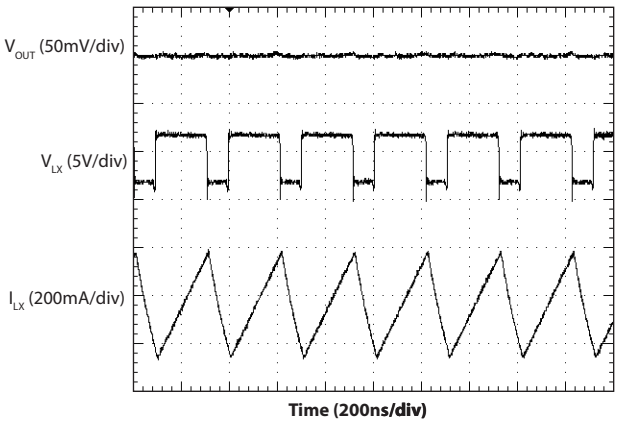


Typical Characteristics (continued)

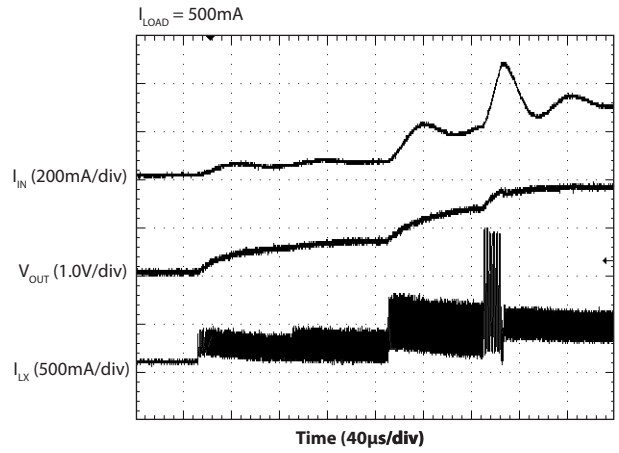
Heavy Load Switching — V_{OUT} = 2.8V



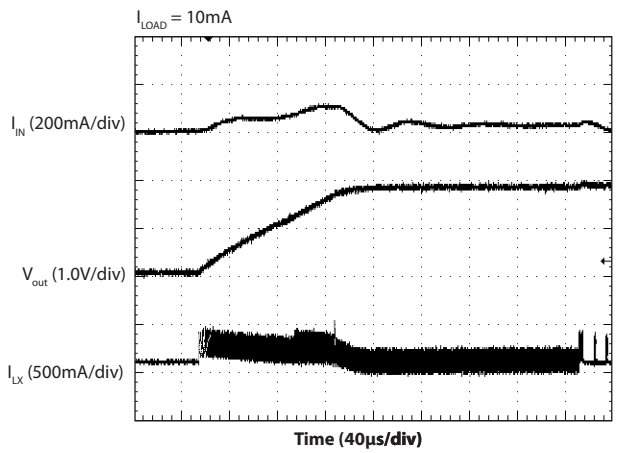
Heavy Load Switching — V_{OUT} = 3.3V



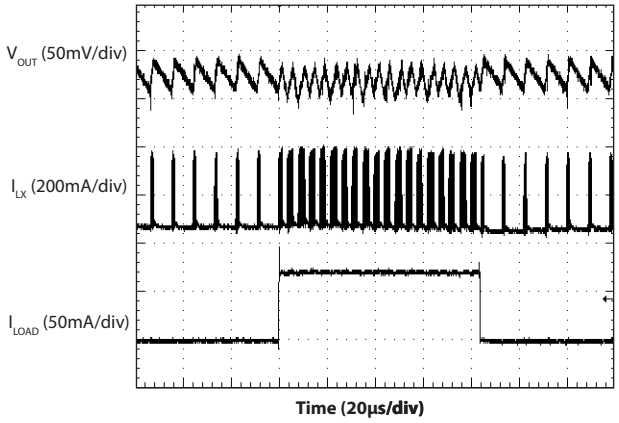
Heavy Load Soft-start



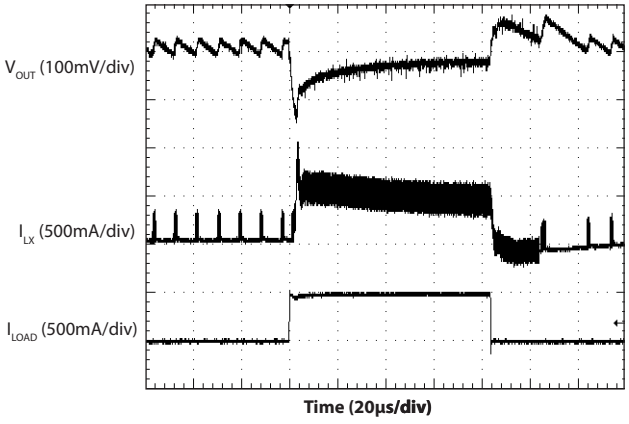
Light Load Soft-start



Load Transient Response — 25 to 90mA

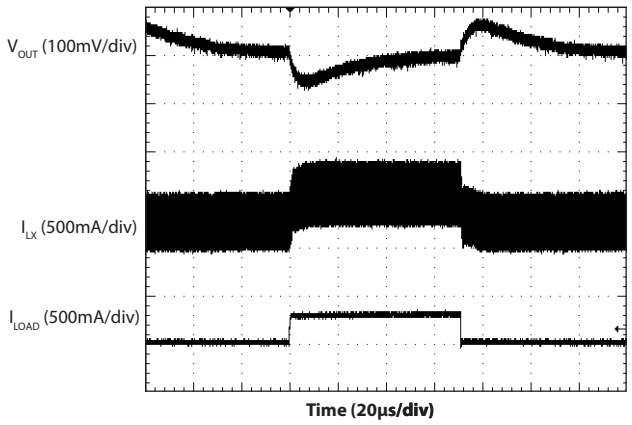


Load Transient Response — 25 to 500mA



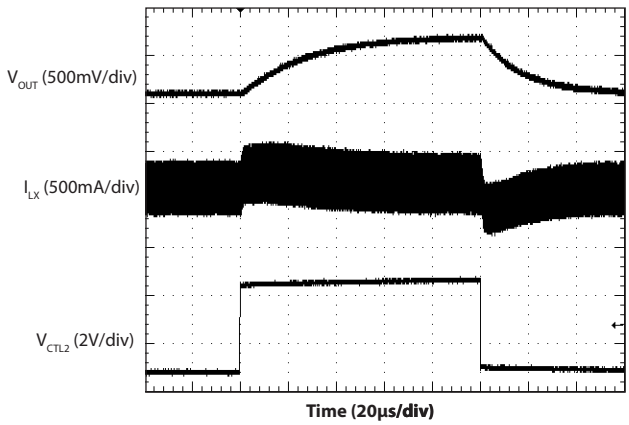
Typical Characteristics (continued)

Load Transient Response — 200 to 500mA



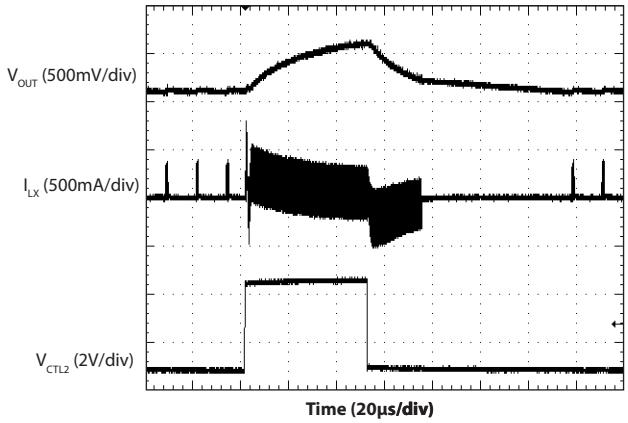
VID Transient Response — PWM

1.2V to 1.8V transition

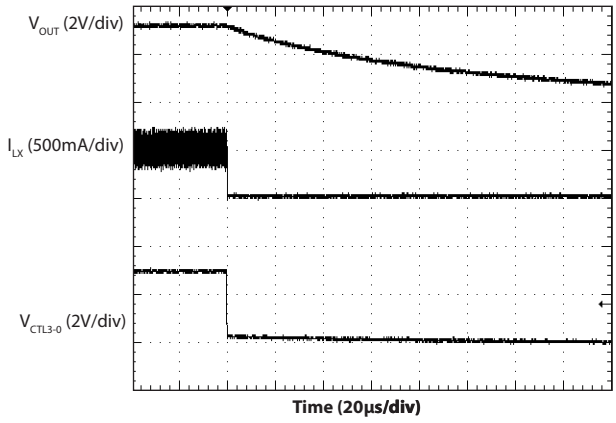


VID Transient Response — PSAVE

1.2V to 1.8V transition

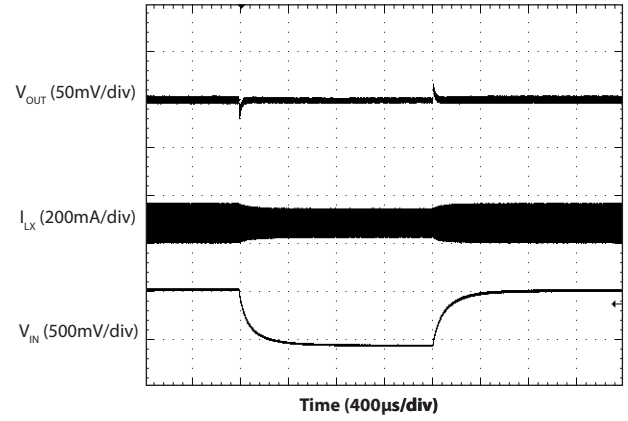


Shutdown Transient Response



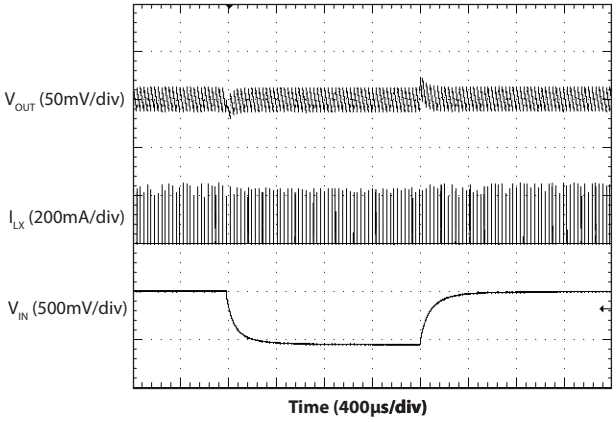
Line Transient Response — PWM

4.0V to 3.5V using Li-Ion battery



Line Transient Response — PSAVE

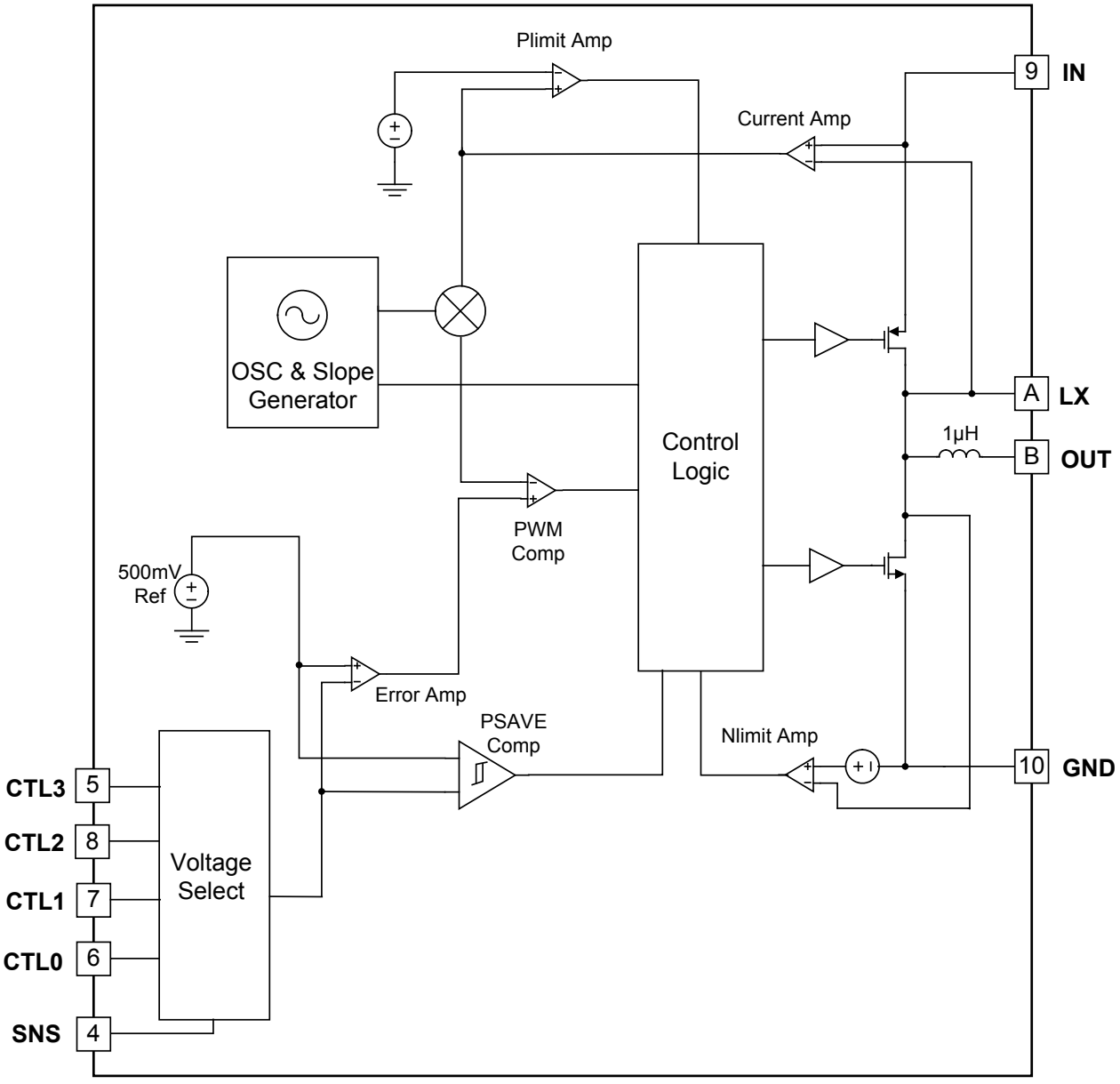
4.0V to 3.5V using Li-Ion battery



Pin Descriptions

Pin	Pin Name	Pin Function
1, 2, 3	LX	Switching node sense pin — for test purposes only
4	SNS	Output sense pin — connect to output capacitor for proper sensing of output voltage.
5	CTL3	Control bit 3 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL3 is pulled above the logic high threshold.
6	CTL0	Control bit 0 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL0 is pulled above the logic high threshold.
7	CTL1	Control bit 1 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL1 is pulled above the logic high threshold.
8	CTL2	Control bit 2 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL2 is pulled above the logic high threshold.
9	IN	Input power supply pin — connect a bypass capacitor from this pin to GND.
10	GND	Ground reference and power ground for the SC202A
11, 12, 13	OUT	Regulator output pin — connect a 10µF ceramic capacitor to this pin for proper filtering.

Block Diagram



A = pins 1, 2, 3
B = pins 11, 12, 13

Applications Information

General Description

The SC202A is a synchronous step-down PWM (Pulse Width Modulated) DC-DC regulator utilizing a 3.5MHz fixed-frequency voltage-mode architecture and an internal 1µH inductor. The device is designed to operate in fixed-frequency PWM mode and enter PSAVE (power save) mode utilizing pulse frequency modulation under light load conditions for maximizing efficiency. Two capacitors are the only external components required — one for input decoupling and one for output filtering. The output voltage is programmable, eliminating the need for external programming resistors. Loop compensation is also internal, eliminating the need for external components to control stability.

Programmable Output Voltage

The SC202A has 15 fixed output voltage levels which can be individually selected by programming the CTL control pins (CTL3-0 — see Table 1 on page 2 for settings). The device is disabled whenever all four CTL pins are pulled low and enabled whenever at least one of the CTL pins is pulled high. This configuration eliminates the need for a dedicated enable pin. Each CTL pin is internally pulled down via 1MΩ if V_{IN} is below 1.5V or if the voltage on the control pin is below the input high voltage. This ensures that the output is disabled when power is applied if there are no inputs to the CTL pins. Each weak pull-down is disabled whenever its pin is pulled high and remains disabled until all CTL pins are pulled low.

The output voltage can be set using different methods. If a static output voltage is required, the CTL pins can be tied to either IN or GND to set the desired voltage whenever power is applied at IN. If enable control is required, each CTL pin can be tied to either GND or to a microprocessor I/O line to create the desired control code whenever the control signal is forced high. This method is equivalent to using the CTL pins collectively as a single enable pin. A third option is to connect each of the four CTL pins to individual microprocessor I/O lines. Any of the 15 output voltages can be programmed using this method. If only two output voltages are needed, the CTL pins can be combined in a way that will reduce the number of I/O lines to 1, 2, or 3, depending on the control code for each desired voltage.

Dynamic Output Voltage Adjustment

Dynamically changing the CTL pins allows dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. This should done using specific procedures. Attention needs to be made so that applying all zeros in a very short period to the CTL pins when changing the output voltage will temporarily disable the device. Therefore it is important to avoid these combinations of all zero when dynamically changing the CTL levels. For example, when the CTLs change from 0001 to 0010 (0.8V to 1.2V), a transitional state of 0000 (shut down) state might occur in a very short period of time, which could result the device to be disabled unintentionally. In order to achieve such operation, the correct logic transition stages should be 001000110001 (1V1.2V0.8V). The 0011 (1.2V) state should be kept short to prevent from the 0000 state.

If the output voltage level is not within the specified the CTL voltage levels, the resistor divider ratio can be switched by a logic voltage level through an external MOSFET to achieve the dynamic output voltage transition.

Secondly, when the CTL pin is toggled for the output voltage to increase, the regulator will increase the inductor current and force the output voltage follow. When the CTL pin is toggled for the output voltage to decrease, the regulator will force the output voltage go down immediately (at heavy load conditions) when the device is in CCM. If the device is in DCM operation (the inductor current does not go negative) then the output voltage will go down as the load current drains the output capacitor.

Adjustable Output Voltage Selection

If an output voltage other than one of the 15 programmable settings is needed, an external resistor divider network can be added to the SC202A to adjust the output voltage setting. This network scales the output based on the resistor ratio and the programmed output setting.

Applications Information (continued)

The resistor values can be determined using the following equation.

$$V_{OUT} = V_{SET} \times \left[\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right] + I_{SNS} \times R_{FB1}$$

where V_{OUT} is the desired output voltage, V_{SET} is the voltage setting selected by the CTL pins, R_{FB1} is the resistor between the output capacitor and the SNS pin, R_{FB2} is the resistor between the SNS pin and ground, and I_{SNS} is the leakage current into the SNS pin during normal operation. The current into the SNS pin is typically 1µA, so the last term of the equation can be neglected if the current through R_{FB2} is much larger than 1µA. Selecting a resistor value of 10kΩ or lower will simplify the design. If I_{SNS} is neglected and R_{FB2} is fixed, R_{FB1} can be determined using the following equation.

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - V_{SET}}{V_{SET}}$$

Inserting resistance in the feedback loop will adversely affect the system's transient performance if feed-forward capacitance is not included in the circuit. The circuit in Figure 1 illustrates how the resistor divider and feed-forward capacitor can be added to the SC202A schematic.

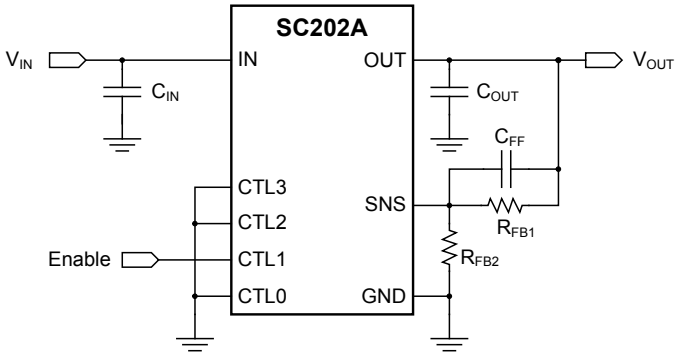


Figure 1 – Application Circuit with External Resistors

The value of feed-forward capacitance needed can be determined using the following equation.

$$C_{FF} = 4 \times 10^{-6} \times \frac{V_{SET}(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - V_{SET})(V_{SET} - 0.5)}$$

To simplify the design, it is recommended to program the output setting to 1.0V, use resistor values smaller than 10kΩ, and include a feed-forward capacitance calculated with the previous equation. If the output voltage is set to 1.0V, the previous equation reduces to the following equation.

$$C_{FF} = 8 \times 10^{-6} \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - 1)}$$

Example:

An output voltage of 1.3V is desired, but this is not a programmable option. What external component values for Figure 1 are needed?

Solution: To keep the circuit simple, set R_{FB2} to 10kΩ so current into the SNS pin can be neglected and set the CTL3-0 pins to 0010 (1.0V setting). The necessary component values for this situation are shown by the following equations.

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - V_{SET}}{V_{SET}} = 3k\Omega$$

$$C_{FF} = 8 \times 10^{-6} \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - 1)} = 5.69nF$$

PWM Operation

Normal PWM operation occurs when the output load current exceeds the PSAVE threshold. In this mode, the PMOS high side switch is activated with the duty cycle required to produce the output voltage programmed by the CTL pins. An internal synchronous NMOS rectifier eliminates the need for an external Schottky diode on the LX pin. The duty cycle (percentage of time PMOS is active) increases as V_{IN} decreases to maintain output voltage regulation. As the input voltage approaches the programmed output voltage, the duty cycle approaches 100% (PMOS always on) and the device enters a pass-through mode until the input voltage increases or the load decreases enough to allow PWM switching to resume.

Power Save Mode Operation

When the load current decreases below the PSAVE threshold, PWM switching stops and the device automatically enters PSAVE mode. This threshold varies depending on the input voltage and output voltage

Applications Information (continued)

setting, optimizing efficiency for all possible load currents in PWM or PSAVE mode. While in PSAVE mode, output voltage regulation is controlled by a series of switching bursts. During a burst, the inductor current is limited to a peak value which controls the on-time of the PMOS switch. After reaching this peak, the PMOS switch is disabled and the inductor current decreases to near 0mA. Switching bursts continue until the output voltage climbs to V_{OUT} +2.5% or until the PSAVE current limit is reached. Switching is then stopped to eliminate switching losses, enhancing overall efficiency. Switching resumes when the output voltage reaches the lower threshold of V_{OUT} and continues until the upper threshold again is reached. Note that the output voltage is regulated hysteretically while in PSAVE mode between V_{OUT} and V_{OUT} + 2.5%. The period and duty cycle while in PSAVE mode are solely determined by V_{IN} and V_{OUT} until PWM mode resumes. This can result in the switching frequency being much lower than the PWM mode frequency.

If the output load current increases enough to cause V_{OUT} to decrease below the PSAVE exit threshold (V_{OUT} -2%), the device automatically exits PSAVE and operates in continuous PWM mode. Note that the PSAVE high and low threshold levels are both set at or above V_{OUT} to minimize undershoot when the SC202A exits PSAVE. Figure 2 illustrates the transitions from PWM mode to PSAVE mode and back to PWM mode.

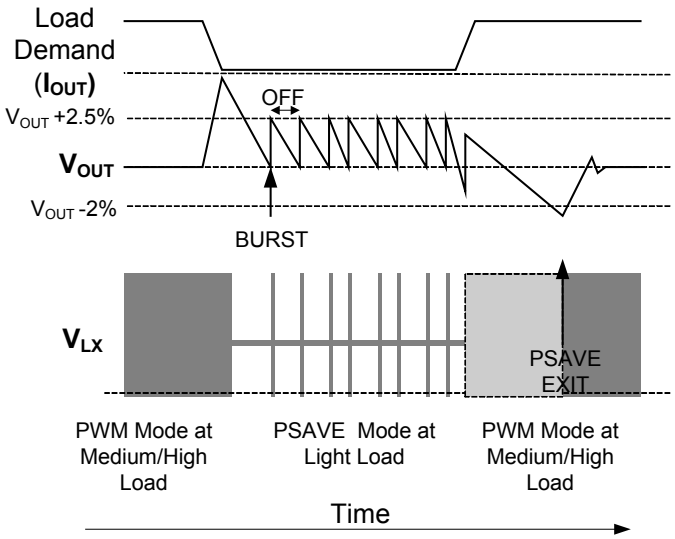


Figure 2 — Transitions Between PWM and PSAVE Modes

Protection Features

The SC202A provides the following protection features:

- Soft-Start Operation
- Over-Voltage Protection
- Current Limit
- Thermal Shutdown
- Under-Voltage Lockout

Soft-Start

The soft-start sequence is activated after a transition from an all zeros CTL code to a non-zero CTL code enables the device. At start-up, the PMOS current limit is stepped through four levels: 25%, 40%, 60%, and 100%. Each step is maintained for 60µs following an internal reference start up of 20µs, resulting in a total nominal start-up period of 260µs. If V_{OUT} reaches 90% of the target within the first 2 steps, the device continues in PSAVE mode at the end of soft-start; otherwise, it goes into PWM mode. Note the V_{OUT} ripple in PSAVE mode can be larger than the ripple in PWM mode.

Over-Voltage Protection

Over-voltage protection ensures the output voltage does not rise to a level that could damage its load. When V_{OUT} exceeds the regulation voltage by 15%, the PWM drive is disabled. Switching does not resume until V_{OUT} has fallen below the regulation voltage by 2%.

Current Limit

The SC202A switching stage is protected by a current limit function. If the output load exceeds the PMOS current limit for 32 consecutive switching cycles, the device enters fold-back current limit mode and the output current is limited to approximately 150mA. Under these conditions, the output voltage will be the product of I_{FB-LIM} and the load resistance. The load must fall below I_{FB-LIM} for the device to exit fold-back current limit mode. This function makes the device capable of sustaining an indefinite short circuit on its output under fault conditions.

Thermal Shutdown

The SC202A has a thermal shutdown feature to protect the device if the junction temperature exceeds 160°C. During thermal shutdown, the PMOS and NMOS switches are both disabled, tri-stating the LX output. When the junction temperature drops by the hysteresis value (20°C),

Applications Information (continued)

the device goes through the soft-start process and resumes normal operation.

Under-Voltage Lockout

UVLO (Under-Voltage Lockout) activates when the supply voltage drops below the falling UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 200mV is included to prevent chattering near the threshold.

C_{OUT} Selection

The internal voltage loop compensation in the SC202A limits the minimum output capacitor value to 10µF. This is due to its influence on the the loop crossover frequency, phase margin, and gain margin. Increasing the output capacitor above this minimum value will reduce the crossover frequency and provide greater phase margin.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

In addition to ensuring stability, the output capacitor serves other important functions. This capacitor determines the output voltage ripple — as capacitance increases, ripple voltage decreases. It also supplies current during a large load step for a few switching cycles until the control loop responds (typically 3 switching cycles). Once the loop responds, regulation is restored and the desired output is reached. During the period prior to PWM operation resuming, the relationship between output voltage and output capacitance can be approximated using the following equation.

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f}$$

This equation can be used to approximate the minimum output capacitance needed to ensure voltage does not droop below an acceptable level. For example, a load step from 50mA to 400mA requiring droop less than 50mV would require the minimum output capacitance as shown by the following equation.

$$C_{OUT} = \frac{3 \times 0.4}{0.05 \times 3.5 \times 10^{6}} = 6.0\mu F$$

In this example, using a standard 10µF capacitor would be adequate to keep voltage droop less than the desired limit. Note that if the voltage droop limit were decreased from 50mV to 25mV, the output capacitance would need to be increased to at least 12µF (twice as much capacitance for half the droop). Capacitance will decrease from the nominal value when a ceramic capacitor is biased with a DC current, so it is important to select a capacitor whose value exceeds the necessary capacitance value at the programmed output voltage. Check the manufacturer's capacitance vs. DC voltage graphs when selecting an output capacitor to ensure the capacitance will be adequate.

Table 2 lists the manufacturers of recommended output capacitor options.

Table 2 — Recommended Output Capacitors

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J106ME47D	10±20%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM21BR60J106K	10±10%	X5R	6.3	2.0x1.25x1.25 0805
Taiyo Yuden JMK107BJ106MA-T	10±20%	X5R	6.3	1.6x0.8x0.8 0603
TDK C1608X5R0J106MT	10±20%	X5R	6.3	1.6x0.8x0.8 0603

C_{IN} Selection

The SC202A input source current will appear as a DC supply current with a triangular ripple imposed on it. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 4.7µF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. For example, a 10µF, 6.3V, X5R ceramic capacitor with 5V DC applied may exhibit a capacitance as low as 4.5µF. The value of required input capacitance is estimated by determining the acceptable input ripple voltage and

Applications Information (continued)

calculating the minimum value required for C_{IN} using the following equation.

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{\Delta V}{I_{OUT}}-ESR\right)f}$$

The input voltage ripple is at maximum level when the input voltage is twice the output voltage (50% duty cycle scenario).

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimize stray inductance, the capacitor should be placed as close as possible to the IN and GND pins. Table 3 lists recommended input capacitor options from different manufacturers.

Table 3 — Recommended Input Capacitors

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J475K	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM188R60J106K	10±10%	X5R	6.3	1.6x0.8x0.8 0603
Taiyo Yuden JMK107BJ475KA	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
TDK C1608X5R0J475KT	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603

PCB Layout Considerations

The layout diagram in Figure 3 shows a recommended PCB top-layer for the SC202A and supporting components. Specified layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can also result.

The following guidelines are recommended for designing a PCB layout:

1. C_{IN} should be placed as close to the IN and GND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to minimize trace impedance. This will also minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. C_{OUT} should be connected as closely as possible to the OUT pin.
3. Use a ground plane referenced to the GND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
4. Route the output voltage feedback/sense trace (connected to the SNS pin) away from the LX node as shown in Figure 3 to minimize noise and magnetic interference.
5. Minimize the resistance from the OUT and GND pins to the load. This will reduce errors in DC regulation due to voltage drops in the traces.
6. The two smaller exposed pads on this package should not be connected to any traces. The area beneath these two pads must be kept clear so that they do not make electrical contact with any traces, including ground.

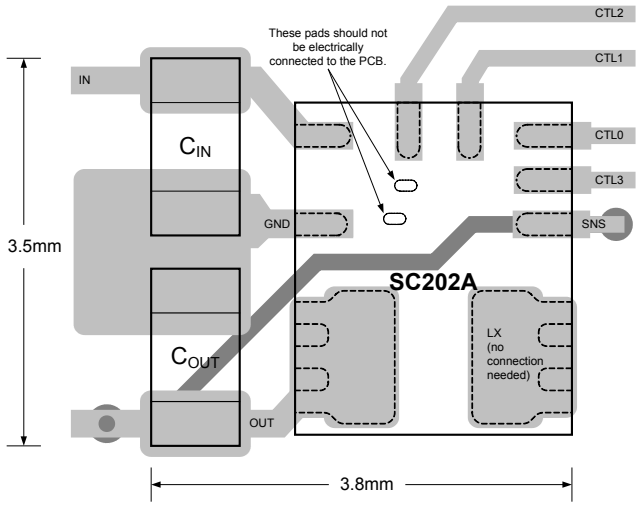
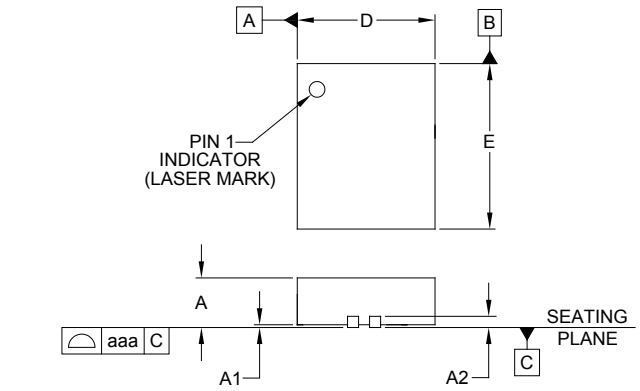
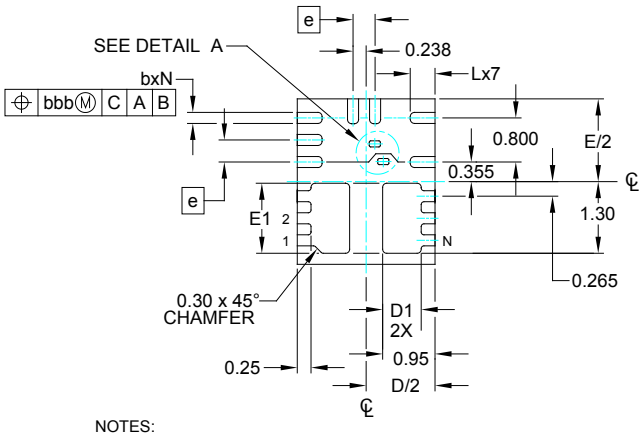


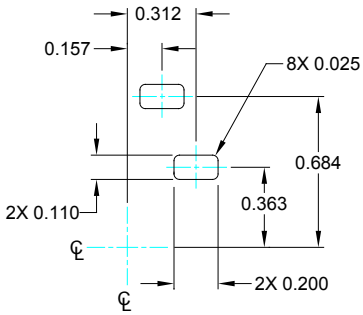
Figure 3 — Recommended PCB Layout

Outline Drawing — MLPQ-13



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	-	1.00
A1	0.00	-	0.05
A2	-	(0.20)	-
b	0.15	0.20	0.25
D	2.40	2.50	2.60
D1	0.60	0.70	0.75
E	2.90	3.00	3.10
E1	1.17	1.27	1.32
e	0.40 BSC		
L	0.40	0.45	0.50
N	13		
aaa	0.08		
bbb	0.10		



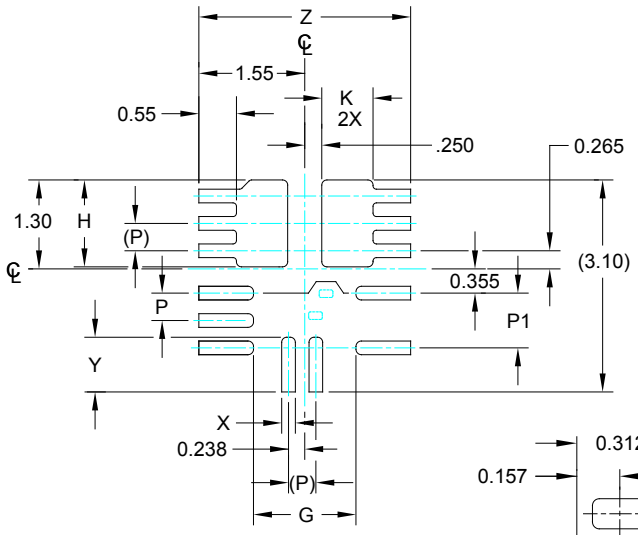


DETAIL A
SCALE: 4/1

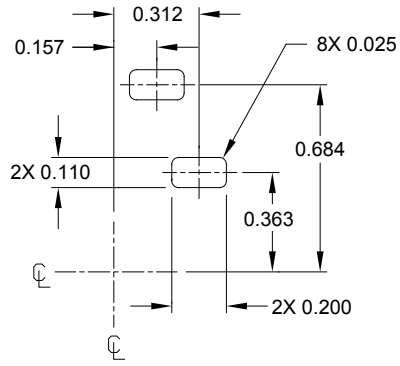
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-13



DIMENSIONS	
DIM	MILLIMETERS
G	1.50
H	1.27
K	0.75
P	0.40
P1	0.80
X	0.20
Y	0.80
Z	3.10



SMALL EXPOSED PADS LOCATION

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. LAND PATTERNS (SOLDER PADS) NOT REQUIRED FOR SMALLER EXPOSED PADS.
4. DO NOT PLACE EXPOSED TRACES OR VIAS UNDER SMALLER EXPOSED PADS.

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