

# MC74VHC540

## Octal Bus Buffer

### Inverting

The MC74VHC540 is an advanced high speed CMOS inverting octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC540 features inputs and outputs on opposite sides of the package and two AND-ed active-low output enables. When either  $\overline{OE1}$  or  $\overline{OE2}$  are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

#### Features

- High Speed:  $t_{PD} = 3.7$  ns (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 4.0$   $\mu$ A (Max) at  $T_A = 25^\circ$  C
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 1.2$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 124 FETs or 31 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

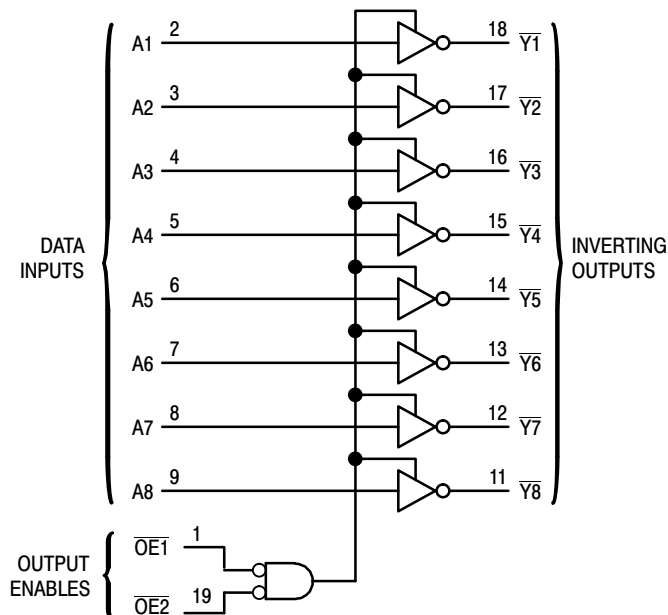


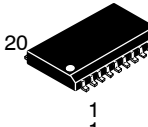
Figure 1. Logic Diagram




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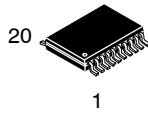
**MARKING DIAGRAMS**



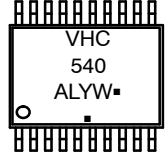
SOIC-20  
DW SUFFIX  
CASE 751D



VHC540  
AWLYYWWG



TSSOP-20  
DT SUFFIX  
CASE 948E



VHC  
540  
ALYW\*

A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

#### PIN ASSIGNMENT

$\overline{OE1}$	1	20	$V_{CC}$
A1	2	19	$\overline{OE2}$
A2	3	18	$\overline{Y1}$
A3	4	17	$\overline{Y2}$
A4	5	16	$\overline{Y3}$
A5	6	15	$\overline{Y4}$
A6	7	14	$\overline{Y5}$
A7	8	13	$\overline{Y6}$
A8	9	12	$\overline{Y7}$
GND	10	11	$\overline{Y8}$

#### FUNCTION TABLE

Inputs			Output $\overline{Y}$
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.



# MC74VHC540

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 55 to 125°C		Unit
				Min	Typ	Max	Min	Max	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5			± 0.25		± 2.5	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	μA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 55 to 125°C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to $\bar{Y}$ (Figures 1 and 3)	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		4.8 7.3	7.0 10.5	1.0 1.0	8.5 12.0	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, $\overline{OE}\bar{n}$ to $\bar{Y}$ (Figures 2 and 4)	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF R <sub>L</sub> = 1kΩ C <sub>L</sub> = 50pF		6.8 9.3	10.5 14.0	1.0 1.0	12.5 16.0	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time, $\overline{OE}\bar{n}$ to $\bar{Y}$ (Figures 2 and 4)	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 50pF R <sub>L</sub> = 1kΩ V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF R <sub>L</sub> = 1kΩ		11.2 6.0	15.4 8.8	1.0 1.0	17.5 10.0	ns
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 50pF (Note 1) V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF (Note 1)			1.5 1.0			ns ns
C <sub>in</sub>	Maximum Input Capacitance			4	10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High Impedance State)			6				pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 2)	Typical @ 25°C, V <sub>CC</sub> = 5.0V		pF
		17		

- Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.
- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per bit). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns, C<sub>L</sub> = 50pF, V<sub>CC</sub> = 5.0V)

Symbol	Parameter	T <sub>A</sub> = 25°C		Unit
		Typ	Max	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.9	1.2	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	- 0.9	- 1.2	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		3.5	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		1.5	V

# MC74VHC540

## SWITCHING WAVEFORMS

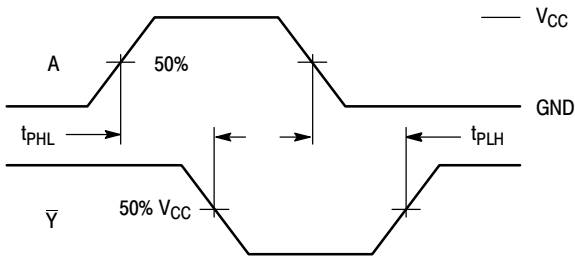


Figure 2.

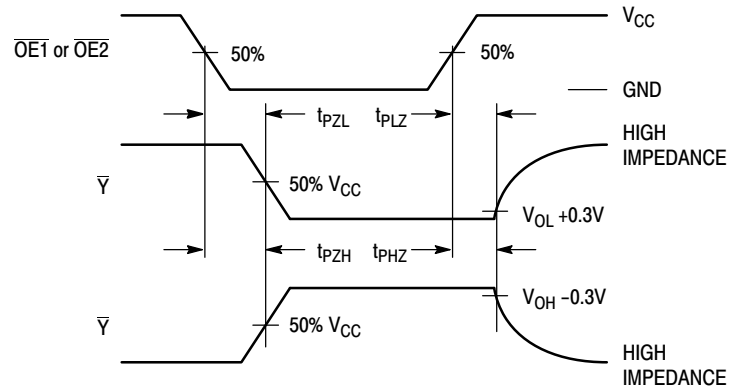
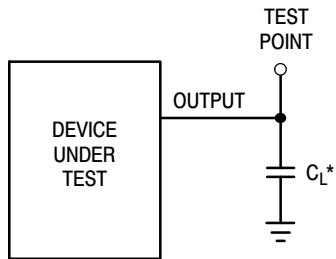


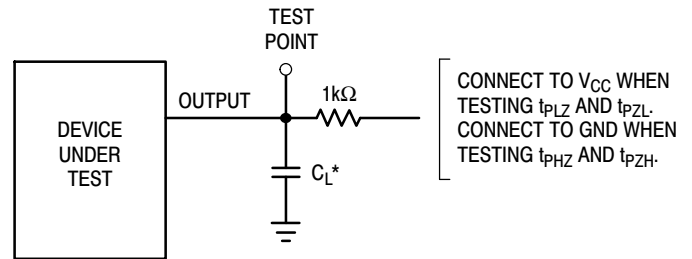
Figure 3.

## TEST CIRCUITS



\*Includes all probe and jig capacitance

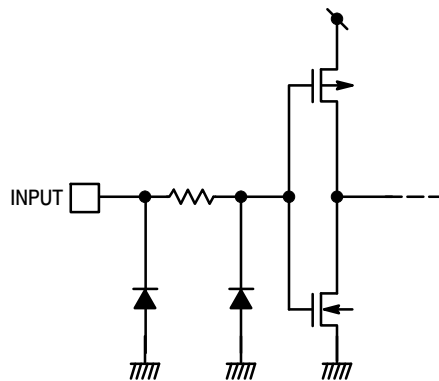
Figure 4.



\*Includes all probe and jig capacitance

Figure 5.

## INPUT EQUIVALENT CIRCUIT



# MC74VHC540

## ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC540DWR2G	SOIC-20 (Pb-Free)	1000 Units / Tape & Reel
MC74VHC540DTR2G	TSSOP-20 (Pb-Free)	2500 Units / Tape & Reel

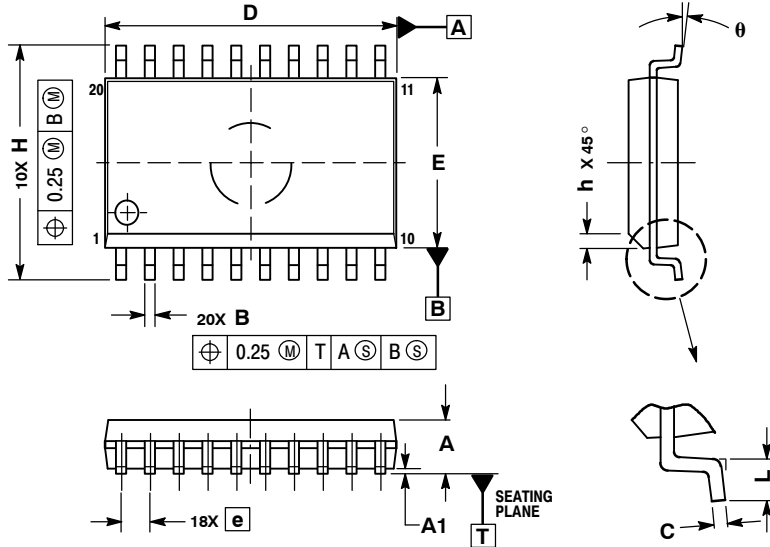
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



# MC74VHC540

## PACKAGE DIMENSIONS


SOIC-20  
DW SUFFIX  
CASE 751D-05  
ISSUE G



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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