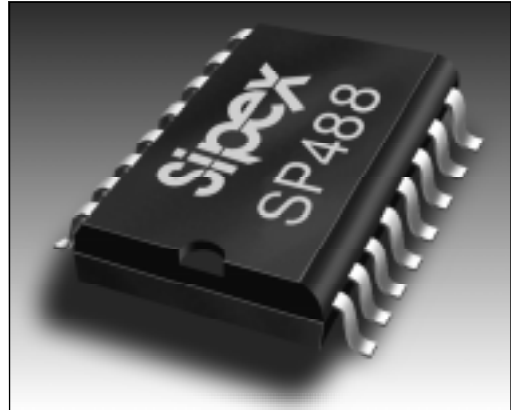


## Quad RS-485/RS-422 Line Receivers

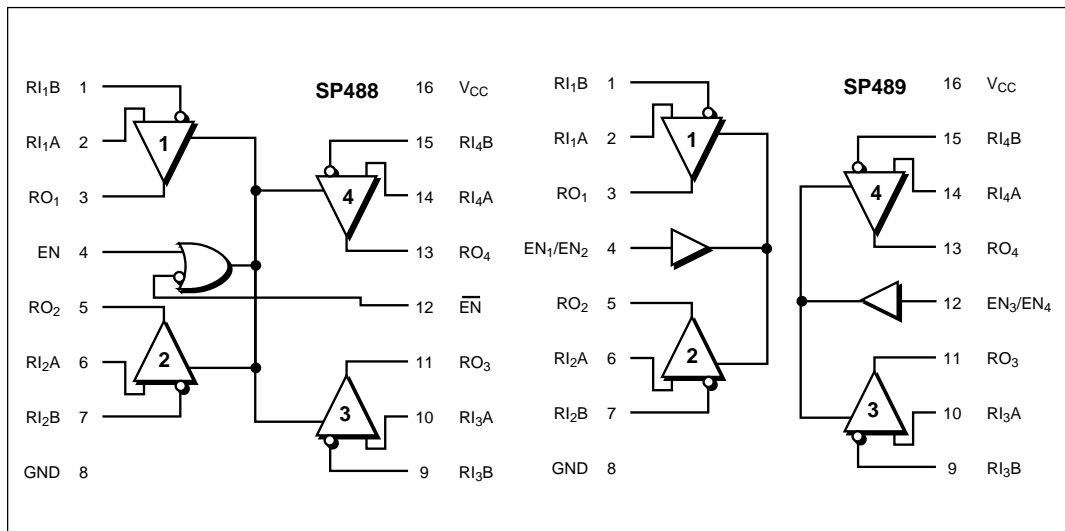
- RS-485 or RS-422 Applications
- Quad Differential Line Receivers
- Tri-state Output Control
- 120ns Typical Receiver Propagation Delays
- -7V to +12V Common Mode Input Range
- 1mA Supply Current
- Single +5V Supply Operation
- Pin Compatible with SN75173, SN75175, LTC488 and LTC489



### DESCRIPTION...

Now available in Lead Free

The **SP488** and **SP489** are low-power quad differential line receivers meeting RS-485 and RS-422 standards. The **SP488** features a common receiver enable control; the **SP489** provides independent receiver enable controls for each pair of receivers. Both feature tri-state outputs and wide common-mode input range. The receivers have a fail-safe feature which forces a logic "1" output when receiver inputs are left floating. Both are available in 16-pin plastic DIP and SOIC packages.



## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V <sub>CC</sub> .....	+7V
Input Voltages	
Logic .....	-0.5V to (V <sub>CC</sub> +0.5V)
Receiver .....	±14V
Receiver Output Voltage .....	-0.5V to (V <sub>CC</sub> +0.5V)
Input Currents	
Logic .....	±25mA
Storage Temperature .....	-65°C to +150°C
Power Dissipation	
Plastic DIP .....	375mW
(derate 7mW/°C above +70°C)	
Small Outline .....	375mW
(derate 7mW/°C above +70°C)	
Lead Temperature (soldering, 10 sec) .....	300°C

## SPECIFICATIONS

V<sub>CC</sub> = 5V±5%; typicals at 25°C; T<sub>MIN</sub> ≤ T<sub>A</sub> ≤ T<sub>MAX</sub> unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
<b>DC CHARACTERISTICS</b>					
Digital Inputs					EN, $\overline{\text{EN}}$ , EN <sub>1</sub> /EN <sub>2</sub> , EN <sub>3</sub> /EN <sub>4</sub>
Voltage			0.8	Volts	
V <sub>IL</sub>	2.0			Volts	
V <sub>IH</sub>			±2	µA	0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
Input Current					
<b>RECEIVER INPUTS</b>					
Input Resistance	12			kOhm	-7V ≤ V <sub>CM</sub> ≤ 12V
Differential Input Threshold	-0.2		+0.2	Volts	-7V ≤ V <sub>CM</sub> ≤ 12V
Input Current (A, B)			+1.0	mA	V <sub>CC</sub> = 0V or 5.25V; I <sub>IN2</sub>
			-0.8	mA	V <sub>IN</sub> = +12V
Maximum Data Rate	10			Mbps	V <sub>IN</sub> = -7V
<b>RECEIVER OUTPUTS</b>					
Output Voltage	3.5			V	I <sub>O</sub> = -4mA; V <sub>ID</sub> = +0.2V
V <sub>OH</sub>			0.4	V	I <sub>O</sub> = +4mA; V <sub>ID</sub> = -0.2V
V <sub>OL</sub>			±1	µA	V <sub>CC</sub> = maximum; 0.4V ≤ V <sub>O</sub> ≤ 2.4V
High Impedance Output Current					
<b>POWER REQUIREMENTS</b>					
Supply Voltage	4.75	5.00	5.25	Volts	
Supply Current		1	5	mA	No load
<b>ENVIRONMENTAL AND MECHANICAL</b>					
Operating Temperature					
-C	0		+70	°C	
-E	-40		+85	°C	
Storage Temperature	-65		+150	°C	
Package					
-S	16-pin Plastic DIP				
-T	16-pin SOIC				

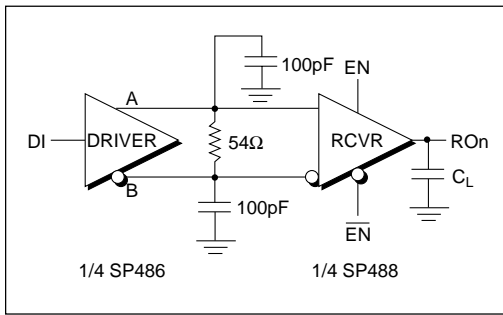


Figure 1. Timing Test Circuit

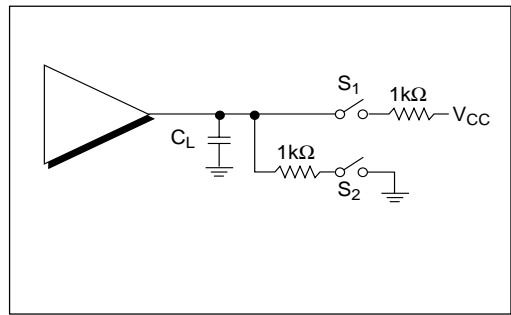


Figure 2. Enable/Disable Timing Test Circuit

## SP488 PINOUT

Pin 1 —  $RI_1B$  — Receiver 1 input B.

Pin 2 —  $RI_1A$  — Receiver 1 input A.

Pin 3 —  $RO_1$  — Receiver 1 Output — If Receiver 1 output is enabled, if  $RI_1A > RI_1B$  by 200mV, Receiver output is high. If Receiver 1 output is enabled, and if  $RI_1A < RI_1B$  by 200mV, Receiver 1 output is low.

Pin 4 — EN — Receiver Output Enable. Please refer to SP488 Truth Table (1).

Pin 5 —  $RO_2$  — Receiver 2 Output — If Receiver 2 output is enabled, if  $RI_2A > RI_2B$  by 200mV, Receiver 2 output is high. If Receiver 2 output is enabled, and if  $RI_2A < RI_2B$  by 200mV, Receiver 2 output is low.

Pin 6 —  $RI_2A$  — Receiver 2 input A.

Pin 7 —  $RI_2B$  — Receiver 2 input B.

Pin 8 — GND — Digital Ground.

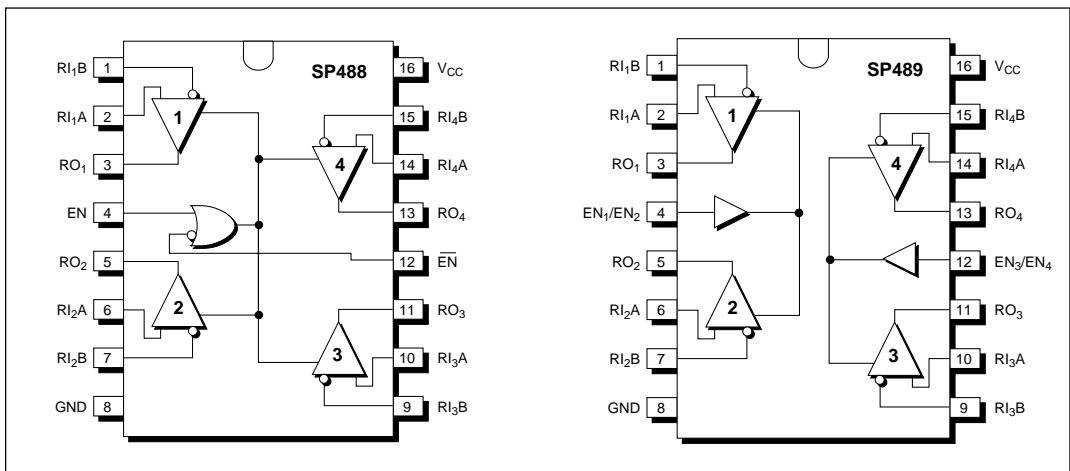
Pin 9 —  $RI_3B$  — Receiver 3 input B.

Pin 10 —  $RI_3A$  — Receiver 3 input A.

Pin 11 —  $RO_3$  — Receiver 3 Output — If Receiver 3 output is enabled, if  $RI_3A > RI_3B$  by 200mV, Receiver 3 output is high. If Receiver 3 output is enabled, and if  $RI_3A < RI_3B$  by 200mV, Receiver 3 output is low.

Pin 12 —  $\overline{EN}$  — Receiver Output Enable. Please refer to SP488 Truth Table (1).

## PINOUT



Pin 13 — RO<sub>4</sub> — Receiver 4 Output — If Receiver 4 output is enabled, if RI<sub>4A</sub> > RI<sub>4B</sub> by 200mV, Receiver 4 output is high. If Receiver 4 output is enabled, and if RI<sub>4A</sub> < RI<sub>4B</sub> by 200mV, Receiver 4 output is low.

Pin 14 — RI<sub>4A</sub> — Receiver 4 input A.

Pin 15 — RI<sub>4B</sub> — Receiver 4 input B.

Pin 16 — Supply Voltage V<sub>cc</sub> — 4.75V ≤ V<sub>cc</sub> ≤ 5.25V.

### SP489 PINOUT

Pin 1 — RI<sub>1B</sub> — Receiver 1 input B.

Pin 2 — RI<sub>1A</sub> — Receiver 1 input A.

Pin 3 — RO<sub>1</sub> — Receiver 1 Output — If receiver 1 output is enabled, if RI<sub>1A</sub> > RI<sub>1B</sub> by 200mV, Receiver output is high. If Receiver 1 output is enabled, and if RI<sub>1A</sub> < RI<sub>1B</sub> by 200mV, Receiver 1 output is low.

Pin 4 — EN1/EN2 — Receiver 1 and 2 Output Enable. Please refer to SP489 Truth Table (2).

Pin 5 — RO<sub>2</sub> — Receiver 2 Output — If Receiver 2 output is enabled, if RI<sub>2A</sub> > RI<sub>2B</sub> by 200mV, Receiver 2 output is high. If Receiver 2 output is enabled, and if RI<sub>2A</sub> < RI<sub>2B</sub> by 200mV, Receiver 2 output is low.

Pin 6 — RI<sub>2A</sub> — Receiver 2 input A.

Pin 7 — RI<sub>2B</sub> — Receiver 2 input B.

Pin 8 — GND — Digital Ground.

DIFFERENTIAL A - B	ENABLES		OUTPUT RO
	EN	EN	
V <sub>ID</sub> ≥ 0.2V	H X	X L	H H
-0.2V < V <sub>ID</sub> < +0.2V	H X	X L	X X
V <sub>ID</sub> ≤ 0.2V	H X	X L	L L
X	L	H	Hi-Z

Table 1. SP488 Truth Table

Pin 9 — RI<sub>3B</sub> — Receiver 3 input B.

Pin 10 — RI<sub>3A</sub> — Receiver 3 input A.

Pin 11 — RO<sub>3</sub> — Receiver 3 Output — If Receiver 3 output is enabled, if RI<sub>3A</sub> > RI<sub>3B</sub> by 200mV, Receiver 3 output is high. If Receiver 3 output is enabled, and if RI<sub>3A</sub> < RI<sub>3B</sub> by 200mV, Receiver 3 output is low.

Pin 12 — EN3/EN4 — Receiver 3 and 4 Output Enable. Please refer to SP489 Truth Table (2).

Pin 13 — RO<sub>4</sub> — Receiver 4 Output — If Receiver 4 output is enabled, if RI<sub>4A</sub> > RI<sub>4B</sub> by 200mV, Receiver 4 output is high. If Receiver 4 output is enabled, and if RI<sub>4A</sub> < RI<sub>4B</sub> by 200mV, Receiver 4 output is low.

Pin 14 — RI<sub>4A</sub> — Receiver 4 input A.

Pin 15 — RI<sub>4B</sub> — Receiver 4 input B.

Pin 16 — Supply Voltage V<sub>cc</sub> — 4.75V ≤ V<sub>cc</sub> ≤ 5.25V.

### FEATURES...

The **SP488** and **SP489** are low-power quad differential line receivers meeting RS-485 and RS-422 standards. The **SP488** features active high and active low common receiver enable controls; the **SP489** provides independent, active high receiver enable controls for each pair of receivers. Both feature tri-state outputs and a -7V to +12V common-mode input range permitting a ±7V ground difference between devices on the communications bus. The **SP488/489** are equipped with a fail-safe feature which forces a logic high at the receiver output when the input is left floating. Data rates up to 10Mbps are supported. Both are available in 16-pin plastic DIP and SOIC packages.

DIFFERENTIAL A - B	ENABLES		OUTPUT RO
	EN <sub>1</sub> /EN <sub>2</sub> or EN <sub>3</sub> /EN <sub>4</sub>		
V <sub>ID</sub> ≥ 0.2V	H		H
-0.2V < V <sub>ID</sub> < +0.2V	H		X
V <sub>ID</sub> ≤ 0.2V	H		L
X	L		Hi-Z

Table 2. SP489 Truth Table

## AC PARAMETERS

$V_{CC} = 5V \pm 5\%$ ; typicals at  $25^{\circ}C$ ;  $0^{\circ}C \leq T_A \leq +70^{\circ}C$  unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
<b>PROPAGATION DELAY</b>					
Receiver Input to Output					$C_L = 15pF$ ; Figure 1, 3
Low to HIGH ( $t_{PLH}$ )		120	250	ns	
High to LOW ( $t_{PHL}$ )		120	250	ns	
Differential Receiver Skew ( $t_{SKD}$ )		13		ns	
Receiver Rise Time ( $t_r$ )					10% to 90%
SP488		30	70	ns	
SP489		30	70	ns	
Receiver Fall Time ( $t_f$ )					90% to 10%
SP488		20	40	ns	
SP489		20	40	ns	
<b>RECEIVER ENABLE</b>					
To Output HIGH		70	150	ns	$C_L = 15pF$ ; Figures 2 and 4 (S2 closed)
To Output LOW		80	200	ns	$C_L = 15pF$ ; Figures 2 and 4 (S1 closed)
<b>RECEIVER DISABLE</b>					
From Output LOW		70	150	ns	$C_L = 15pF$ ; Figures 2 and 4 (S1 closed)
From Output HIGH		70	150	ns	$C_L = 15pF$ ; Figures 2 and 4 (S2 closed)

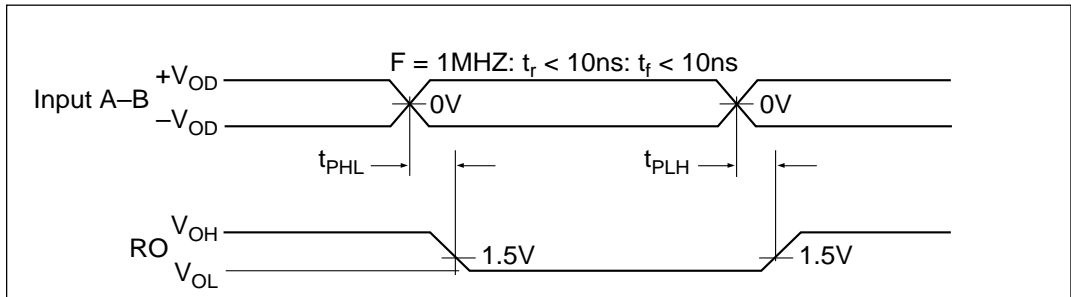


Figure 3. Receiver Propagation Delays

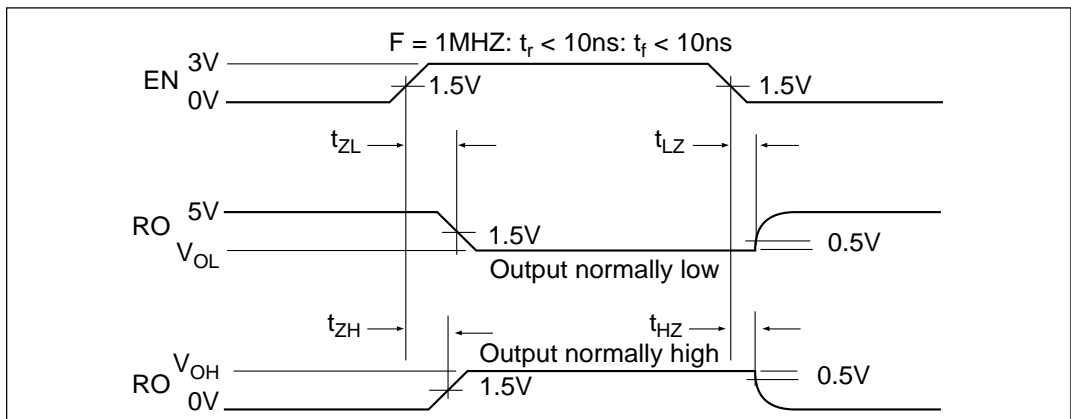


Figure 4. Receiver Enable/Disable Timing

## ORDERING INFORMATION

### Quad RS485 Receivers:

Model	Enable/Disable	Temperature Range	Package
SP488CS	Common; active Low and Active High	.. 0°C to +70°C	16-pin Plastic DIP
SP488CT	Common; active Low and Active High	.. 0°C to +70°C	16-pin SOIC
SP488ES	Common; active Low and Active High	.. -40°C to +85°C	16-pin Plastic DIP
SP488ET	Common; active Low and Active High	.. -40°C to +85°C	16-pin SOIC
SP489CS	One per driver pair; active High	..... 0°C to +70°C	16-pin Plastic DIP
SP489CT	One per driver pair; active High	..... 0°C to +70°C	16-pin SOIC
SP489ES	One per driver pair; active High	..... -40°C to +85°C	16-pin Plastic DIP
SP489ET	One per driver pair; active High	..... -40°C to +85°C	16-pin SOIC

Now available in Lead Free. To order add "-L" to the part number.  
Example: SP488/TR= Normal, SP488TR-L = Lead Free



SIGNAL PROCESSING EXCELLENCE

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