High Accuracy Ultralow I_Q, 300 mA, anyCAP Low Dropout Regulator

ADP3333

FEATURES

- **High accuracy over line and load: ±0.8% @ 25°C, ±1.8% over temperature**
- **Ultralow dropout voltage: 230 mV (maximum) @ 300 mA**
- **Requires only C_{OUT} = 1.0 μF for stability**
  - **anyCAP is stable with any type of capacitor (including MLCC)**
- **Current and thermal limiting**
- **Low noise**
- **Low shutdown current: < 1 μA**
- **2.6 V to 12 V supply range**
- **−40°C to +85°C ambient temperature range**
- **Ultrasmall 8-lead MSOP package**

APPLICATIONS

- **Cellular phones**
- **PCMCIA cards**
- **Personal digital assistants (PDAs)**
- **DSP/ASIC supplies**

GENERAL DESCRIPTION

The ADP3333 is a member of the ADP333x family of precision low dropout (LDO) anyCAP® voltage regulators. Pin compatible with the MAX8860, the ADP3333 operates with a wider input voltage range of 2.6 V to 12 V and delivers a load current up to 300 mA. ADP3333 stands out from other conventional LDOs with a novel architecture and an enhanced process that enables it to offer performance advantages over its competition. Its patented design requires only a 1.0 μF output capacitor for stability. This device is insensitive to output capacitor equivalent series resistance (ESR) and is stable with any good quality capacitor, including ceramic (MLCC) types for space-restricted applications. The ADP3333 achieves exceptional accuracy of ±0.8% at room temperature and ±1.8% over temperature, line, and load variations. The dropout voltage of the ADP3333 is only 140 mV (typical) at 300 mA. This device also includes a safety current limit, thermal overload protection, and a shutdown feature. In shutdown mode, the ground current is reduced to less than 1 μA. The ADP3333 has ultralow quiescent current, 70 μA (typical) in light load situations.

FUNCTIONAL BLOCK DIAGRAM

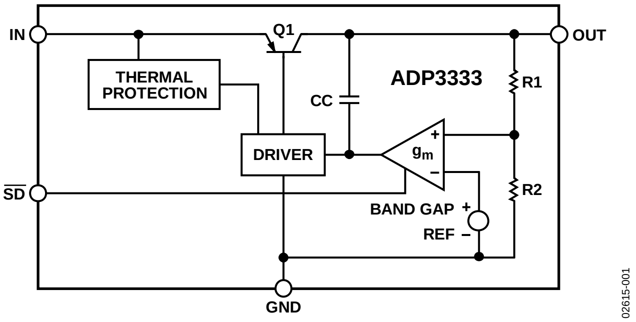

Figure 1.

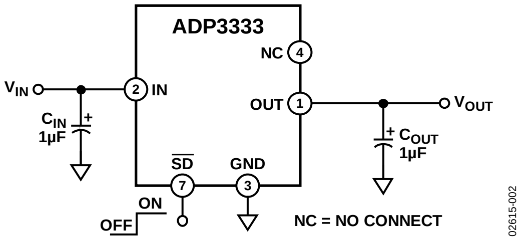

Figure 2. Typical Application Circuit

Rev. B

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ADP3333* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1072: How to Successfully Apply Low Dropout Regulators
- AN-262: Low-Noise Low Drop-Out Regulator for Portable Equipment

Data Sheet

- ADP3333: High Accuracy Ultralow I_Q, 300 mA, anyCAP® Low Dropout Regulator Data Sheet

TOOLS AND SIMULATIONS

- ADI Linear Regulator Design Tool and Parametric Search
- ADIsimPower™ Voltage Regulator Design Tool

REFERENCE DESIGNS

- CN0075
- CN0153
- CN0214

DESIGN RESOURCES

- ADP3333 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP3333 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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8/03—Data Sheet Changed from Rev. 0 to Rev. A

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SPECIFICATIONS

V_{IN} = 6.0 V, C_{IN} = C_{OUT} = 1.0 μF, T_J = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Condition	Min	Typ	Max	Unit
OUTPUT						
Voltage Accuracy[2]	V_{OUT}	$V_{IN} = V_{OUTNOM}$ + 0.3 V to 12 V, I_L = 0.1 mA to 300 mA, T_J = 25°C	−0.8		+0.8	%
		$V_{IN} = V_{OUTNOM}$ + 0.3 V to 12 V, I_L = 0.1 mA to 300 mA	−1.8		+1.8	%
Line Regulation[2]	$\Delta V_{IN}/\Delta V_{OUT}$	$V_{IN} = V_{OUTNOM}$ + 0.3 V to 12 V, T_J = 25°C		0.04		mV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_L = 0.1 mA to 300 mA, T_J = 25°C		0.04		mV/mA
Dropout Voltage	$V_{DROPOUT}$	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 300 mA		140	230	mV
		I_L = 200 mA		105	185	mV
		I_L = 0.1 mA		30		mV
Peak Load Current	I_{LDPK}	$V_{IN} = V_{OUTNOM}$ + 1 V		600		mA
Output Noise	V_{NOISE}	f = 10 Hz to 100 kHz, C_L = 10 μF, I_L = 300 mA		45		μV rms
GROUND CURRENT						
In Regulation	I_{GND}	I_L = 300 mA		2.0	5.5	mA
		I_L = 300 mA, T_J = 25°C		2.0	4.3	mA
		I_L = 300 mA, T_J = 85°C		1.5	3.3	mA
		I_L = 200 mA		1.4		mA
		I_L = 10 mA		200	275	μA
		I_L = 0.1 mA		70	100	μA
In Dropout	I_{GND}	$V_{IN} = V_{OUTNOM}$ − 100 mV, I_L = 0.1 mA		70	190	μA
		$V_{IN} = V_{OUTNOM}$ − 100 mV, I_L = 0.1 mA, T_J = 0°C to 125°C		70	160	μA
In Shutdown	I_{GNDSD}	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	1	μA
SHUTDOWN						
Threshold Voltage	$V_{\overline{THSD}}$	Regulator on	2.0			V
		Regulator off			0.4	V
$\overline{SD}$ Input Current	$I_{\overline{SD}}$	$0 \leq \overline{SD} \leq 12$ V		0.85	7	μA
		$0 \leq \overline{SD} \leq 5$ V		0.8	4.5	μA
Output Current in Shutdown	I_{OSD}	T_J = 25°C, V_{IN} = 12 V		0.01	1	μA
		T_J = 125°C, V_{IN} = 12 V		0.01	1	μA

[1] Application stable with no load.

[2] V_{IN} = 2.6 V for models with $V_{OUTNOM} \leq 2.3$ V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Input Supply Voltage	−0.3 V to +16 V
Shutdown Input Voltage	−0.3 V to +16 V
Power Dissipation	Internally Limited
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead MSOP (4-Layer)	158	°C/W
8-Lead MSOP (2-Layer)	220	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

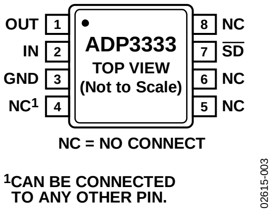


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT	Output of the Regulator. Bypass to ground with a 1.0 µF or larger capacitor.
2	IN	Input Pin. Bypass to ground with a 1.0 µF or larger capacitor.
3	GND	Ground Pin.
4 to 6, 8	NC	No Connect. Best thermal performance is achieved when the NC pins are connected to the GND plane.
7	$\overline{\text{SD}}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, connect this pin to the IN pin.

TYPICAL PERFORMANCE CHARACTERISTICS

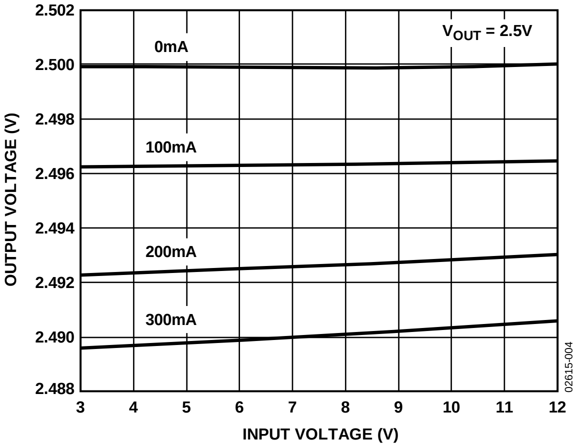


Figure 4. Line Regulation Output Voltage vs. Input Voltage

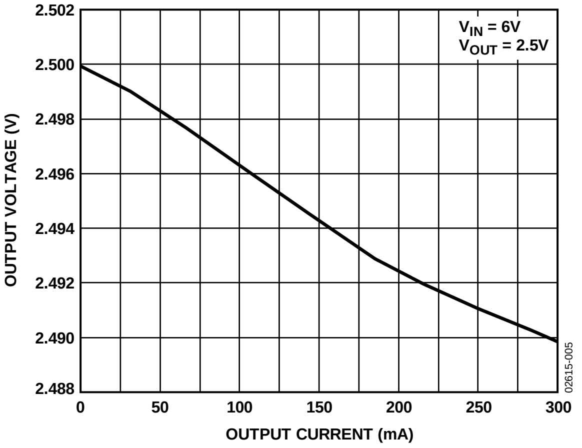


Figure 5. Output Voltage vs. Output Current

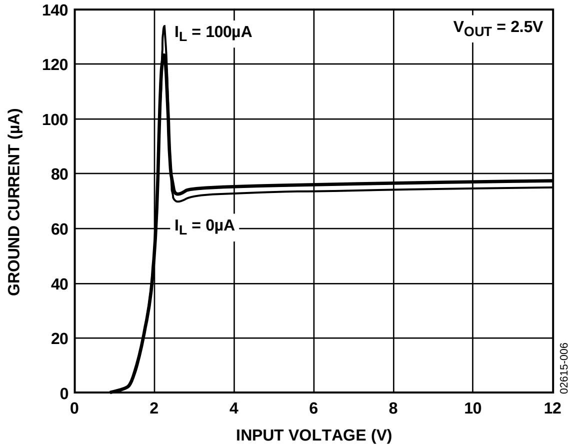


Figure 6. Ground Current vs. Input Voltage

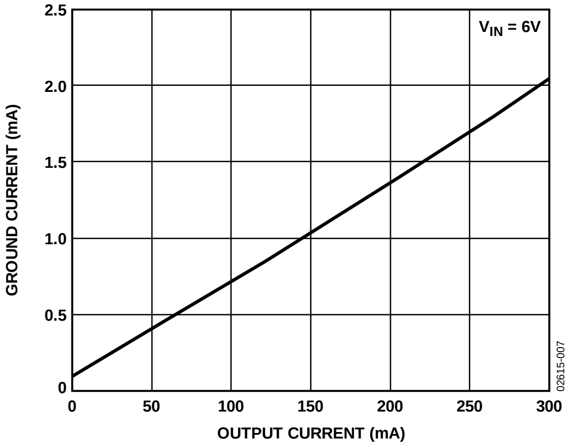


Figure 7. Ground Current vs. Output Current

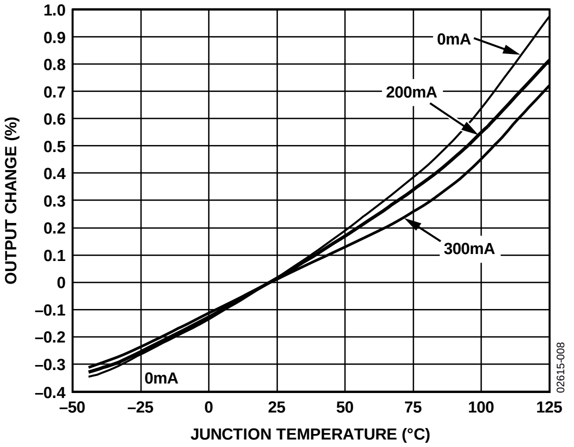


Figure 8. Output Voltage Variation % vs. Junction Temperature

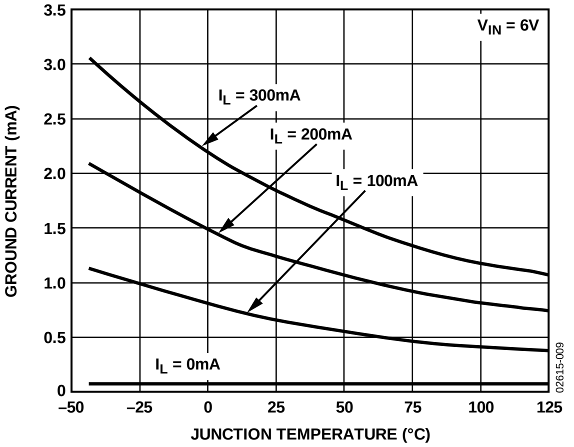


Figure 9. Ground Current vs. Junction Temperature

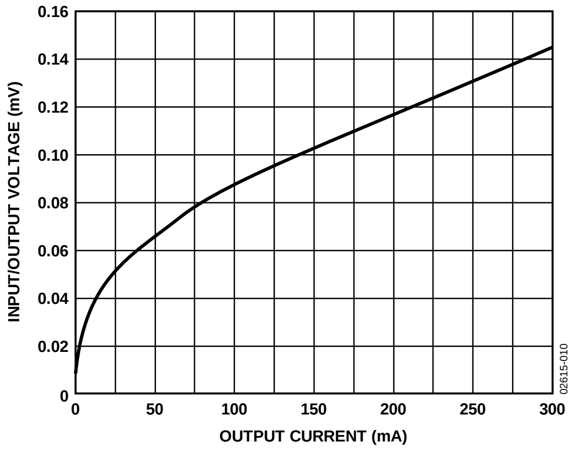


Figure 10. Dropout Voltage vs. Output Current

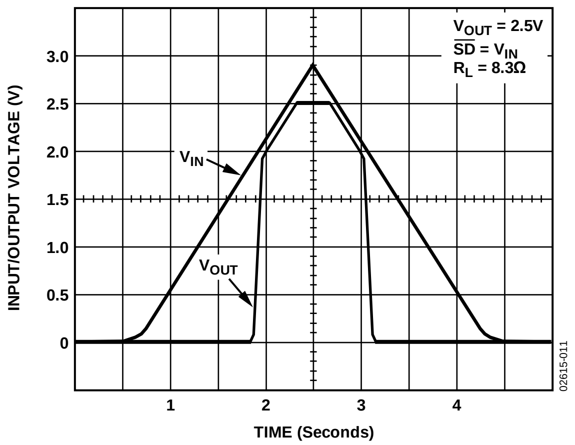


Figure 11. V_{OUT} During Power-Up/Power-Down

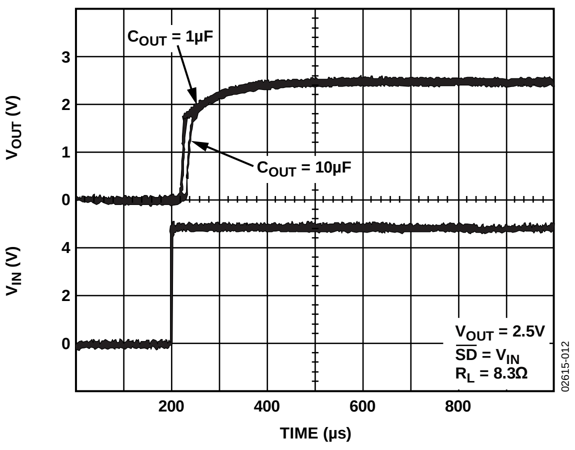


Figure 12. Power-Up Response

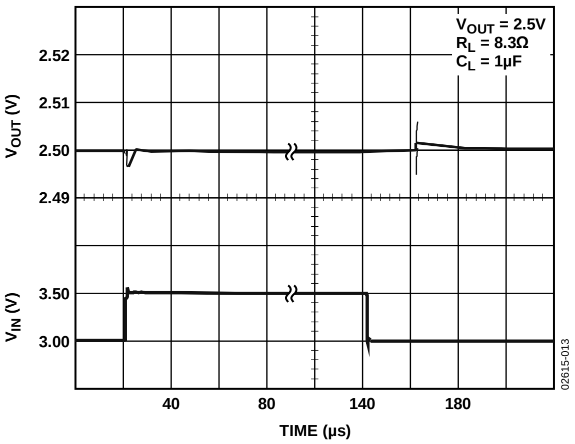


Figure 13. Line Transient Response, C_L = 1 µF

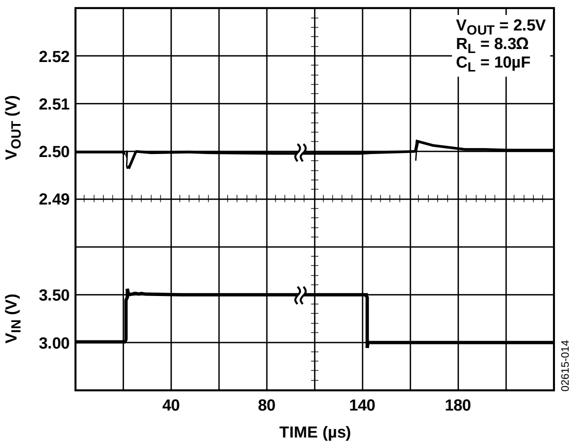


Figure 14. Line Transient Response, C_L = 10 µF

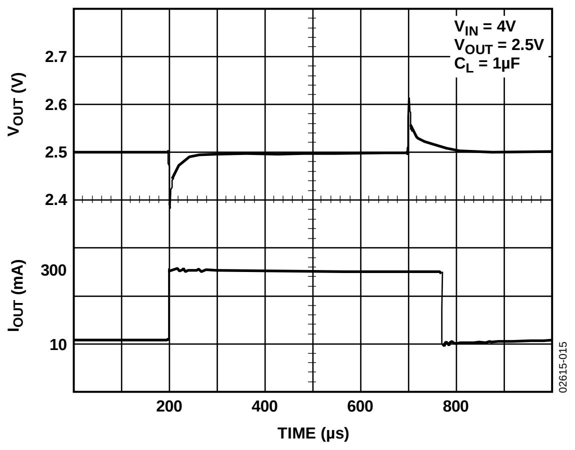


Figure 15. Load Transient Response, C_L = 1 µF

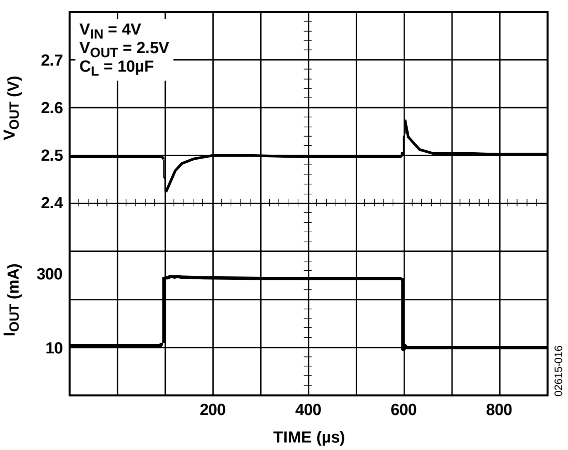


Figure 16. Load Transient Response, C_L = 10 μF

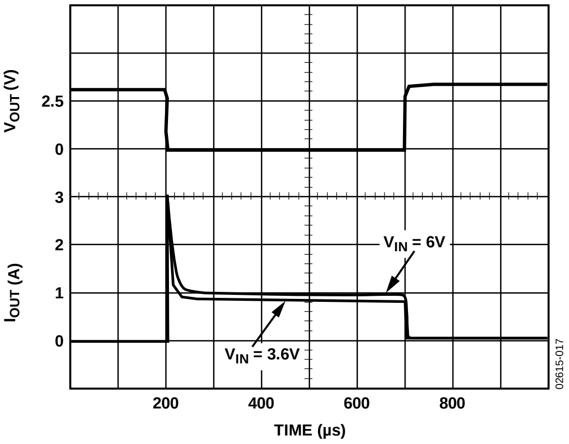


Figure 17. Short-Circuit Current

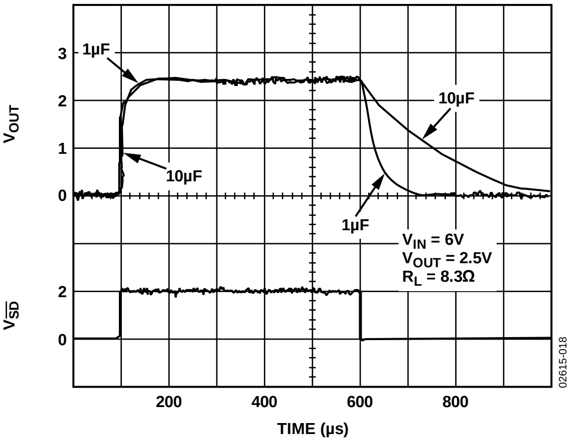


Figure 18. Turn-On/Turn-Off Response

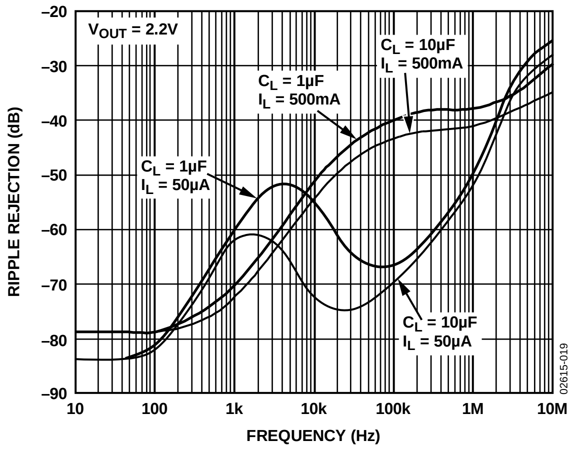


Figure 19. Power Supply Ripple Rejection

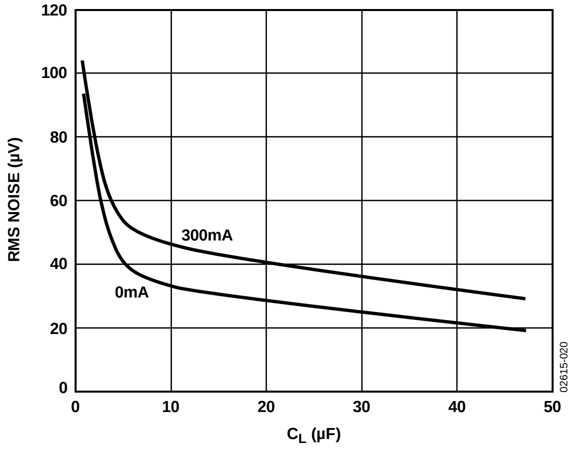


Figure 20. RMS Noise vs. C_L (10 Hz to 100 kHz)

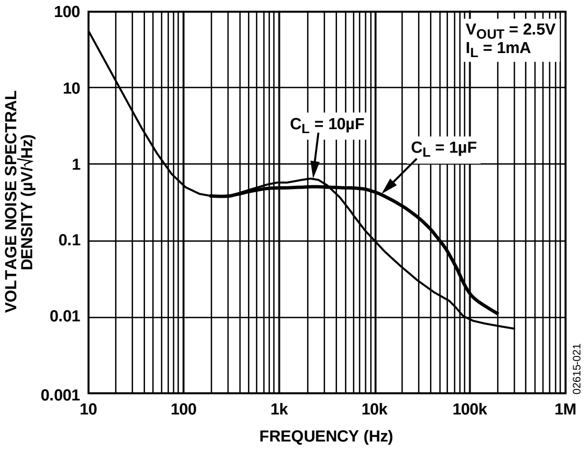


Figure 21. Output Noise Density

THEORY OF OPERATION

The ADP3333 anyCAP LDO uses a single control loop for regulation and reference functions (see Figure 22). The output voltage is sensed by a resistive voltage divider consisting of R1 and R2 that is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

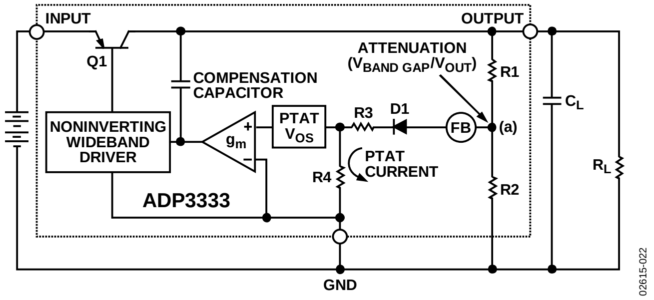


Figure 22. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that at equilibrium it produces a large, temperature-proportional input offset voltage that is repeatable and very well controlled. The temperature proportional offset voltage is combined with the complementary diode voltage to form a virtual band gap voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources and leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the band gap voltage to the output voltage. Although the R1/R2 resistor divider is loaded by the diode, D1, and a second divider consisting of R3 and R4, the values can be chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider so that the error resulting from base current loading in conventional circuits is avoided.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value required to keep conventional LDOs stable changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3333 anyCAP LDO, this is no longer true. This device can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. Its innovative design allows the circuit to be stable with just a small 1.0 μF capacitor on the output. Additional advantages of the pole splitting scheme include superior line noise rejection and very high regulator gain, which leads to excellent line and load regulation. An impressive ±1.8% accuracy is guaranteed over line, load, and temperature.

Additional features of the circuit include current limit and thermal shutdown.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The stability and transient response of the LDO is a function of the output capacitor. The ADP3333 is stable with a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 1.0 µF is all that is needed for stability. Larger capacitors can be used if high current surges on the output are anticipated. The ADP3333 is stable with extremely low ESR capacitors (ESR ≈ 0), such as multilayer ceramic capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types falls below the minimum rated value over temperature or with dc voltage. Ensure that the capacitor provides at least 1.0 µF of capacitance over temperature and dc bias.

Input Bypass Capacitor

An input bypass capacitor is not strictly required but is recommended in any application involving long input wires or high source impedance. Connecting a 1.0 µF capacitor from the input to ground reduces the circuit's sensitivity to printed circuit board (PCB) layout and input transients. If a larger output capacitor is necessary, then a larger value input capacitor is also recommended.

OUTPUT CURRENT LIMIT

The ADP3333 is short-circuit protected by limiting the pass transistor's base drive current. The maximum output current is limited to about 1 A (see Figure 17).

THERMAL OVERLOAD PROTECTION

The ADP3333 is protected against damage due to excessive power dissipation by its thermal overload protection circuit. Thermal protection limits the die temperature to a maximum of 165°C. Under extreme conditions (that is, high ambient temperature and power dissipation) where the die temperature starts to rise above 165°C, the output current is reduced until the die temperature drops to a safe level.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, the device's power dissipation should be externally limited so that the junction temperature does not exceed 125°C.

CALCULATING JUNCTION TEMPERATURE

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT})\, I_L + (V_{IN})\, I_{GND}$$

where I_L and I_{GND} are the load current and ground current, and V_{IN} and V_{OUT} are the input and output voltages, respectively.

Assuming the worst-case operating conditions are $I_L = 300$ mA, $I_{GND} = 2.0$ mA, $V_{IN} = 4.0$ V, and $V_{OUT} = 3.0$ V, the device power dissipation is

$$P_D = (4.0\text{ V} - 3.0\text{ V})\ 300\text{ mA} + (4.0\text{ V})\ 2.0\text{ mA} = 308\text{ mW}$$

The package used on the ADP3333 has a thermal resistance of 158°C/W for 4-layer boards. The junction temperature rise above ambient is approximately equal to

$$T_{JA} = 0.308\text{ W} \times 158°\text{C/W} = 48.7°\text{C}$$

Therefore, to limit the junction temperature to 125°C, the maximum allowable ambient temperature is

$$T_{A(MAX)} = 125°\text{C} - 48.7°\text{C} = 76.3°\text{C}$$

SHUTDOWN MODE

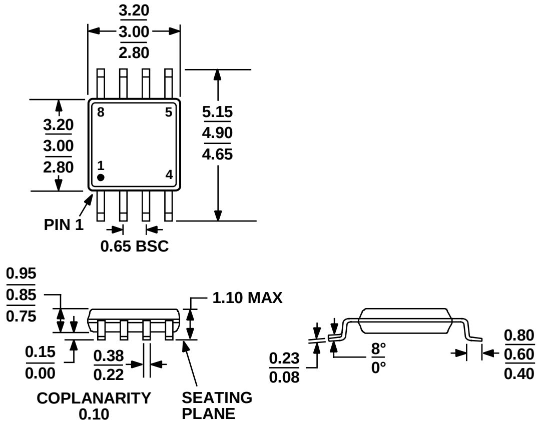
Applying a high signal to the shutdown pin, $\overline{\text{SD}}$, or connecting it to the input pin, $\overline{\text{IN}}$, turns the output on. Pulling the shutdown pin to 0.3 V or below, or connecting it to ground, turns the output off. In shutdown mode, the quiescent current is reduced to less than 1 µA.

PCB LAYOUT CONSIDERATIONS

Use the following general guidelines when designing printed circuit boards:

- Keep the output capacitor as close as possible to the output and ground pins.
- Keep the input capacitor as close as possible to the input and ground pins.
- PCB traces with larger cross sectional areas remove more heat from the ADP3333. For optimum heat transfer, use thick copper with wide traces.
- Connect the NC pins (Pin 4, Pin 5, Pin 6, and Pin 8) to ground for better thermal performance.
- The thermal resistance can be decreased by approximately 10% by adding a few square centimeters of copper area to the lands connected to the pins of the LDO.
- Use additional copper layers or planes to reduce the thermal resistance. Again, connecting the other layers to the GND and NC pins of the ADP3333 is best, but not necessary. When connecting the ground pad to other layers, use multiple vias.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 23. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP3333ARM-1.5-RL	−40°C to +85°C	1.5	8-Lead MSOP	RM-8	LKA
ADP3333ARM-1.5-RL7	−40°C to +85°C	1.5	8-Lead MSOP	RM-8	LKA
ADP3333ARM-1.8-RL	−40°C to +85°C	1.8	8-Lead MSOP	RM-8	LKB
ADP3333ARM-1.8-RL7	−40°C to +85°C	1.8	8-Lead MSOP	RM-8	LKB
ADP3333ARM-2.5-RL	−40°C to +85°C	2.5	8-Lead MSOP	RM-8	LKC
ADP3333ARM-2.5-RL7	−40°C to +85°C	2.5	8-Lead MSOP	RM-8	LKC
ADP3333ARM-2.77-RL	−40°C to +85°C	2.77	8-Lead MSOP	RM-8	LKD
ADP3333ARM-2.77-R7	−40°C to +85°C	2.77	8-Lead MSOP	RM-8	LKD
ADP3333ARM-3-REEL	−40°C to +85°C	3	8-Lead MSOP	RM-8	LKE
ADP3333ARM-3-REEL7	−40°C to +85°C	3	8-Lead MSOP	RM-8	LKE
ADP3333ARM-3.15-RL	−40°C to +85°C	3.15	8-Lead MSOP	RM-8	LKF
ADP3333ARM-3.15-R7	−40°C to +85°C	3.15	8-Lead MSOP	RM-8	LKF
ADP3333ARM-3.3-RL	−40°C to +85°C	3.3	8-Lead MSOP	RM-8	LKG
ADP3333ARM-3.3-RL7	−40°C to +85°C	3.3	8-Lead MSOP	RM-8	LKG
ADP3333ARM-5-REEL	−40°C to +85°C	5	8-Lead MSOP	RM-8	LKH
ADP3333ARM-5-REEL7	−40°C to +85°C	5	8-Lead MSOP	RM-8	LKH
ADP3333ARMZ-1.5-R7[1]	−40°C to +85°C	1.5	8-Lead MSOP	RM-8	L1X
ADP3333ARMZ-1.5-RL[1]	−40°C to +85°C	1.5	8-Lead MSOP	RM-8	L1X
ADP3333ARMZ-1.8-RL[1]	−40°C to +85°C	1.8	8-Lead MSOP	RM-8	L1U
ADP3333ARMZ-1.8RL7[1]	−40°C to +85°C	1.8	8-Lead MSOP	RM-8	L1U
ADP3333ARMZ-2.5-RL[1]	−40°C to +85°C	2.5	8-Lead MSOP	RM-8	L1V
ADP3333ARMZ-2.5-R7[1]	−40°C to +85°C	2.5	8-Lead MSOP	RM-8	L1V
ADP3333ARMZ-2.77R7[1]	−40°C to +85°C	2.77	8-Lead MSOP	RM-8	L1Y
ADP3333ARMZ-3-R7[1]	−40°C to +85°C	3.0	8-Lead MSOP	RM-8	L1W
ADP3333ARMZ-3.15R7[1]	−40°C to +85°C	3.15	8-Lead MSOP	RM-8	L1Z
ADP3333ARMZ-3.3-R7[1]	−40°C to +85°C	3.3	8-Lead MSOP	RM-8	L20
ADP3333ARMZ-3.3-RL[1]	−40°C to +85°C	3.3	8-Lead MSOP	RM-8	L20
ADP3333ARMZ-5-R7[1]	−40°C to +85°C	5.0	8-Lead MSOP	RM-8	L21
ADP3333ARMZ-5-RL[1]	−40°C to +85°C	5.0	8-Lead MSOP	RM-8	L21

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[1] Z = RoHS Compliant Part.

NOTES

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