AS3701

Micro-PMIC

General Description

The AS3701 is a small compact PMU for small size and low power applications.

AS3701 features one 500mA DCDC buck converter operating from 1MHz up to 4MHz, two 200mA LDOs, two 40mA current sinks and offers additional GPIO functions. Further, the device contains an integrated linear battery charger with constant current and constant voltage operation. The wide charging current range going from 11mA up to 500mA and the integrated battery temperature monitoring with selectable NTC beta values make this device suitable for a great variety of applications.

The single supply voltage may vary from 2.7V to 5.5V and all functionalities of AS3701 can be controlled via the I^2C interface.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3701, Micro-PMIC are listed below:

Figure 1:
Added Value of Using AS3701

Benefits	Features
• Multiple rails in a compact design for low power applications	• 2 x 200mA universal LDO (1.2V to 3.3V) • 500mA Step-down DCDC (0.6125V to 3.35V) • 2 programmable current sources up to 40mA • Possible external PWM dimming input
• Self-contained Li-Ion battery charger with power path	• Linear charger with internal transistor • 500mA max charging current • Trickle-, Constant Current and Constant Voltage operation (3.82V to 4.44V) • Charger timeout and temperature supervision • NTC beta selection
• Flexible multi-purpose IOs for general control tasks and for standalone operation without I^2C interface	• Wake-up / Stand-by / Power-down input • PWM input/output • Interrupt input/output • Low battery and Power Good output • Charging and USB current setting input • Charger control input/output

Benefits	Features
• Flexible and fast adaption to different processors/applications	• OTP programmable Boot sequence
• Power saving control according to the processor´s needs	• Stand-by function with programmable voltages
• Self-contained start-up and safety shutdown feature	• I^2C control interface • ON-key with 4/8s emergency power-down • POR with Reset I/O
• Cost effective, small package optimized for PCB cost or size	• 17-balls WL-CSP with 0.4mm pitch • 20-balls WL-CSP with 0.4mm pitch

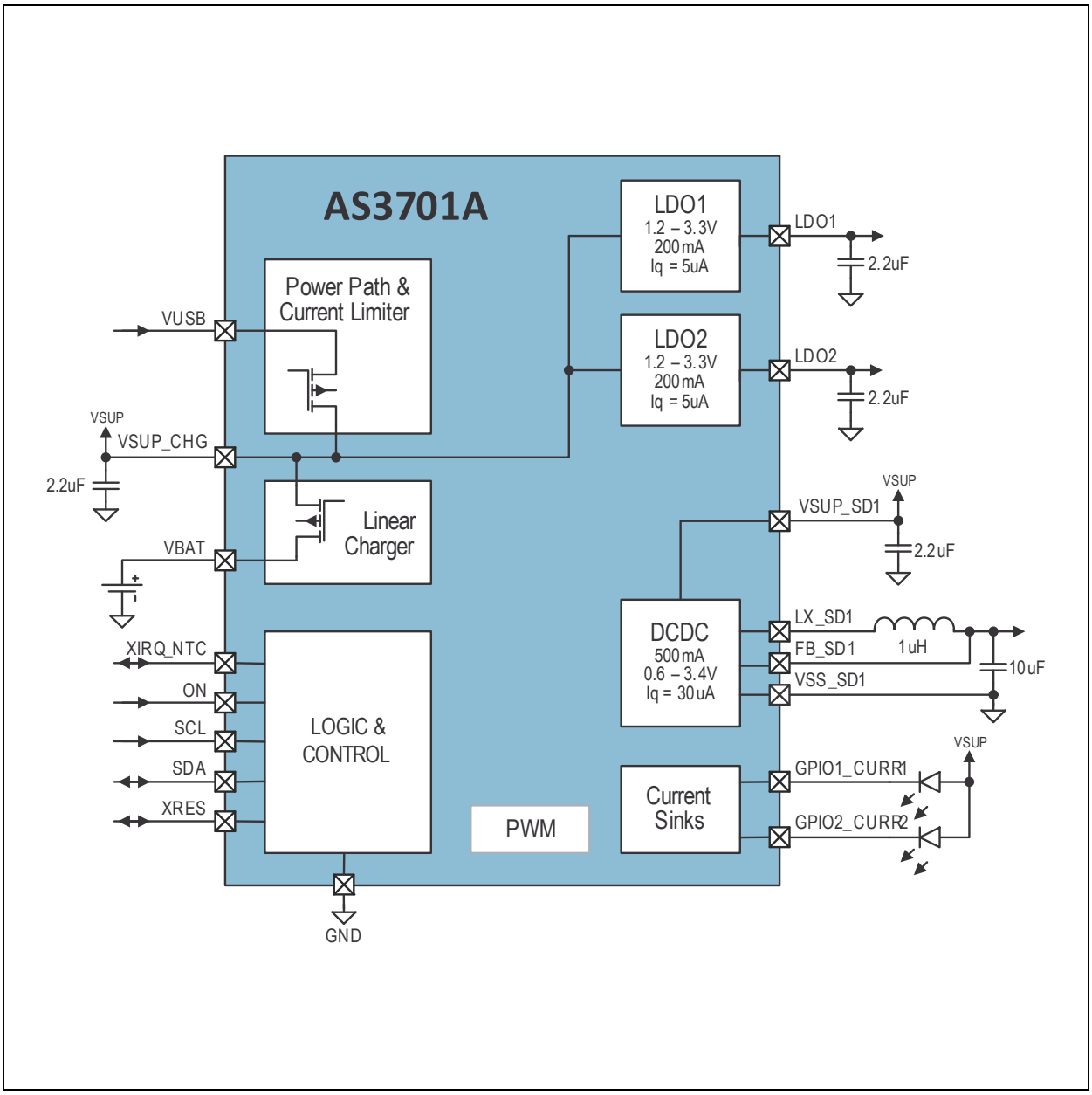
Applications

The device is a PMU for low power applications like sport watches, smart watches, handheld GPS devices, mobile phones and any other 1-cell Li+ powered devices.

Block Diagram

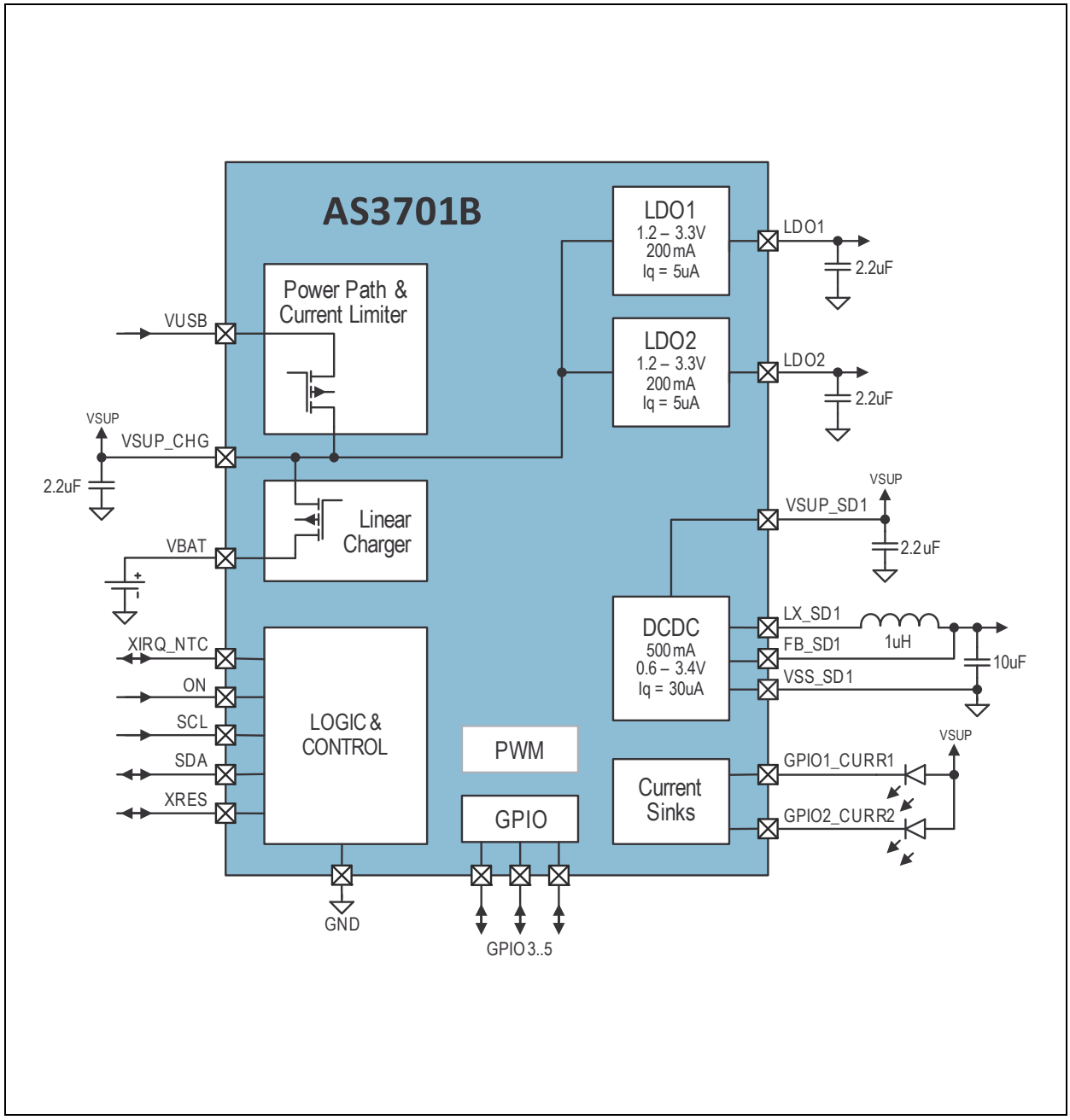
The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS3701A



Block Diagram: This figure shows the block diagram of the AS3701A

Figure 3:
Functional Blocks of AS3701B



Block Diagram: This figure shows the block diagram of the AS3701B

Pin Assignments

Figure 4:
17-balls WL-CSP Pin Assignment for AS3701A

Pin Assignments: Shows the top view pin assignment of the AS3701A

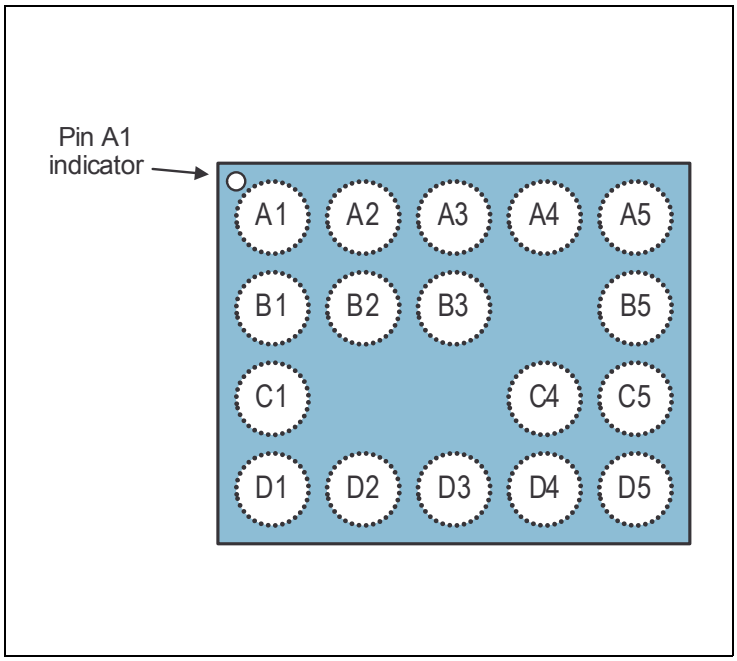


Figure 5:
20-balls WL-CSP Pin Assignment for AS3701B

Pin Assignments: Shows the top view pin assignment of the AS3701B

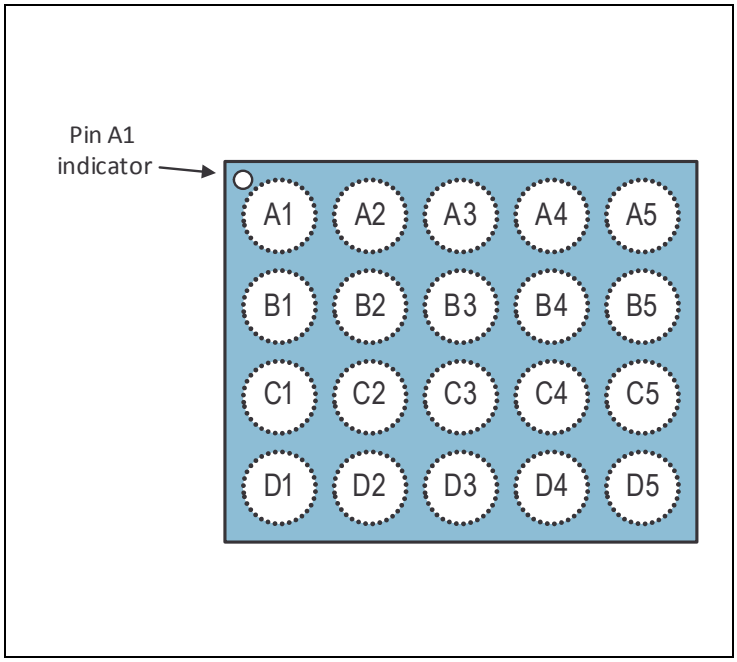


Figure 6:
Pin Description

Pin Number		Pin Name	I/O	Description	Max. Voltage	If Not Used
17 Balls	20 Balls					
A2	A2	VUSB	S	Wall adapter or USB Bus Power input (before protection)	5.5V	pull-down to GND
A1	A1	VSUP_CHG	SIO	Current limiter output, LDO1 & LDO2 pos. supply terminal	VSUP	Mandatory
D2	D2	VSUP_SD1	S	DCDC pos. supply terminal	VSUP	Mandatory
B1	B1	VBAT	S	Li-Ion Battery Terminal	5.5V	Open
A5	A5	GND	AIO	Reference GND	-	Mandatory
A4	A4	LDO1	AO	LDO1 Output	3.3V	Open
A3	A3	LDO2	AO	LDO2 Output	3.3V	Open
D1	D1	LX_SD1	AIO	DCDC Step Down Switch Output to Coil	5.5V	Open
B2	B2	FB_SD1	AI	DCDC Step Down Feedback Pin	3.6V	Open
D4	D4	XRES	DIO	Reset IO	VSUP	Open
D3	D3	ON	DI	Power Up Input	5.5V	Open
B3	B3	XIRQ_NTC	AIO	Interrupt Output or NTC Input	VSUP	Open
D5	D5	SCL	DI	2-wire Serial IF Clock Input	VSUP	pull-up to VSUP
C4	C4	SDA	DIO	2-wire Serial IF Data I/O	VSUP	pull-up to VSUP
C5	C5	GPIO1_ CURR1	DIO	General Purpose IO1 or LED Channel 1	VSUP	Open
B5	B5	GPIO2_ CURR2	DIO	General Purpose IO2 or LED Channel 2	VSUP	Open
-	B4	GPIO3	DIO	General Purpose IO3	VSUP	Open
-	C2	GPIO4	DIO	General Purpose IO4	VSUP	Open
-	C3	GPIO5	DIO	General Purpose IO5	VSUP	Open
C1	C1	VSS_SD1	AIO	GND connector of DCDC	-	Mandatory

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{GND}	Supply voltage to ground 5V pins	-0.5	7.0	V	Applicable for pins VSUP_CHG, VSUP_SD1, VBAT, VUSB, LX_SD1, SCL, SDA, ON, XRES, XIRQ_NTC, GPIO3, GPIO4, GPIO5, GPIO1_CURR1, GPIO2_ CURR2
V_{GND}	Supply voltage to ground 3V pins	-0.5	5.0	V	Applicable for pins LDO1, LDO2, FB_SD1
	Voltage difference between ground terminals	-0.5	0.5	V	Applicable for pins GND, VSS_SD1
I_{SCR}	Input current (latch-up immunity)	-100	100	mA	JEDEC JESD78
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous power dissipation		0.96	W	P_T [(1)] for WL-CSP20 (R_{THJA} ~ *57K/W*)
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge (human body model)	±2		kV	JEDEC JESD22-A114F

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_A	Operating temperature	-40	85	°C	
R_{THJA}	Junction to ambient thermal resistance			°C/W	R_{THJA} typ. 57K/W
T_J	Junction temperature		125	°C	
T_{STRG}	Storage temperature range	-55	125	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 (2)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	1			Represents an unlimited floor life time

Note(s):

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices"

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 8:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	Pin VSUP	2.7		5.5	V
I_{Q_ACTIVE}	Active mode quiescent current	Normal operating current		26		uA
$I_{Q\_STAND-BY}$	Stand-by quiescent current	Normal operating current (Oscillator ON)		26		
		Normal operating current (Oscillator OFF)		11.5		
$I_{POWEROFF}$	Shutdown current	*power_off* = 1		1.2		

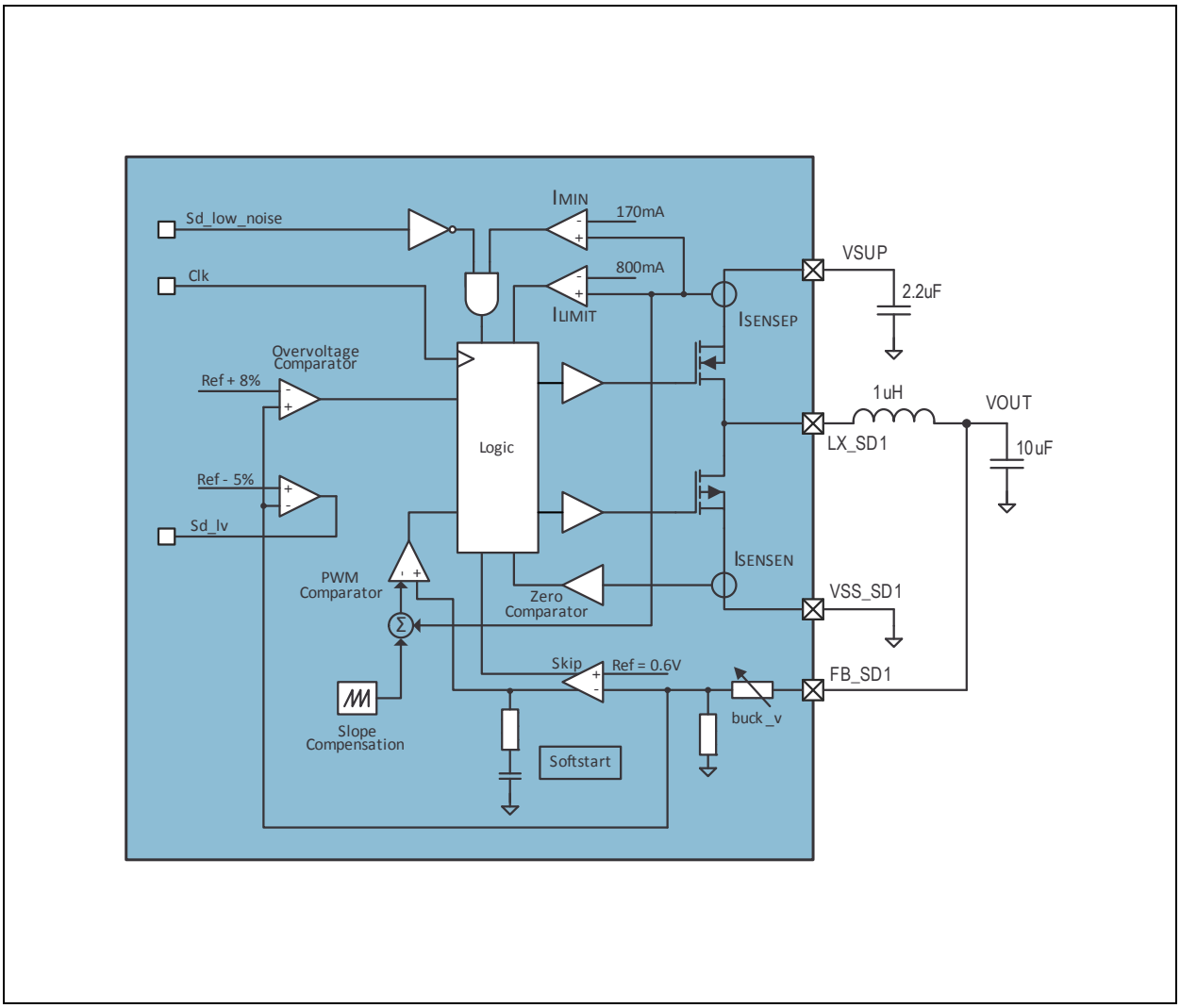
Electrical Characteristics: V_{SUP} = 3.7V, $V_{OUT} < V_{IN}$ – 0.5V, T_{AMB} = -40°C to 85°C, typ. values @ T_{AMB} = 25°C (unless otherwise specified)

Detailed Description – Power Management Functions

Step Down Converter

The step-down converter is a high-efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches, efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to the maximum output current, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC Converter and the coil during overload condition.

Figure 9:
DCDC Step-Down Converter Block Diagram

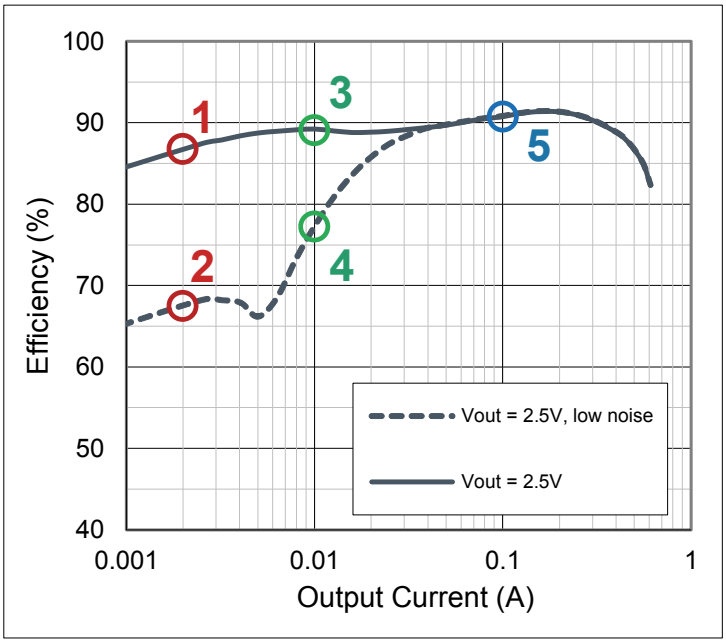


Mode Settings

To allow optimized performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input/output ripple.

Figure 10:
DCDC Step-Down Converter Mode Settings

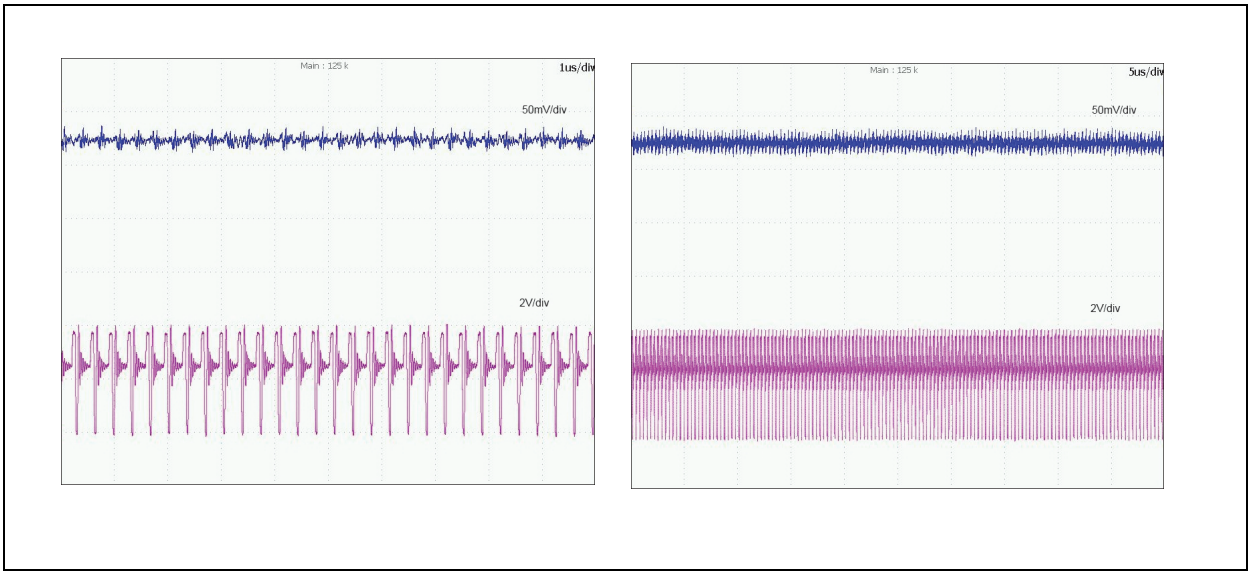
Mode Setting: This graph shows the difference of the efficiency curves for high efficiency and low noise mode setting. V_{SUP} = 3.7V, V_{OUT} = 2.5V, f_{SW} = 3MHz, T_{AMB} = 25°C.



Low-Ripple, Low-Noise Operation

Low-ripple, low-noise operation can be enabled by setting the bit *sd_low_noise [SD_control1]* to 1.
In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current, the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. Resultant the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to t_{MIN_ON} to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency at light loads, especially at low input to output voltage differences.

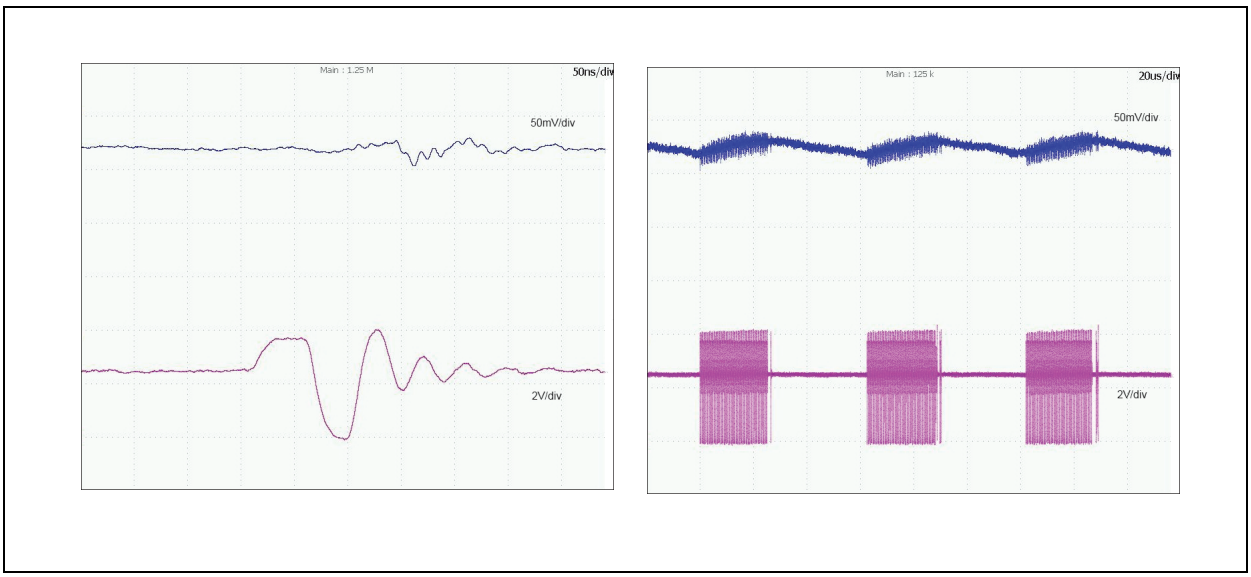
Figure 11:
Switching Behavior at Operating Point 4



Operating Point 4: These graphs show the switching behavior referring to the operating point 4 from figure10. Here the mode is set to low noise/low ripple operation and the DCDC is continuously switching at 10mA load current.

Only in the case the load current gets so small, that less than the minimum on time of the PMOS would be needed to keep the loop in regulation, the regulator will enter low power mode operation.

Figure 12:
Switching Behavior at Operating Point 2



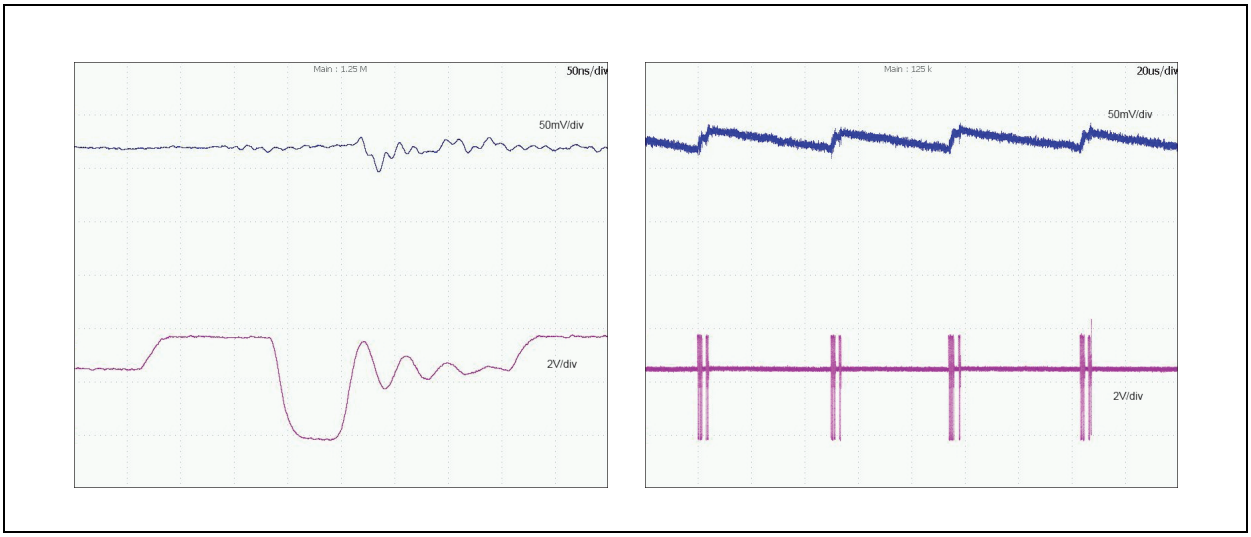
Operating Point 2: These graphs show the switching behavior referring to the operating point 2 from figure10. Here the mode is set to low noise/low ripple operation and the DCDC has already started to skip pulses, as the minimum PMOS ON time of 40ns has been reached and the load current is further decreasing down to 2mA.

High-Efficiency Operation (Default Setting)

High-efficiency operation is enabled by setting the bit sd_low_noise [SD_control1] to 0.

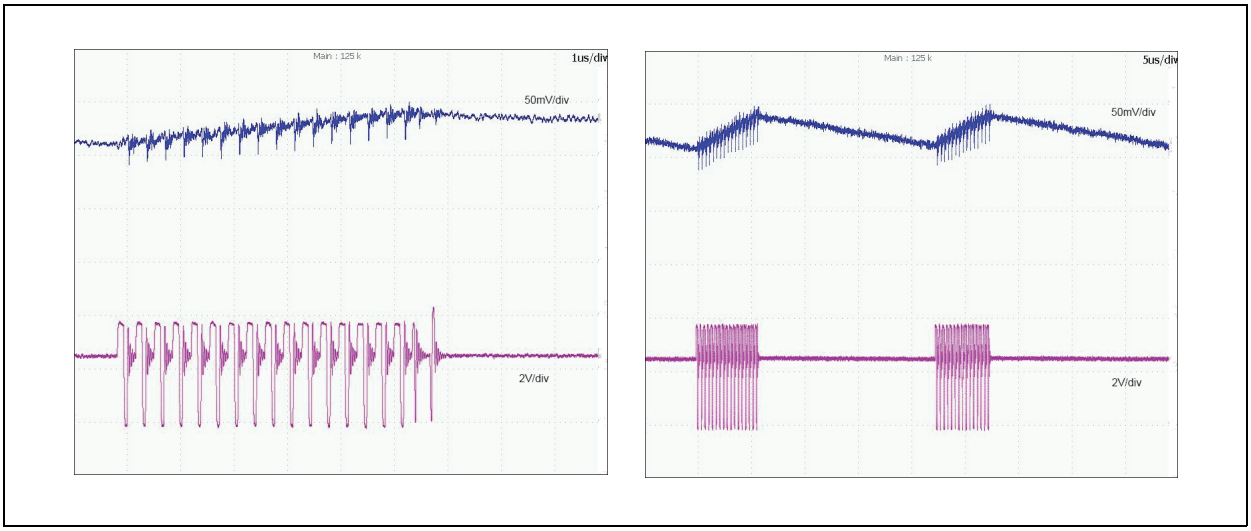
In this mode there is a minimum coil current necessary before switching OFF the PMOS. Resultant there are less pulses necessary at low output loads, and therefore the efficiency increases. As drawback, this mode increases the ripple up to a higher output current.

Figure 13:
Switching Behavior at Operating Point 1



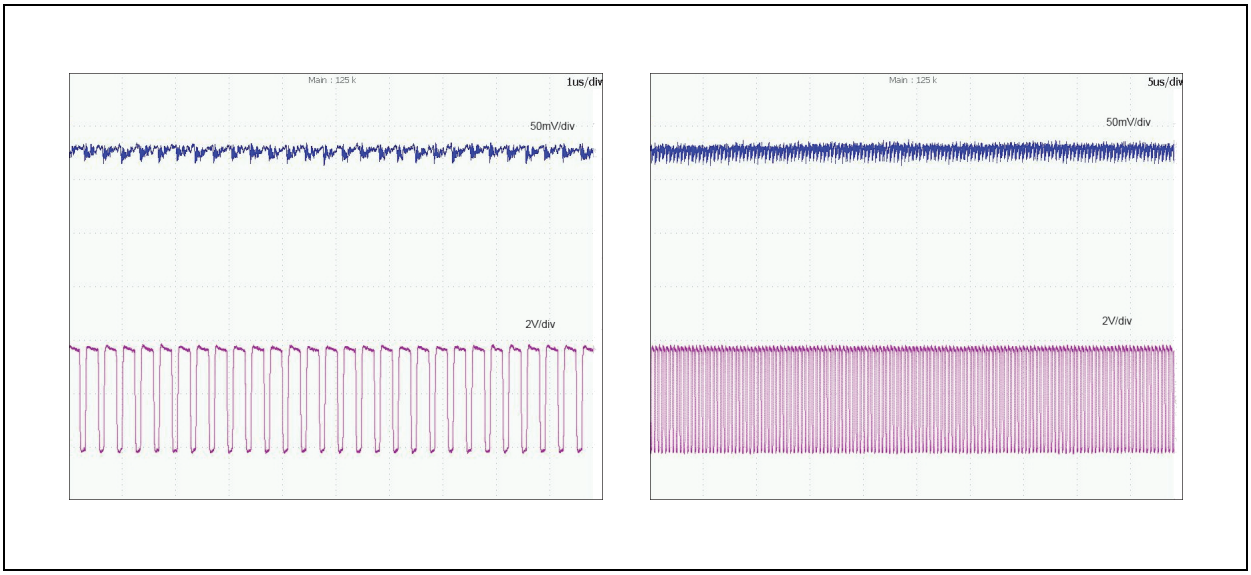
Operating Point 1: These graphs show the switching behavior referring to the operating point 1 from figure10. Here the mode is set to high efficiency operation and the DCDC is in skipping mode at 2mA load current. Here a minimum coil current during the PMOS ON time is needed, hence more energy can be stored, the duration between the bursts is longer and the efficiency increases.

Figure 14:
Output Voltage Ripple Measurement at Operating Point 3



Operating Point 3: These graphs show the switching behavior referring to the operating point 3 from figure10. Here the mode is set to high efficiency operation and comparing to operating point 4 the DCDC is still in skipping mode at 10mA load current and keeps the efficiency higher.

Figure 15:
Output Voltage Ripple Measurement at Operating Point 5



Operating Point 5: These graphs show the switching behavior referring to the operating point 5 from figure10. Here the load current is 100mA and high enough to keep the DCDC always in a continuous switching operation regardless of the mode setting.

Low Power Mode Operation (Automatically Controlled)

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/undershoots by immediately turning ON the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

Dynamic Voltage Management

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled with *dvm_enable [SD_control2]*. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. The DVM time can be chosen between 8us and 16us by setting the bit *dvm_time [SD_control2]*. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator.

The mode is enabled by setting the bit *sd_fast [SD_control1]* to 1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency can be set to 1, 2, 3 or 4MHz and this mode is selected by setting *sd1_freq [SD1Voltage]* and *sd1_fsel [SD_control1]* to the appropriate values.

Parameters

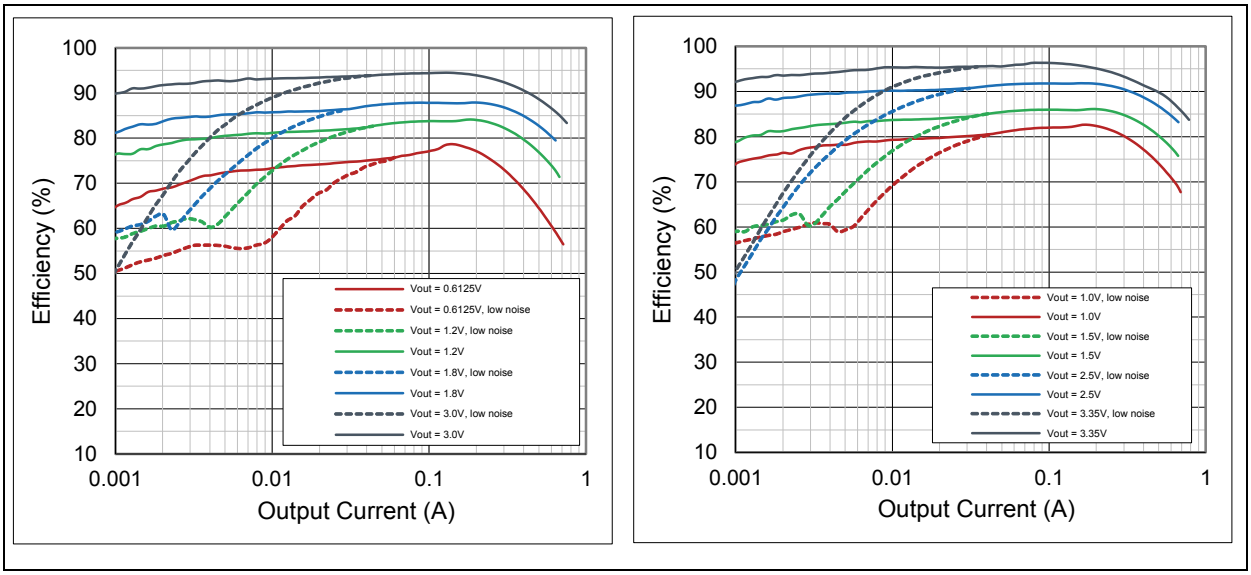
Figure 16:
DCDC Step-Down Converter Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input Voltage	Pin VSUP	2.7		5.5	V
V_{OUT}	Regulated Output Voltage		0.6125		3.35	V
V_{OUT_TOL}	Output Voltage Tolerance	min. 40mV	-3		+3	%
I_{LIMIT}	Current Limit			800		mA
R_{PMOS}	P-switch ON resistance			0.36	1	Ω
R_{NMOS}	N-switch ON resistance			0.33	1	Ω
f_{SW}	Switching Frequency		1	3	4	MHz
I_{LOAD}	Load Current			500		mA
I_{SUP_DCDC}	Current Consumption	Operating Current without Load		27		uA
		Shutdown Current		0.1		
t_{MIN_ON}	Minimum ON Time			40		ns

Figure 17:
DCDC Step-Down Converter External Components

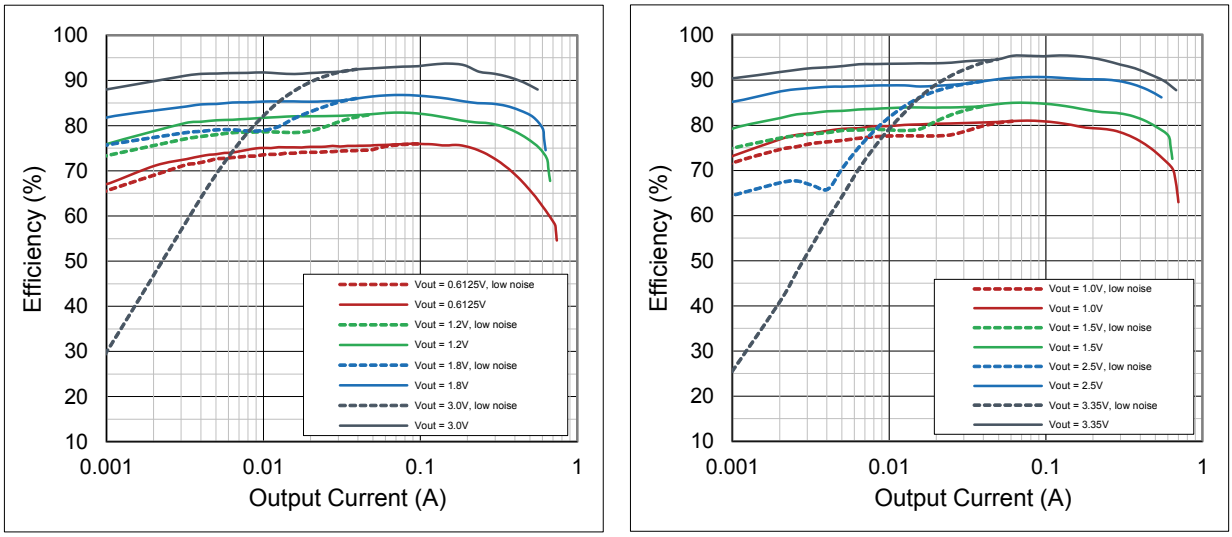
Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{FB_SD1}	Output Capacitor	Ceramic X5R or X7R	8	10		µF
C_{VSUP_SD1}	Input Capacitor	Ceramic X5R or X7R		2.2		µF
L_{SD1}	Inductor	4MHz operation		1		µH
		3MHz operation		1		
		2MHz operation		1		
		1MHz operation		2.2		

Figure 18:
DCDC Step Down Converter Efficiency vs. Load Current at 1MHz



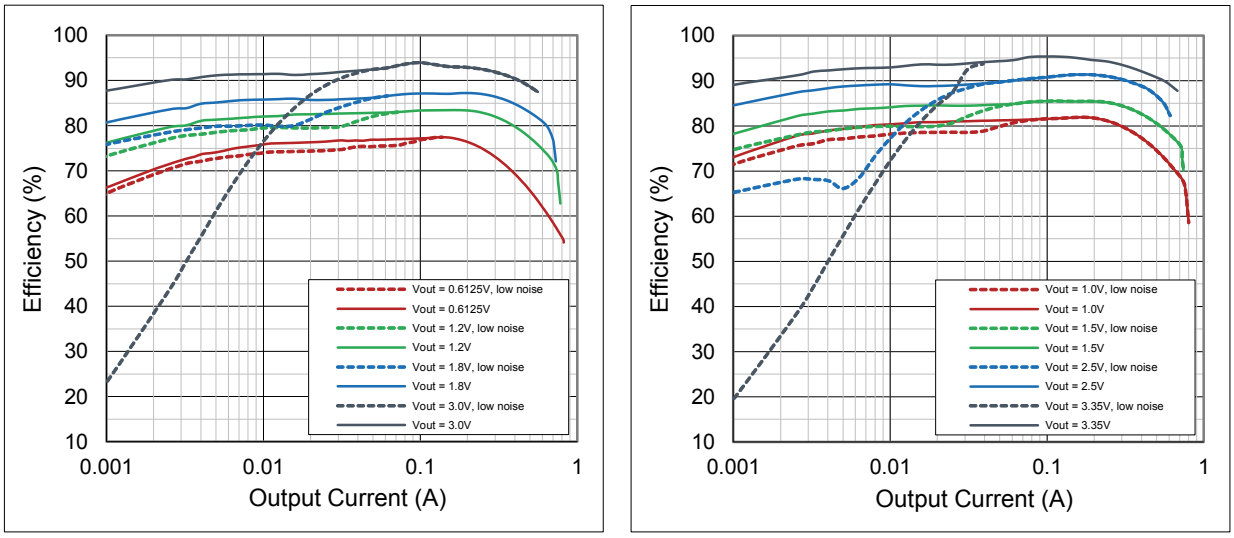
DCDC Efficiency vs. Output Current: V_{SUP} = 3.7V, f_{SW} = 1MHz, Murata LQM2HPN2R2MG0L 2.2µH coil, T_{AMB} = 25°C.

Figure 19:
DCDC Step Down Converter Efficiency vs. Load Current at 2MHz



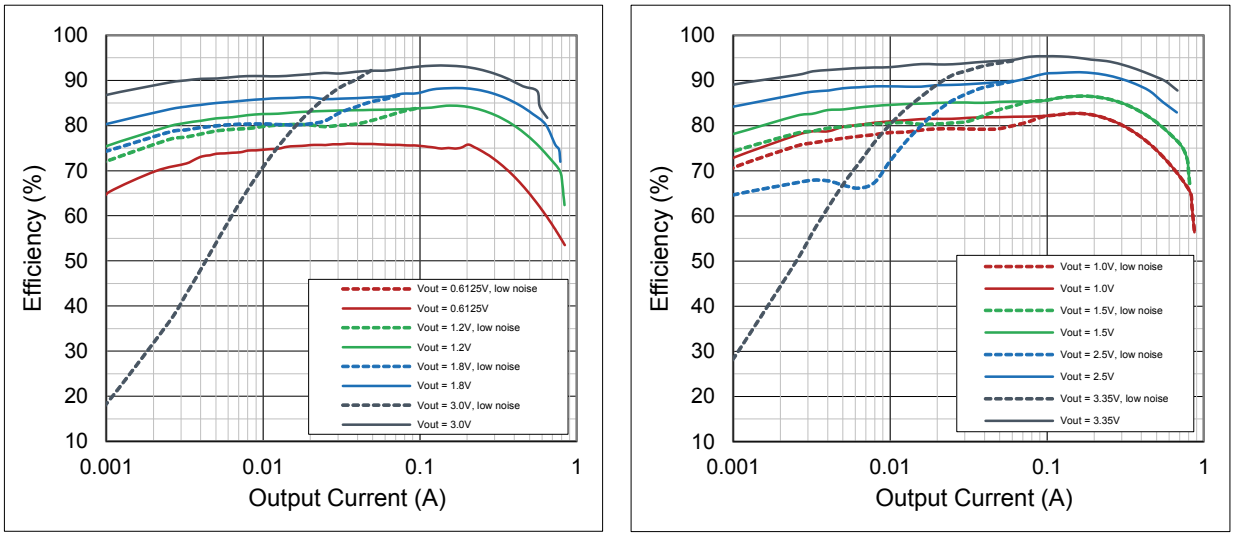
DCDC Efficiency vs. Output Current: V_{SUP} = 3.7V, f_{SW} = 2MHz, Murata LQM2HPN1R0MG0L 1uH coil, T_{AMB} = 25°C.

Figure 20:
DCDC Step Down Converter Efficiency vs. Load Current at 3MHz



DCDC Efficiency vs. Output Current: V_{SUP} = 3.7V, f_{SW} = 3MHz, Murata LQM2HPN1R0MG0L 1uH coil, T_{AMB} = 25°C.

Figure 21:
DCDC Step Down Converter Efficiency vs. Load Current at 4MHz

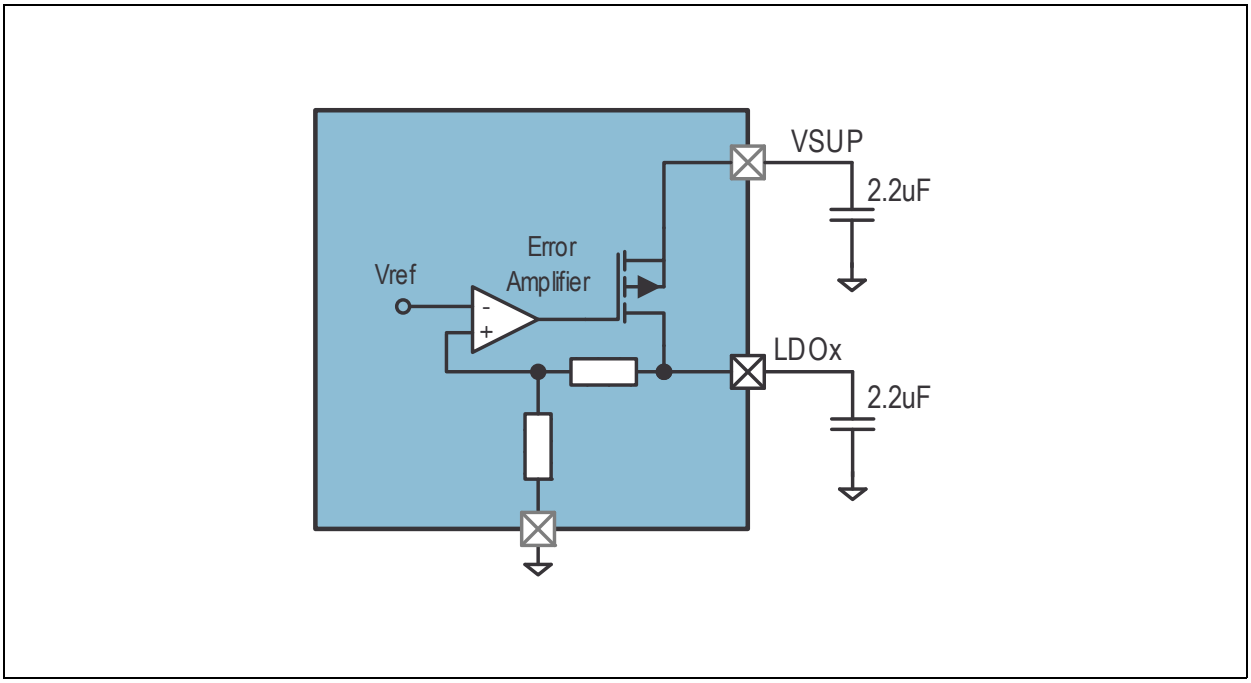


DCDC Efficiency vs. Output Current: V_{SUP} = 3.7V, f_{SW} = 4MHz, Murata LQM2HPN1R0MG0L 1uH coil, T_{AMB} = 25°C.

Universal IO LDO Regulator

This LDO is a low-power and low-quiescent current linear-regulator specifically designed for space-limited applications. This device can supply loads up to 200mA and consist of an error amplifier, and a P-channel MOSFET pass transistor.

Figure 22:
Universal IO LDO Regulator Block Diagram



Parameters

Figure 23:
Universal IO LDO Regulator Electrical Characteristics

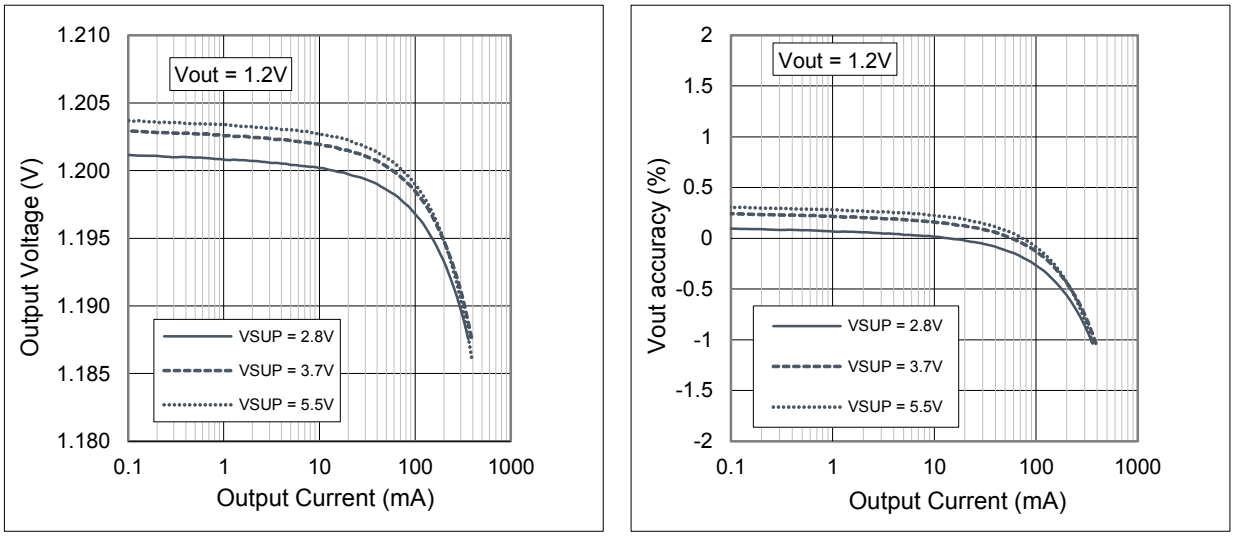
Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP	2.7		5.5	V
ΔV_{OUT}	Output voltage accuracy	I_{OUT} = 1mA, V_{OUT} > 2V T_{AMB} = 25°C	-2		+2	%
		I_{OUT} = 100uA to 200mA V_{OUT} > 2V	-3		+3	
		I_{OUT} = 1mA, V_{OUT} ≤ 2V T_{AMB} = 25°C	-20		+20	mV
		I_{OUT} = 100uA to 200mA V_{OUT} ≤ 2V	-50		+50	
V_{OUT}	Output voltage range		1.2		3.3	V

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{LNR}	Line regulation static	V_{IN} = 2.7V to 5.5V I_{OUT} = 1mA		0.07		%/V
	Line regulation dynamic	V_{IN} = 2.7V to 5.5V within 15us I_{OUT} = 1mA		20		mV
V_{LDR}	Load regulation static	I_{OUT} = 100uA to 200mA		0.014		%/mA
	Load regulation dynamic	I_{OUT} = 100uA to 200mA within 15us		30		mV
R_{ON}	ON resistance			0.5	1	Ω
I_{OUT}	Guaranteed load current	RMS	200			mA
I_{LIMIT}	Short-circuit	V_{OUT} = 0V		230		mA
I_Q	Quiescent current	no Load		5		uA
		I_{OUT} = 100µA		5		
		I_{OUT} = 200mA		15		
I_{OFF}	Shutdown supply current	LDO disabled		0.1	1	uA
t_{START}	Startup time			750		us
$t_{SHUTDOWN}$	Shutdown time			500		us

Figure 24:
Universal IO LDO Regulator External Components

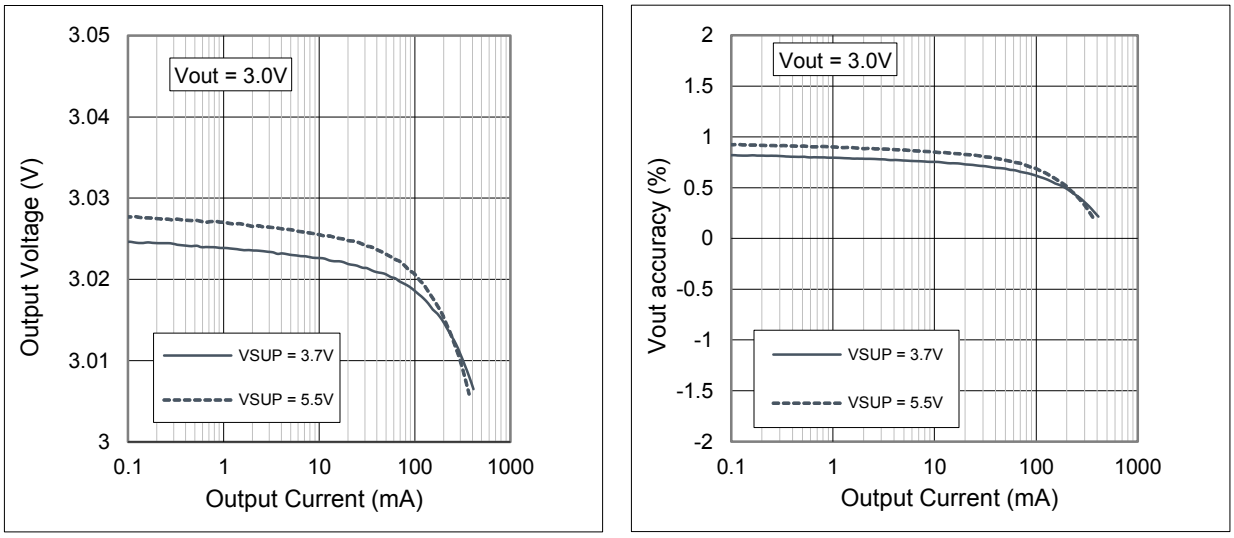
Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{LDOx}	Output capacitor	Ceramic X5R or X7R	2.2	10		µF

Figure 25:
LDO Output Voltage vs. Output Current 1/2



LDO Output Voltage vs. Output Current: V_{OUT} = 1.2V, T_{AMB} = 25°C.

Figure 26:
LDO Output Voltage vs. Output Current 2/2



LDO Output Voltage vs. Output Current: V_{OUT} = 3.0V, T_{AMB} = 25°C.

Figure 27:
LDO Load Transient Response 1/2

LDO Load Transient Response:
V_{SUP} = 3.7V, V_{OUT} = 1.2V, t_{RISE} = 15us,
I_{OUT} = 100uA to 200mA, T_{AMB} = 25°C.
(Blue channel: V_{OUT}; Red channel: I_{OUT})

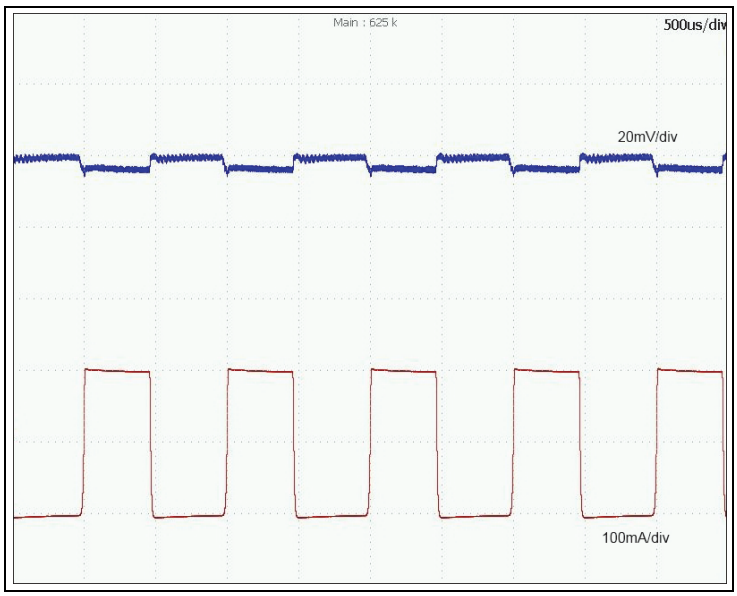
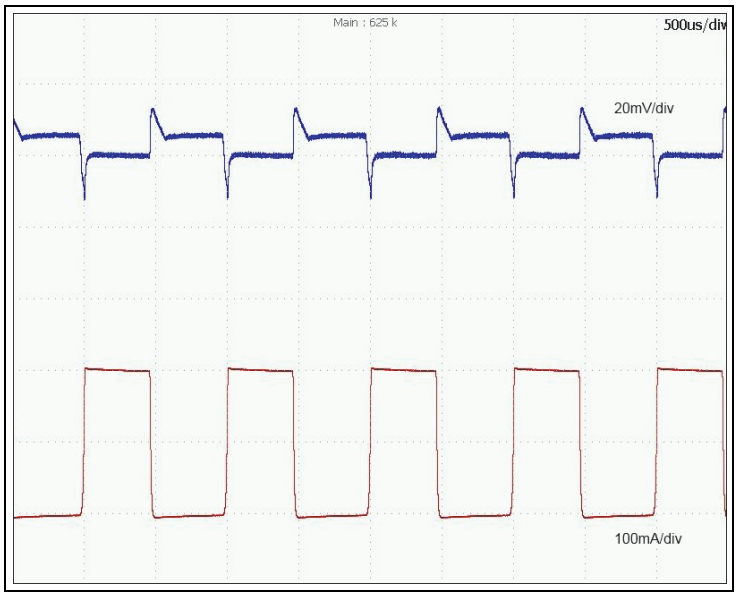


Figure 28:
LDO Load Transient Response 2/2

LDO Load Transient Response:
V_{SUP} = 3.7V, V_{OUT} = 3.0V, t_{RISE} = 15us,
I_{OUT} = 100uA to 200mA, T_{AMB} = 25°C.
(Blue channel: V_{OUT}; Red channel: I_{OUT})



Linear Charger

This block can be used to charge Li-Ion batteries. Requiring less external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

- Charge adapter detection
- Power Path management for dead battery startup
- Low current Trickle charging
- Constant current charging
- Constant voltage charging
- Operation without battery
- Battery presence indication
- NTC temperature supervision
- Input current limitation

Figure 29:
Linear Charger Block Diagram

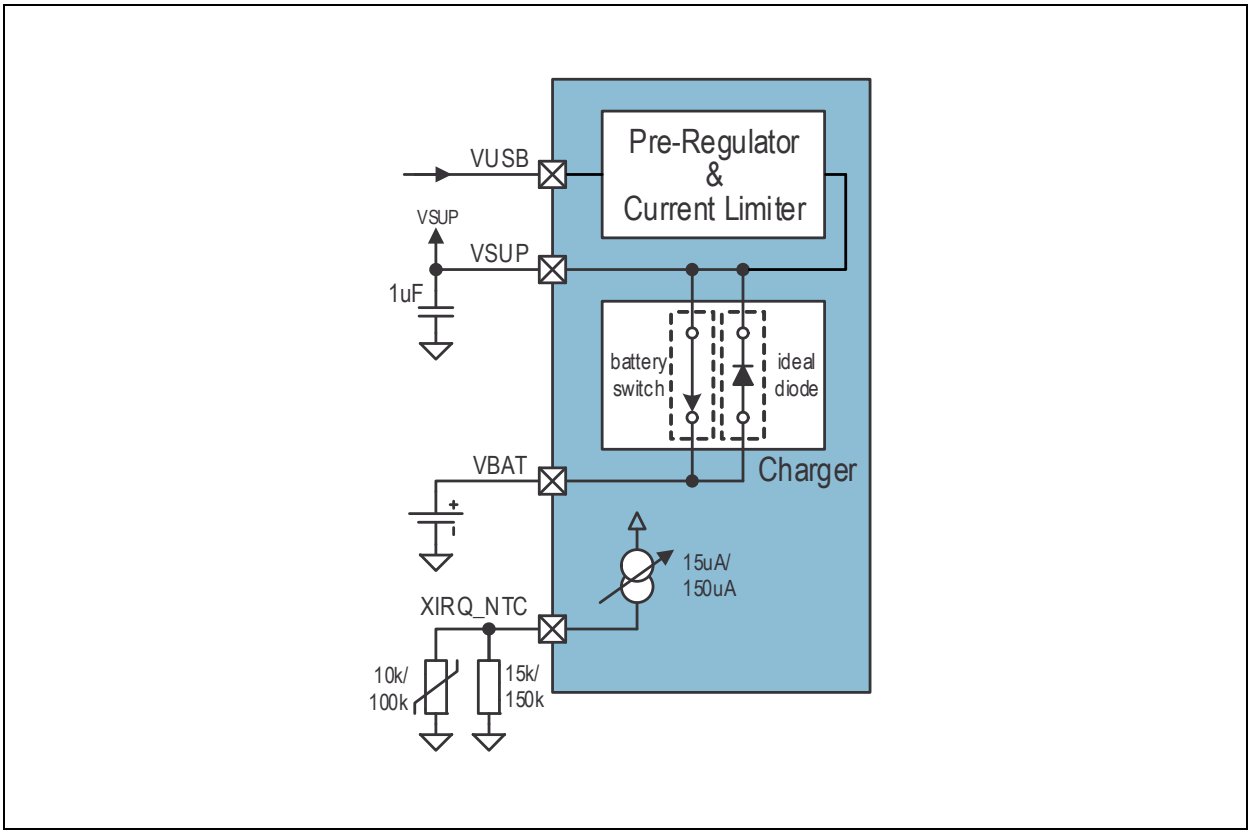
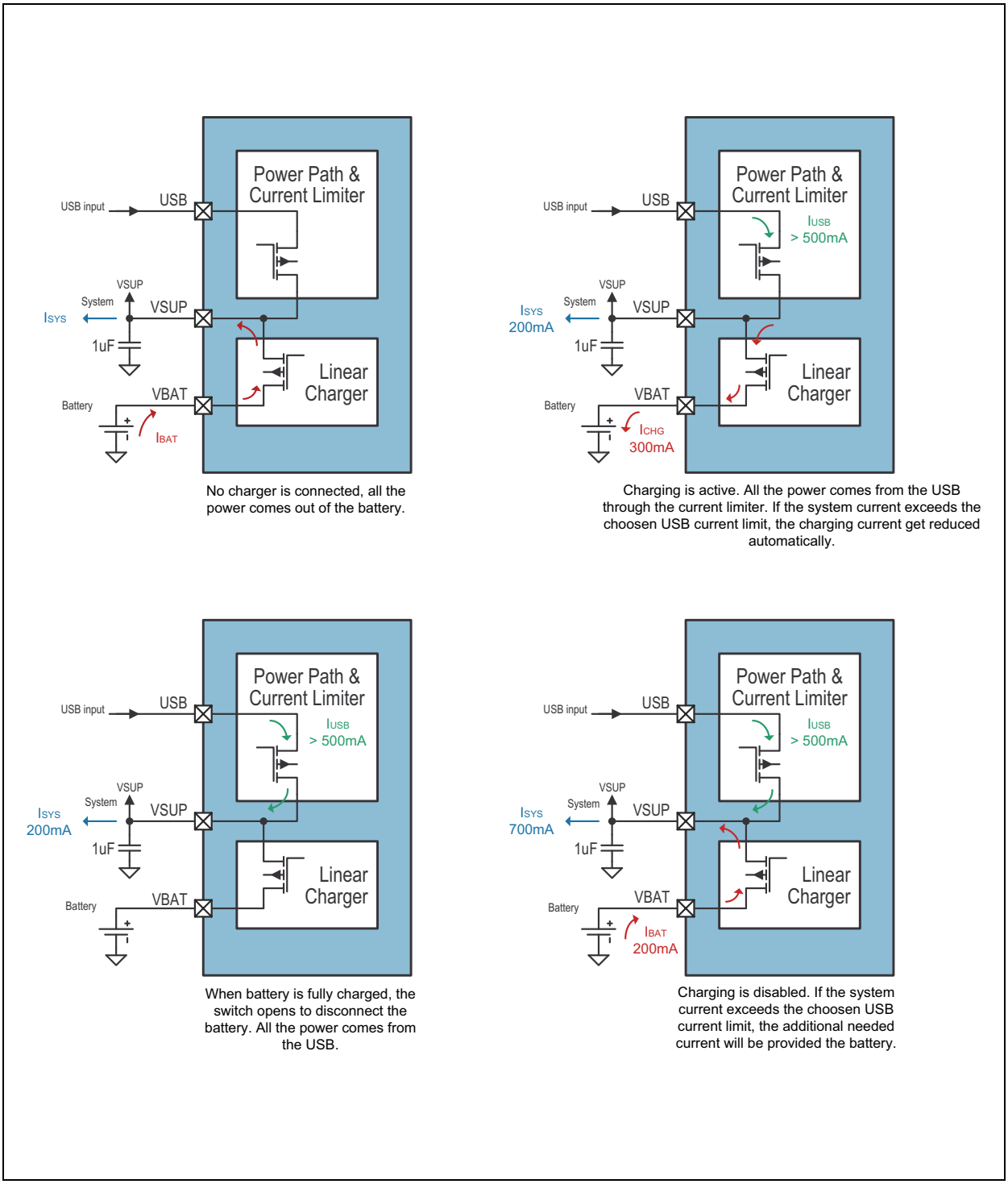


Figure 30:
Linear Charger Modes



Charging Modes: This figure describes the 4 different charger modes.

Charging Cycle Description

Charge Adapter Detection

The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VUSB pin. If the adapter voltage exceeds the battery voltage at pin VBAT by V_{CHDET} the *ChDet [ChargerStatus2]* will be set. The detection circuit will reset the charge controller (bit *ChDet* is cleared) as soon as the voltage at the VUSB pin drops to only V_{CHMIN} above the battery voltage. In case the AS3701 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VUSB pin. The Charger detection can be disabled by setting the bit *chdet_off [ChargerStatus2]* to "1", which results in a further decrease of internal power consumption.

Low Current (Trickle) Charging

Trickle charge mode is started when an external charge adapter has been detected, the bit *bat_charging_enable [ChargerControl]* is set and the battery voltage at pin VBAT is below the $V_{TRICKLE}$ threshold; bits *ChDet* and *Trickle [ChargerStatus1]* will be set. In this mode the charge current will be limited to TrickleCurrent *[ChargerCurrentControl]* to prevent undue stress in case of deeply discharged batteries. Once $V_{TRICKLE}$ has been exceeded, the charger will change over to constant current charging (Trickle is cleared).

Constant Current Charging

Constant current charging is initiated when *bat_charging_enable [ChargerControl]* and the battery voltage at pin VBAT is above the $V_{TRICKLE}$ and below V_{CHOFF}. The bit *CCM [ChargerStatus1]* is set when the charger has started, and the charge current will be limited by the battery charge controller. The current for the Constant Current Charging can be selected out of the range defined in *ConstantCurrent [ChargerCurrentControl]* if the bit *cc_range_select [ChargerControl]* is set to "0" or out of the range defined in *TrickleCurrent [ChargerCurrentControl]* if the bit *cc_range_select [ChargerControl]* is set to "1". When the battery approaches full charge, its voltage will reach the charge termination threshold V_{CHOFF}. V_{CHOFF} depends on the *ChVoltEOC [ChargerVoltageControl]* bits settings. Top-OFF charge will be started and the bit *CVM [ChargerStatus1]* will be set.

Constant Voltage Charging

Constant voltage charge mode is initiated and the bit *CVM [ChargerStatus1]* will be set when the V_{CHOFF} threshold has been reached. The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drops below 5% or 50% of the Constant Current value (depends on the

setting of the bit *eoc_current [ChargerCurrentControl]*). If the measured charge current is less than or equal to *eoc_current*, the charging cycle is terminated and *EOC [ChargerStatus1]* is set.

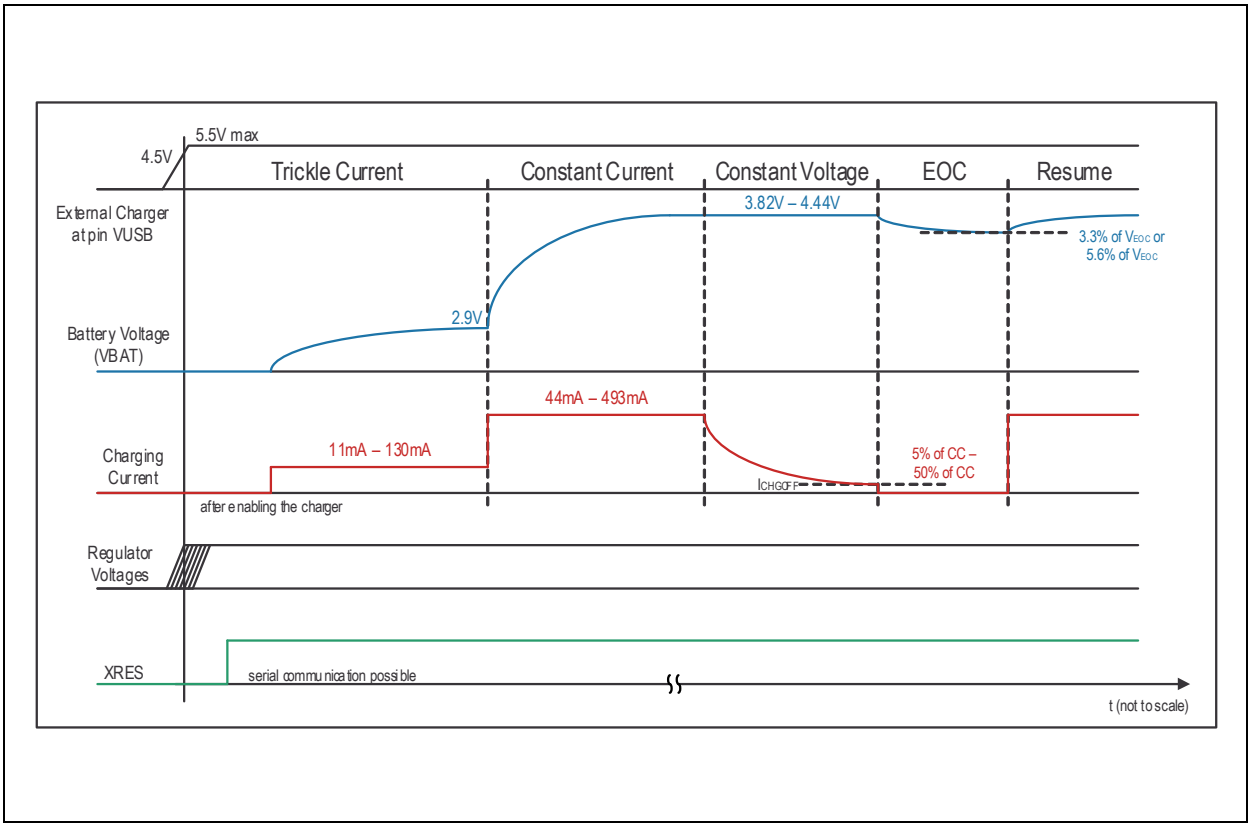
Resume

If EOC is reached and the bit *AutoResume [ChargerControl]* is set, the charging will immediately start again, if the battery voltage falls below the specified resume voltage *ChVoltResume [ChargerConfig1]*. This voltage can be set either to 3.33% or 5.56% of *ChVoltEOC [ChargerVoltageControl]*.

Figure 31:
Resume Voltage Levels

ChVoltResume	ChVoltEOC						
	3.82V	3.84V	…	4.20V	…	4.42V	4.44V
3.33%	127mV	128mV	…	140mV	…	147mV	148mV
5.56%	212mV	213mV	…	233mV	…	246mV	247mV

Figure 32:
Linear Charger States



Charging States: This figure describes the characteristics of the charging current and the battery voltage for each different charging state.

Stop Charging Conditions

There are multiple safety features implemented triggering a stop_charging condition.

These are the following:

- Battery temperature is too high: If *ntc_high_on [ChargerSupervision]* = 1 and the voltage at pin NTC (GPIO3, GPIO4 or XIRQ_NTC) is below $V_{BATTEMP}$.
- Battery temperature is too low: If *ntc_low_on [ChargerSupervision]* = 1 and the voltage at pin NTC (GPIO3, GPIO4 or XIRQ_NTC) is above $V_{BATTEMP}$.
- Charging timeout timer expired: If *ch_timeout [ChargerConfig2]* > 0 and charging time has been exceeded. (Can be reset by unplugging the charger, setting *bat_charging_enable [ChargerControl]* = 0 or writing *charging_tmax [ChargerConfig2]* = 0)
- Die temperature > 140°C (*ov_temp_140 [OvertemperatureControl]* is set)
- Reset is initiated (each Reset reason forces a stopping of the charging)

Battery Presence Indication

After EOC state is reached, a timer for NOBAT detection is started. If there is no battery present, the VBAT voltage will drop to VRESUME. Depending on the load on VBAT and the capacitor on VBAT this might take some milliseconds to 1 second. If *AutoResume [ChargerControl]* is enabled, the charger will restart charging (Constant Current Charging) after 100ms delay.

The 100ms dead time is necessary to get a battery oscillation frequency below 10Hz, if there is no battery present.

If the NOBAT detection timer is below 2 seconds after reaching the EOC state, and this happens 2 times in serial, the bit *NoBat [ChargerStatus1]* is set. If a battery is inserted, the bit will be reset after the timer exceeds the 2 seconds.

NTC Supervision

Configuration

The AS3701 also features a supply for an external NTC resistor to measure the battery temperature while charging. For AS3701A, the pin XIRQ_NTC can be used as the NTC input pin, whilst AS3701B additionally offers the GPIO3 and GPIO4. With the bit *NTC_input [ChargerSupervision]* the NTC Supervision can be configured.

Figure 33:
NTC Supervision Configuration

NTC_input		NTC Supervision Configuration
0	0	no NTC supervision (1)
0	1	XIRQ_NTC pin
1	0	GPIO3 pin (2)
1	1	GPIO4 pin (2)

Note(s):

1. If no NTC supervision is selected, all NTC relevant bits are ineffective
2. AS3701B only

NTC Resistor

Depending on the used resistor value of the NTC (10k or 100k) the internal NTC current (150uA for 10k or 15uA for 100k) can be selected via *ntc_10k [ChargerSupervision]*.

High/Low Temperature

The battery high temperature supervision can be enabled with *ntc_high_on [ChargerSupervision]*. If the temperature is higher than 45°C or 60°C (depending on *ntc_mode [ChargerSupervision]*) the charger will stop operation. When the battery temperature drops and the voltage on NTC pin rises above $V_{BATTEMP\_HIGH\_OFF}$, the charger will start charging again.

The battery low temperature supervision can be enabled with *ntc_low_on [ChargerSupervision]*. If the temperature is lower than 0°C the charger will stop operation. When the battery temperature rises and the voltage on NTC pin falls below $V_{BATTEMP\_LOW\_OFF}$, the charger will start charging again.

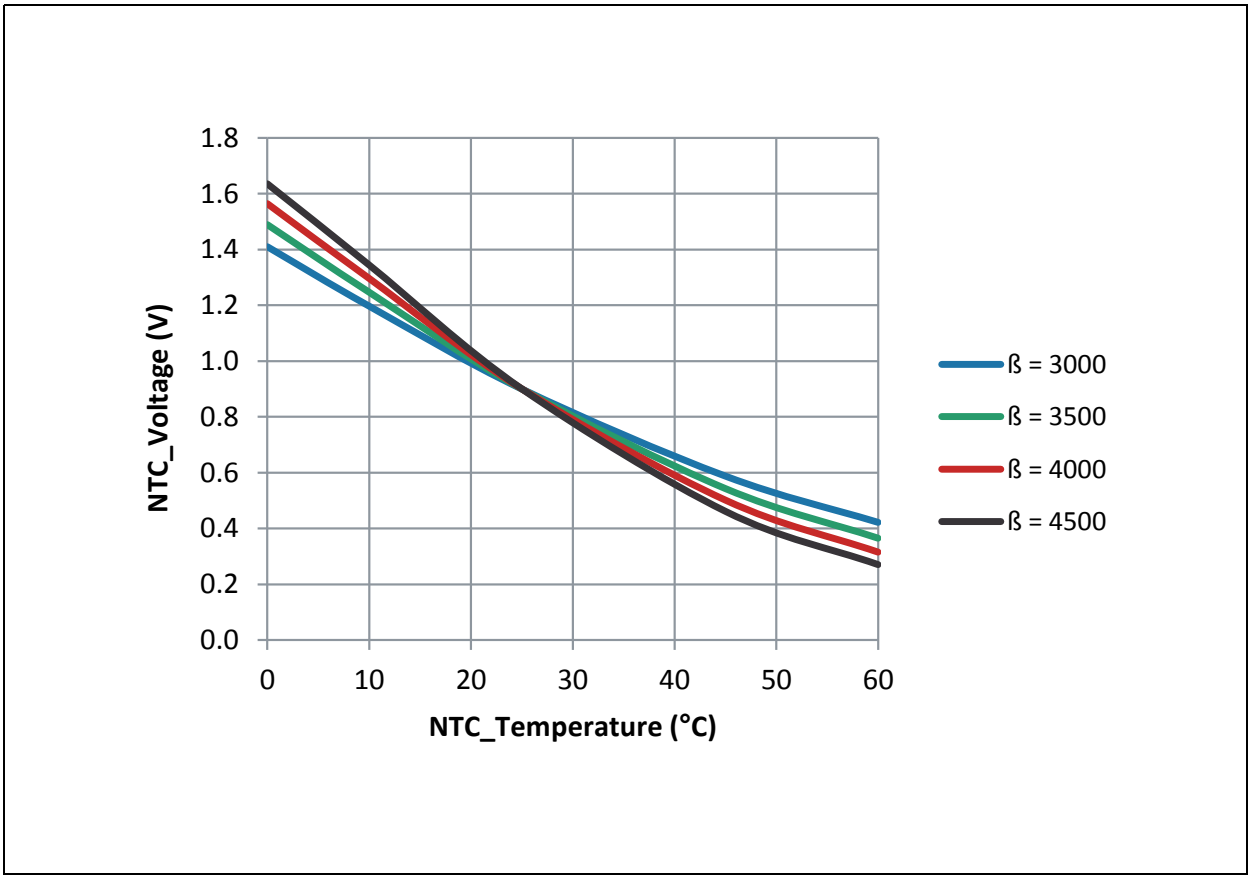
For the high and low temperature supervision a temperature hysteresis is included to avoid an oscillation of the charger.

The supply for the NTC will be on when either the *ntc_ high_on* or *ntc_low_on* bit is set, no matter if a charger is detected or not.

NTC ß-Correction

To keep the voltage drop over the whole temperature range inside of the comparator threshold voltage range, a 15k (150k) parallel resistor to the 10k (100k) NTC is needed. With the bit *ntc_beta [ChargerSupervision]* 4 different ß-values depending on the used NTC resistor can be selected.

Figure 34:
NTC ß Influence Over Temperature



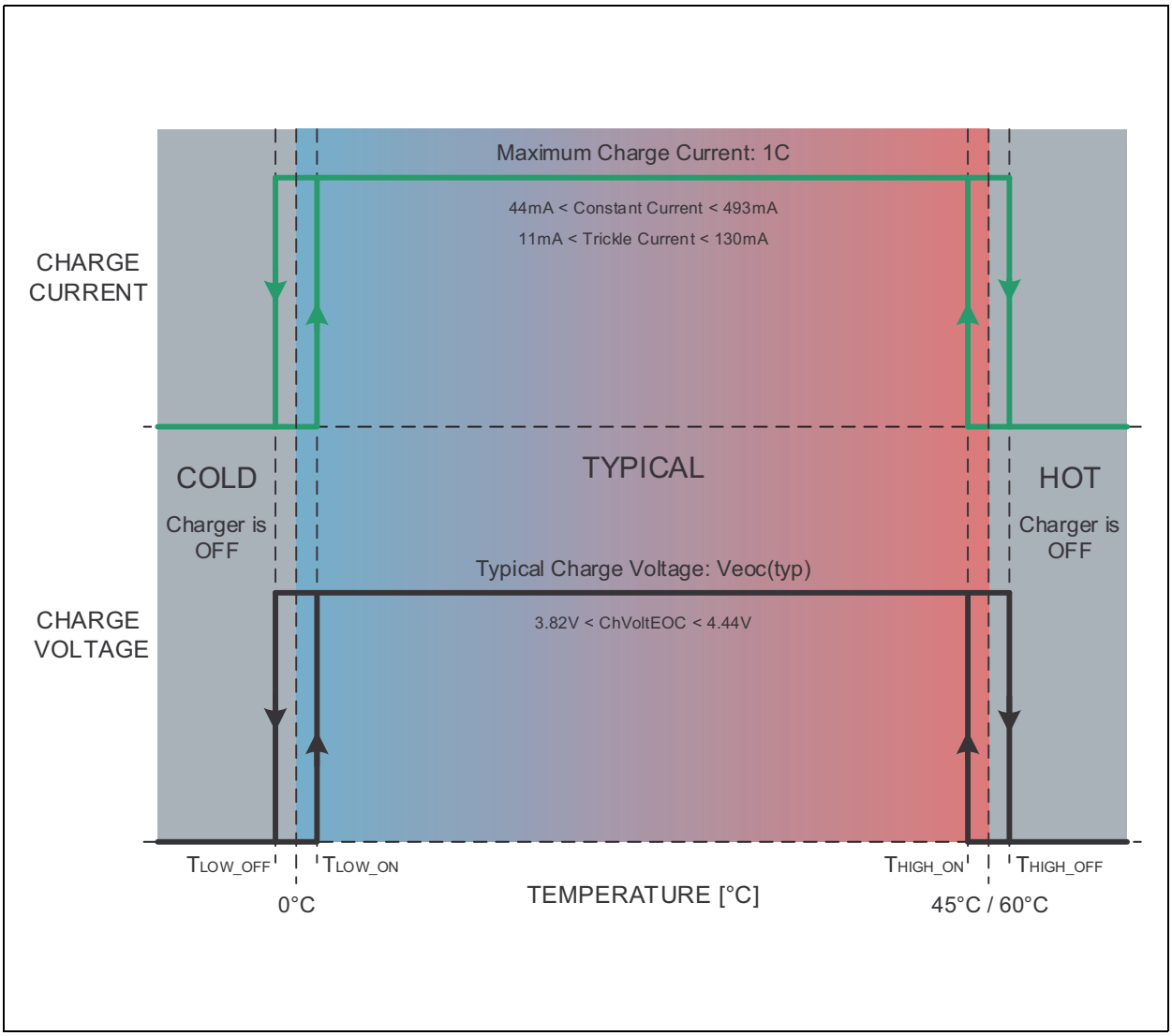
NTC ß Influence Diagram: Shows the voltage drop over the NTC resistor depending on the temperature for 4 different ß values using R_{NTC}=10kΩ, R_p=15kΩ and I_{NTC}=150uA.

Figure 35:
NTC Threshold Voltages

Temperature		ß				Unit
		3000	3500	4000	4500	
Low temperature	0°C	1.41	1.49	1.56	1.63	V
High temperature	45°C	0.59	0.54	0.50	0.46	V
	60°C	0.42	0.37	0.31	0.27	V

NTC Supervision: Comparator threshold voltages for different temperatures and ß using R_{NTC}=10kΩ, R_p=15kΩ and I_{NTC}=150uA.

Figure 36:
High/Low Temperature Supervision



Temperature Supervision Diagram: Shows the voltage and current settings for the high and low temperature supervision.

Parameters

Figure 37:
Linear Charger Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
$I_{TRICKLE}$	Trickle current	11 steps programmable		11.. 130		mA
$V_{TRICKLE}$	Trickle to constant current threshold	V_{BAT} rising		2.9		V
I_{CHG}	Constant current	*cc_range_select* = 0		44.. 493		mA
		cc_range_select = 1		11.. 130		mA
		@ 70mA	-8%	70	+8%	mA
V_{EOC}	Charge termination threshold	Programmable in 20mV steps		3.82.. 4.44		V
		end of charge is true	4.15	4.2	4.25	V
I_{EOC}	EOC current level	referring to I_{CHG} (VSUP > 3V)		5.. 50		%
I_{USB_limit}	VUSB input current limit	@470mA	420	470	500	mA
V_{SUP_prereg}	Voltage supplied from Preregulator	Depending on the bit *vsup_voltage*		4.4.. 5.5		V
V_{RESUME}	Resume Voltage limit to start charger	VBAT falling threshold referring to V_{EOC} (depending on bit *ChVoltResume*)		3.3 5.6		%
$VSUP_{MIN}$	VSUP level for charging current reduction, to avoid voltage drop on VSUP	Trickle or constant current will be regulated down, if VSUP drops below this threshold	-6%	3.9	+3%	V
				4.2		
				4.5		
				4.7		
V_{CHDET}	Charger detection hysteresis	V_{USB} - V_{BAT} Hysteresis is > 40mV	50	75	105	mV
V_{CHMIN}			0	20	35	mV
I_{REV_OFF}	Reverse current shut down	VSUP = 5V, V_{USB} open		<1		uA
R_{ON_BATSW}	Battery switch ON-resistance			0.4		Ω

Current Sinks

The following description of the Current Sinks refers only to the pins GPIO1_CURR1 and GPIO2_CURR2. Hence the suffix "X" stands either for 1 or for 2.

The AS3701 contains 2 GPIO pins (GPIO1_CURR1 and GPIO2_CURR2), providing general purpose current sinks when the register *gpioX_mode [GPIOXcontrol]* is set to CURRx input. Next to this setting, the register *gpioX_iosf [GPIOXcontrol]* must be set to one of the GPIO output functions (please see the GPIO section in the following chapter "Detailed Description – System Functions").

Parameters

Figure 38:
Current Sinks Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
I_{CURRx}	CURR1_current = 01h – FFh CURR2_current = 01h – FFh	Resolution = 156.86uA	0.16		40	mA
I_{CURRx_TOL}	CURR current accuracy	CURRx_current = 40h	9.3	10	10.7	mA
V_{CURRx}	Voltage compliance	During normal operation	0.5		5.5	V
$V_{PROTECT}$	Maximum voltage at pin CURRx to protect driver transistor	I_{SINK} > 20mA guaranteed by design			V_{BAT} + 2V	V

Detailed Description – System Functions

Start-Up

Normal Start-Up

The following gives a brief description on a start-up from scratch (battery or charger insertion). More details can be found in the start-up flow chart.

A start-up can be activated from 5 different sources:

- Battery insertion from scratch
- Charger insertion from scratch (VBAT < *ResVoltFall*)
- ON-key has been pulled high in power_off mode
- Reset cycle
- *ResVoltRise* level was reached

During a normal reset cycle a normal startup happens:

- Setting USB current limit and ResVoltRise
- Startup State machine reads out the internal Boot-OTP. The start-up sequence of SD Converter, LDOs and GPIOs are controlled by the Boot-OTP
- Reset-Timer is set by the Boot-OTP
- The reset is released when the Reset Timer expires (external pin XRES)

Parameter

Figure 39:
Start-Up Condition

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{ON_IL}	Low level voltage	ON pin			0.4	V
V_{ON_IH}	High level voltage	ON pin	1.4			V
I_{ON_PD} (1)	Pull down current	Bit *on_invert* = 0 (active high)	4	12		uA

Note(s):

1. The internal pull-down resistor is just active if the bit on_invert is set to "0" (active high configuration). If the ON-key works active low (on_invert = 1) the internal pull-down resistor is deactivated and an external pull-up resistor is needed in push-button configuration!

Figure 40:
Start-Up Flowchart

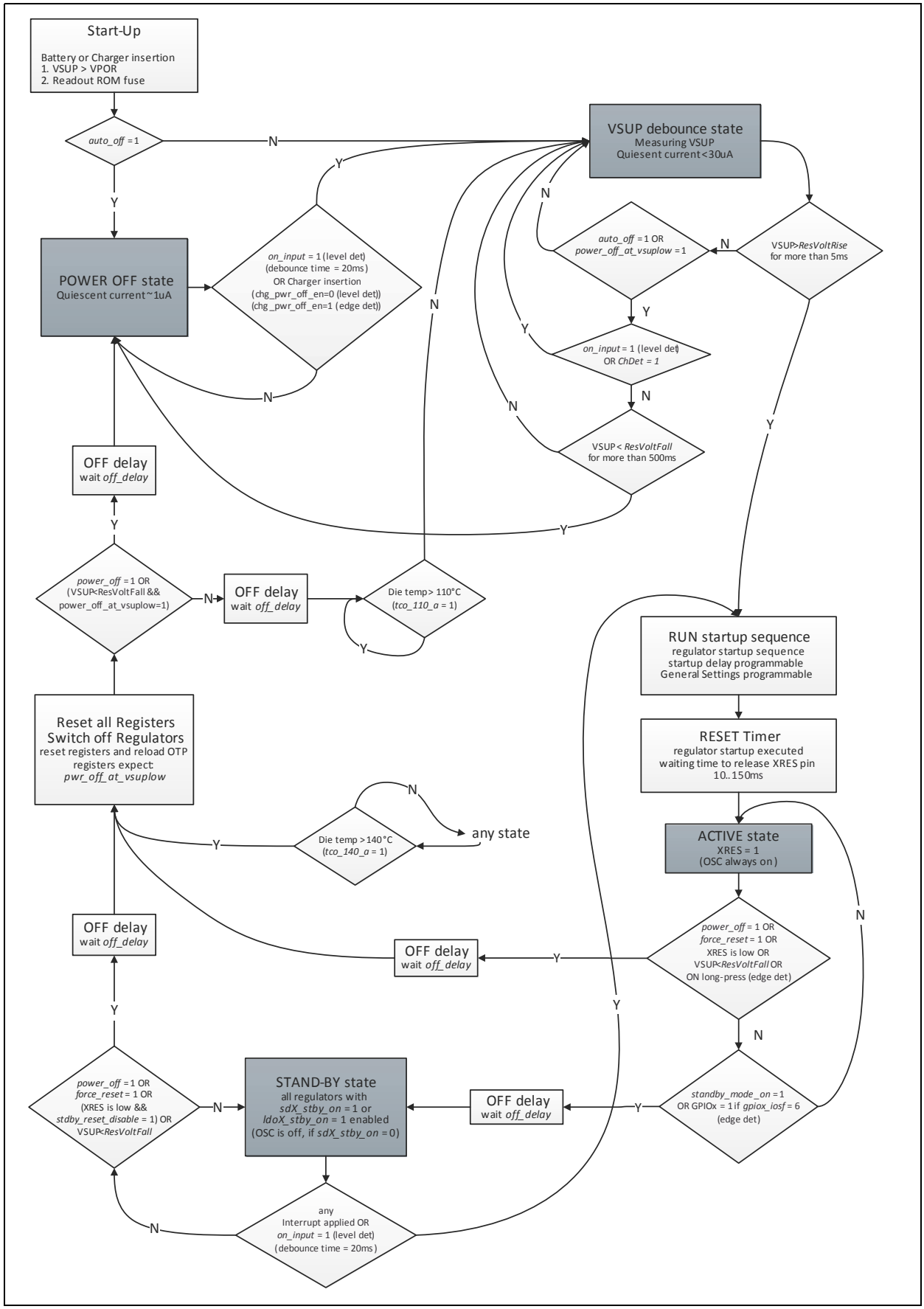
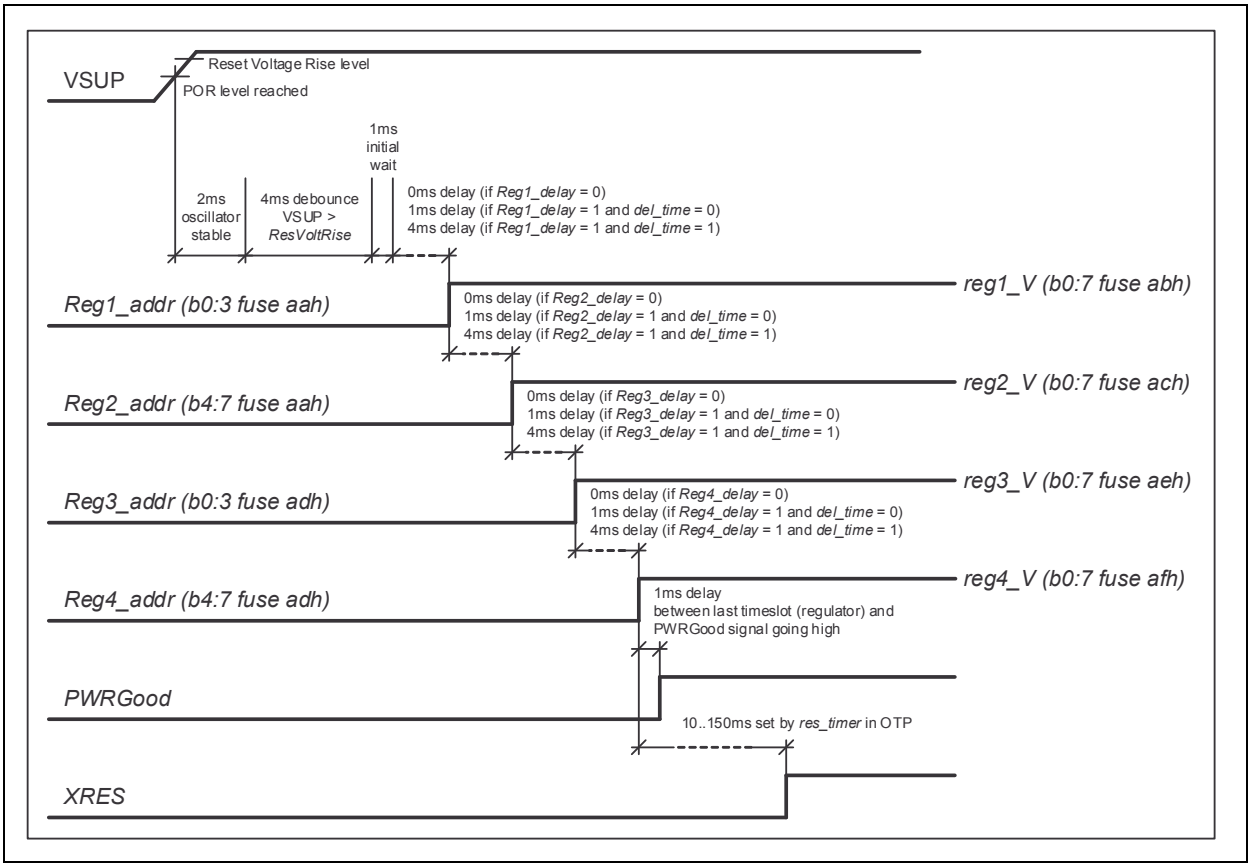
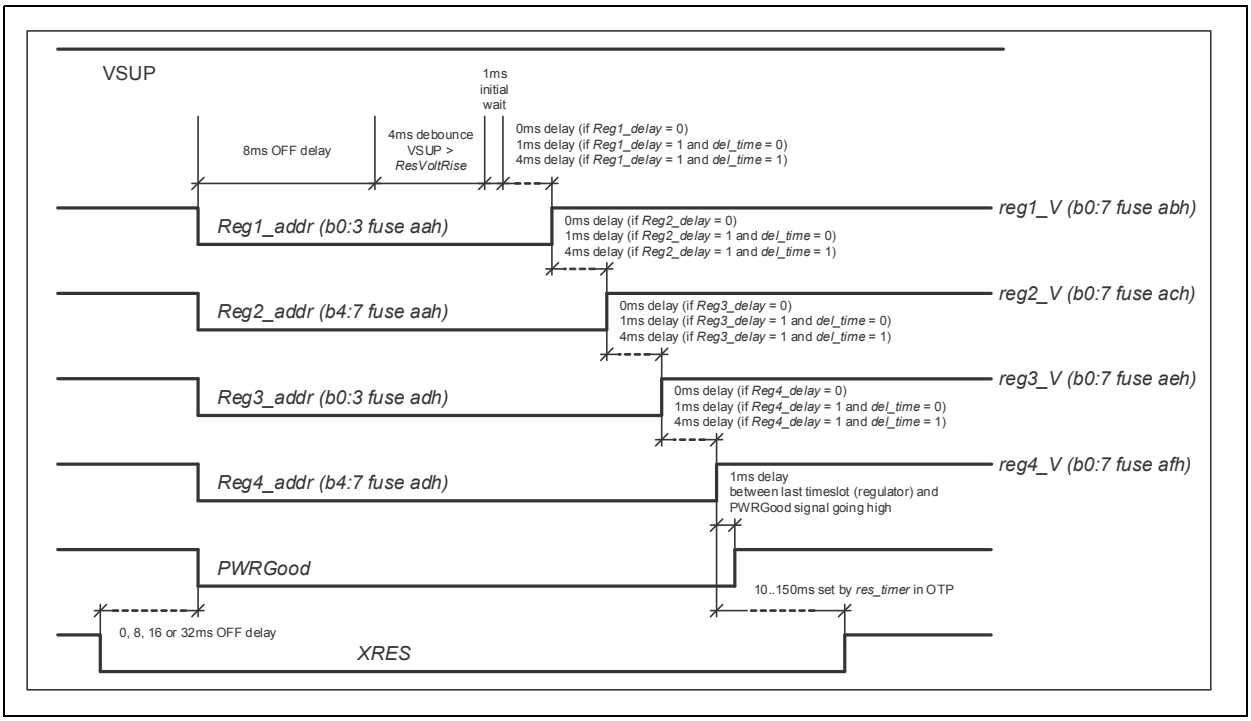


Figure 41:
Start-Up Sequence Diagram 1/2



Start-Up Sequence: This diagram shows the timing of a startup from scratch (battery or charger insertion)

Figure 42:
Start-Up Sequence Diagram 2/2



Start-Up Sequence: This diagram shows the timing of a reset command followed by a startup

Reset

XRES is a low active bi-directional pin. An external pull-up to the periphery supply has to be added. During each reset cycle the following states are controlled by the AS3701:

- Pin XRES is forced to GND
- Normal startup with programmable power-ON sequence and regulator voltages
- Reset is active until the programmable reset timer (set by res_timer [ResetTimer]) expires
- All registers are set to their default values after power-ON, except the reset control- and status-registers.
- XRES is pulled high by the external resistor and the whole system is leaving the reset state

Note(s): Programming is controlled by the internal Boot-OTP

RESET Reasons

Reset can be activated from the below mentioned different sources:

- VPOR has been reached (VSUP rising from the scratch)
- ResVoltFall was reached (VSUP < ResVoltFall [Battery_voltage_monitor])
- Software forced reset (*force_reset [ResetControl]* = 1)
- XRES is pulled to low
- ON-key long press (on_tast_sw is set to "0")
- Over-temperature

Voltage Detection

A Reset gets initiated, if VSUP rises from scratch and reaches the V_{POR} level. The pin XRES is only released if VSUP is above *ResVoltRise*.
V_{XRES_fall} is only accepted if the reset condition is longer than V_{XRES_mask}. This guard time is used to avoid a complete reset of the system in case of short drops of VSUP.

Software Forced Reset

Writing “1” into the register bit *force_reset [ResetControl]* immediately starts a reset cycle. The bit *force_reset* is automatically cleared by this reset.

External Triggered Reset

If the pin XRES is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

Long ON-Key Press

For a reset initiated with a long ON-key press, this feature must be enabled by setting the bit *onkey_lpress_en [ResetControl]* to "1". When applying a high level on the ON input pin for 4s/8s (depending on *on_lpress_delay [ReferenceControl]*) a reset gets initiated, if the bit *onkey_lpress_reset [ReferenceControl]* is set to "1". This is thought as a safety feature when the SW hangs up. A long ON key reset is just possible, if the ON key works as a push-button (*on_tast_sw [ReferenceControl]* is set to "0")

Figure 43:
ON-Key Long Press RESET Behavior

onkey_ lpress_en	onkey_ lpress_reset	on_ lpress_ delay	on_tast_sw	Long Press Behavior
0	X	X	X	No ON-key long press reset possible
1	1	0	0	8s long press on the ON-push-button forces a reset
1	1	1	0	4s long press on the ON-push- button forces a reset
1	1	X	1	No reset possible, if ON-key works as a switch

Over-Temperature Reset

A reset cycle is getting started, if the over-temperature threshold is reached and the bit *ov_temp_140 [OvertemperatureControl]* is set.

Parameter

Figure 44:
XRES Input Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{XRES_IL}	RESET low level voltage				20% of VSUP	V
V_{XRES_IH}	RESET high level voltage		60% of VSUP			V

Figure 45:
Reset Levels

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{POR}	Overall power on reset	Monitor on VSUPpower ON reset for all internal functions	1.5	2.0	2.3	V
V_{XRES_rise}	RESET level for V_{SUP} rising	Monitor voltage on VSUP rising level		ResVolt Rise(1)		V
V_{XRES_fall}	RESET Level for V_{SUP} falling	Monitor voltage on VSUP falling level		2.7		V
		if *SupResEn* = 1 only		ResVolt Fall(2)		V
V_{XRES_mask}	Mask time for VXRES_fall Duration for VBAT < ResVoltFall until a reset cycle is started (3)	*FastResEn* = 0		3		ms
		FastResEn = 1		64		us

Note(s):

1. The selection of the range and level is done via OTP. It´s recommended to set the ResVoltRise level 200mV above the ResVoltFall level to have a hysteresis
2. 2.7V is the default value, other levels can be set via SW
3. XRES signal is debounced with the specific mask time for rising- and falling slope of V_{BAT}

Stand-By

Stand-by allows shutting down all rails or just a selected number and can be achieved by one of the following cases:

Enter Via GPIO

To enter the Stand-by mode via GPIO command, the following settings have to be done:

- Enable just these interrupt sources which should lead to leave the stand-by mode
- Make sure that the specified interrupt is inactive (clear the Register *[InterruptStatus]* by register reading)
- Set the *gpioX_mode [GPIOxcontrol]* to input and the *gpioX_iosf [GPIOxcontrol]* should be set to *Stand-by + vselect input* (*gpioX_iosf = 6)*
- Set *RegX_select [Reg_Control]* and *RegX_voltage [RegX_Voltage]* if another voltage is needed during stand-by for up to 2 regulators
- Define which regulators should be kept powered during Stand-by mode (*sdX_stby_on* and *ldoX_stby_on [Reg_standby_mod1]*)
- Set the *off_delay [Startup_Control]* for going into stand-by after the GPIO command
- Activate the selected GPIO

Enter Via SW

To enter the Stand-by mode via I²C command, the following settings have to be done:

- Enable just these interrupt sources which should lead to leave the stand-by mode
- Make sure that the specified interrupt is inactive (clear the Register *[InterruptStatus]* by register reading)
- Define which regulators should be kept powered during Stand-by mode (*sdX_stby_on* and *ldoX_stby_on [Reg_standby_mod1]*)
- Set the *off_delay [Startup_Control]* for going into stand-by after the I²C command
- Set *standby_mode_on [ReferenceControl]* to 1

During Stand-by all regulators are switched OFF, except those, which are selected either with *RegX_select [Reg_Control]* or with *sdX_stby_on* and *ldoX_stby_on [Reg_standby_mod1]*. XRES goes active (can be disabled with *standby_reset_disable [Sartup_Control]*) and pwr_good goes inactive. Furthermore, to save power especially in this mode, the internal oscillator is just working, when it is needed.

Leaving Stand-By

Stand-by can be terminated by:

- Any kind of interrupt (if it was defined right before going into Stand-by)
- ON-key push-button press (*on_tast_sw* is set to “0”)
- Reset
- Power OFF
- Over-temperature

Power OFF

During power OFF state all circuits are shut-OFF. Thus the current consumption of AS3701 is reduced to about 1uA. Except the reset control registers, all other registers are set to their default value after power-ON.

The chip stays in power OFF mode until

- The external pin ON is pulled high
- The charger is inserted or
- The VPOR level is touched to start a complete reset cycle.

The AS3701 can be set into Power OFF if one of the following conditions occur:

- *ResVoltFall* was reached (VSUP < *ResVoltFall [Battery_voltage_monitor]*)
- Software forced power OFF (*power_off [ResetControl]* = 1)

- ON-key long press
- *auto_off [Startup_Control]* is enabled (VSUP rising from the scratch)

Voltage Detection

If VSUP falls below *ResVoltFall* for longer than 500ms and the bit *power_off_at_vsuplow [Startup_Control]* is set to "1", the PMIC enters the Power Off mode.

Software Forced Power OFF

To put the chip into power off mode, write '1' into *power_off [ResetControl]*. In ON-key-switch configuration the AS3701 will startup immediately again, if the switch is in ON position.

The bit *power_off* bit is automatically cleared by a startup and its associated reset cycle.

Long ON-Key Press

For a power OFF asserted with a long ON-key press, this feature must be enabled by setting the bit *onkey_lpress_en [ResetControl]* to "1". When applying a high level on the ON input pin for 4s/8s (depending on *on_lpress_delay [ReferenceControl]*) a power off gets initiated, if the bit *onkey_lpress_reset [ReferenceControl]* is set to "0". A long ON key power off is possible, if the ON key works as a push-button or as a switch.

Figure 46:
ON-Key Long Press Power OFF Behavior

onkey_ lpress_en	onkey_lpress_ reset	on_reset_ delay	on_tast_sw	Long Press Behavior
0	X	X	X	No ON-key long press power OFF is possible
1	0	0	0	8s long press on the ON-push-button forces a power OFF (1)
1	0	1	0	4s long press on the ON-push-button forces a power OFF (1)
1	0	0	1	Forces a power OFF after 8s, if ON-switch is set to OFF position (2)
1	0	1	1	Forces a power OFF after 4s, if ON-switch is set to OFF position (2)

Note(s):

1. If a USB charger adapter is connected, the ON-key push-button long press would only force a power-off, if the bit chg_pwr_off_en is set to "1"!
2. If a USB charger adapter is connected and the bit chg_pwr_off_en is set to "0" (level detection), the ON-key-switch OFF position has no influence. The PMIC will stay in Activemode as long as the USB adapter is present! If a USB adapter is connected and the bit chg_pwr_off_en is set to "1" (edge detection), the PMIC can be set into Power-OFF via I^2C, if the ON-key switch is also in OFF position!

Auto-OFF

If VSUP is rising from the scratch and the bit *auto_off [Startup_Control]* is set to "1", the PMIC enters immediately the Power-OFF mode right after VSUP reaches the *ResVoltRise*.
If the ON-key is in switch configuration the Auto-OFF feature only works, when the switch is in OFF position during VSUP rising from scratch!

Internal References

Description

The internal 2.0V reference and the oscillator are powered either via the VUSB input pin or via the VBAT input pin, depending on which level is higher. The internal oscillator is used for PWM, SD frequency and all timings, which are needed for the charger, the startup sequence and reset delays.

Parameter

Figure 47:
Reference Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	Accuracy of internal reference clock	Adjustable by serial interface register *clk_int*	-12	f_{CLK}	+12	%

Reference Parameter: Shows the key electrical parameter of the on-chip oscillator

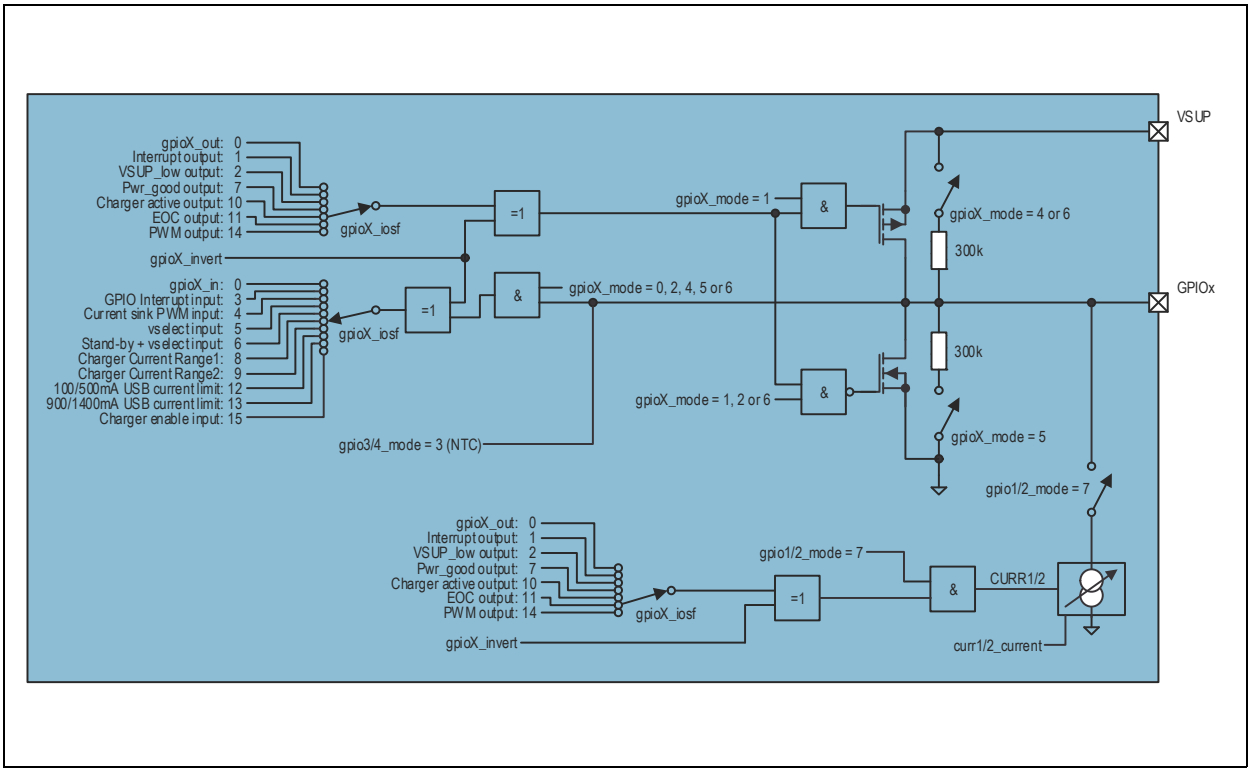
GPIO Pins

AS3701A contains 2 GPIO pins and AS3701B offers 5 GPIO pins. Each of the pins can be configured as digital input, digital input (with pull-up or pull-down), push-pull output or open drain output (with or without pull-up). When configured as output the output source can be a register bit, or the PWM generator.

Additional the GPIO1 and GPIO2 can be configured as a Current sink and the GPIO3 and GPIO4 (only available in AS3701B) can offer an input to connect a NTC for supervising the battery temperature.

The polarity of the input and output signals can be inverted with the corresponding *gpioX_invert [GPIOXcontrol]* bit, all further descriptions refer to normal (non-inverted) mode.

Figure 48:
GPIO Block Diagram



GPIO Block Diagram: Shows the internal structure of the IO pads

Figure 49:
GPIO Pin Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{GPIO_max}	Max voltage on GPIOx pins	Pin VSUP is used as supply for the GPIO pins			VSUP + 0.3	V
V_{OL}	Low level output voltage	I_{OL}=+1mA digital output			+0.4	V
V_{OH}	High level output voltage	I_{OH}=–1mA; digital push-pull output	0.8*VSUP			V
V_{IL}	Low level input voltage	digital input			20% of VSUP	V
V_{IH}	High level input voltage	digital input	60% of VSUP			V
$I_{LEAKAGE}$	Leakage current	high impedance			1	µA
$R_{pull-up}$	Pull-up resistance	if enabled; VSUP = 3.7V		300		kΩ
$R_{pull-down}$	Pull-down resistance	if enabled; VSUP = 3.7V		300		kΩ

GPIO Pins: Shows the key electrical parameter of the GPIO pins. VSUP = 2.7 to 5.5V; unless otherwise mentioned

IO Functions

Normal IO Operation

If set to input, the logic level of the signal present at the GPIOx pin can be read from *gpioX_in [GPIOsignal_in]*. This mode is also used for the ON/OFF control of the DCDC and LDOs. The selection, which regulator is controlled by which GPIO, is done with the *gpio_ctrl_sdX [GPIO_ctrl2]* or *gpio_ctrl_ldoX [GPIO_ctrl2]* bits.
The *gpioX_mode [GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *gpioX_in*.

If the output mode is chosen, *gpioX_out [GPIOsignal_out]* specifies the logic level of the GPIOx pin.
The *gpioX_mode [GPIOxcontrol]* should be set to output.
The *gpioX_iosf [GPIOxcontrol]* should be set to *gpioX_out*.

For GPIO1 and GPIO2, the logic level of the output signal can be visualized via the Current sinks. In this case the *gpioX_mode [GPIOxcontrol]* should be set to CURRx.

Interrupt Output

GPIOx pin logic state is derived from the interrupt signal XIRQ. Whenever an interrupt is present the GPIOx pin will be pulled high.
The *gpioX_mode [GPIOxcontrol]* should be set to output.
The *gpioX_iosf [GPIOxcontrol]* should be set to *Interrupt output*.

For GPIO1 and GPIO2, the Interrupt output signal can be visualized via the Current sinks. In this case the *gpioX_mode [GPIOxcontrol]* should be set to CURRx.

VSUP_low Output

GPIOx pin will go high, if VSUP falls below ResVoltFall and *SupResEn [Battery_voltage_monitor]* = 0.
The *gpioX_mode [GPIOxcontrol]* should be set to output.
The *gpioX_iosf [GPIOxcontrol]* should be set to *VSUP_low output*.

For GPIO1 and GPIO2, the VSUP_low output signal can be visualized via the Current sinks. In this case the *gpioX_mode [GPIOxcontrol]* should be set to CURRx.

PWRGOOD Output

This signal will go high at the end of the start-up sequence. This can be used as a second reset signal to the processor to e.g. start oscillators.
The *gpioX_mode [GPIOxcontrol]* should be set to output.
The *gpioX_iosf [GPIOxcontrol]* should be set to *Pwr_good output*.

For GPIO1 and GPIO2, the Pwr_good output signal can be visualized via the Current sinks. In this case the *gpioX_mode [GPIOxcontrol]* should be set to CURRx.

Charger Active Output

When selected, the GPIOx will go high if the charger is active.
The *gpioX_mode [GPIOxcontrol]* should be set to output.
The *gpioX_iosf [GPIOxcontrol]* should be set to *Charger active output*.

For GPIO1 and GPIO2, the Charger active output signal can be visualized via the Current sinks. In this case the *gpioX_mode [GPIOxcontrol]* should be set to CURRx.

EOC Output

When selected, the GPIOx will go high if the charger has reached the EOC state.
The *gpioX_mode [GPIOxcontrol]* should be set to output.
The *gpioX_iosf [GPIOxcontrol]* should be set to *EOC output*.

For GPIO1 and GPIO2, the EOC output signal can be visualized via the Current sinks. In this case the *gpioX_mode [GPIOxcontrol]* should be set to CURRx.

PWM Output

When selected, the GPIOx output provides the PWM signal generated by the internal programmable PWM generator. Its timing is defined by *pwm_h_time [pwm_control_h]*, *pwm_l_*

time [pwm_control_l] and *pwm_div [ReferenceControl]*.
The *gpioX_mode [GPIOxcontrol]* should be set to output.
The *gpioX_iosf [GPIOxcontrol]* should be set to *PWM output*.

For GPIO1 and GPIO2, the PWM output signal can be visualized via the Current sinks. In this case the *gpioX_mode [GPIOxcontrol]* should be set to CURRx.

GPIO Interrupt Input

A falling or rising edge will set the *gpio_int* bit.
The *gpioX_mode [GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *GPIO Interrupt input*.

Current Sink PWM Input

The GPIO is used as PWM input for the current sink to control the current. 100% PMW mode will set the current to the value set in *currX_current [currX_value]* register.
The gpioX_mode *[GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *Current sink PWM input*.

Vselect Input

As long as the GPIOx pin is low the DCDC/LDOs operate with the normal register settings. If the GPIOx pin goes high, the settings will change to the ones stored in *RegX_voltage [RegX_Voltage]*.
The *gpioX_mode [GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *vselect input*.

GPIO1 and GPIO2 may be used to control two regulators separately.

Figure 50:
GPIO Vselect Modes

gpio1_ iosf	gpio2_ iosf	gpio3_ iosf	gpio4_ iosf	gpio5_ iosf	Vselect Mode
≠5	≠5	≠5	≠5	≠5	No voltage select by GPIO for regulator
5	≠5	≠5	≠5	≠5	GPIO1 controls regulator selected by *reg1_select* and *reg2_select*
≠5	5	≠5	≠5	≠5	GPIO2 controls regulator selected by *reg1_select* and *reg2_select*
5	5	≠5	≠5	≠5	GPIO1 controls regulator selected by *reg1_select* GPIO2 controls regulator selected by *reg2_select*
≠5	≠5	5	≠5	≠5	GPIO3 controls regulator selected by *reg1_select* and *reg2_select* (1)
≠5	≠5	≠5	5	≠5	GPIO4 controls regulator selected by *reg1_select* and *reg2_select* (1)

gpio1_ iosf	gpio2_ iosf	gpio3_ iosf	gpio4_ iosf	gpio5_ iosf	Vselect Mode
≠5	≠5	≠5	≠5	5	GPIO5 controls regulator selected by *reg1_select* and *reg2_select* (1)

IO Functions: Shows the different Vselect control modes, depending on the setting of the GPIO special function 5.

Note(s):
1. AS3701B only

Stand-By and Vselect Input

This mode is very similar to the Vselect mode described in the previous paragraph. The chip is set into stand-by mode when the GPIOx pin goes high and wakes up again when the pin is pulled low and the *gpio_restart_int_m [InterruptMask2]* has been set before going into stand-by. Additional to the stand-by feature, the voltage setting of 2 regulators can be changed with the same command. This requires the setting of the corresponding regulator (*sd1_stby_on* and/or *ldo1_stby_on* and/or *ldo2_stby_on [Reg_standby_mod1]*).
The *gpioX_mode [GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *Stand-by + vselect input*.

Figure 51:
Stand-By and Vselect Modes

gpio1 _iosf	gpio2 _iosf	gpio3 _iosf	gpio4 _iosf	gpio5 _iosf	Vselect Mode	Stand-By Control
≠6	≠6	≠6	≠6	≠6	No voltage select by GPIO for regulator	No
6	≠6	≠6	≠6	≠6	GPIO1 controls regulator selected by *reg1_select* and *reg2_select*	Yes
≠6	6	≠6	≠6	≠6	GPIO2 controls regulator selected by *reg1_select* and *reg2_select*	Yes
≠6	≠6	6	≠6	≠6	GPIO3 controls regulator selected by *reg1_select* and *reg2_select* (1)	Yes
≠6	≠6	≠6	6	≠6	GPIO4 controls regulator selected by *reg1_select* and *reg2_select* (1)	Yes
≠6	≠6	≠6	≠6	6	GPIO5 controls regulator selected by *reg1_select* and *reg2_select* (1)	Yes

IO Functions: Shows the different Vselect and stand-by control modes, depending on the setting of the GPIO special function 6.

Note(s):
1. AS3701B only

Charger Current Range 1

With this function the charging current (trickle current and constant current) can be set to 11mA(trickle) + 133mA(constant) or 22mA(trickle) + 223mA(constant).
The gpioX_mode *[GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *Charger Current Range1*.

Charger Current Range 2

With this function the charging current (trickle current and constant current) can be set to 33mA(trickle) + 357mA(constant) or 45mA(trickle) + 493mA(constant).
The gpioX_mode *[GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *Charger Current Range2*.

100/500mA Charger Input

With this function the charger input current limiter can be set to 100mA or 500mA.
The gpioX_mode *[GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *100/500mA USB current limit*.

800/1100mA Charger Input

With this function the charger input current limiter can be set to 800mA or 1100mA.
The gpioX_mode *[GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *800/1100mA USB current limit*.

Charging Enable Input

When pulling the GPIO to high the charger is being enabled and vice versa. This is to enable the charger without I^2C communication.
The gpioX_mode *[GPIOxcontrol]* should be set to input.
The *gpioX_iosf [GPIOxcontrol]* should be set to *Charger enable input*.

Supervisor

The Step Down DCDC Converter has an integrated over-current protection. An over-temperature protection of the chip is also integrated which can be switched ON with the serial interface signal *temp_pmc_on [OvertemperatureControl]* (enabled by default; it is not recommended to disable the over-temperature protection).

Temperature Supervision

The chip has two signals for the serial interface: *ov_temp_110* and *ov_temp_140 [OvertemperatureControl]*.
The flag *ov_temp_110* is automatically reset if the overtemperature condition is removed, whereas *ov_temp_140* has to be reset by the serial interface with the signal *rst_ov_temp_140 [OvertemperatureControl]*. If the flag *ov_temp_140* is set, an automatic reset of the complete chip is initiated. The chip will only start-up when the temperature falls below the T110 level (including hysteresis). The flag *ov_temp_140* is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown.

Figure 52:
Over-Temperature Protection

Symbol	Parameter	Note	Min	Typ	Max	Unit
T_{110}	ov_temp_110 rising threshold		95	110	125	°C
T_{140}	ov_temp_140 rising threshold		125	140	155	°C
T_{HYST}	ov_temp_110 and ov_temp_140 hysteresis			5		°C

Interrupt Generation

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the InterruptMask registers are set by pulling low the pin XIRQ. All the interrupt sources can be enabled in the Interrupt Mask registers. If an interrupt occurs, the Interrupt Status registers get set and cleared automatically after the host controller has read them.

To prevent the AS3701 device from losing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is completed, a logical AND operation with the bit wise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register, before the clearing process has completed, will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

Wire-Serial Control Interface

Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

I²C Protocol

Figure 53:
I²C Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after Stop	R	1 bit
Sr	Repeated Start	R	1 bit
DW	Device address for Write	R	1000 0000b (80h)
DR	Device address for Read	R	1000 0001b (81h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	During acknowledge

I²C Write Access

Byte Write and Page Write formats are used to write data to the slave.

Figure 54:
I²C Byte Write

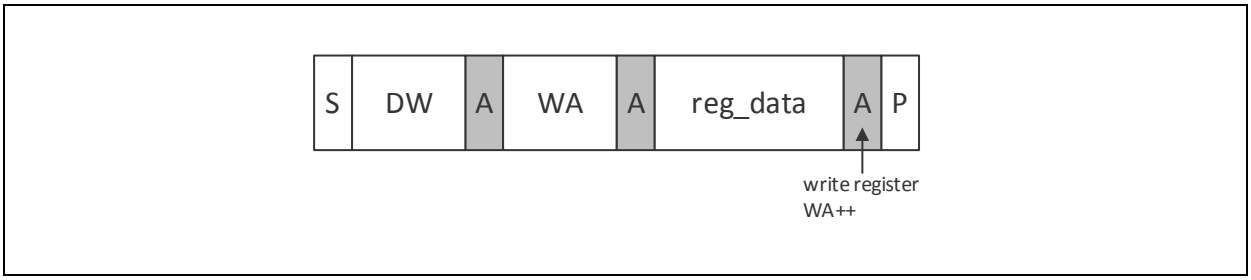
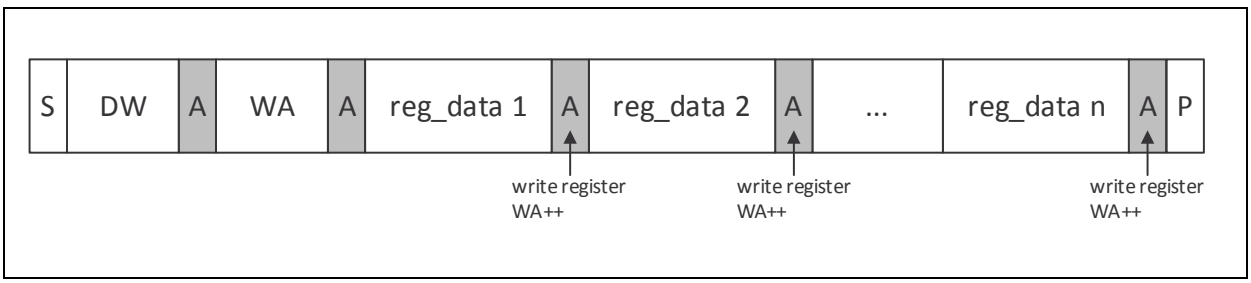


Figure 55:
I²C Page Write



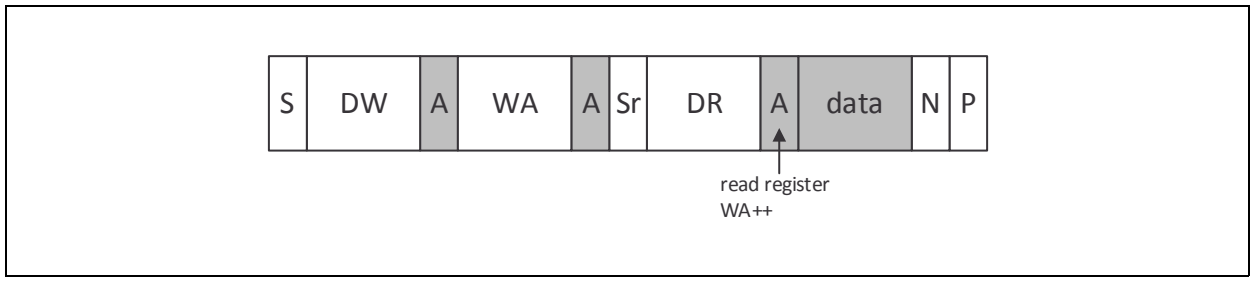
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

I²C Read Access

Random, Sequential and Current Address Read are used to read data from the slave.

Figure 56:
I²C Random Read

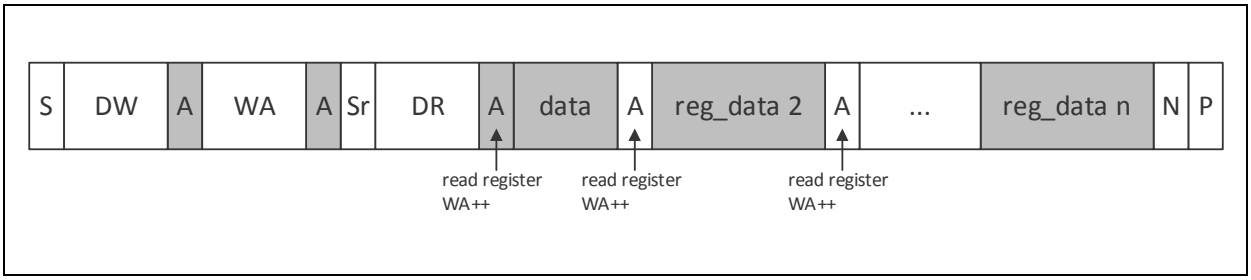


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

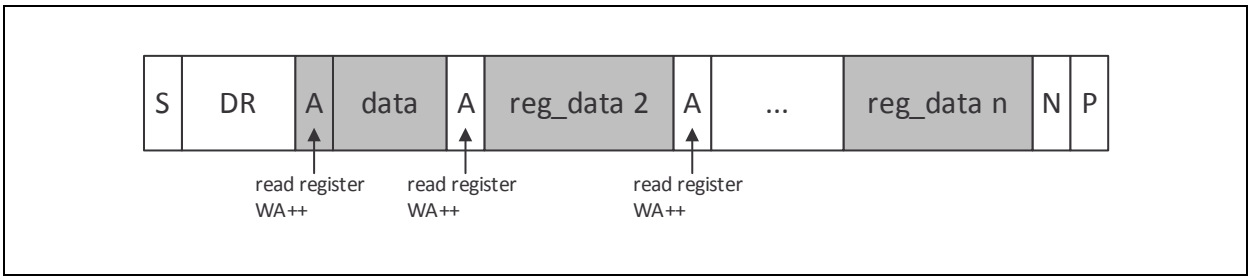
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 57:
I²C Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 58:
I²C Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

I²C Parameter

Figure 59:
I²C Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	SCL,SDA Low Level input voltage				0.4	V
V_{IH}	SCL,SDA High Level input voltage		1.4			V

Register Description

Figure 60:
Register Overview

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
01h	SD1Voltage	sd1_frequ	sd1_vsel<6:0>						
02h	LDO1Voltage	ldo1_on	ldo1_ilimit	ldo1_vsel<5:0>					
03h	LDO2Voltage	ldo2_on	ldo2_ilimit	ldo2_vsel<5:0>					
09h	GPIO1control	gpio1_invert	gpio1_mode<6:4>			gpio1_iosf<3:0>			
0ah	GPIO2control	gpio2_invert	gpio2_mode<6:4>			gpio2_iosf<3:0>			
0bh	GPIO3control	gpio3_invert	gpio3_mode<6:4>			gpio3_iosf<3:0>			
0ch	GPIO4control	gpio4_invert	gpio4_mode<6:4>			gpio4_iosf<3:0>			
0dh	GPIO5control	gpio5_invert	gpio5_mode<6:4>			gpio5_iosf<3:0>			
20h	GPIOsignal_out	-			gpio5_out	gpio4_out	gpio3_out	gpio2_out	gpio1_out
21h	GPIOsignal_in	-			gpio5_in	gpio4_in	gpio3_in	gpio2_in	gpio1_in
22h	Reg1_Voltage	-	Reg1_voltage<6:0>						
23h	Reg2_Voltage	-	Reg2_voltage<6:0>						
24h	Reg_Control	-		Reg2_select<5:4>		-		Reg1_select<1:0>	
25h	GPIO_ctrl1	-	gpio_ctrl_ldo2<6:4>			-	gpio_ctrl_ldo1<2:0>		
26h	GPIO_ctrl2	-					gpio_ctrl_sd1<2:0>		
30h	SD_control1	sd1_enable	sd1_low_ noise	sd1_fast	sd1_fsel	-		dvm_enable	dvm_time

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
32h	Battery_voltage_monitor	FastResEn	SupResEn	ResVoltFall<5:3>			ResVoltRise<2:0>		
33h	Startup_control	chg_pwr_off_en	power_off_at_vsuplow	stby_reset_disable	auto_off	off_delay<3:2>		res_timer<1:0>	
35h	ReferenceControl	on_lpress_delay	on_tast_sw	onkey_lpress_reset	standby_mode_on	clk_int<3:2>		pwm_div<1:0>	
36h	ResetControl	reset_reason<7:4>				onkey_lpress_en	on_input	power_off	force_reset
37h	Overtemperature Control	tco_140_a	tco_110_a	temp_test<5:4>		rst_ov_temp_140	ov_temp_140	ov_temp_110	temp_pmc_on
39h	Reg_standby_mod1	-				disable_regpd	sd1_stby_on	ldo2_stby_on	ldo1_stby_on
41h	pwm_control_l	pwm_l_time<7:0>							
42h	pwm_control_h	pwm_h_time<7:0>							
43h	curr1_value	curr1_current<7:0>							
44h	curr2_value	curr2_current<7:0>							
73h	RegStatus	-	curr2_lv	curr1_lv	-				sd1_lv
74h	InterruptMask1	LowBat_int_m	ovtmp_int_m	onkey_int_m	chdet_int_m	eoc_int_m	resume_int_m	nobat_int_m	trickle_int_m
75h	InterruptMask2	gpio5_int_m	gpio4_int_m	gpio3_int_m	gpio2_int_m	gpio1_int_m	gpio_restart_int_m	sd1_lv_int_m	bat_temp_m
77h	InterruptStatus1	LowBat_int_i	ovtmp_int_i	onkey_int_i	chdet_int_i	eoc_int_i	resume_int_i	nobat_int_i	trickle_int_i
78h	InterruptStatus2	gpio5_int_i	gpio4_int_i	gpio3_int_i	gpio2_int_i	gpio1_int_i	gpio_restart_int_i	sd1_lv_int_i	bat_temp_i

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
80h	ChargerControl	cc_range_ select	AutoResume	bat_ charging_ enable	usb_chgEn	usb_current<3:0>			
81h	ChargerVoltageC ontrol	Vsup_min<7:6>		-	ChVoltEOC<4:0>				
82h	ChargerCurrentCo ntrol	TrickleCurrent<7:4>				ContantCurrent<3:0>			
83h	ChargerConfig1	Charging_ 1Hz_clk	ChVoltResum e	temp_sel<5:4>		vsup_voltage<3:1>			-
84h	ChargerConfig2	eoc_current<7:5>			charging_ tmax	ch_timeout<3:0>			
85h	Chargersupervisio n	ntc_high_on	ntc_low_on	ntc_10k	ntc_mode	NTC_input<3:2>		ntc_beta<1:0>	
86h	ChargerStatus1	NoBat	temp_cond<6:5>		EOC	CVM	Trickle	Resume	CCM
87h	ChargerStatus2	-				chdet_off	ChDet	batsw_mode<1:0>	
8eh	LockRegister	-			-	-	charger_lock	reg_lock<1:0>	
90h	ASIC_ID1	ID1<7:0>							
91h	ASIC_ID2	-				revision<3:0>			
a5h	Fuse5	del_time	sequ_on						
a6h	Fuse6						on_tast_sw	onkey_ lpress_reset	on_invert

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
a7h	Fuse7	auto_off	chg_pwr_off_en	res_timer<5:4>		sd1_fsel	sd1_fast	power_off_at_vsuplow	i2c_deva_bit1
a8h	Fuse8	usb_current<7:4>				ResVoltRise<3:1>			on_lpress_delay
a9h	Fuse9	Reg4_del	Reg3_del	Reg2_del	Reg1_del	SupResEn	onkey_lpress_en	NTC_input<1:0>	
aah	Fuse10	Reg2_addr<7:4>				Reg1_addr<3:0>			
abh	Fuse11	reg1_V<7:0>							
ach	Fuse12	reg2_V<7:0>							
adh	Fuse13	Reg4_addr<7:4>				Reg3_addr<3:0>			
aeh	Fuse14	reg3_V<7:0>							
afh	Fuse15	reg4_V<7:0>							

Detailed Register Description

Figure 61:
SD1Voltage

Addr:01h		SD1Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	sd1_frequ	b0	RW	Selects between high and low frequency 0 : 1 MHz if sd1_fsel=0, 2MHz if sd1_fsel=1 1 : 3 MHz if sd1_fsel=0, 4MHz if sd1_fsel=1
6:0	sd1_vsel	b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00h : DC/DC powered down 01h-40h : V_SD1=0.6V+sd1_vsel*12.5mV 41h-70h : V_SD1=1.4V+(sd1_vsel-40h)*25mV 71h-7Fh : V_SD1=2.6V+(sd1_vsel-70h)*50mV

Figure 62:
LDO1Voltage

Addr:02h		LDO1Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	ldo1_on	b0	RW	Switch ON of LDO1 0 : LDO OFF 1 : LDO ON
6	ldo1_ilimit	b0	RW	Sets current limit of LDO1 0 : 100mA operating range 1 : 200mA operating range
5:0	ldo1_vsel	b000000	RW	The voltage select bits set the LDO output voltage 00h-2Ah : V_LDO1=1.2V+ldo1_vsel*50mV 2Bh-3Fh : do not use

Figure 63:
LDO2Voltage

Addr:03h		LDO2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo2_on	b0	RW	Switch ON of LDO2 0 : LDO OFF 1 : LDO ON
6	ldo2_ilimit	b0	RW	Sets current limit of LDO2 0 : 100mA operating range 1 : 200mA operating range
5:0	ldo2_vsel	b000000	RW	The voltage select bits set the LDO output voltage 00h-2Ah : V_LDO2=1.2V+ldo2_vsel*50mV 2Bh-3Fh : do not use

Figure 64:
GPIO1control

Addr:09h		GPIO1control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio1_invert	b0	RW	Invert GPIO1 input/output 0 : Normal Mode 1 : Invert input or output
6:4	gpio1_mode	b011	RW	Selects the GPIO1 mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : IO(open drain, only NMOS is active) 3 : Input (tristate) 4 : Input with pullup 5 : Input with pulldown 6 : IO(open drain(NMOS)with pullup) 7 : CURR1
3:0	gpio1_iosf	b0000	RW	Selects the GPIO1 special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on reg1_select and reg2_select, if gpio2_iosf=5 then apply on reg1_select only) 6 : standby+Vselect+restart interrupt input 7 : pwr_good output 8 : 11mA(TrickleCurrent=0), 133mA(ConstantCurrent=2) / 23mA(TrickleCurrent=1), 223mA(ConstantCurrent=4) 9 : 35mA(TrickleCurrent=2), 358mA(ConstantCurrent=7) / 47mA(TrickleCurrent=3), 494mA(ConstantCurrent=10) 10 : Charger active output 11 : EOC output 12 : 100mA(usb_Current=0) / 500mA(usb_Current=8) 13 : 800mA(usb_Current=11) / 1100mA(usb_Current=13) 14 : PWM output 15 : Charger enable input

Figure 65:
GPIO2control

Addr:0ah		GPIO2control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio2_invert	b0	RW	Invert GPIO2 input/output 0 : Normal Mode 1 : Invert input or output
6:4	gpio2_mode	b011	RW	Selects the GPIO2 mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : IO(open drain, only NMOS is active) 3 : Input (tristate) 4 : Input with pullup 5 : Input with pulldown 6 : IO(open drain(NMOS)with pullup) 7 : CURR2
3:0	gpio2_iosf	b0000	RW	Selects the GPIO2 special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on reg1_select and reg2_select, if gpio1_iosf=5 then apply on reg2_select only) 6 : standby+Vselect+restart interrupt input 7 : pwr_good output 8 : 11mA(TrickleCurrent=0), 133mA(ConstantCurrent=2) / 23mA(TrickleCurrent=1), 223mA(ConstantCurrent=4) 9 : 35mA(TrickleCurrent=2), 358mA(ConstantCurrent=7) / 47mA(TrickleCurrent=3), 494mA(ConstantCurrent=10) 10 : Charger active output 11 : EOC output 12 : 100mA(usb_Current=0) / 500mA(usb_Current=8) 13 : 800mA(usb_Current=11) / 1100mA(usb_Current=13) 14 : PWM output 15 : Charger enable input

Figure 66:
GPIO3control

Addr:0bh		GPIO3control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio3_invert	b0	RW	Invert GPIO3 input/output 0 : Normal Mode 1 : Invert input or output
6:4	gpio3_mode	b011	RW	Selects the GPIO3 mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : IO(open drain, only NMOS is active) 3 : NTC input (tristate) 4 : Input with pullup 5 : Input with pulldown 6 : IO(open drain(NMOS)with pullup) 7 : NA
3:0	gpio3_iosf	b0000	RW	Selects the GPIO3 special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on reg1_select and reg2_select) 6 : standby+Vselect+restart interrupt input 7 : pwr_good output 8 : 11mA(TrickleCurrent=0), 133mA(ConstantCurrent=2) / 23mA(TrickleCurrent=1), 223mA(ConstantCurrent=4) 9 : 35mA(TrickleCurrent=2), 358mA(ConstantCurrent=7) / 47mA(TrickleCurrent=3), 494mA(ConstantCurrent=10) 10 : Charger active output 11 : EOC output 12 : 100mA(usb_Current=0) / 500mA(usb_Current=8) 13 : 800mA(usb_Current=11) / 1100mA(usb_Current=13) 14 : PWM output 15 : Charger enable input

Figure 67:
GPIO4control

Addr:0ch		GPIO4control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio4_invert	b0	RW	Invert GPIO4 input/output 0 : Normal Mode 1 : Invert input or output
6:4	gpio4_mode	b011	RW	Selects the GPIO4 mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : IO(open drain, only NMOS is active) 3 : NTC input (tristate) 4 : Input with pullup 5 : Input with pulldown 6 : IO(open drain(NMOS)with pullup) 7 : NA
3:0	gpio4_iosf	b0000	RW	Selects the GPIO4 special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on reg1_select and reg2_select) 6 : standby+Vselect+restart interrupt input 7 : pwr_good output 8 : 11mA(TrickleCurrent=0), 133mA(ConstantCurrent=2) / 23mA(TrickleCurrent=1), 223mA(ConstantCurrent=4) 9 : 35mA(TrickleCurrent=2), 358mA(ConstantCurrent=7) / 47mA(TrickleCurrent=3), 494mA(ConstantCurrent=10) 10 : Charger active output 11 : EOC output 12 : 100mA(usb_Current=0) / 500mA(usb_Current=8) 13 : 800mA(usb_Current=11) / 1100mA(usb_Current=13) 14 : PWM output 15 : Charger enable input

Figure 68:
GPIO5control

Addr:0dh		GPIO5control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio5_invert	b0	RW	Invert GPIO5 input/output 0 : Normal Mode 1 : Invert input or output
6:4	gpio5_mode	b011	RW	Selects the GPIO5 mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : IO(open drain, only NMOS is active) 3 : Input (tristate) 4 : Input with pullup 5 : Input with pulldown 6 : IO(open drain(NMOS)with pullup) 7 : NA
3:0	gpio5_iosf	b0000	RW	Selects the GPIO5 special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on reg1_select and reg2_select) 6 : standby+Vselect+restart interrupt input 7 : pwr_good output 8 : 11mA(TrickleCurrent=0), 133mA(ConstantCurrent=2) / 23mA(TrickleCurrent=1), 223mA(ConstantCurrent=4) 9 : 35mA(TrickleCurrent=2), 358mA(ConstantCurrent=7) / 47mA(TrickleCurrent=3), 494mA(ConstantCurrent=10) 10 : Charger active output 11 : EOC output 12 : 100mA(usb_Current=0) / 500mA(usb_Current=8) 13 : 800mA(usb_Current=11) / 1100mA(usb_Current=13) 14 : PWM output 15 : Charger enable input

Figure 69:
GPIOsignal_out

Addr:20h		GPIOsignal_out		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	gpio5_out	b0	RW	This bit determines the output signal of the GPIO5 pin when selected as output source.
3	gpio4_out	b0	RW	This bit determines the output signal of the GPIO4 pin when selected as output source.
2	gpio3_out	b0	RW	This bit determines the output signal of the GPIO3 pin when selected as output source.
1	gpio2_out	b0	RW	This bit determines the output signal of the GPIO2 pin when selected as output source.
0	gpio1_out	b0	RW	This bit determines the output signal of the GPIO1 pin when selected as output source.

Figure 70:
GPIOsignal_in

Addr:21h		GPIOsignal_in		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	gpio5_in	b0	RO	This bit reflects the logic level of the GPIO5 pin when configured as digital input pin.
3	gpio4_in	b0	RO	This bit reflects the logic level of the GPIO4 pin when configured as digital input pin.
2	gpio3_in	b0	RO	This bit reflects the logic level of the GPIO3 pin when configured as digital input pin.
1	gpio2_in	b0	RO	This bit reflects the logic level of the GPIO2 pin when configured as digital input pin.
0	gpio1_in	b0	RO	This bit reflects the logic level of the GPIO1 pin when configured as digital input pin.

Figure 71:
Reg1_Voltage

Addr:22h		Reg1_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	Reg1_voltage	b0000000	RW	This register is mapped to the register address 0h+Reg1_select , if gioX_iosf=5 or 6 (Vselect input), and input = 1. This feature allows voltage switching of a predefined regulator with just one GPIO input 0 ..7Fh: Selects voltage and ilimit of LDO or DCDC

Figure 72:
Reg2_Voltage

Addr:23h		Reg2_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	Reg2_voltage	b0000000	RW	This register is mapped to the register address 0h+Reg1_select , if gioX_iosf=5 or 6 (Vselect input), and input = 1. This feature allows voltage switching of a predefined regulator with just one GPIO input 0 ..7Fh: Selects voltage and ilimit of LDO or DCDC

Figure 73:
Reg_Control

Addr:24h		Reg_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:4	Reg2_select	b0000	RW	Select regulator for mapping of Reg2_voltage; 0 : NA 1 : Select 01h SD1Voltage 2 : Select 02h LDO1Voltage 3 : Select 03h LDO2Voltage
1:0	Reg1_select	b0000	RW	Select regulator for mapping of Reg1_voltage; 0 : NA 1 : Select 01h SD1Voltage 2 : Select 02h LDO1Voltage 3 : Select 03h LDO2Voltage

Figure 74:
GPIO_ctrl1

Addr:25h		GPIO_ctrl1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:4	gpio_ctrl_ldo2	b000	RW	0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3 4 : Controlled by GPIO4 5 : Controlled by GPIO5 6 : NA 7 : NA
2:0	gpio_ctrl_ldo1	b000	RW	0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3 4 : Controlled by GPIO4 5 : Controlled by GPIO5 6 : NA 7 : NA

Figure 75:
GPIO_ctrl2

Addr:26h		GPIO_ctrl2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2:0	gpio_ctrl_sd1	b000	RW	0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3 4 : Controlled by GPIO4 5 : Controlled by GPIO5 6 : NA 7 : NA

Figure 76:
SD_control1

Addr:30h		SD_control1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd1_enable	b1	RW	Global stepdown SD1 enable 0 : SD1 disabled 1 : SD1 enabled
6	sd1_low_ noise	b0	RW	Enables low noise mode of SD1. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of >100mA applied in skip mode 1 : Low noise mode. Only minimum on time applied in skip mode
5	sd1_fast	b0	RW_SM	Selects a faster regulation mode for SD1 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required
4	sd1_fsel	b0	RW_SM	Selects between high and low frequency range 0 : 1 MHz if sd1_frequ=0, 3MHz if sd1_frequ=1 1 : 2 MHz if sd1_frequ=0, 4MHz if sd1_frequ=1
1	dvm_enable	b0	RW	Enabling of Dynamic Voltage Management If voltage of SD1 is changed during operation (sd1_vsel) voltage is de/increased by single steps 0 : DVM disabled 1 : DVM enabled
0	dvm_time	b0	RW	Time steps of DVM voltage change of SD1 0 : 8 usec time delay between steps 1 : 16 usec time delay between steps

Figure 77:
Battery_voltage_monitor

Addr:32h		Battery_voltage_monitor		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FastResEn	b0	RW	0 : Vresetfall debounce time = 3msec 1 : Vresetfall debounce time = 64usec
6	SupResEn	b0	RW_SM	0 : A reset is generated if VSUP falls below 2.7V (1) 1 : A reset is generated if VSUP falls below ResVoltFall
5:3	ResVoltFall	b000	RW_SM	This value determines the reset level ResVoltFall for falling VBAT. It is recommended to set this value at least 200mV lower than ResVoltRise 0 : 2.7V 1 : 2.9V 2 : 3.1V 3 : 3.2V 4 : 3.3V 5 : 3.4V 6 : 3.5V 7 : 3.6V
2:0	ResVoltRise	b001	RO	This value determines the reset level ResVoltRise for rising VBAT. It is recommended to set this value at least 200mV higher than ResVoltFall 0 : 2.7V 1 : 2.9V 2 : 3.1V 3 : 3.2V 4 : 3.3V 5 : 3.4V 6 : 3.5V 7 : 3.6V

Note(s):

1. If VBAT falls below ResVoltFall only an interrupt is generated (if enabled) and the uProcessor can shut down the system.

Figure 78:
Startup_Control

Addr:33h		Startup_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	chg_pwr_off_en	b0	RO	Select charger detection in power OFF mode Read only (OTP setting) 0 : Exit of Power OFF mode, if charger is detected (level detection) 1 : Exit of Power OFF mode, if charger insertion is detected (rising edge detection)
6	power_off_at_vsuplow	b0	RW_SM	Switch ON Power OFF mode if low VSUP is detected during active or standby mode (Pin ON= low and bit auto_off=0) 0 : If low battery is detected, continuously monitor battery voltage and startup if battery voltage is above ResVoltRise 1 : If low battery is detected, enter power OFF mode
5	stby_reset_disable	b0	RW	Disable Reset output signal (PIN XRES) in standby mode 0 : Normal mode, reset is active in standby mode 1 : No reset in standby mode and during exit of standby mode
4	auto_off	b0	RO	Defines startup behavior at first battery insertion 0 : Startup of chip if VBAT>ResVoltRise 1 : Enter power OFF mode (Startup with ON key or charger insertion)
3:2	off_delay	b01	RW	Set Delay between I^2C command, GPIO or Reset signal for power_off, standby mode or reset and execution of that command 0 : No delay 1 : 8 msec (default) 2 : 16 msec 3 : 32 msec
1:0	res_timer	b00	RW_SM	Set RESTime, after the last regulator has started 0 : RESTIME=10ms (default) 1 : RESTIME=50ms 2 : RESTIME=100ms 3 : RESTIME=150ms

Figure 79:
ReferenceControl

Addr:35h		ReferenceControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	on_lpress_ delay	b0	RW_SM	Sets the ON reset delay time 0 : 8 sec (if onkey_lpress_en=1) 1 : 4 sec (if onkey_lpress_en=1)
6	on_tast_sw	b0	RO	Selects mode of ON input 0 : ON key works as push-button 1 : ON key works as switch
5	onkey_lpress_ reset	b0	RW_SM	Selects behavior for ONKEY longpress 0 : Long onkey press forces change to power_off mode (if on_tast_sw=0 and onkey_lpress_en=1) 1 : Long onkey press forces a reset (if on_tast_sw=0 and onkey_lpress_en=1)
4	standby_ mode_on	b0	RW_SM	Setting to 1 sets the PMU into standby mode. All regulators are disabled except those regulators enabled by Reg_standby_mod. XRES will be pulled to low. A normal startup of all regulators will be done with any interrupt (has to be enabled before entering standby mode).
3:2	clk_int	b00	R_PUSH	Sets the internal CLK frequency fCLK used for DCDCs, PWM, ... 0 : 4 MHz (default) 1 : 3.8 MHz 2 : 3.6 MHz 3 : 3.4 MHz All frequencies, timings and delays in this datasheet are based on 4MHz clk_int
1:0	pwm_div	b00	RW	This bit defines the divider ratio of the prescaler for the PWM generator 0 : Divide by 1 1 : Divide by 2 2 : Divide by 4 3 : Divide by 16

Figure 80:
ResetControl

Addr:36h		ResetControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	reset_reason	b0000	RW_SM	Flags to indicate to the software the reason for the last reset 0 : VPOR has been reached (battery or charger insertion from scratch) 1 : ResVoltFall was reached (battery voltage drop below 2.75V) 2 : Software forced by force_reset 3 : Software forced by power_off and ON was pulled high 4 : Software forced by power_off and charger was detected 5 : External triggered through the pin XRES 6 : Reset caused by overtemperature T140 7 : NA 8 : Reset caused by 4/8 seconds ON key press 9 : NA 10 : NA 11 : Reset caused by interrupt in standby mode 12 : Reset caused by ON pulled high in standby mode
3	onkey_lpress_en	b0	RW_SM	0 : ONKEY longpress feature disabled 1 : ONKEY longpress feature enabled
2	on_input	b0	R_PUSH	Read:This flag represents the state of the ON pad directly Write: Setting to 1 resets the 4/8 sec. Onkey longpress timer
1	power_off	b0	RW_SM	Setting to 1 starts a reset cycle, but waits after the Reg_off state for a falling edge on the pin ON or until the charger is detected
0	force_reset	b0	RW	Setting to 1 starts a complete reset cycle

Figure 81:
OvertemperatureControl

Addr:37h		OvertemperatureControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	tco_140_a	b0	RO	Only used for production test
6	tco_110_a	b0	RO	Only used for production test
5:4	temp_test	b00	RW	
3	rst_ov_temp_140	b0	RW	If the overtemperature threshold 2 has been reached, the flag ov_temp_140 is set and a reset cycle is started. ov_temp_140 should be reset by writing 1 and afterwards 0 to rst_ov_temp_140
2	ov_temp_140	b0	RO	Flag that the overtemperature threshold 2 (T140) has been reached - this flag is not reset by a overtemperature caused reset and has to be reset by rst_ov_temp_140
1	ov_temp_110	b0	RO	Flag that the overtemperature threshold 1 (T110) has been reached
0	temp_pmc_on	b1	RW	Switch ON/OFF of temperature supervision; default: ON - all other bits are only valid if set to 1 Leave at 1, do not disable

Figure 82:
Reg_standby_mod1

Addr:39h		Reg_standby_mod1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	disable_regpd	b0	RW	This bit disables the pulldown of all regulators 0 : Normal operation approx. 1kohm pulldown of all regulators 1 : Pulldown disabled >100kohm of all regulators
2	sd1_stby_on	b0	RW	Enable Step down 1 in standby mode
1	ldo2_stby_on	b0	RW	Enable LDO2 in standby mode
0	ldo1_stby_on	b0	RW	Enable LDO1 in standby mode

Figure 83:
pwm_control_l

Addr:41h		pwm_control_l		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pwm_l_time	b00000000	RW	This bit defines the low time of the pwm generator in 1MHz units 0 : pwm_div * 1usec 1 : pwm_div * 2usec 2 : pwm_div * 3usec ... : ... 255 : pwm_div * 256usec

Figure 84:
pwm_control_h

Addr:42h		pwm_control_h		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pwm_h_time	b00000000	RW	This bit defines the high time of the pwm generator in 1MHz units 0 : pwm_div * 1usec 1 : pwm_div * 2usec 2 : pwm_div * 3usec ... : ... 255 : pwm_div * 256usec

Figure 85:
curr1_value

Addr:43h		curr1_value		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr1_current	b00000000	RW	Defines the current into CURR1 if *gpio1_mode* = 7 0 : Power down (default state) 1 : 0.15686mA (LSB) ... : ... 255 : 40mA

Figure 86:
curr2_value

Addr:44h		curr2_value		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr2_current	b00000000	RW	Defines the current into CURR2 if *gpio2_mode* = 7 0 : Power down (default state) 1 : 0.15686mA (LSB) ... : ... 255 : 40mA

Figure 87:
RegStatus

Addr:73h		RegStatus		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	curr2_lv	b0	RO	Bit is set when voltage of current sink CURR2 drops below low voltage threshold (1ms debounce time default)
5	curr1_lv	b0	RO	Bit is set when voltage of current sink CURR1 drops below low voltage threshold (1ms debounce time default)
0	sd1_lv	b0	RO	Bit is set when voltage of step down1 drops below low voltage threshold (-5%) (1ms debounce time default)

Figure 88:
InterruptMask1

Addr:74h		InterruptMask1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LowBat_int_m	b1	RW	Rising edge only
6	ovtmp_int_m	b1	RW	Rising edge only
5	onkey_int_m	b1	RW	Rising and falling edge
4	chdet_int_m	b1	RW	Rising and falling edge
3	eoc_int_m	b1	RW	Rising and falling edge
2	resume_int_m	b1	RW	Rising and falling edge
1	nobat_int_m	b1	RW	Rising and falling edge
0	trickle_int_m	b1	RW	Rising and falling edge

Figure 89:
InterruptMask2

Addr:75h		InterruptMask2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio5_int_m	b1	RW	Rising and falling edge
6	gpio4_int_m	b1	RW	Rising and falling edge
5	gpio3_int_m	b1	RW	Rising and falling edge
4	gpio2_int_m	b1	RW	Rising and falling edge
3	gpio1_int_m	b1	RW	Rising and falling edge
2	gpio_restart_int_m	b1	RW	Falling edge only
1	sd1_lv_int_m	b1	RW	Rising edge only
0	bat_temp_m	b1	RW	Rising and falling edge

Figure 90:
InterruptStatus1

Addr:77h		InterruptStatus1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LowBat_int_i	b0	RO	Bit is set when VSUP drops below ResVoltFall
6	ovtmp_int_i	b0	RO	Bit is set when 110deg is exceeded
5	onkey_int_i	b0	RO	
4	chdet_int_i	b0	RO	
3	eoc_int_i	b0	RO	
2	resume_int_i	b0	RO	
1	nobat_int_i	b0	RO	
0	trickle_int_i	b0	RO	

Figure 91:
InterrupStatus2

Addr:78h		InterrupStatus2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio5_int_i	b0	RO	
6	gpio4_int_i	b0	RO	
5	gpio3_int_i	b0	RO	
4	gpio2_int_i	b0	RO	
3	gpio1_int_i	b0	RO	
2	gpio_restart_int_i	b0	RO	
1	sd1_lv_int_i	b0	RO	
0	bat_temp_i	b0	RO	

Figure 92:
ChargerControl

Addr:80h		ChargerControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	cc_range_ select	b0	RW	Defines the charging current range for constant current mode 0 : High current range 1 : Low current range
6	AutoResume	b0	RW	0 : Charging does not restart automatically in EOC when bit Resume is set. 1 : Charging will restart automatically in EOC when bit Resume is set and vbat is below resume level
5	bat_charging_ enable	b0	RW	0 : USB is supplying VSUP, but battery switch is open. USB charger regulates to Vsup_voltage 1 : Normal battery charger operation form usb charger
4	usb_chgEn	b1	RW	ON/OFF control of USB charger input
3:0	usb_Current	b0000	RW	Sets the USB input current limit. 0 : 94mA (default) 1 : 141mA 2 : 189mA 3 : 237mA 4 : 285mA 5 : 332mA 6 : 380mA 7 : 428mA 8 : 470mA 9 : 517mA 10 : 600mA 11 : 764mA 12 : 889mA 13 : 1065mA 14 : NA 15 : NA

Figure 93:
ChargerVoltageControl

Addr:81h		ChargerVoltageControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Vsup_min	b01	RW	Regulate down battery charging current on that level of Vsup during trickle charging and constant current charging, to prevent voltage drop on vsup: 0 : 3.90V 1 : 4.20V (default) 2 : 4.50V 3 : 4.70V
4:0	ChVoltEOC	b10011	RW	Sets the end-of-charge voltage level VCHOFF. 0 : 3.82V 1 : 3.84V ... 19 : 4.20V (default) ... 31 : 4.44V

Figure 94:
ChargerCurrentControl

Addr:82h		ChargerCurrentControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	TrickleCurrent	b0000	RW	Sets the charging current limit in trickle current mode. 0 : 11mA (default) 1 : 23mA 2 : 35mA 3 : 47mA 4 : 59mA 5 : 70mA 6 : 82mA 7 : 94mA 8 : 106mA 9 : 118mA 10 : 130mA 11 : NA 12 : NA 13 : NA 14 : NA 15 : NA
3:0	Constant Current	b0000	RW	Sets the charging current limit in constant current mode. 0 : 44mA if cc_range_select=0, 11mA if cc_range_select=1 (default) 1 : 88mA if cc_range_select=0, 23mA if cc_range_select=1 2 : 133mA if cc_range_select=0, 35mA if cc_range_ select=1 3 : 178mA if cc_range_select=0, 47mA if cc_range_ select=1 4 : 223mA if cc_range_select=0, 59mA if cc_range_ select=1 5 : 268mA if cc_range_select=0, 70mA if cc_range_ select=1 6 : 313mA if cc_range_select=0, 82mA if cc_range_ select=1 7 : 358mA if cc_range_select=0, 94mA if cc_range_ select=1 8 : 403mA if cc_range_select=0, 106mA if cc_range_ select=1 9 : 448mA if cc_range_select=0, 118mA if cc_range_ select=1 10 : 494mA if cc_range_select=0, 130mA if cc_range_ select=1) 11 : NA 12 : NA 13 : NA 14 : NA 15 : NA

Figure 95:
ChargerConfig1

Addr:83h		ChargerConfig1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Charging_ 1Hz_clk	b0	RW	Sets the mode for the charging output status (*gpioX_iosf* = 10) 0 : Normal operation: charging=1, not charging=0 1 : 1Hz blinking operation: charging=1Hz, not charging=0
6	ChVolt Resume	b0	RW	Sets the resume voltage level VCHRES 0 : 3.33% of ChVoltEOC (140mV default) 1 : 5.56% of ChVoltEOC (233mV default)
5:4	temp_sel	b00	RW	Selects temperature regulation of charging current (die temp.) 0 : 120degC 1 : 130degC 2 : 110degC 3 : 90degC
3:1	vsup_voltage	b100	RW	Voltage regulation of VSUP of the input current limiter 0 : 4.4V 1 : 4.5V 2 : 4.6V 3 : 4.7V 4 : 4.8V (default) 5 : 4.9V 6 : 5.0V 7 : 5.5V

Figure 96:
ChargerConfig2

Addr:84h		ChargerConfig2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	eoc_current	b001	RW	Sets eoc current 0 : 5% of ConstantCurrent 1 : 10% of ConstantCurrent (default) 2 : 15% of ConstantCurrent 3 : 20% of ConstantCurrent 4 : 25% of ConstantCurrent 5 : 30% of ConstantCurrent 6 : 40% of ConstantCurrent 7 : 50% of ConstantCurrent
4	charging_tmax	b0	R_PUSH	Write: reset charger timeout counter 0 : Read: no timeout reached 1 : Charging timeout reached and charging stopped
3:0	ch_timeout	b0111	RW	Charging timeout timer 0 : OFF 1 : 0.5h 2 : 1h 3 : 1.5h 4 : 2h 5 : 2.5h 6 : 3h 7 : 3.5h(default) 8 : 4h 9 : 4.5h 10 : 5h 11 : 5.5h 12 : 6h 13 : 6.5h 14 : 7h 15 : 7.5h

Figure 97:
ChargerSupervision

Addr:85h		ChargerSupervision		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ntc_high_on	b1	RW	Enables the battery high temperature supervision via NTC resistor (depends on ntc_mode) 0 : NTC battery 45/60deg temp supervision disabled 1 : NTC battery 45/60deg temp supervision enabled
6	ntc_low_on	b0	RW	Enables the battery low temperature supervision via NTC resistor 0 : NTC battery 0deg temp supervision disabled 1 : NTC battery 0deg temp supervision enabled
5	ntc_10k	b0	RW	Select NTC resistor 0 : 100k (ntc_current = 15uA) 1 : 10k (ntc_current = 150uA)
4	ntc_mode	b0	RW	Defines the temperature level for the battery high temperature supervision 0 : 45deg 1 : 60deg
3:2	NTC_input	b00	RW	Defines the NTC input 0 : no NTC input 1 : XIRQ_NTC pin 2 : GPIO3 pin 3 : GPIO4 pin
1:0	ntc_beta	b00	RW	Sets the ntc beta 0 : 3000 (0deg:1.41V & 45deg:0.59V/60deg:0.42V) 1 : 3500 (0deg:1.49V & 45deg:0.54V/60deg:0.37V) 2 : 4000 (0deg:1.56V & 45deg:0.50V/60deg:0.31V) 3 : 4500 (0deg:1.63V & 45deg:0.46V/60deg:0.27V)

Figure 98:
ChargerStatus1

Addr:86h		ChargerStatus1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	NoBat	b0	R	Bit is set when battery detection circuit indicates that no battery is connected to the system.
6:5	temp_cond	b00	R	Indicates temperature condition 0 : Battery is in typical condition (0deg < battemp < 45/60deg) 1 : Battery is in cold condition (battemp < 0deg) 2 : Battery is in hot condition (battemp > 45/60deg) 3 : NA
4	EOC	b0	R	Bit is set if End of charge state has been reached
3	CVM	b0	R	Bit is set if charger is operating in constant voltage mode
2	Trickle	b0	R	Bit is set, if charger is operating in trickle current. Vbat<2.9V
1	Resume	b0	R	Bit is set if Battery voltage is below resume level
0	CCM	b0	R	Bit is set if charger is operating in constant current mode

Figure 99:
ChargerStatus2

Addr:87h		ChargerStatus2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	chdet_off	b0	RW	SW can turn OFF charger detection circuit for power-OFF state 0 : Charger detection is always enabled 1 : Charger detection is disabled in power-OFF state
2	ChDet	b0	R	Bit is set when external charge adapter has been detected on pin USB
1:0	batsw_mode	b00	R	Bit indicates the status of the battery switch operation mode 0 : Battery switch is open, no ideal diode operation (just for charger start-up) 1 : Battery switch is open, ideal diode operation (charger connected but EOC reached) 2 : Battery switch is closed and acting as a voltage limited current source (charging) 3 : Battery switch is closed (charger disconnected)

Figure 100:
LockRegister

Addr:8eh		LockRegister		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	charger_lock	b0	R	Enables lock of the charger registers 81h, 82h, 83h, 84h Chargervoltagecontrol, Chargercurrentcontrol, Chargerconfig1, Chargerconfig2 Bits can only be set. Reset only with full reset cycle
1:0	reg_lock	b00	R	Enables lock of Regulator voltages Bits can only be set. Reset only with full reset cycle Disable write to testmodes registers if LDO_lock>0 writing stepdown voltage to 0 should be possible all the time to allow switching ON the regulator. Writing a nonzero value after that should restore the old value 0 : No lock 1 : Lock of voltage of LDOs (LDOx_vsel) (all bits) and voltage of StepDownBits(sdx_vsel) [5:6] only 2 : Lock voltage of StepDownBits(sdx_vsel) [5:6] only 3 : Lock voltage of StepDown (all bits) and LDOs (all bits).

Figure 101:
ASIC_ID1

Addr:90h		ASIC_ID1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ID1	b00010001	RO	

Figure 102:
ASIC_ID2

Addr:91h		ASIC_ID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	revision	b0000	RO	

Figure 103:
Fuse5

Addr:a5h		Fuse5		
Bit	Bit Name	Default	Access	Bit Description
7	del_time	b0	RW	
6	sequ_on	b0	RW	

Figure 104:
Fuse6

Addr:a6h		Fuse6		
Bit	Bit Name	Default	Access	Bit Description
2	on_tast_sw	b0	RW	Selects mode of ON input 0 : ON key works as push-button 1 : ON key works as switch
1	onkey_lpress_ reset	b0	RW	Selects behavior for ONKEY longpress 0 : Long onkey press forces change to power_off mode (if on_tast_sw=0 and onkey_lpress_en=1) 1 : Long onkey press forces a reset (if on_tast_sw=0 and onkey_lpress_en=1)
0	on_invert	b0	RW	Inverts the ON input 0 : ON input is active high (default) 1 : ON input is active low

Figure 105:
Fuse7

Addr:a7h		Fuse7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	auto_off	b0	RW	Defines startup behavior at first battery insertion 0 : Startup of chip if VBAT>ResVoltRise 1 : Enter power OFF mode (Startup with ON key or charger insertion)
6	chg_pwr_off_en	b0	RW	Enable power OFF mode, if charger is detected 0 : Exit of Power OFF mode, if charger is detected (level) 1 : Exit of Power OFF mode, if charger insertion is detected (rising edge only)
5:4	res_timer	b00	RW	Set RESTime, after the last regulator has started 0 : RESTIME=10ms 1 : RESTIME=50ms 2 : RESTIME=100ms 3 : RESTIME=150ms
3	sd1_fsel	b0	RW	Selects between high and low frequency range 0 : 1 MHz if sd1_frequ=0, 3MHz if sd1_frequ=1 1 : 2 MHz if sd1_frequ=0, 4MHz if sd1_frequ=1
2	sd1_fast	b0	RW	Selects a faster regulation mode for SD1 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required
1	power_off_at_vsuplow	b0	RW	Switch ON Power OFF mode if low VSUP is detected during active or standby mode (Pin ON= low and bit auto_off=0) 0 : If low battery is detected, continuously monitor battery voltage and startup if battery voltage is above ResVoltrise 1 : If low battery is detected, enter power OFF mode
0	i2c_deva_bit1	b0	RW	

Figure 106:
Fuse8

Addr:a8h		Fuse8		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	usb_current	b0000	RW	Sets the USB input current limit. 0 : 94mA (default) 1 : 141mA 2 : 189mA 3 : 237mA 4 : 285mA 5 : 332mA 6 : 380mA 7 : 428mA 8 : 470mA 9 : 517mA 10 : 600mA 11 : 764mA 12 : 889mA 13 : 1065mA 14 : NA (1065mA) 15 : NA (1065mA)
3:1	ResVoltRise	b000	RW	This value determines the reset level ResVoltRise for rising VBAT. ResVoltFall is set to ResVoltRise-200mV by default 0 : 2.7V 1 : 2.9V 2 : 3.1V 3 : 3.2V 4 : 3.3V 5 : 3.4V 6 : 3.5V 7 : 3.6V
0	on_lpress_delay	b0	RW	Selects default state of the bit on_lpress_delay

Figure 107:
Fuse9

Addr:a9h		Fuse9		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reg4_del	b0	RW	Define delay for timeslot4 (regulator 4)
6	Reg3_del	b0	RW	Define delay for timeslot3 (regulator 3)
5	Reg2_del	b0	RW	Define delay for timeslot2 (regulator 2)
4	Reg1_del	b0	RW	Define delay for timeslot1 (regulator 1)
3	SupResEn	b0	RW	Presets that bit
2	onkey_lpress_en	b0	RW	Select default state of the onkey_lpress_en
1:0	NTC_input	b00	RW	Defines the NTC input 0 : No NTC input 1 : XIRQ_NTC pin 2 : GPIO3 pin 3 : GPIO4 pin

Figure 108:
Fuse10

Addr:aah		Fuse10		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reg2_addr	b0000	RW	Define startup regulator 2 0 : NA (00h) 1 : SD1 (01h) 2 : LDO1 (02h) 3 : LDO2 (03h) 4 : NA (04h) 5 : NA (05h) 6 : NA (06h) 7 : NA (07h) 8 : NA (08h) 9 : GPIO1 (09h) 10 : GPIO2 (0ah) 11 : GPIO3 (0bh) 12 : GPIO4 (0ch) 13 : GPIO5 (0dh) 14 : NA (0eh) 15 : NA (0fh)
3:0	Reg1_addr	b0000	RW	Define startup regulator 1 0 : NA (00h) 1 : SD1 (01h) 2 : LDO1 (02h) 3 : LDO2 (03h) 4 : NA (04h) 5 : NA (05h) 6 : NA (06h) 7 : NA (07h) 8 : NA (08h) 9 : GPIO1 (09h) 10 : GPIO2 (0ah) 11 : GPIO3 (0bh) 12 : GPIO4 (0ch) 13 : GPIO5 (0dh) 14 : NA (0eh) 15 : NA (0fh)

Figure 109:
Fuse11

Addr:abh		Fuse11		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reg1_V	b00000000	RW	Define startup voltage for regulator 1

Figure 110:
Fuse12

Addr:ach		Fuse12		
Bit	Bit Name	Default	Access	Bit Description
7:0	reg2_V	b00000000	RW	Define startup voltage for regulator 2

Figure 111:
Fuse13

Addr:adh		Fuse13		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reg4_addr	b0000	RW	Define startup regulator 4 0 : NA (00h) 1 : SD1 (01h) 2 : LDO1 (02h) 3 : LDO2 (03h) 4 : NA (04h) 5 : NA (05h) 6 : NA (06h) 7 : NA (07h) 8 : NA (08h) 9 : GPIO1 (09h) 10 : GPIO2 (0ah) 11 : GPIO3 (0bh) 12 : GPIO4 (0ch) 13 : GPIO5 (0dh) 14 : NA (0eh) 15 : NA (0fh)
3:0	Reg3_addr	b0000	RW	Define startup regulator 3 0 : NA (00h) 1 : SD1 (01h) 2 : LDO1 (02h) 3 : LDO2 (03h) 4 : NA (04h) 5 : NA (05h) 6 : NA (06h) 7 : NA (07h) 8 : NA (08h) 9 : GPIO1 (09h) 10 : GPIO2 (0ah) 11 : GPIO3 (0bh) 12 : GPIO4 (0ch) 13 : GPIO5 (0dh) 14 : NA (0eh) 15 : NA (0fh)

Figure 112:
Fuse14

Addr:aeh		Fuse14		
Bit	Bit Name	Default	Access	Bit Description
7:0	reg3_V	b00000000	RW	Define startup voltage for regulator 3

Figure 113:
Fuse15

Addr:afh		Fuse15		
Bit	Bit Name	Default	Access	Bit Description
7:0	reg4_V	b00000000	RW	Define startup voltage for regulator 4

Application Information

Figure 114:
Application Schematic

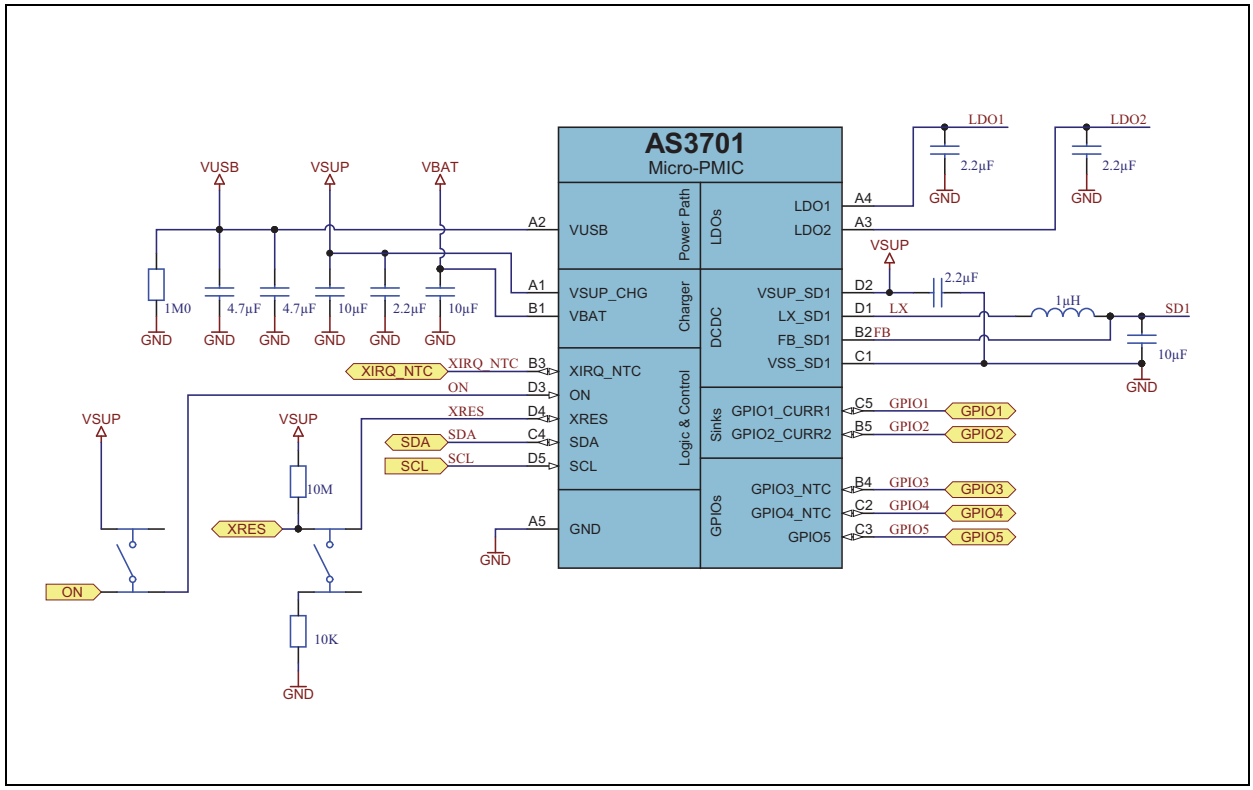


Figure 115:
Layout Guidelines for AS3701A

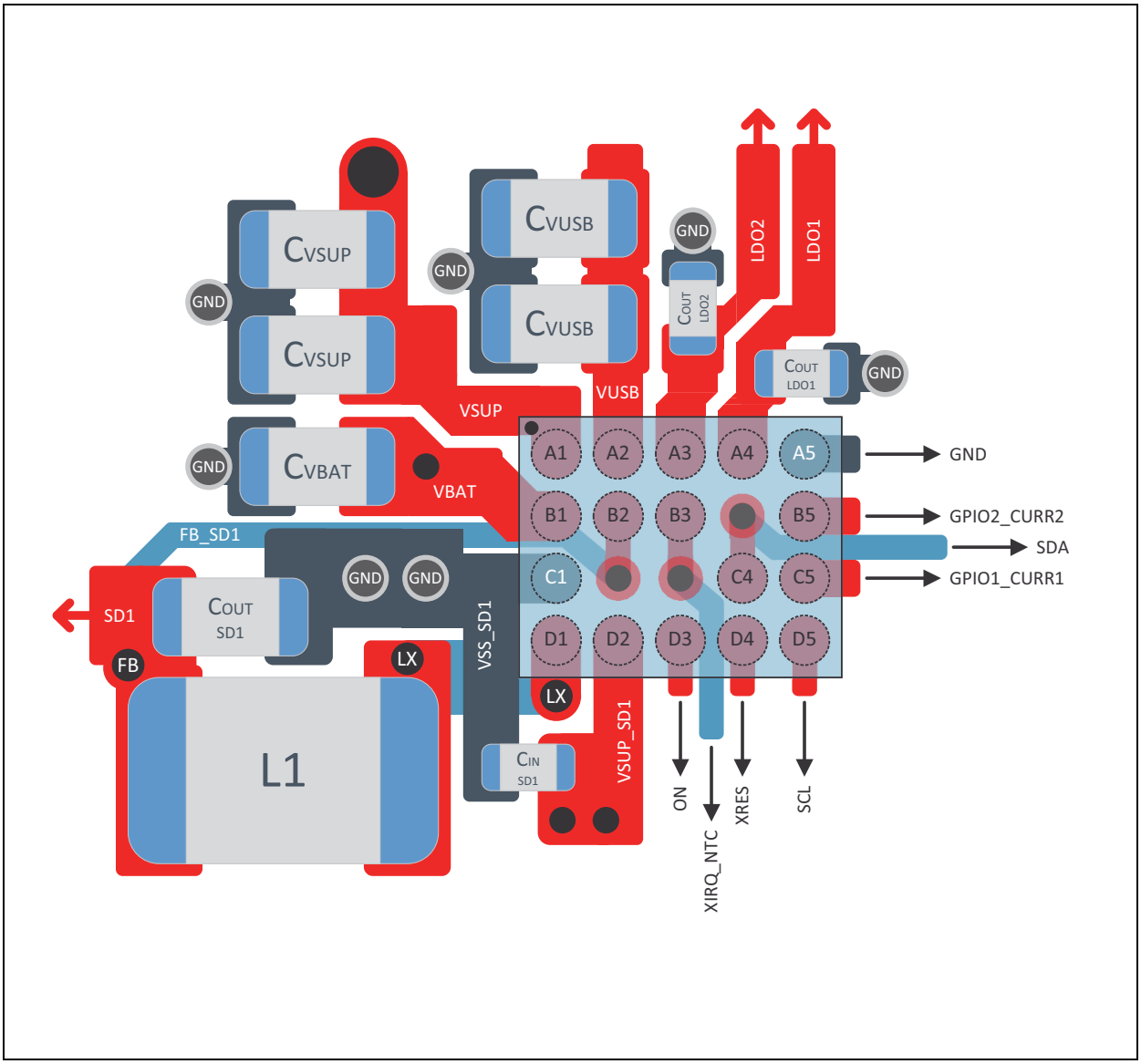
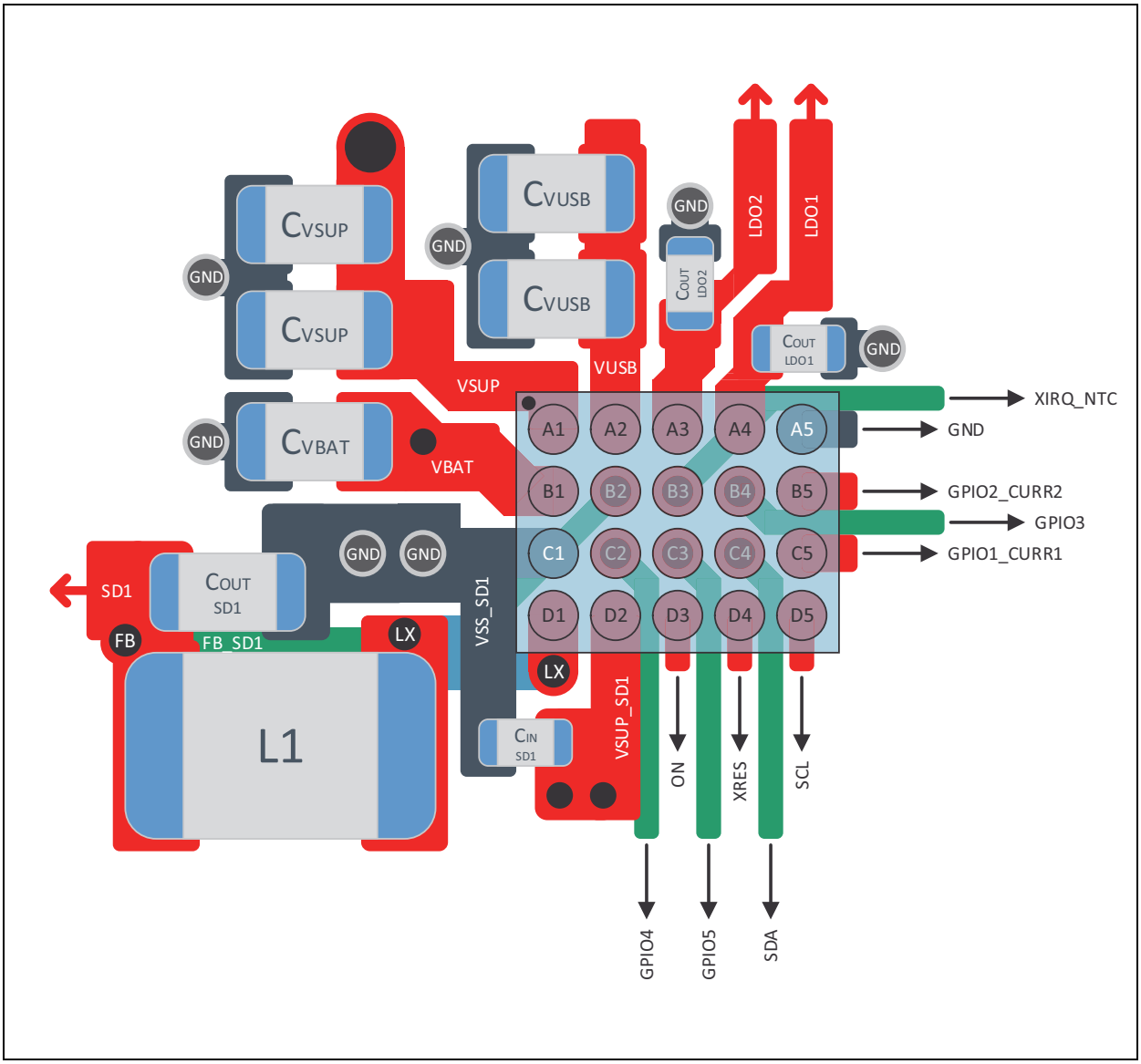
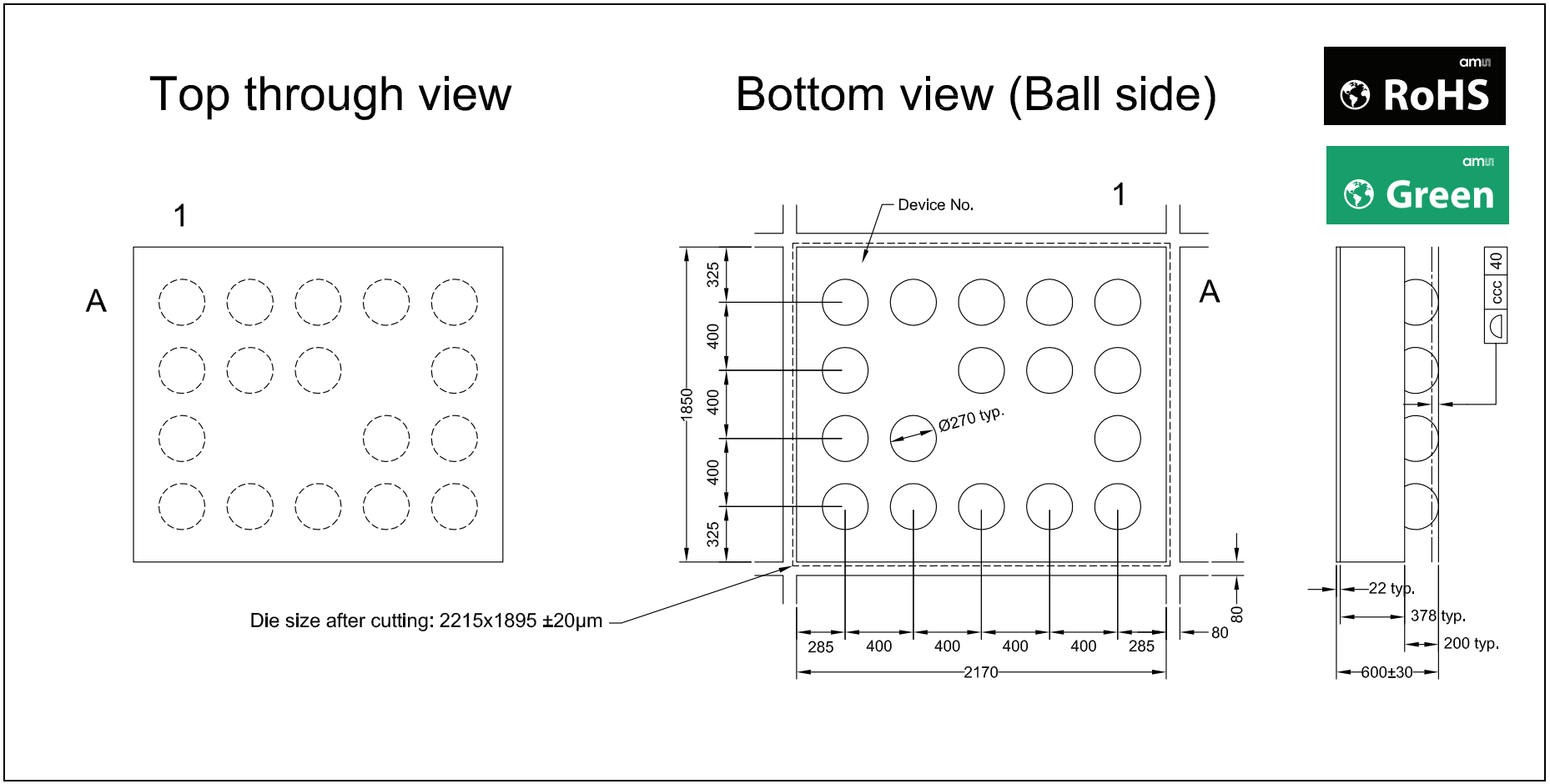


Figure 116:
Layout Guidelines for AS3701B



Package Drawings & Markings

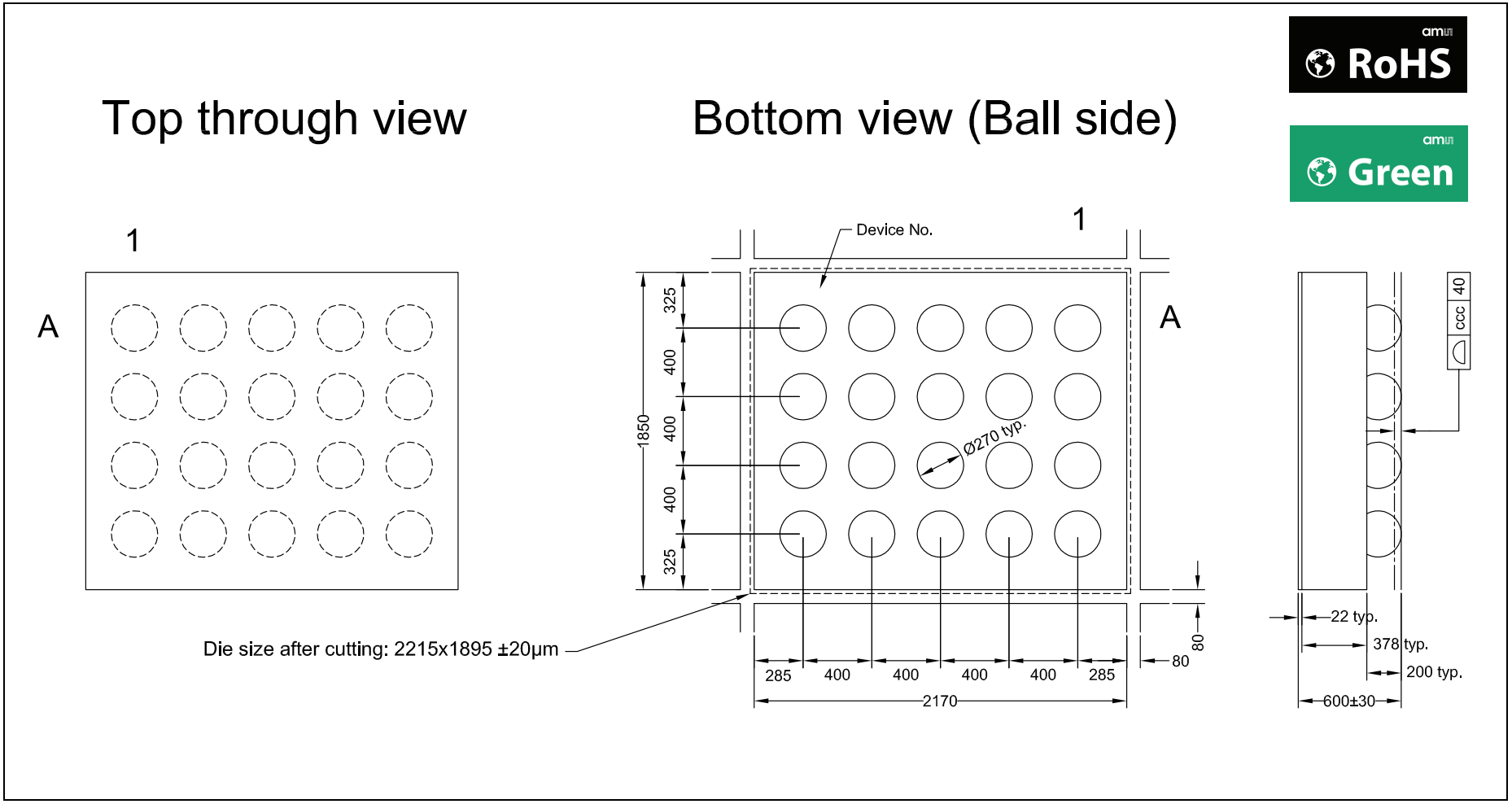
Figure 117:
CSP-17 0.4mm Pitch Package Drawing



Note(s):

1. Pin 1 = A1
2. ccc Coplanarity
3. All dimensions are in µm

Figure 118:
CSP-20 0.4mm Pitch Package Drawing



Note(s):

1. Pin 1 = A1
2. ccc Coplanarity
3. All dimensions are in µm

Figure 119:
AS3701A Marking

AS3701A Marking: Shows the package marking of the AS3701A product version

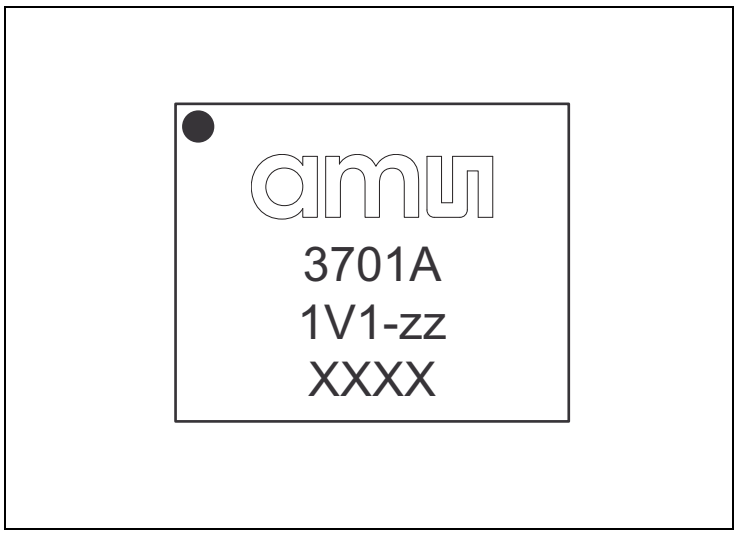


Figure 120:
AS3701B Marking

AS3701B Marking: Shows the package marking of the AS3701B product version

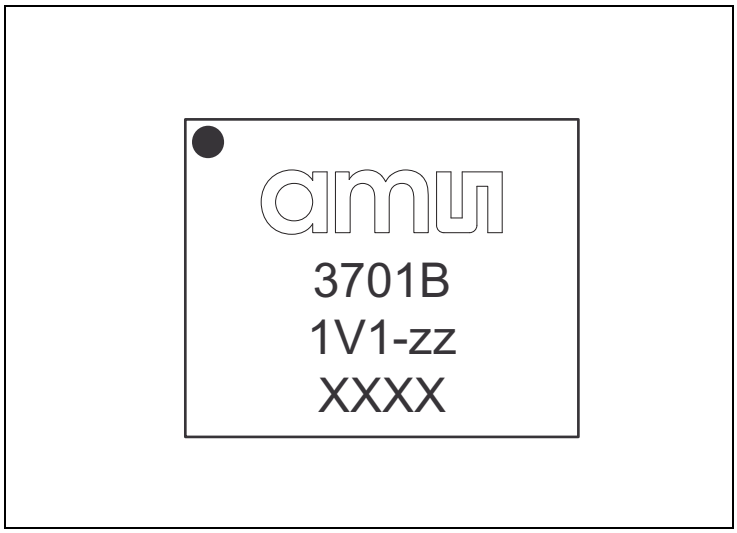


Figure 121:
Package Code

XXXX
Trace code

Figure 122:
Start-Up Revision Code

1V1-zz	Sequence
1V1-ES	Engineering samples, no sequence programmed or sequence programmed on request
1V1-00	Standard programming (no sequence programmed)
1V1-??	Other customer specified sequence programmed during production test (1)

Start-Up Revision Code: Shows the coding of the different startup sequences

Note(s):

1. Dedicated OTP startup sequence settings available upon request. Please contact www.ams.com/Technical-Support

Ordering & Contact Information

Figure 123:
Ordering Information

Ordering Code	Marking	OTP Programming	Delivery Form	Package
AS3701A-BWLT-ES	3701A 1V1-ES	Sequence programmable on request	T & R	17-Ball WL-CSP
AS3701A-BWLT-??	3701A 1V1-??	Customer specified sequence	T & R	17-Ball WL-CSP
AS3701B-BWLT-ES	3701B 1V1-ES	Sequence programmable on request	T & R	20-Ball WL-CSP
AS3701B-BWLT-00	3701B 1V1-00	Default sequence	T & R	20-Ball WL-CSP
AS3701B-BWLT-??	3701B 1V1-??	Customer specified sequence	T & R	20-Ball WL-CSP

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 1-06 (2015-Nov-19) to current revision 1-07 (2016-Apr-05)	Page
Updated Figure 44	37
Updated Figure 49	43

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide