PI6C4911504-03

High Performance LVPECL Fanout Buffer

Features

- 4 LVPECL outputs
- Up to 1.5GHz output frequency
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Two selectable inputs
- Low delay from input to output (Tpd typ. 1.5ns)
- 2.5V / 3.3V power supply
- Industrial temperature support
- TSSOP-20 package

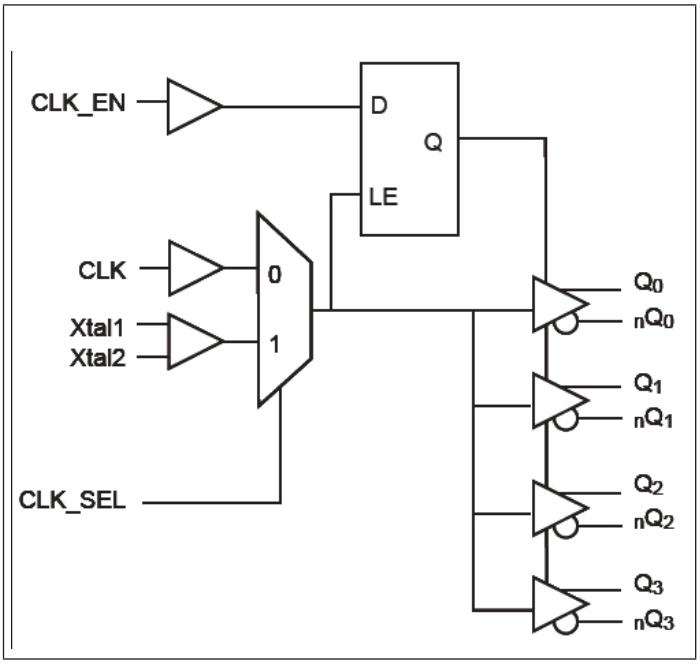
Description

The PI6C4911504-03 is a high performance fanout buffer device which supports up to 1.5GHz frequency. PI6C4911504-03 features selectable single-ended clock or crystal inputs and translates to four LVPECL outputs. The outputs are synchronized with input clock during asynchronous assertion /deassertion of CLK_EN pin. PI6C4911504-03 is ideal for crystal or LVCMOS/LVTTL to LVPECL translation. Typical clock translation and distribution applications are data-communications and telecommunications.This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

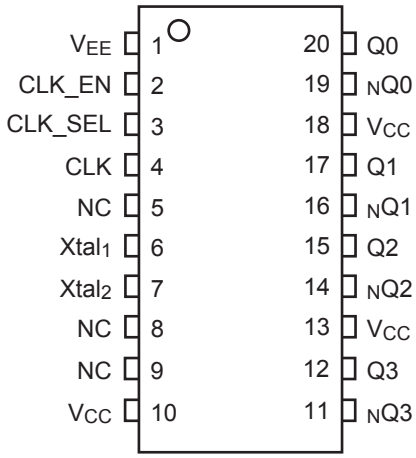
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (20-Pin TSSOP)



Pinout Table

Pin #	Pin Name	Type		Description
1	V_{EE}	Power		Negative power supply
2	CLK_EN	Input	Pullup	Clock output enable/ disable
3	CLK_SEL	Input	Pulldown	Clock input source selection pin
4	CLK	Input	Pulldown	Clock input
5	NC	-		No Connect
6	XTAL1	Input		Xtal input
7	XTAL2	Output		Xtal output
8, 9	NC	-		No connect
10, 13, 18	V_{CC}	Power		Power supply
11, 12	nQ3 Q3	Output		LVPECL output clock
14, 15	nQ2 Q2	Output		LVPECL output clock
16, 17	nQ1 Q1	Output		LVPECL output clock
19, 20	nQ0 Q0	Output		LVPECL output clock

Note: Pullup and Pulldown are for internal input resistors

Function Table

Table 1: Clock source input select function

CLK_SEL	Function
0	CLK is the selected reference input
1	XTAL is the selected input

Table 2: Clock output select function

CLK_EN	Function
0	All outputs disabled. Qx disabled low, nQx disabled High.
1	All outputs enabled.

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
Supply Voltage to Ground Potential (VCC)..... -0.5 to +4.65V
Inputs (Referenced to GND) ..... -0.5 to Vcc+0.5V
Clock Output (Referenced to GND)..... -0.5 to Vcc+0.5V
Soldering Temperature (Max of 10 seconds) .....+260°C
Latch up.....200mA

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		3.135		3.465	V
			2.375		2.625	V
I_{DD}	Power Supply Current	All outputs unloaded			130	mA
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		V_{CC}=3.3V	2.0		V_{CC}+0.3	V
V_{IL}	Input low voltage		V_{CC}=3.3V	-0.3		0.8	V
V_{IH}	Input high voltage		V_{CC}=2.5V	1.7		V_{CC}+0.3	V
V_{IL}	Input low voltage		V_{CC}=2.5V	-0.3		0.7	V
I_{IH}	Input High current	CLK, CLK_SEL				150	uA
		CLK_EN				10	uA
I_{IL}	Input Low current	CLK, CLK_SEL		-10			uA
		CLK_EN		-150			uA
C_{IN}	Input capacitance				4		pF
$R_{PULLUP/PULLDOWN}$	Input pullup and pulldown resistor				50		kΩ

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	V_{CC}=3.3V	2.1		2.6	V
		V_{CC}=2.5V	1.3		1.75	
V_{OL}	Output Low voltage	V_{CC}=3.3V	1.0		1.8	V
		V_{CC}=2.5V	0.4		0.8	

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL			1500	MHz
T_r	Output rise time	From 20% to 80%		150		ps
T_f	Output fall time	From 80% to 20%		150		ps
T_{ODC}	Output duty cycle		48		52	%
V_{PP}	Output swing Single-ended	LVPECL outputs	400			mV
T_j	Buffer additive jitter RMS			0.03		ps
T_{SK}	Output Skew	4 outputs devices, outputs in same bank, with same load, at DUT.		25		ps
T_{PD}	Propagation Delay			1500		ps
T_{OD}	Valid to HiZ		200			ns
T_{OE}	HiZ to valid		200			ns

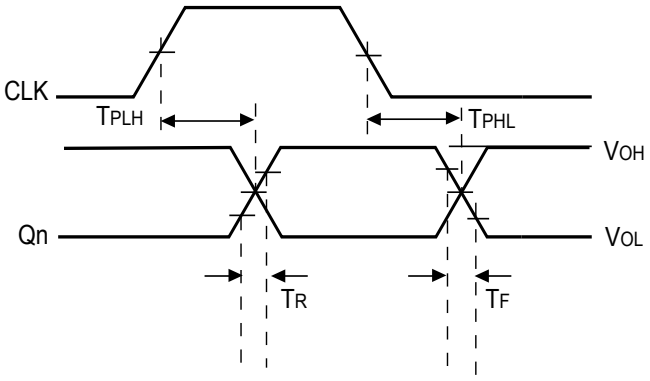
Notes:
All parameters are measured with CMOS input of 266MHz unless stated otherwise

Crystal Characteristics

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Mode of Oscillation			Fundamental		
Frequency		12		50	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

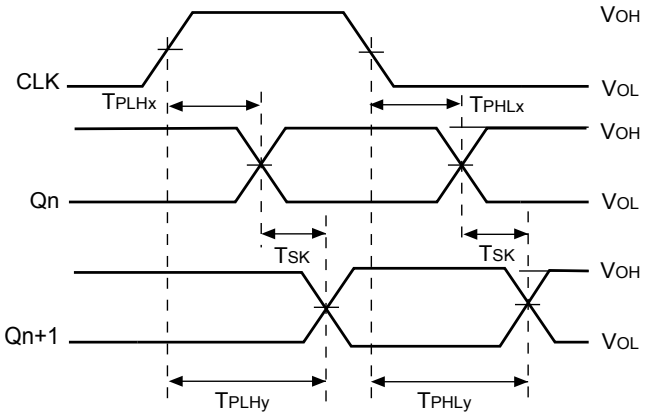
Propagation Delay

Propagation Delay T_{PD}



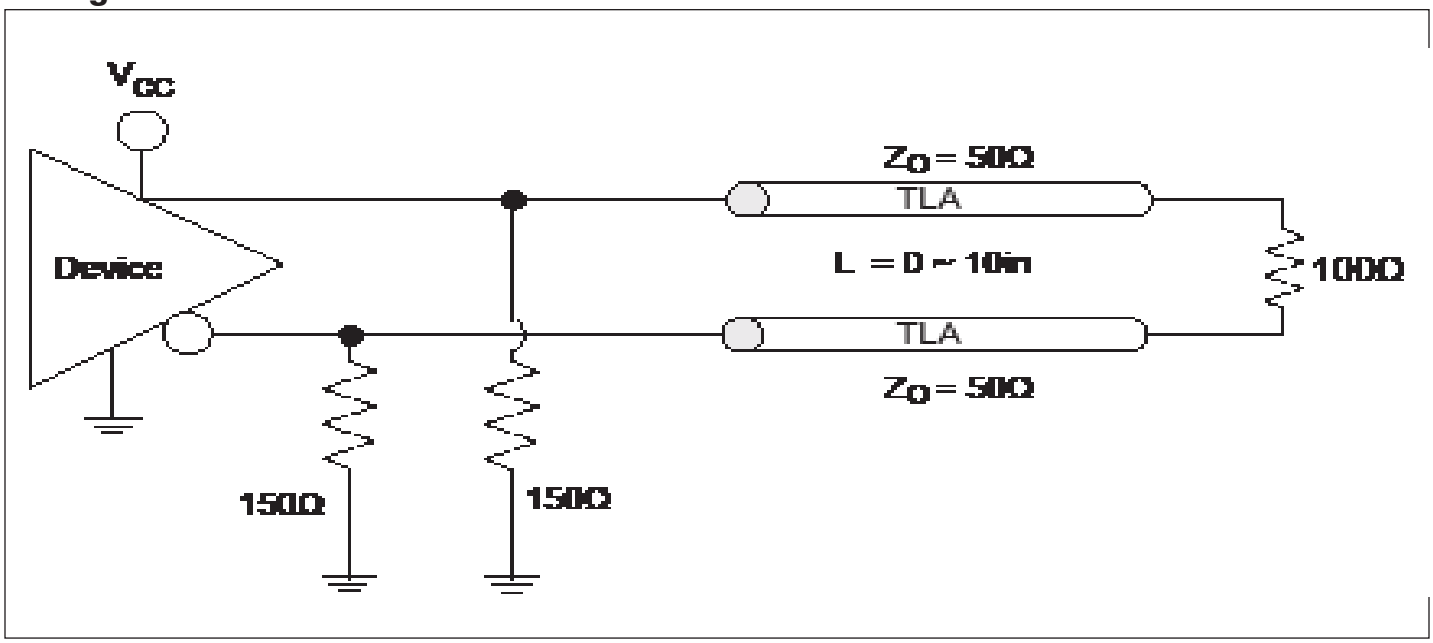
Output Skew

Output Skew T_{SK}

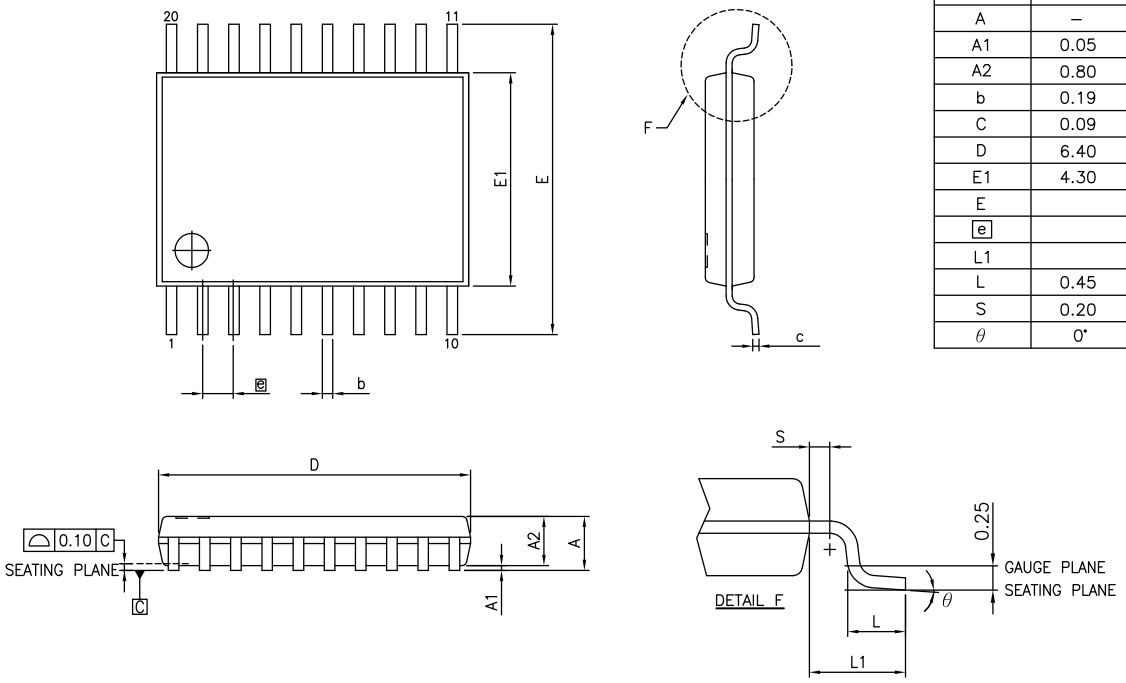


$T_{SK} = T_{PLHy} - T_{PLHx}$ or $T_{SK} = T_{PHLy} - T_{PHLx}$

Configuration Test Load Board Termination for LVPECL



Packaging Mechanical: 20-Contact TSSOP (L)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. Refer JEDEC MO-153F/AC
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 20-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1311 **REVISION: F**

12-0373

Ordering Information

Ordering Number	Package Code	Package Description
PI6C4911504-03LIE	L	Pb-free & Green 20-Contact TSSOP

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **E = Pb-free and Green**
- **X suffix = Tape/Reel**