ICS873033

HIGH SPEED, ÷4 DIFFERENTIAL-TO-3.3V, 5V LVPECL/ECL CLOCK GENERATOR

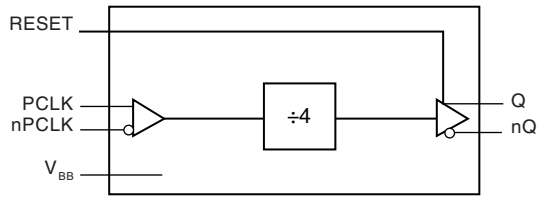
GENERAL DESCRIPTION

The ICS873033 is a high speed, high performance Differential-to-3.3V, 5V LVPECL/ECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS873033 is characterized to operate from either a 3.3V or a 5V power supply.

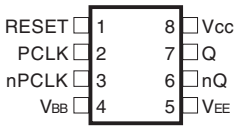
FEATURES

- One differential 3.3V, 5V LVPECL / ECL output
- One differential PCLK, nPCLK input pair
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Input frequency: 3.2GHz (maximum)
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Additive phase jitter, RMS: 0.20ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 3.0V to 5.5V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -5.5V to -3.0V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS873033
8-Lead SOIC
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

ICS873033
8-Lead TSSOP, 118 mil
3mm x 3mm x 0.95mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	RESET	Input	Pulldown	Reset pin. Single-ended 100h LVPECL interface levels.
2	PCLK	Input	Pulldown	Clock input. Default LOW when left floating. LVPECL interface levels.
3	nPCLK	Input	Pulldown	Clock input. LVPECL interface levels.
4	V_{BB}	Output		Bias voltage.
5	V_{EE}	Power		Negative supply pin.
6, 7	nQ, Q	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Positive supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ

TABLE 3. TRUTH TABLE

Inputs			Outputs	
PCLK	nPCLK	RESET	Q	nQ
X	X	LH	L	H
LH	HL	L	÷4	÷4

LH = LOW to HIGH transistion
HL = HIGH to LOW transistion

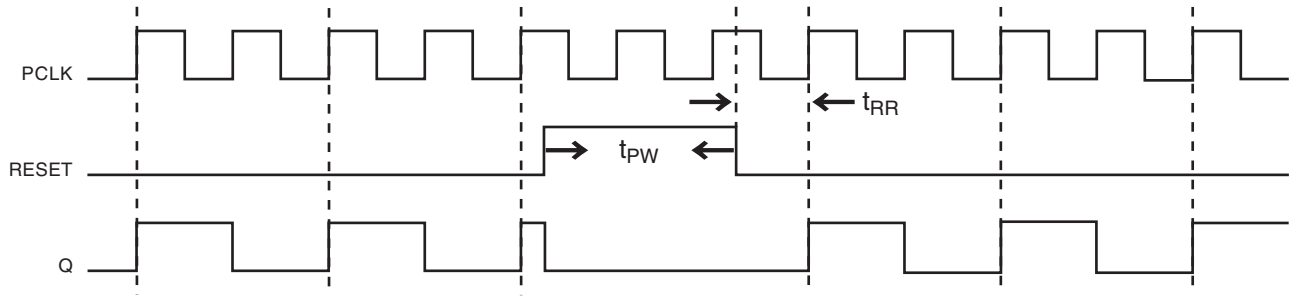


FIGURE 1. TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) for 8 Lead SOIC	112.7°C/W (0 lfpm)
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) for 8 Lead TSSOP	101.7°C/W (0 m/s)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.0V TO 5.5V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.0	3.3	5.5	V
I_{EE}	Power Supply Current				30	mA

TABLE 4B. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.33	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage(Single-Ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage(Single-Ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference		1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	-10			-10			-10			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3V to -2.2V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		3.875	3.975	4.08	3.925	3.995	4.07	3.995	4.03	4.065	V
V_{OL}	Output Low Voltage; NOTE 1		3.105	3.245	3.38	3.125	3.22	3.315	3.14	3.235	3.33	V
V_{IH}	Input High Voltage(Single-Ended)		3.775		4.06	3.775		4.06	3.775		4.06	V
V_{IL}	Input Low Voltage(Single-Ended)		3.13		3.465	3.13		3.465	3.13		3.465	V
V_{BB}	Output Voltage Reference		3.56		3.68	3.56		3.68	3.56		3.68	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		5	1.2		5	1.2		5	V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	-10			-10			-10			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2V to -0.5V.
NOTE 1: Outputs terminated with 50W to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

TABLE 4D. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.5V TO -3.0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage(Single-Ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage(Single-Ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference		-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	PCLK, nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK, nPCLK	-10			-10			-10			µA

Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

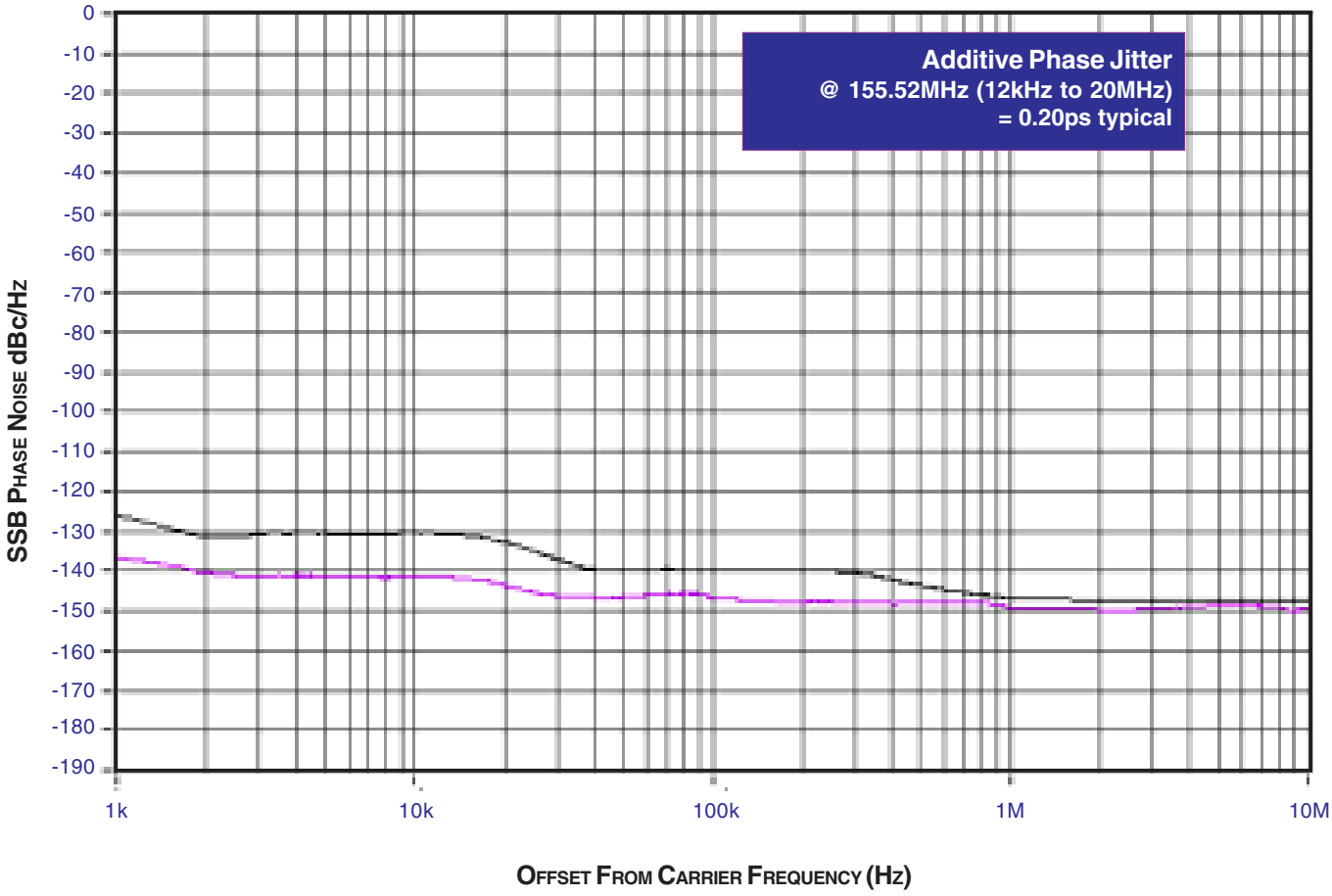
TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.5V TO -3.0V OR V_{CC} = 3.0V TO 5.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Input Frequency				3.2			3.2			3.2	GHz
t_{PD}	Propagation Delay; NOTE 1		300		475	300	430	530	350	450	550	ps
$t$jit(Ø)	Buffer Additive Phase Jitter, RMS; 155.52MHz, Integration Range 12kHz - 20MHz; Refer to Additive Phase Jitter Section			0.20			0.20			0.20		ps
t_{RR}	Set/Reset Recovery; NOTE 2		150	100		200	100		200	100		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%	100		250	100		250	100		250	ps
t_{PW}	Pulse Width; NOTE 3	RESET	550	480		550	480		550	480		ps

All parameters are measured at f ≤ 1.7GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: See Figure 1, Timing Diagram.

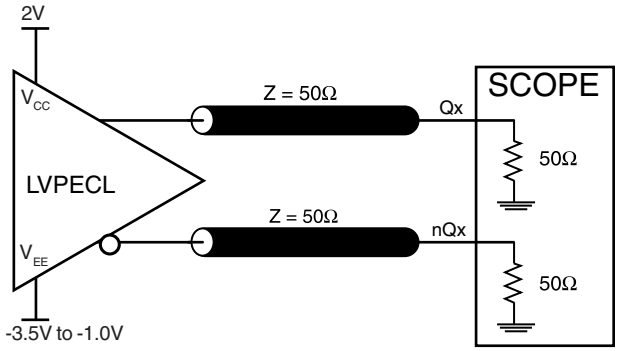
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

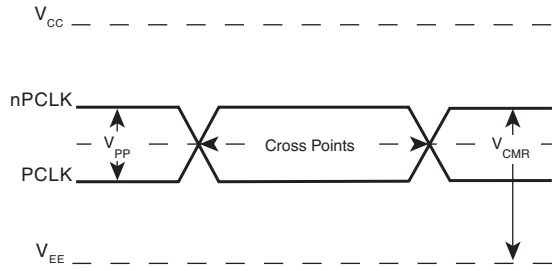


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

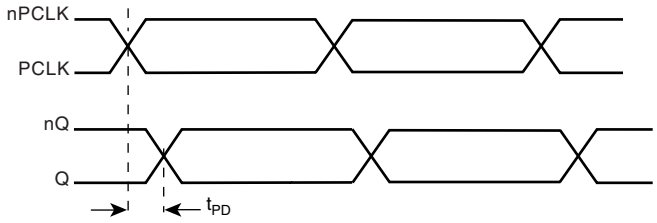
PARAMETER MEASUREMENT INFORMATION



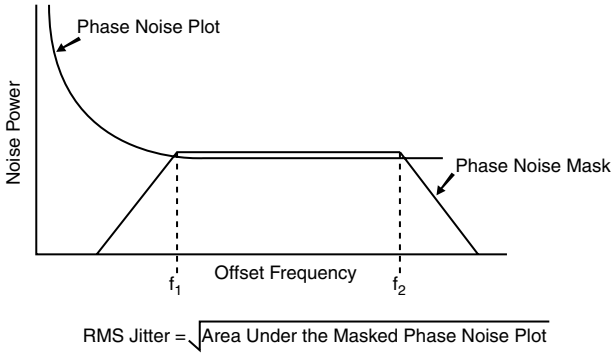
OUTPUT LOAD AC TEST CIRCUIT



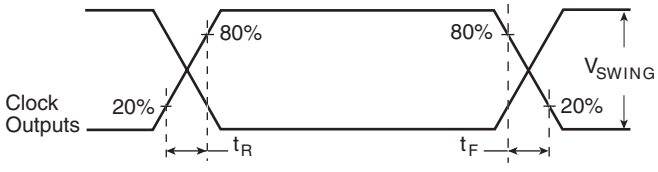
DIFFERENTIAL INPUT LEVEL



PROPAGATION DELAY



RMS PHASE JITTER



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

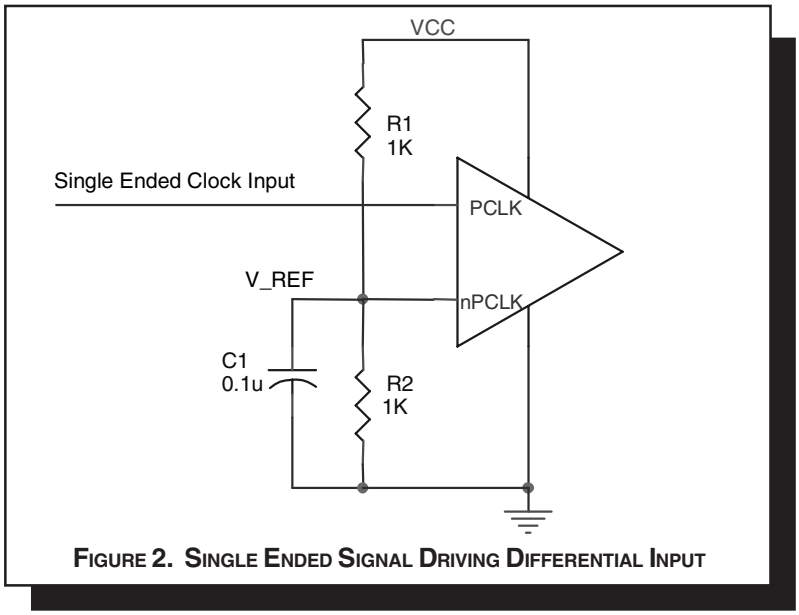


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 3 shows an example of the differential input that can be wired to accept single ended levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

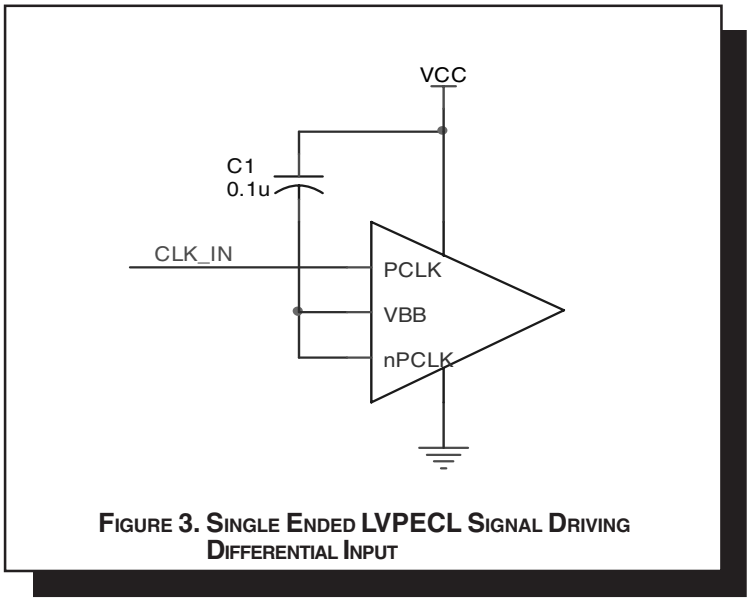


FIGURE 3. SINGLE ENDED LVPECL SIGNAL DRIVING DIFFERENTIAL INPUT

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

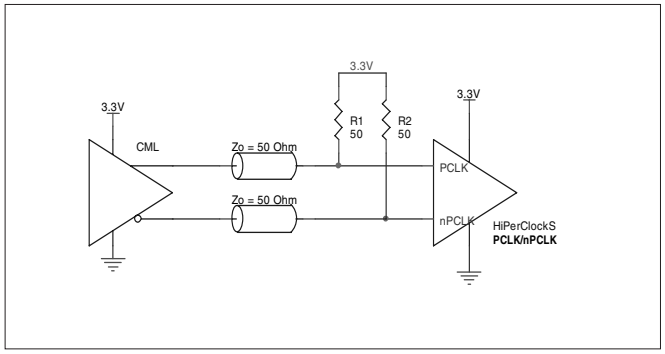


FIGURE 4A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

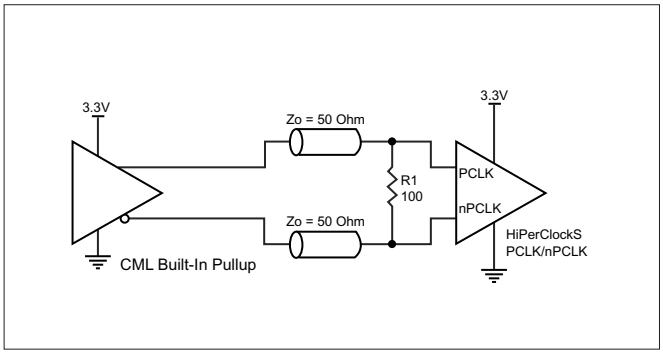


FIGURE 4B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

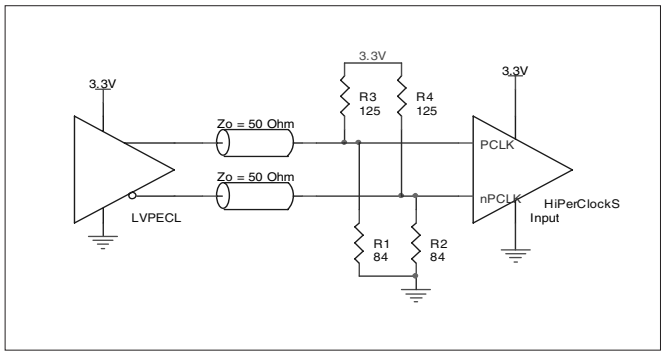


FIGURE 4C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

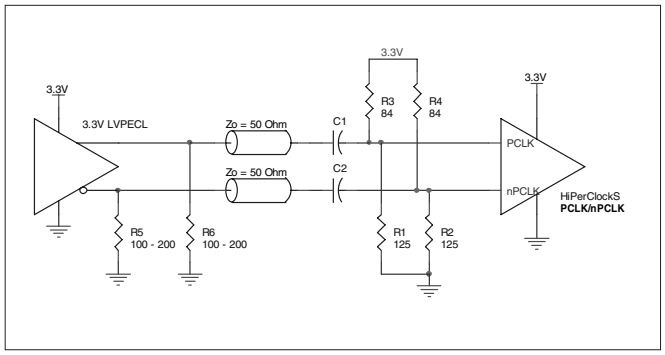


FIGURE 4D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

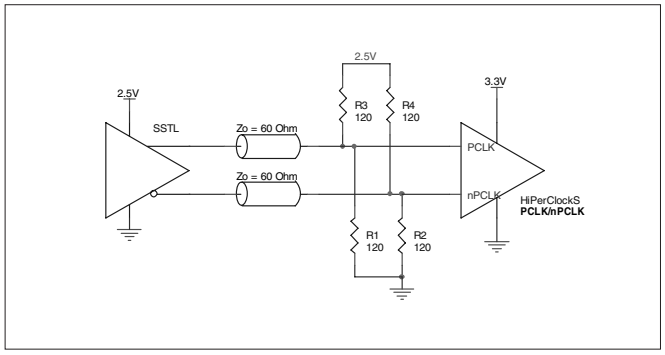


FIGURE 4E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

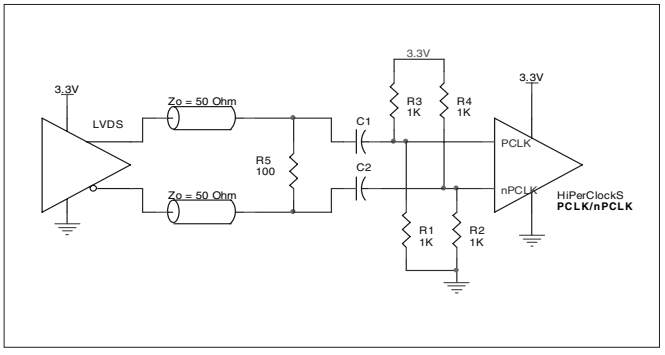


FIGURE 4F. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

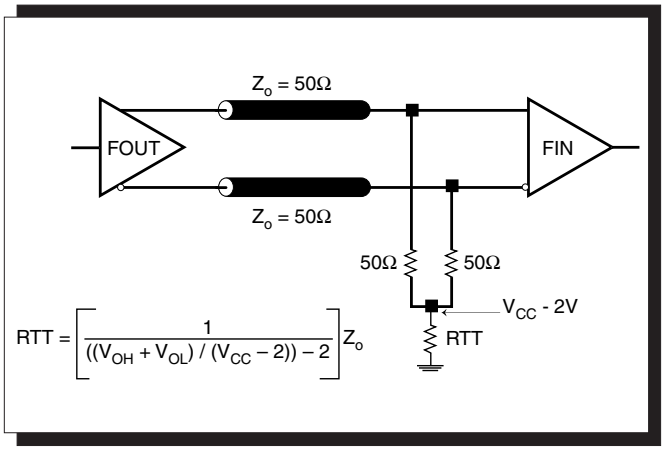


FIGURE 5A. LVPECL OUTPUT TERMINATION

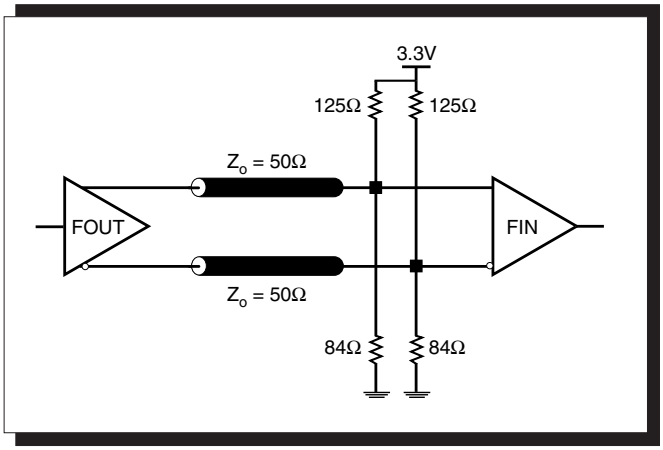


FIGURE 5B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 5V LVPECL OUTPUT

This section shows examples of 5V LVPECL output termination. *Figure 6A* shows standard termination for 5V LVPECL. The termination requires matched load of 50Ω resistors pull down to V_{CC} - 2V = 3V at the receiver. *Figure 6B* shows Thevenin equivalence of Figure 6A. In actual application where the 3V DC power supply is not available, this approached is normally used.

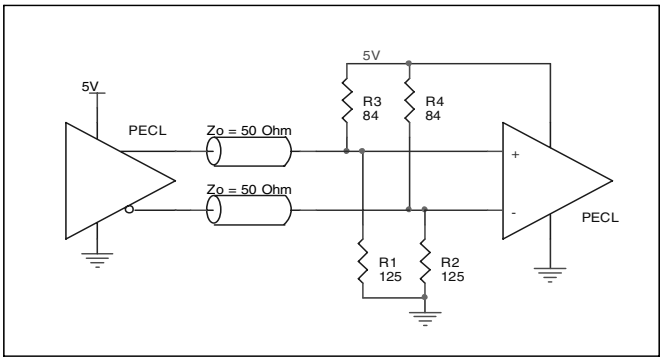


FIGURE 6A. STANDARD 5V PECL OUTPUT TERMINATION

FIGURE 6B. 5V PECL OUTPUT TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS873033.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS873033 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 5.5V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 5.5V * 30mA = **165mW**
- Power $(outputs)_{MAX}$ = **30.94mW/Loaded Output pair**

Total Power $_{MAX}$ (5.5V, with all outputs switching) = 165mW + 30.94mW = **195.94mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.196W * 103.3°C/W = 105.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6A. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 6B. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

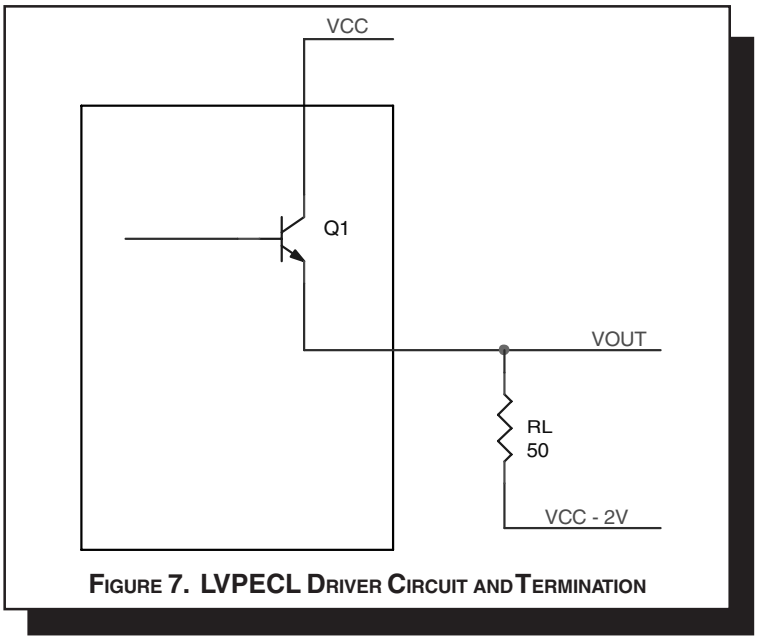


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.935V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.935V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.67V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.67V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V =$ **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V =$ **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.94mW**

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS873033 is: 165

Pin compatible with MC100EP33

PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

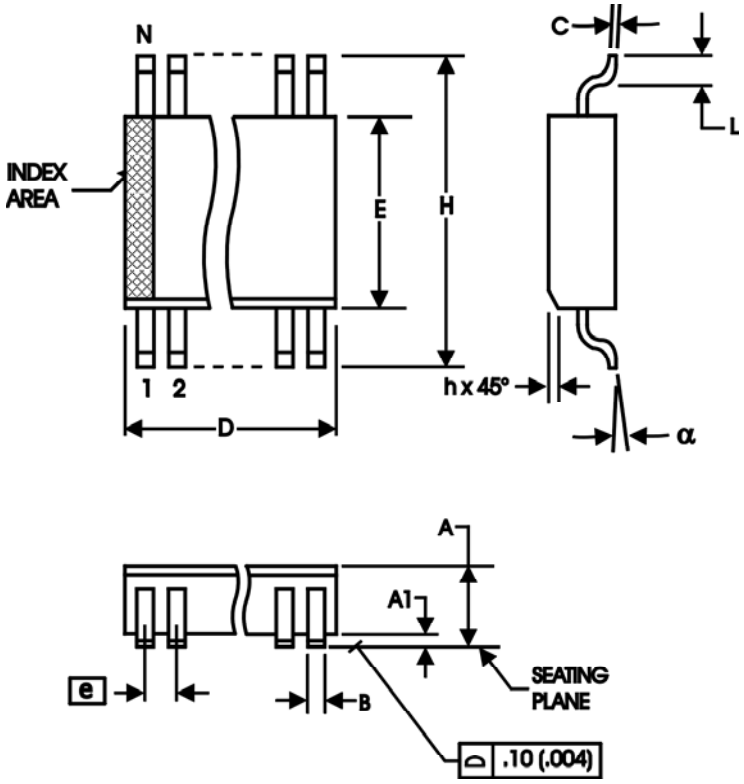


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

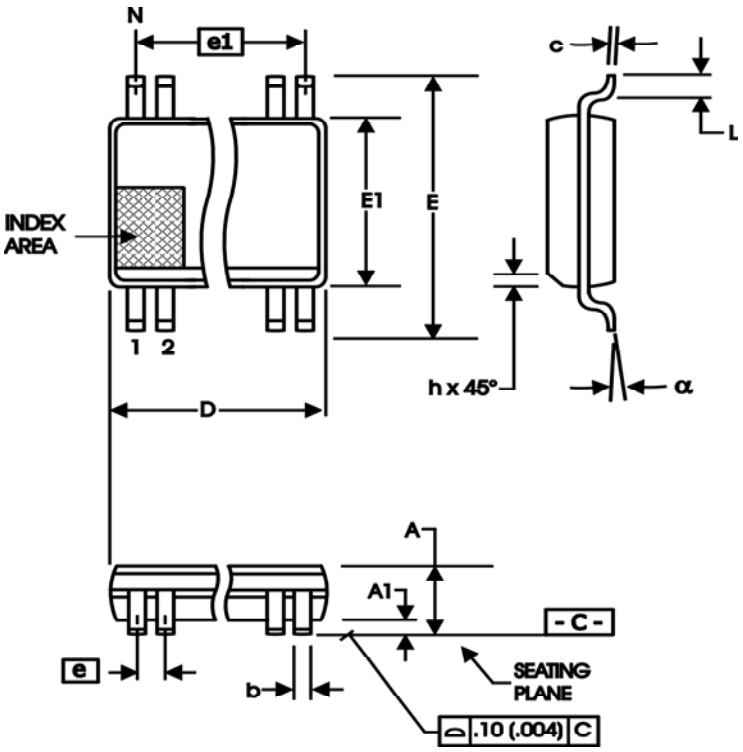


TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.10
A1	0	0.15
A2	0.79	0.97
b	0.22	0.38
c	0.08	0.23
D	3.00 BASIC	
E	4.90 BASIC	
E1	3.00 BASIC	
e	0.65 BASIC	
e1	1.95 BASIC	
L	0.40	0.80
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-187

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS873033AM	873033AM	8 lead SOIC	tube	-40°C to 85°C
ICS873033AMT	873033AM	8 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS873033AMLF	873033AL	8 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS873033AMLFT	873033AL	8 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C
ICS873033AG	033A	8 lead TSSOP	tube	-40°C to 85°C
ICS873033AGT	033A	8 lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS873033AGLF	TBD	8 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS873033AGLFT	TBD	8 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T9	16	Ordering Information - Added TSSOP package marking	12/19/07