

N-channel 100 V, 0.002 Ω typ., 180 A STripFET™ F7
Power MOSFETs in H²PAK-2 and H²PAK-6 packages

Datasheet - production data

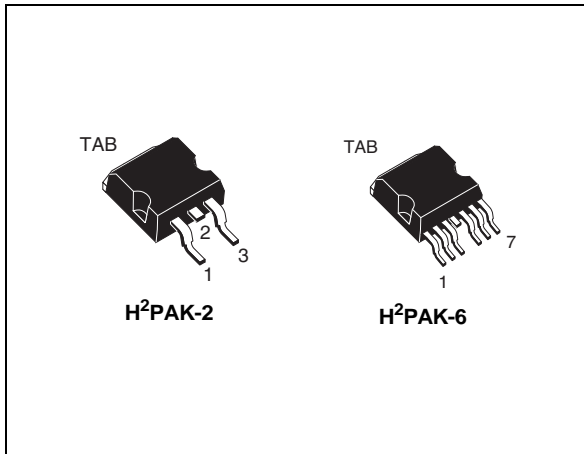
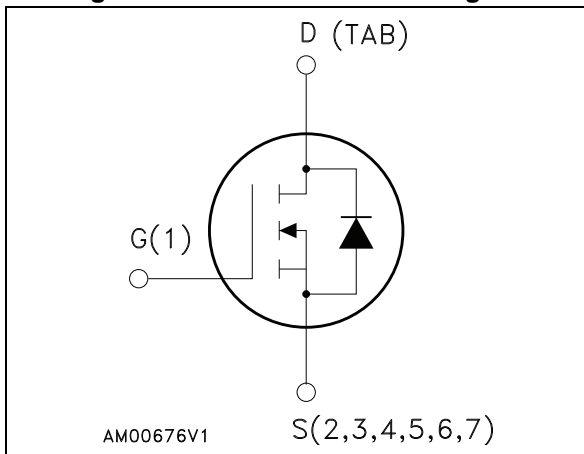


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D
STH240N10F7-2	100 V	0.0025 Ω	180 A
STH240N10F7-6			

- Ultra low on-resistance
- 100% avalanche tested

Applications

- High current switching applications

Description

These N-channel Power MOSFETs utilize the STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STH240N10F7-2	240N10F7	H ² PAK-2	Tape and reel
STH240N10F7-6		H ² PAK-6	

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves) 6
- 3 Test circuits 8**
- 4 Package mechanical data 9**
 - 4.1 H2PAK-2, STH240N10F7-2 10
 - 4.2 H2PAK-6, STH240N10F7-6 13
- 5 Revision history 16**

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	500	mJ
T_j	Operating junction temperature	- 55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting $T_j = 25^\circ\text{C}$, $I_d = 45\text{A}$, $V_{dd} = 50\text{V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu A$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 100\ V$			1	μA
		$V_{GS} = 0, V_{DS} = 100\ V, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0, V_{GS} = +20\ V$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ V, I_D = 60\ A$		0.002	0.0025	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 25\ V, f = 1\ MHz$	-	11550	-	pF
C_{oss}	Output capacitance		-	2950	-	pF
C_{riss}	Reverse transfer capacitance		-	217	-	pF
Q_g	Total gate charge	$V_{DD} = 50\ V, I_D = 180\ A,$	-	160	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\ V$	-	48	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14)	-	38	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ V, I_D = 90\ A, R_G = 4.7\ \Omega, V_{GS} = 10\ V$ (see Figure 13 , Figure 18)	-	49	-	ns
t_r	Rise time		-	139	-	ns
$t_{d(off)}$	Turn-off delay time		-	110	-	ns
t_f	Fall time		-	112	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS}=0, I_{SD}=180\text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD}=180\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD}=64\text{ V}, T_j=150^\circ\text{C}$ (see Figure 15)	-	108		ns
Q_{rr}	Reverse recovery charge		-	315		nC
I_{RRM}	Reverse recovery current		-	5.8		A

1. Pulse width limited by safe operating area.
2. Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

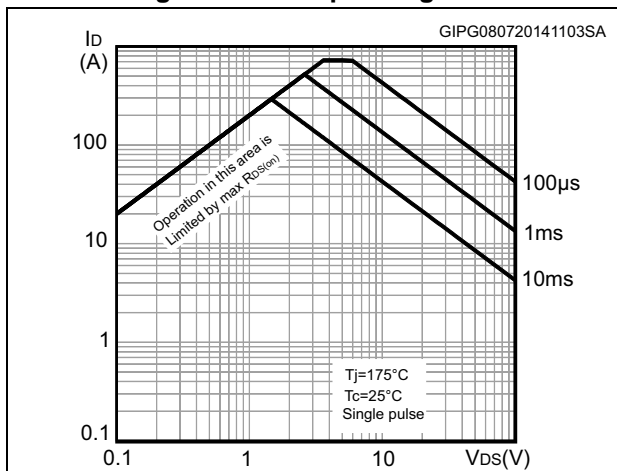


Figure 3. Thermal impedance

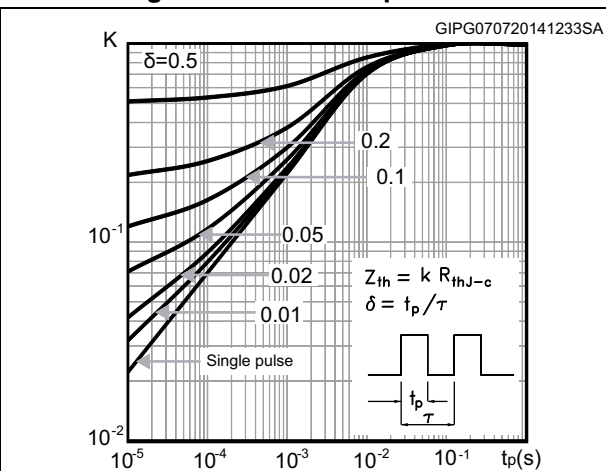


Figure 4. Output characteristics

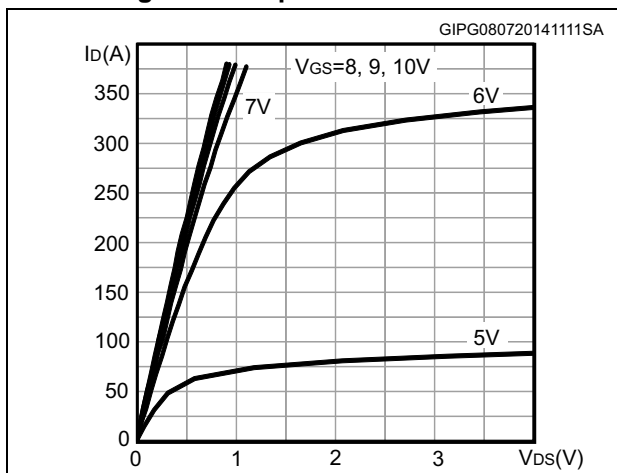


Figure 5. Transfer characteristics

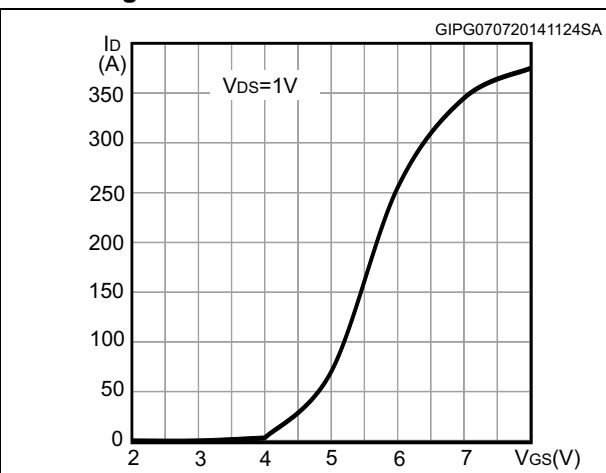


Figure 6. Gate charge vs gate-source voltage

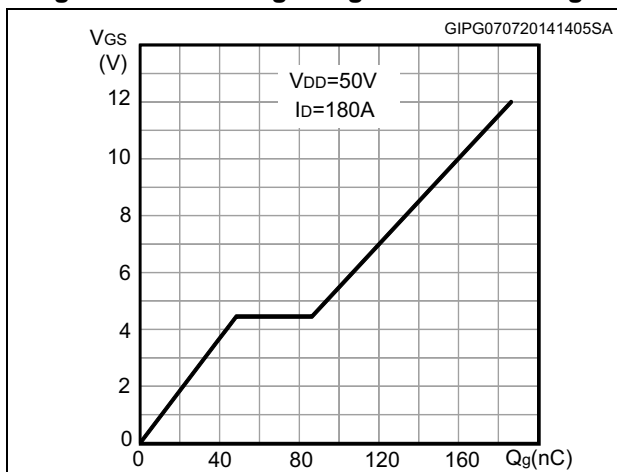


Figure 7. Static drain-source on-resistance

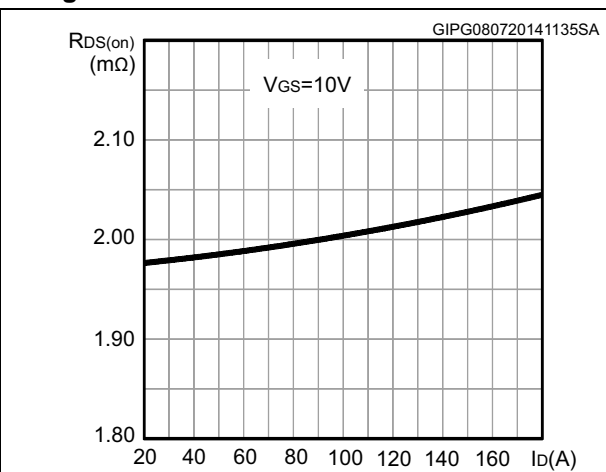


Figure 8. Capacitance variations

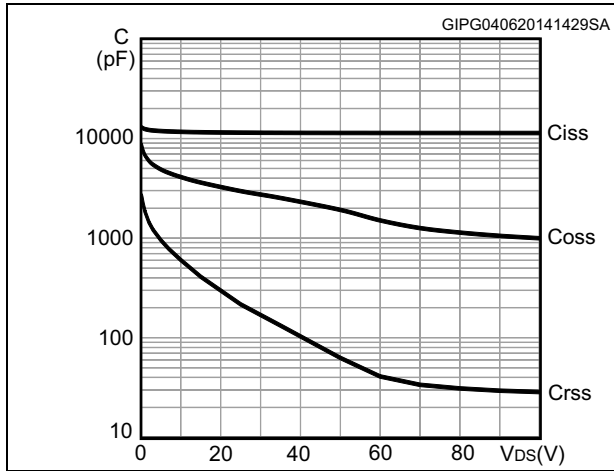


Figure 9. Normalized gate threshold voltage vs temperature

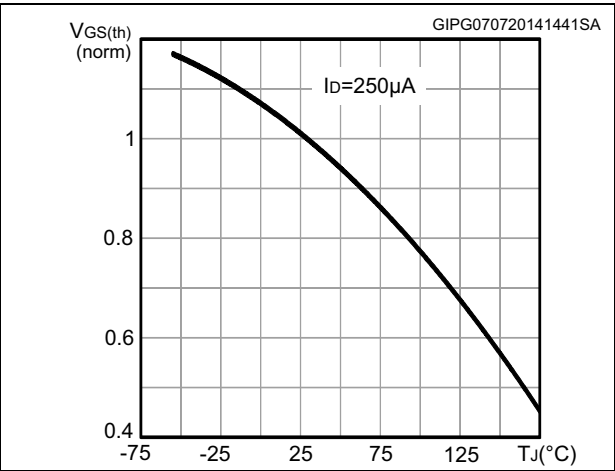


Figure 10. Normalized on-resistance vs temperature

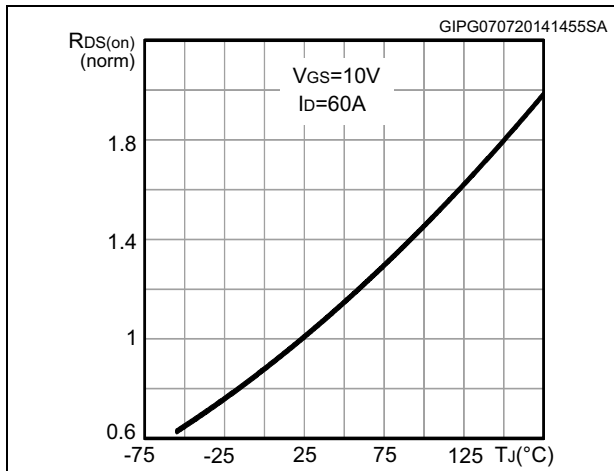


Figure 11. Normalized V(BR)DSS vs temperature

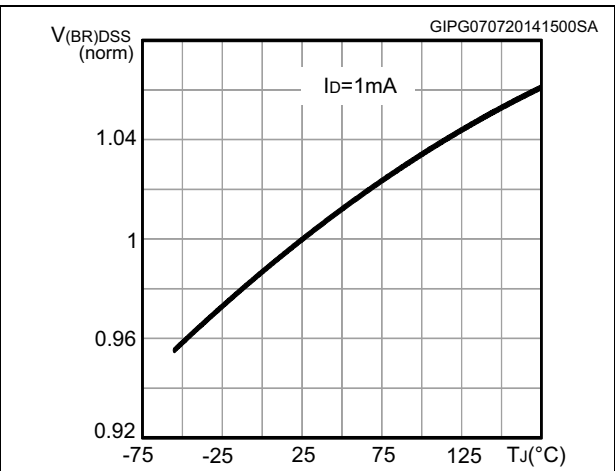
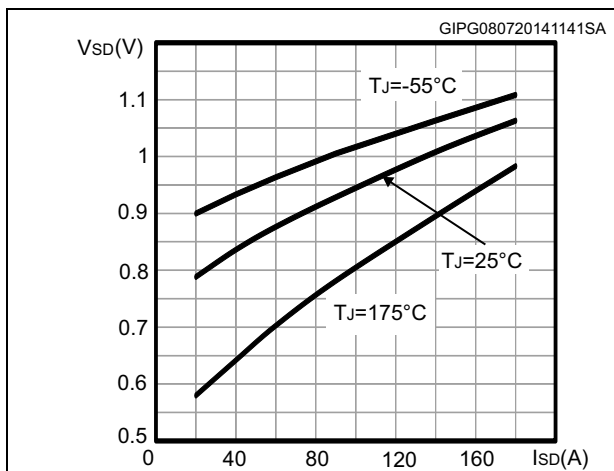


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

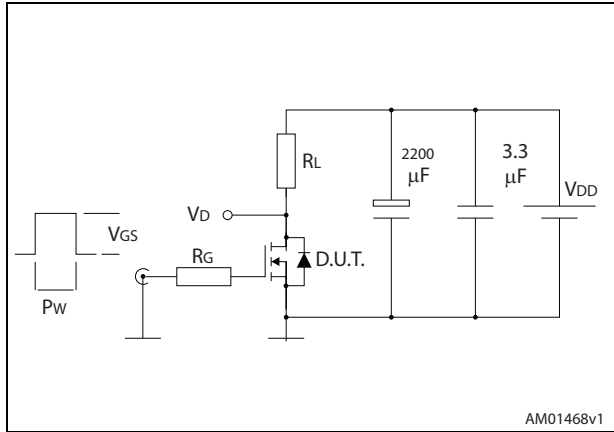


Figure 14. Gate charge test circuit

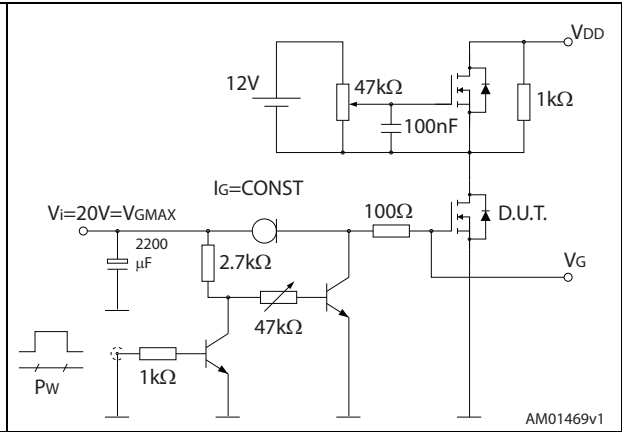


Figure 15. Test circuit for inductive load switching and diode recovery times

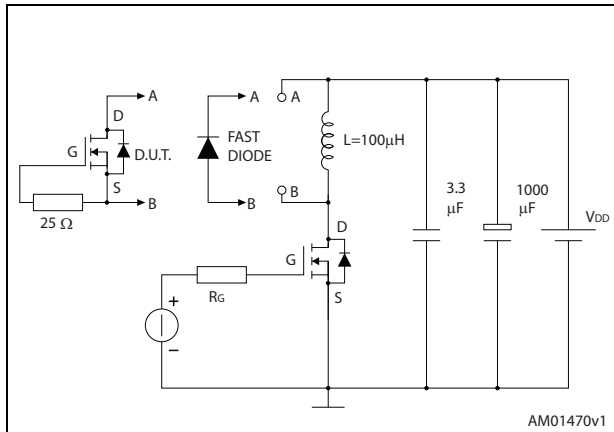


Figure 16. Unclamped inductive load test circuit

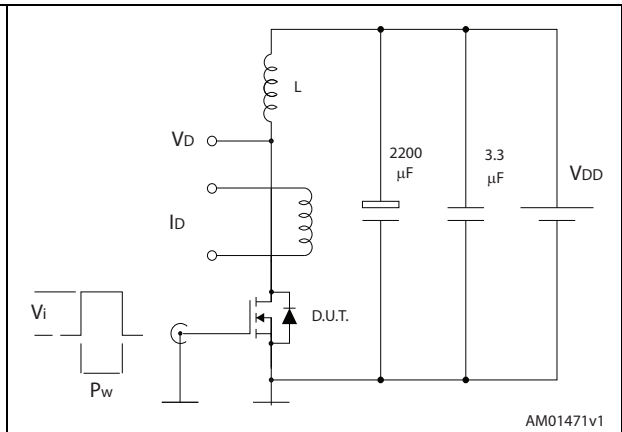


Figure 17. Unclamped inductive waveform

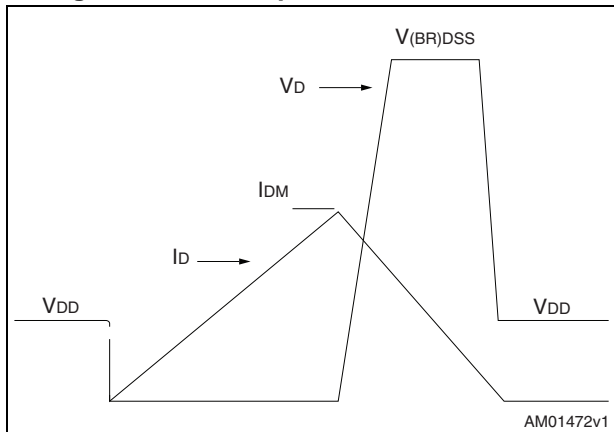
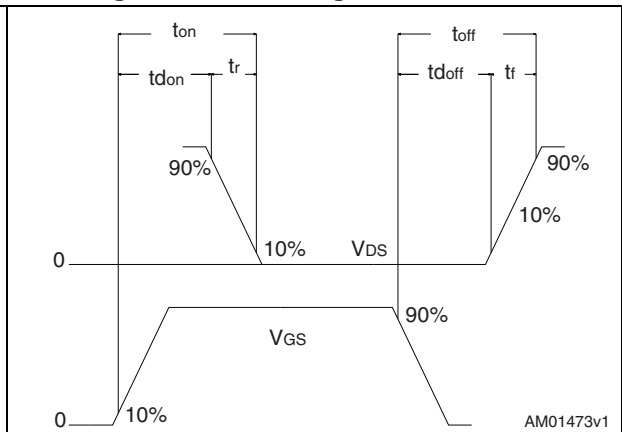


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 H²PAK-2, STH240N10F7-2

Figure 19. H²PAK-2 drawing

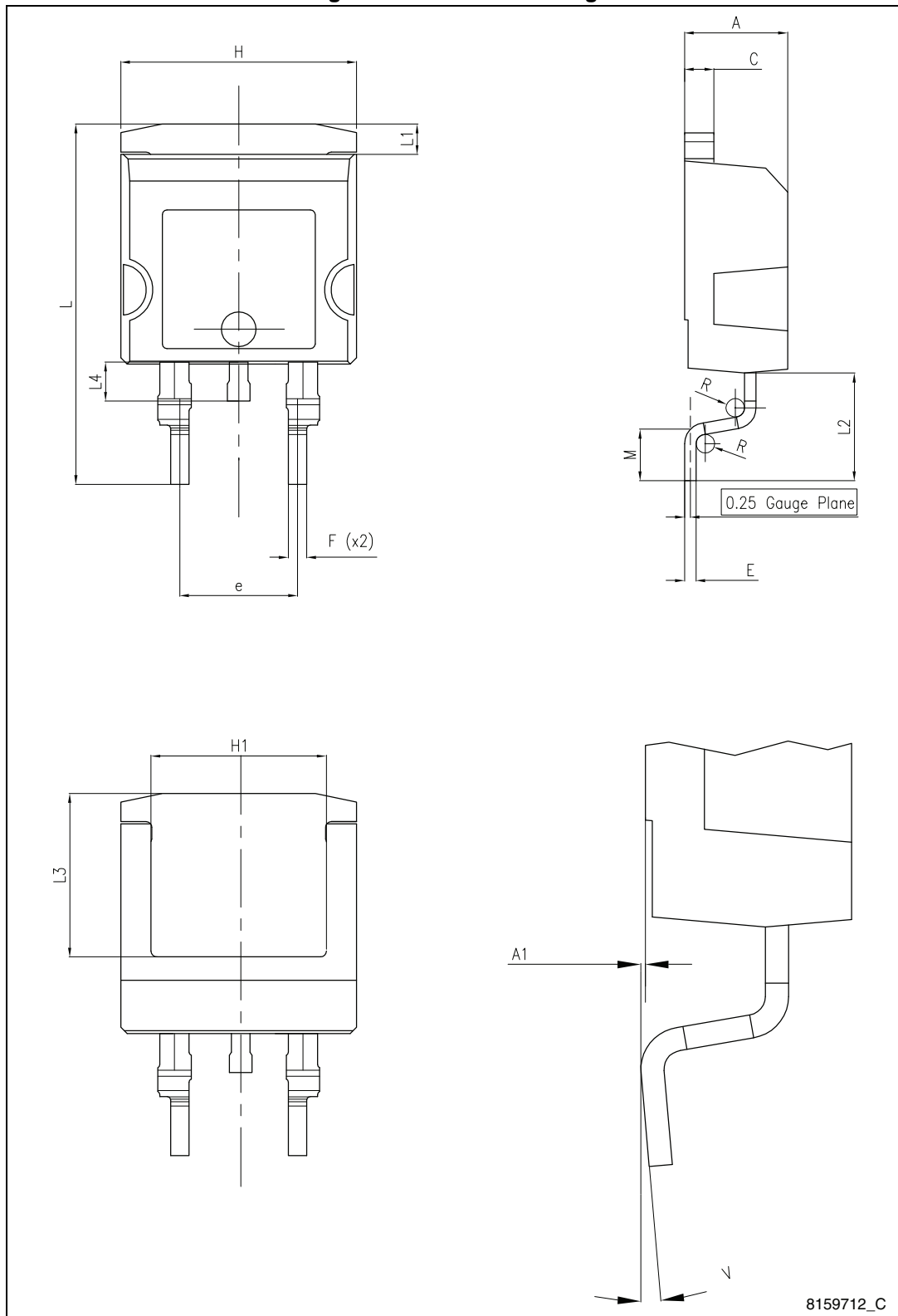
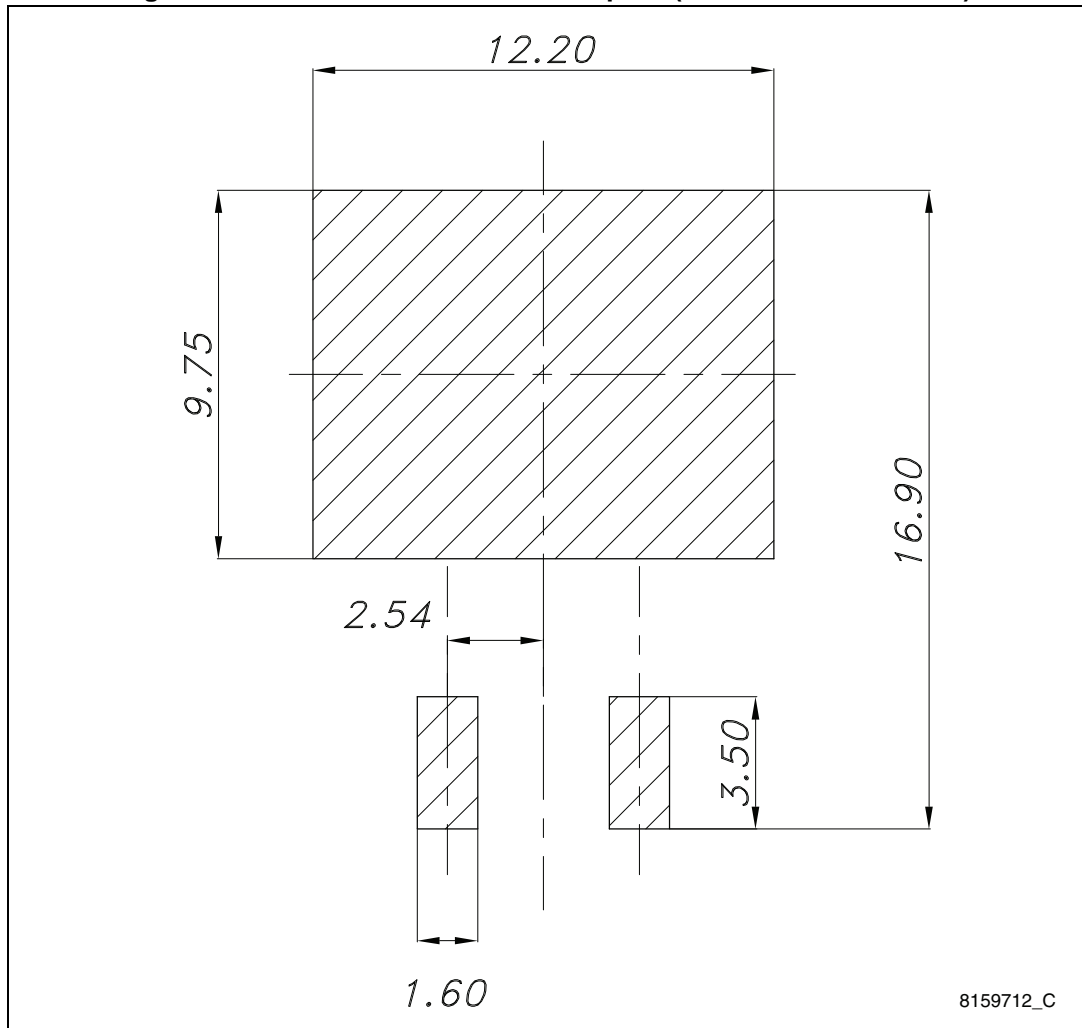


Table 8. H²PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20. H²PAK-2 recommended footprint (dimensions are in mm)



8159712_C

4.2 H²PAK-6, STH240N10F7-6

Figure 21. H²PAK-6 drawing

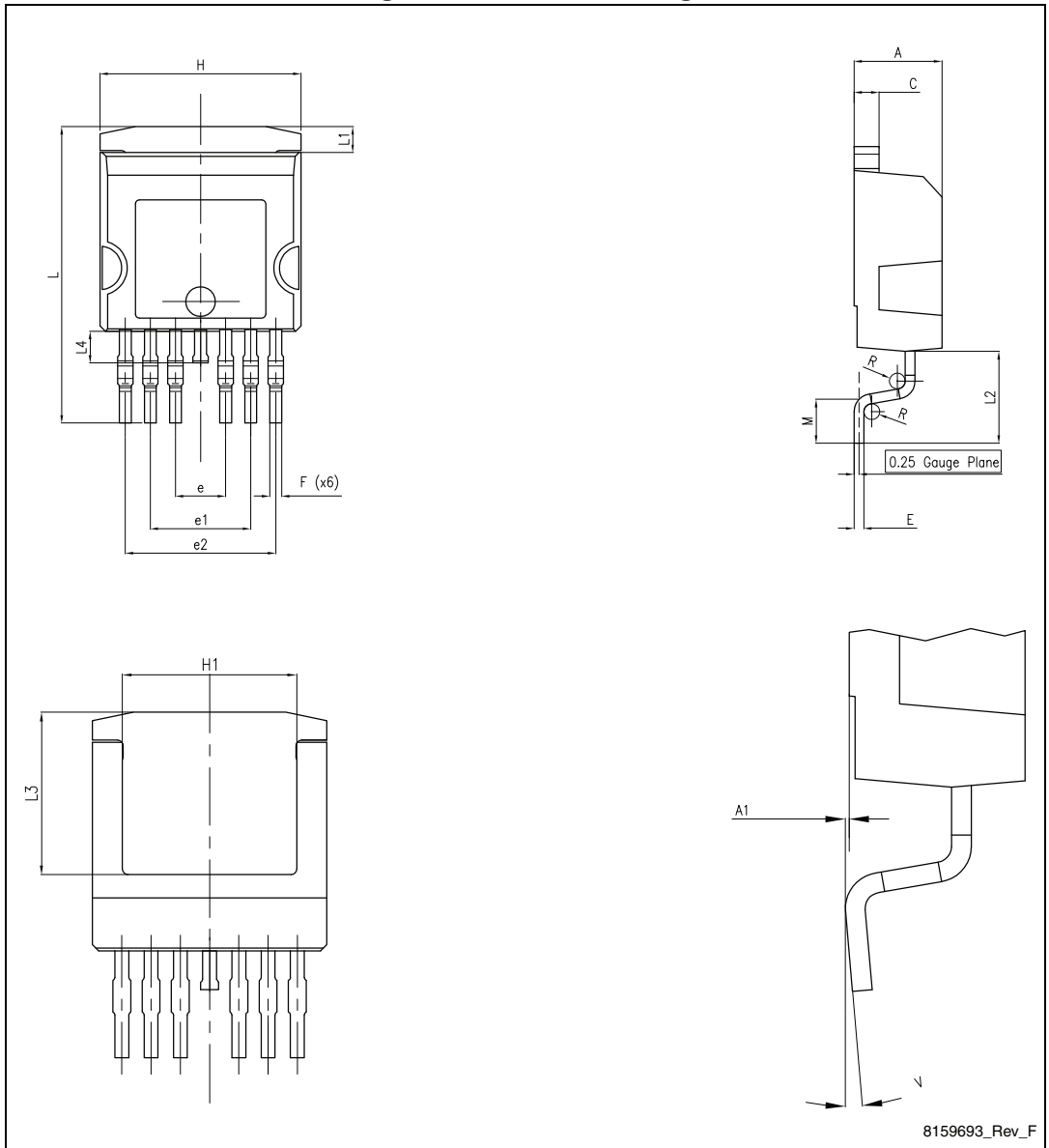
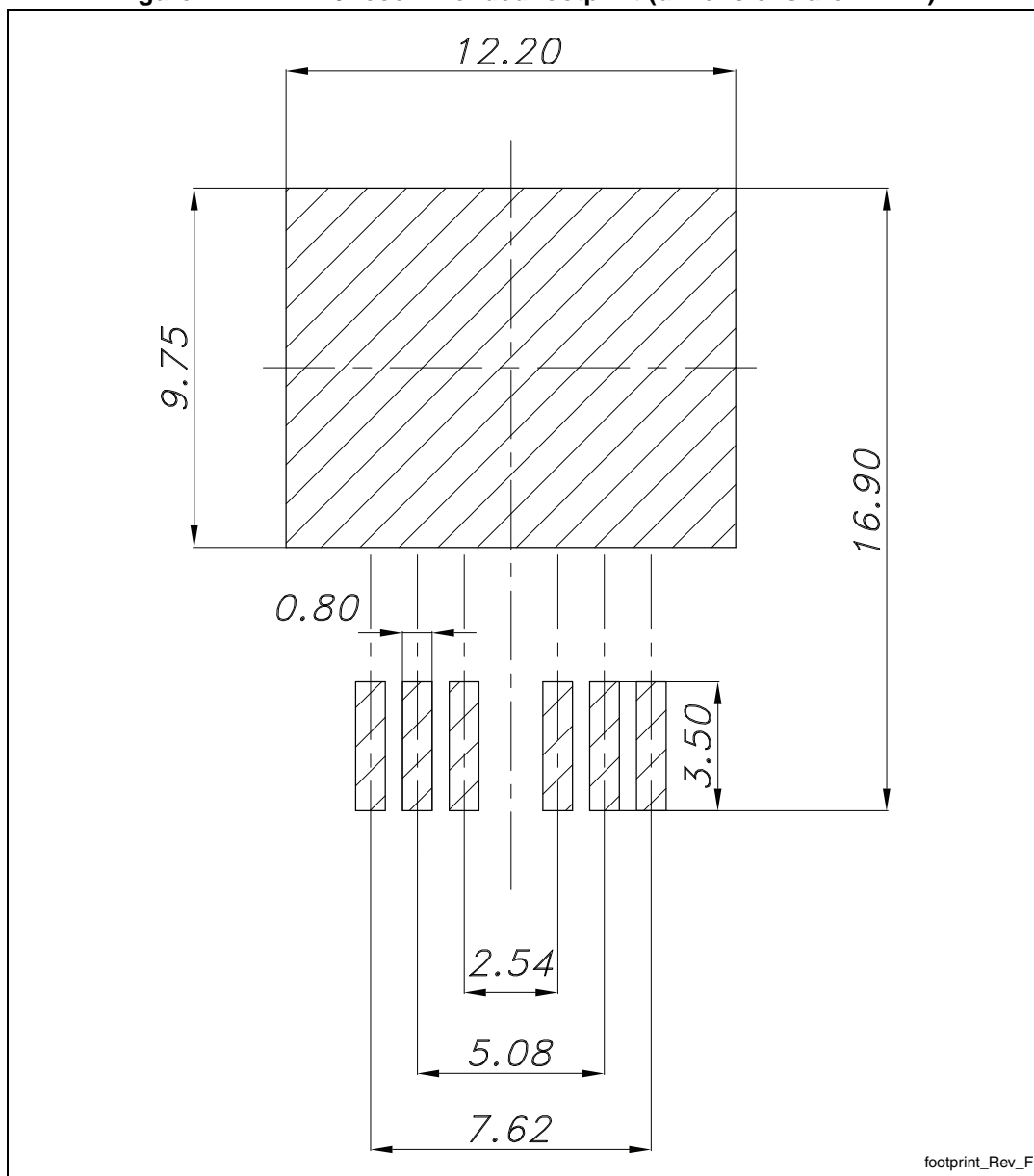


Table 9. H²PAK-6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 22. H²PAK-6 recommended footprint (dimensions are in mm)



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-May-2014	1	First release.
23-Jul-2014	2	<ul style="list-style-type: none">– Modified: title and description– Added: Section 2.1: Electrical characteristics (curves)– Minor text changes

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