

MC74VHCT50A

Noninverting Buffer / CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74VHCT50A is a hex noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

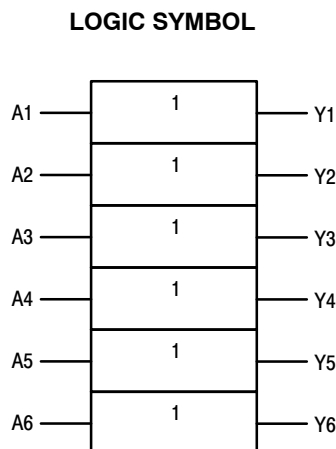
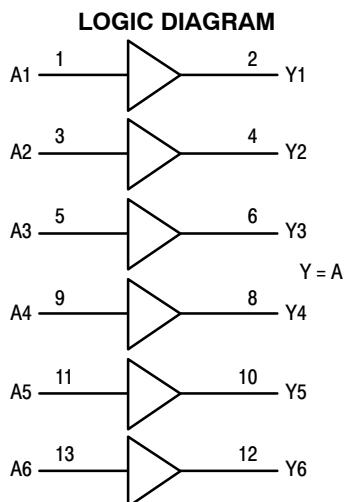
The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHCT50A input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHCT50A to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

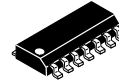
Features

- High Speed: $t_{PD} = 3.5$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

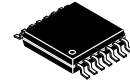


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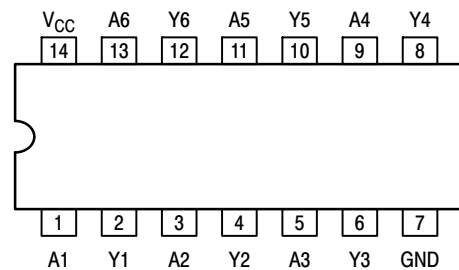


14-LEAD SOIC
D SUFFIX
CASE 751A



14-LEAD TSSOP
DT SUFFIX
CASE 948G

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 4 of this data sheet.

FUNCTION TABLE

| A Input | Y Output |
|---------|----------|
| L | L |
| H | H |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHCT50A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------------|---|----------------------------|----------------|
| V_{CC} | DC Supply Voltage | - 0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage | - 0.5 $\leq V_I \leq$ +7.0 | V |
| V_{OUT} | DC Output Voltage Output in HIGH or LOW State | - 0.5 $\leq V_O \leq$ +7.0 | V |
| I_{IK} | DC Input Diode Current | - 20 | mA |
| I_{OK} | DC Output Diode Current | \pm 20 | mA |
| I_O | DC Output Source/Sink Current | \pm 25 | mA |
| I_{CC} | DC Supply Current per Supply Pin | \pm 50 | mA |
| I_{GND} | DC Ground Current per Ground Pin | \pm 50 | mA |
| T_{STG} | Storage Temperature Range | - 65 to + 150 | $^{\circ}$ C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | $^{\circ}$ C |
| T_J | Junction Temperature under Bias | + 150 | $^{\circ}$ C |
| θ_{JA} | Thermal Resistance (Note 1) SOIC TSSOP | 125 170 | $^{\circ}$ C/W |
| P_D | Power Dissipation in Still Air SOIC TSSOP | 500 450 | mW |
| V_{ESD} | ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) | > 2000 > 200 2000 | V |
| $I_{Latch-Up}$ | Latch-Up Performance Above V_{CC} and Below GND at 85 $^{\circ}$ C (Note 5) | \pm 300 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Max | Unit |
|--|------------|------------|-----------------|--------------|
| DC Supply Voltage | V_{CC} | 2.0 | 5.5 | V |
| DC Input Voltage | V_{IN} | 0.0 | 5.5 | V |
| DC Output Voltage $V_{CC} = 0$ High or Low State | V_{OUT} | 0.0 0.0 | 5.5 V_{CC} | V |
| Operating Temperature Range | T_A | -55 | +125 | $^{\circ}$ C |
| Input Rise and Fall Time $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$ | t_r, t_f | 0 0 | 100 20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

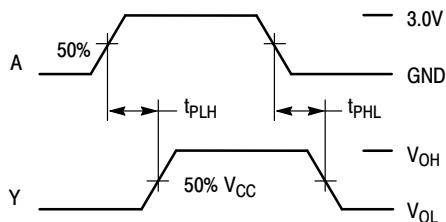
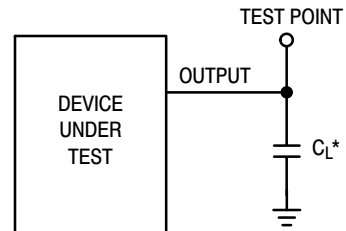


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

MC74VHCT50A

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | T _A ≤ 125°C | | Unit | |
|-------------------|---|--|------------------------|-----------------------|------------|--------------------|-----------------------|--------------------|------------------------|--------------------|--------------|----|
| | | | | Min | Typ | Max | Min | Max | Min | Max | | |
| V _{IH} | Minimum High-Level Input Voltage | | 3.0 4.5 5.5 | 1.2 2.0 2.0 | | | 1.2 2.0 2.0 | | 1.2 2.0 2.0 | | V | |
| V _{IL} | Maximum Low-Level Input Voltage | | 3.0 4.5 5.5 | | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | | V |
| V _{OH} | Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 3.0 4.5 | 2.9 4.4 | 3.0 4.5 | | 2.9 4.4 | | 2.9 4.4 | | V | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | 2.34 3.66 | | V | |
| V _{OL} | Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 3.0 4.5 | | 0.0 0.0 | 0.1 0.1 | | 0.1 0.1 | | 0.1 0.1 | | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OL} = 8 mA | 3.0 4.5 | | | | 0.36 0.36 | | 0.44 0.44 | | 0.52 0.52 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 2.0 | | 20 | | 40 | | μA |
| I _{CC} T | Quiescent Supply Current | Input: V _{IN} = 3.4 V | 5.5 | | | 1.35 | | 1.50 | | 1.65 | | mA |
| I _{OFF} | Output Leakage Current | V _{OUT} = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A ≤ 85°C | | T _A ≤ 125°C | | Unit |
|--|--|--|-----------------------|------------|-------------|-----------------------|-------------|------------------------|-------------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Y | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 5.5 8.0 | 7.9 11.4 | 1.0 1.0 | 9.5 13.0 | | | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 6.2 7.0 | 7.5 8.5 | | 8.5 9.5 | | 9.5 10.5 | |
| C _{IN} | Maximum Input Capacitance | | | 5 10 | | | 10 | | 10 | pF |

| | | | | |
|-----------------|--|---|--|----|
| C _{PD} | Power Dissipation Capacitance (Note 6) | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
| | | 15 | | |

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

| Symbol | Characteristic | T _A = 25°C | | Unit |
|------------------|--|-----------------------|------|------|
| | | Typ | Max | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 0.8 | 1.0 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | -0.8 | -1.0 | V |
| V _{IHD} | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| V _{ILD} | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

MC74VHCT50A

ORDERING INFORMATION

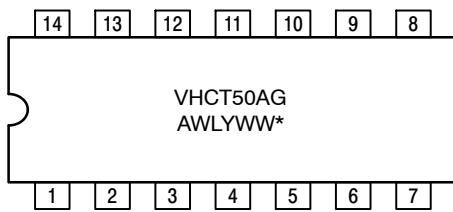
| Device | Package | Shipping† |
|------------------|-----------------------|--------------------|
| MC74VHCT50ADR2G | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |
| MC74VHCT50ADTR2G | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |
| NLVVHCT50ADTR2G* | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

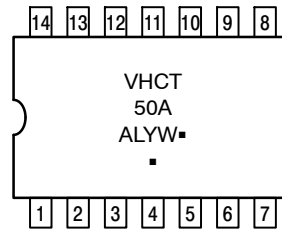
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS

(Top View)



14-LEAD SOIC
D SUFFIX
CASE 751A



14-LEAD TSSOP
DT SUFFIX
CASE 948G

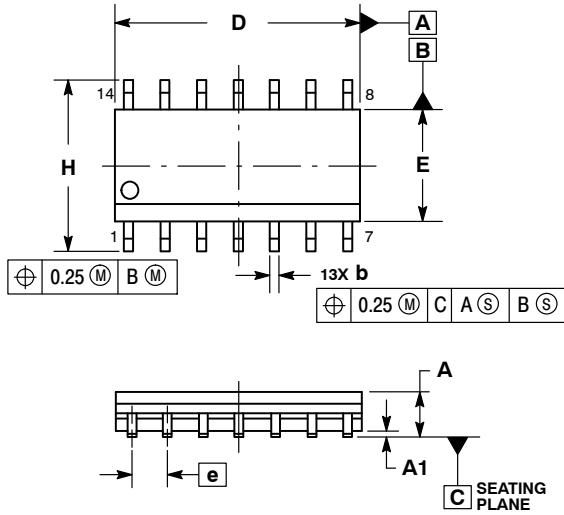
A = Assembly Location
 WL, L = Wafer Lot
 Y = Year
 WW, W = Work Week
 G or ▪ = Pb-Free Package

*See Applications Note #AND8004/D for date code and traceability information.

MC74VHCT50A

PACKAGE DIMENSIONS

SOIC-14 NB
D SUFFIX
CASE 751A-03
ISSUE K

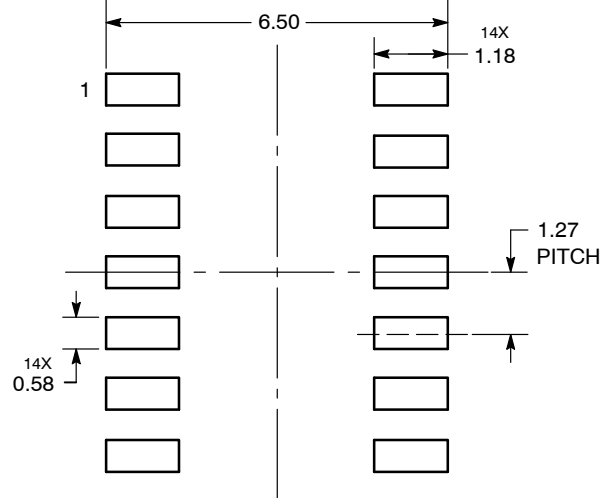


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



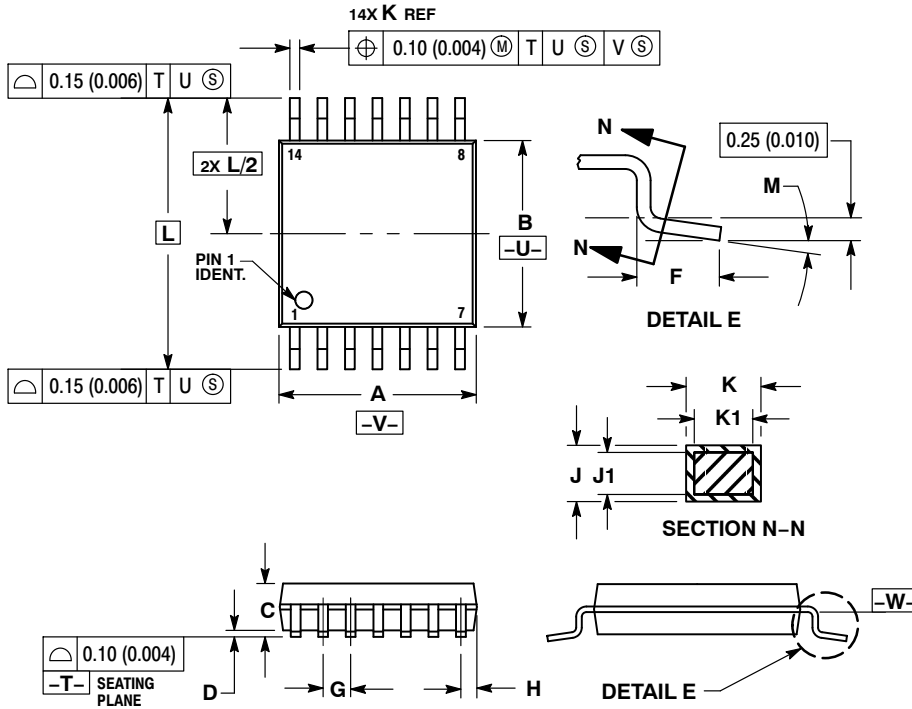
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHCT50A

PACKAGE DIMENSIONS

TSSOP-14
CASE 948G
ISSUE B

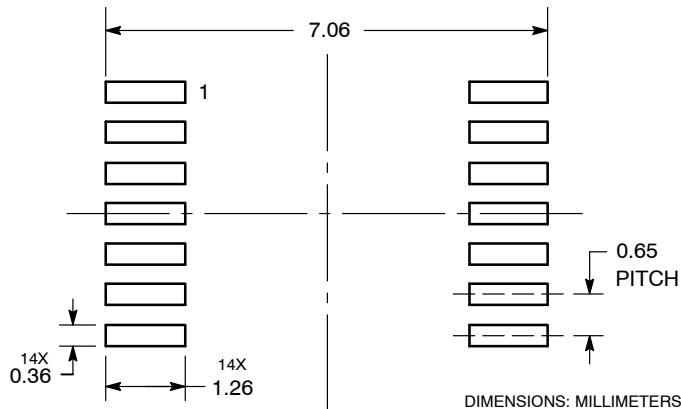


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT



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