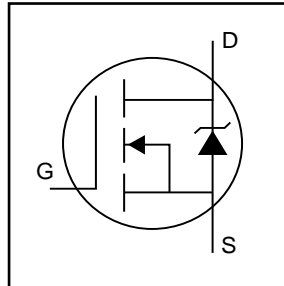


- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated

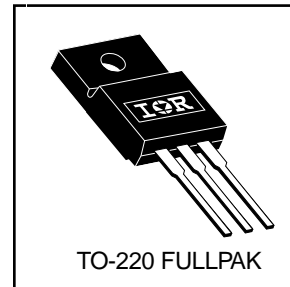


| |
|----------------------------|
| $V_{DSS} = 55V$ |
| $R_{DS(on)} = 0.016\Omega$ |
| $I_D = 36A$ |

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

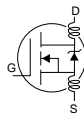
| | Parameter | Max. | Units |
|---------------------------|--|--------------------|-------|
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 36 | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 25 | |
| I_{DM} | Pulsed Drain Current ①⑥ | 210 | |
| $P_D @ T_C = 25^\circ C$ | Power Dissipation | 42 | W |
| | Linear Derating Factor | 0.28 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy ②⑥ | 270 | mJ |
| I_{AR} | Avalanche Current ①⑥ | 32 | A |
| E_{AR} | Repetitive Avalanche Energy ① | 4.2 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③⑥ | 5.6 | V/ns |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | | |
| | Mounting torque, 6-32 or M3 screw | 10 lbf•in (1.1N•m) | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|---------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 3.6 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 65 | |

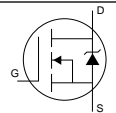
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|-------|-------|---------------------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 55 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.052 | — | V/ $^\circ\text{C}$ | Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.016 | Ω | $V_{GS} = 10V, I_D = 22A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Transconductance | 22 | — | — | S | $V_{DS} = 25V, I_D = 32A$ ⑥ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 55V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -20V$ |
| Q_g | Total Gate Charge | — | — | 89 | nC | $I_D = 32A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 20 | | $V_{DS} = 44V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 39 | | $V_{GS} = 10V$, See Fig. 6 and 13 ④⑥ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 11 | — | ns | $V_{DD} = 28V$ |
| t_r | Rise Time | — | 78 | — | | $I_D = 32A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 32 | — | | $R_G = 5.1\Omega$ |
| t_f | Fall Time | — | 48 | — | | $R_D = 0.85\Omega$, See Fig. 10 ④⑥ |
| L_D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L_S | Internal Source Inductance | — | 7.5 | — | | |
| C_{iss} | Input Capacitance | — | 1900 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 620 | — | | $V_{DS} = 25V$ |
| C_{rss} | Reverse Transfer Capacitance | — | 270 | — | | $f = 1.0\text{MHz}$, See Fig. 5 ⑥ |
| C | Drain to Sink Capacitance | — | 12 | — | | $f = 1.0\text{MHz}$ |



Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|------|------|------|-------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 36 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ①⑥ | — | — | 210 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 22A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 94 | 140 | ns | $T_J = 25^\circ\text{C}, I_F = 32A$ |
| Q_{rr} | Reverse Recovery Charge | — | 360 | 540 | nC | $di/dt = 100A/\mu s$ ④⑥ |



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 530\mu H$
 $R_G = 25\Omega, I_{AS} = 32A$. (See Figure 12)
- ③ $I_{SD} \leq 32A$, $di/dt \leq 250A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $t = 60s, f = 60\text{Hz}$
- ⑥ Uses IRFZ48N data and test conditions

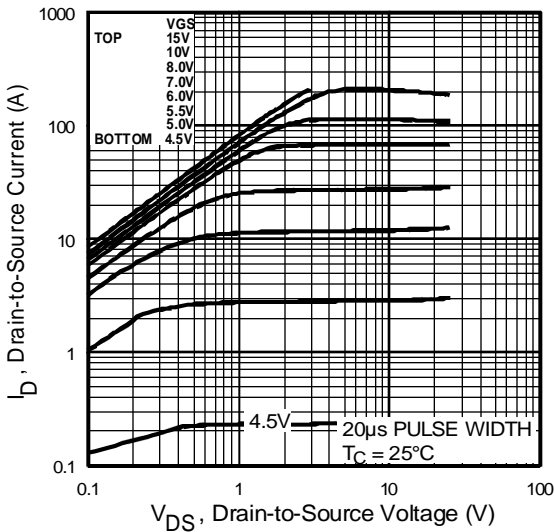


Fig 1. Typical Output Characteristics,
 $T_J = 25^\circ\text{C}$

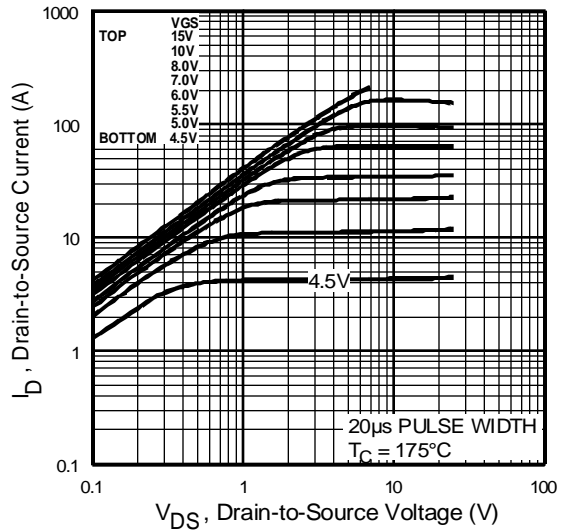


Fig 2. Typical Output Characteristics,
 $T_J = 175^\circ\text{C}$

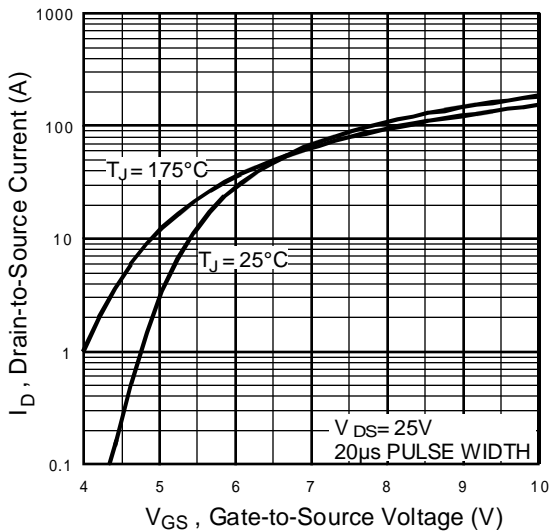


Fig 3. Typical Transfer Characteristics

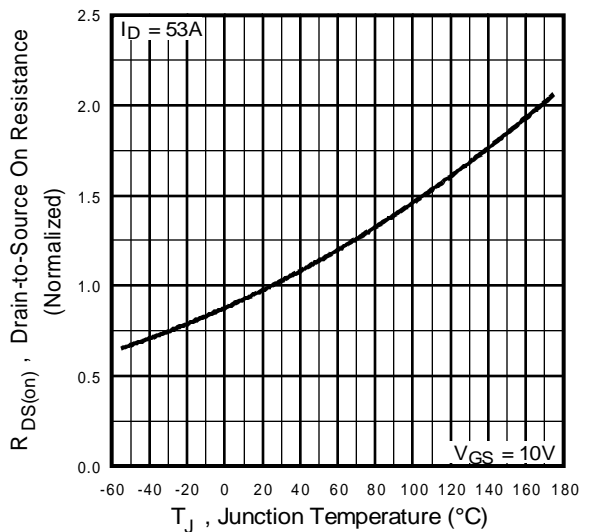


Fig 4. Normalized On-Resistance
Vs. Temperature

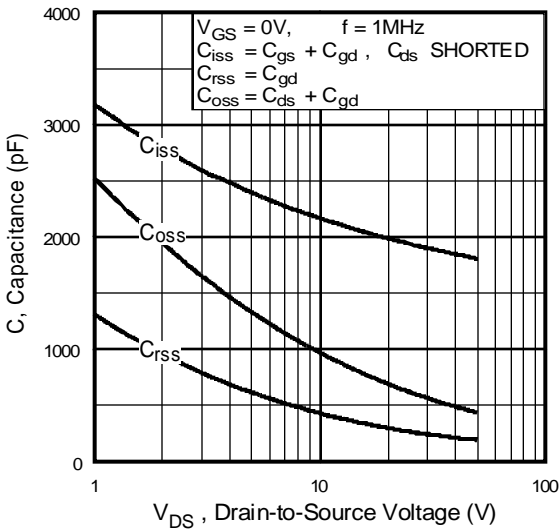


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

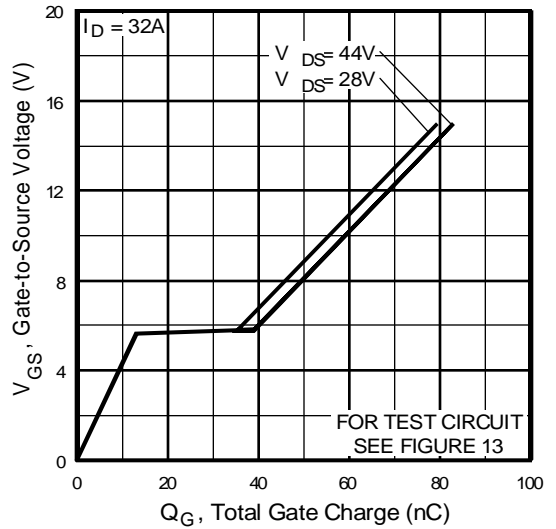


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

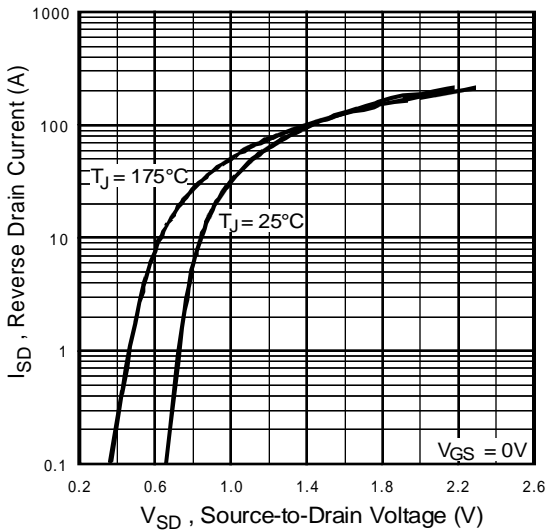


Fig 7. Typical Source-Drain Diode Forward Voltage

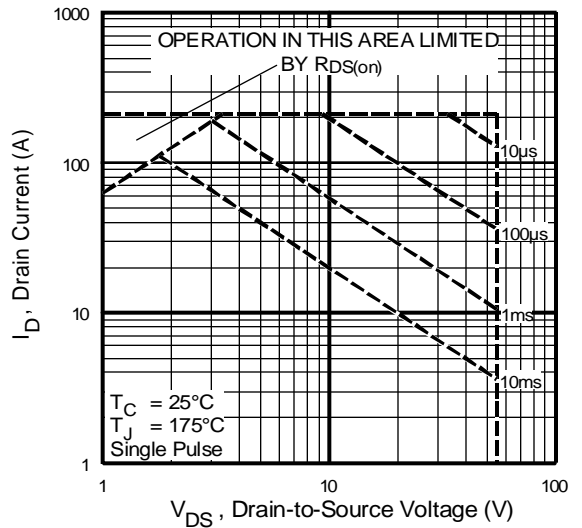


Fig 8. Maximum Safe Operating Area

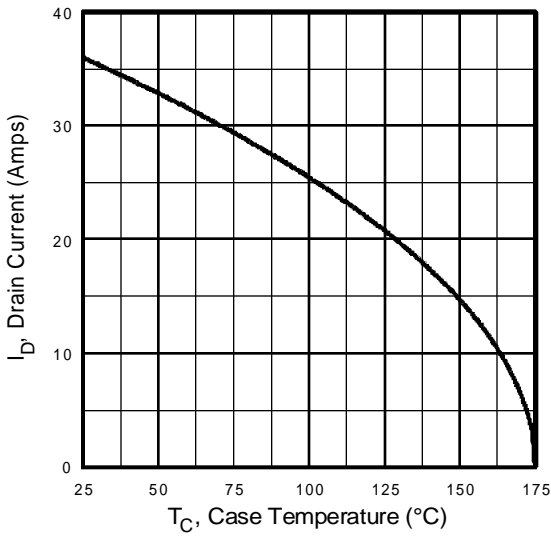


Fig 9. Maximum Drain Current Vs. Case Temperature

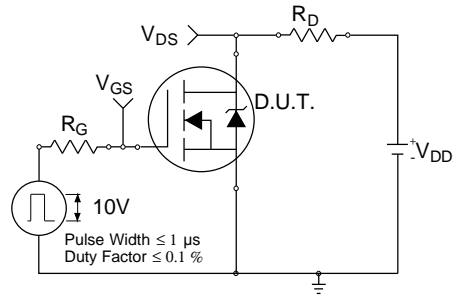


Fig 10a. Switching Time Test Circuit

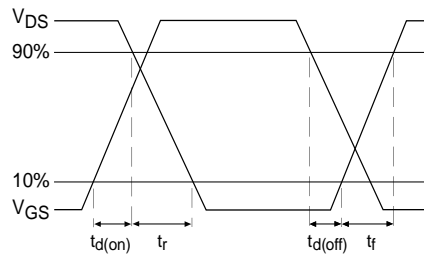


Fig 10b. Switching Time Waveforms

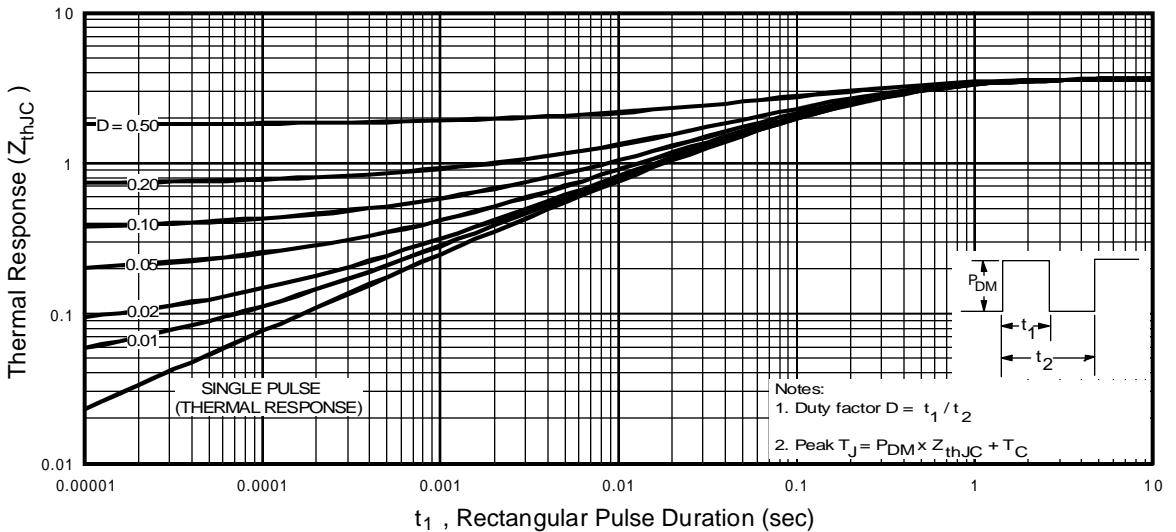


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

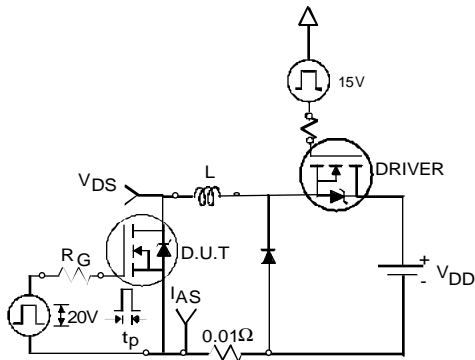


Fig 12a. Unclamped Inductive Test Circuit

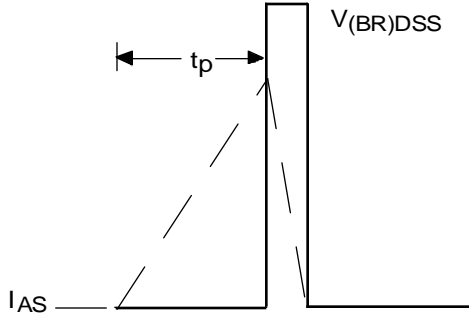


Fig 12b. Unclamped Inductive Waveforms

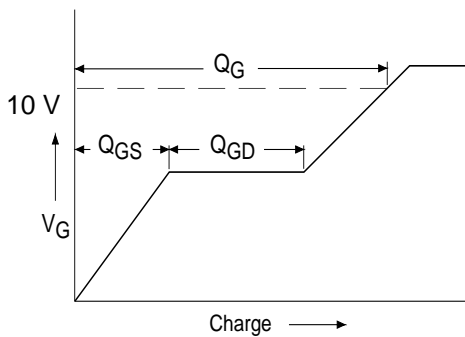


Fig 13a. Basic Gate Charge Waveform

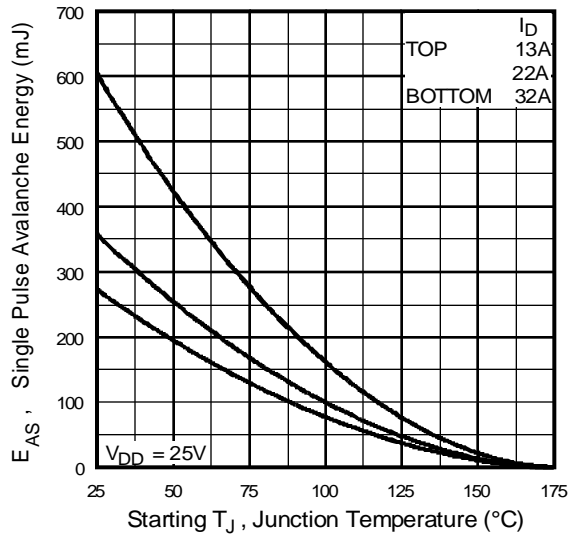


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

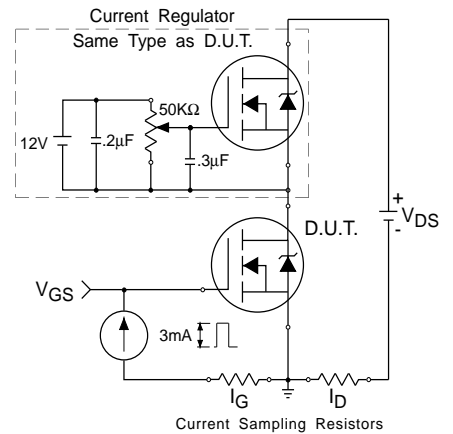
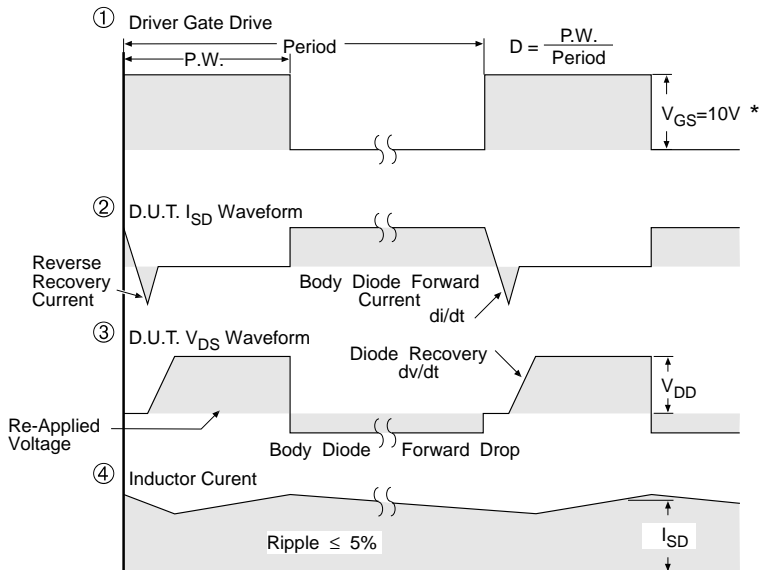
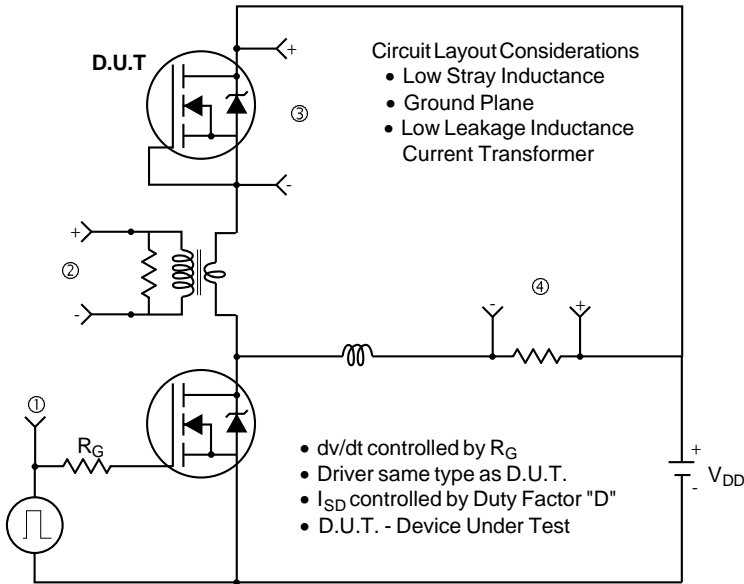


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

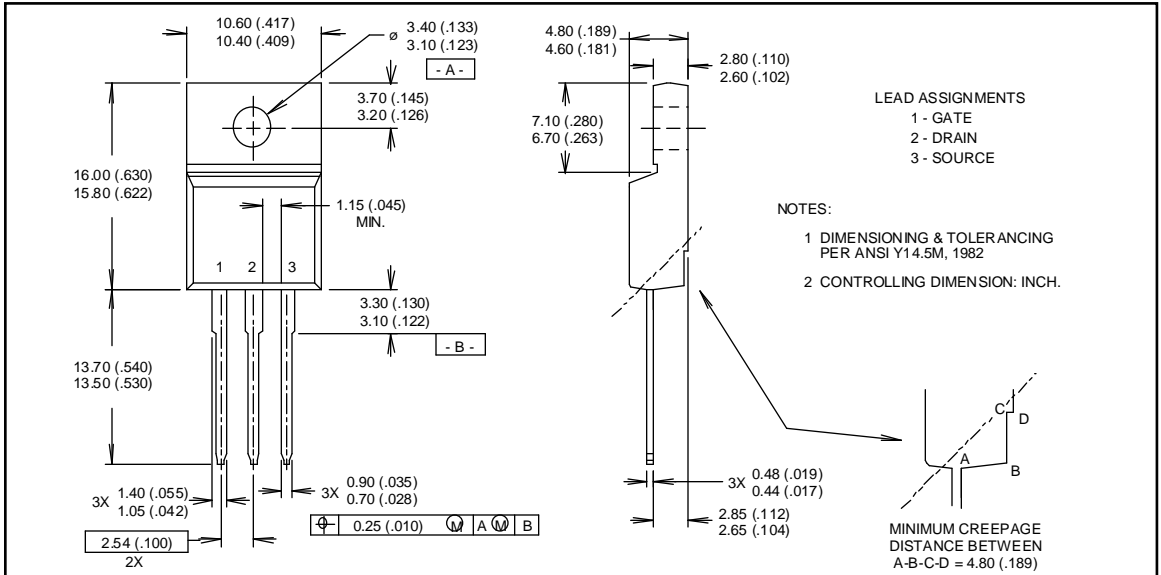
Fig 14. For N-Channel HEXFETS

IRFIZ48N



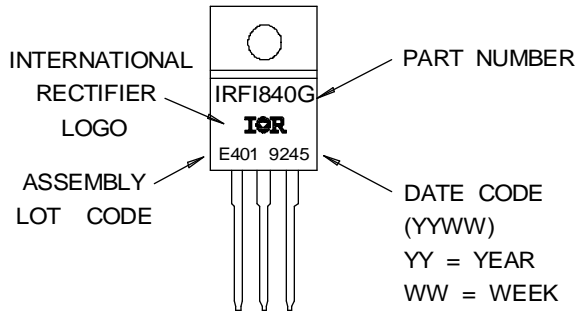
Package Outline — TO-220 Fullpak

Dimensions are shown in millimeters (inches)



Part Marking

EXAMPLE : THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE E401



WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 3-30-4 Nishi-Ikeburo 3-Chome, Toshima-Ki, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

<http://www.irf.com/>

Data and specifications subject to change without notice.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>