

## Evaluation Board for **AD7779** 24-Bit, 8-Channel, Simultaneous Sampling, Sigma-Delta ADC with Power Scaling

### FEATURES

Full featured evaluation board for the **AD7779**  
PC control in conjunction with the Analog Devices, Inc.,  
system demonstration platform (SDP), **EVAL-SDP-CH1Z**  
PC software control and data analysis  
Time and frequency domain  
Standalone hardware capability

### ONLINE RESOURCES

Evaluation Kit Contents  
**EVAL-AD7779FMCZ** evaluation board  
**AD7779** evaluation software  
Documents Needed  
**AD7779** data sheet  
**EVAL-AD7779FMCZ** user guide  
Required Software  
**AD7779** evaluation software

### EQUIPMENT NEEDED

**EVAL-AD7779FMCZ** evaluation board  
System demonstration platform—high speed (SDP-H1)  
controller board (**EVAL-SDP-CH1Z**)  
DC/AC signal source (Audio Precision or similar)  
USB cable  
PC running Windows 7 with USB 2.0 port  
External +9 V supply (for standalone use)

### GENERAL DESCRIPTION

The **EVAL-AD7779FMCZ** evaluation kit features the **AD7779** 24-bit, analog-to-digital converter (ADC). The board interfaces with the System Demonstration Platform SDP-H1 controller board (**EVAL-SDP-CH1Z**). This controller board supplies power to the **EVAL-AD7779FMCZ** evaluation board and also connects to a PC using a Windows® operating system via a USB cable. The **AD7779** evaluation software fully configures the **AD7779** device register functionality and provides dc and ac time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

The **EVAL-AD7779FMCZ** is an evaluation board that allows the user to evaluate the features of the ADC. The user PC software executable controls the **AD7779** over the USB cable through the SDP-H1 controller board.

Full specifications on the **AD7779** are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.

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**REVISION HISTORY**

2/16—Revision 0: Initial Version

## EVALUATION BOARD PHOTOGRAPH

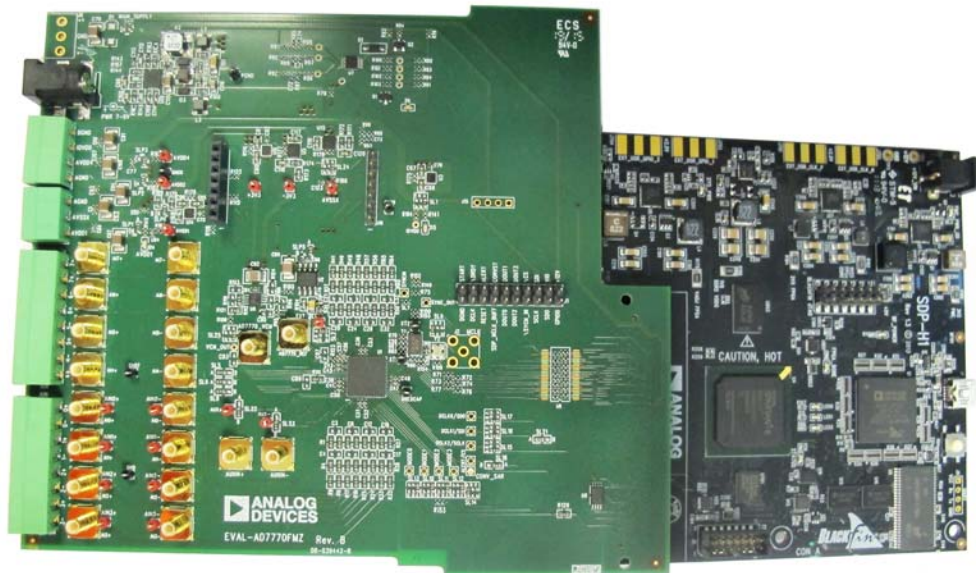


Figure 1. EVAL-AD7779FMCZ Evaluation Board with SDP-H1 Controller Board

13560-001

## EVAL-AD7779FMCZ QUICK START GUIDE

To begin using the evaluation board, take the following steps:

1. Ensure the evaluation board is disconnected from the USB port of the PC. Install the [AD7779](#) evaluation software from the CD included in the evaluation board kit. Restart the PC after the software installation is complete. (For complete software installation instructions, see the Software Installation section.)
2. Connect the SDP-H1 board to the evaluation board: CON J4 of the SDP-H1 board adapts to the receiving socket on the [EVAL-AD7779FMCZ](#) printed circuit board (PCB).

3. Ensure that the boards are connected firmly together.
4. By default, the power for the evaluation board is supplied from the SDP-H1 controller board. A number of power options available; see Table 3 for more information.
5. Connect the SDP-H1 board to the PC using the supplied USB cable.
6. Launch the [AD7779](#) evaluation software from the **Analog Devices** subfolder in the **Programs** menu.

Note that pin control mode is not directly supported in the Rev. H version of the software.

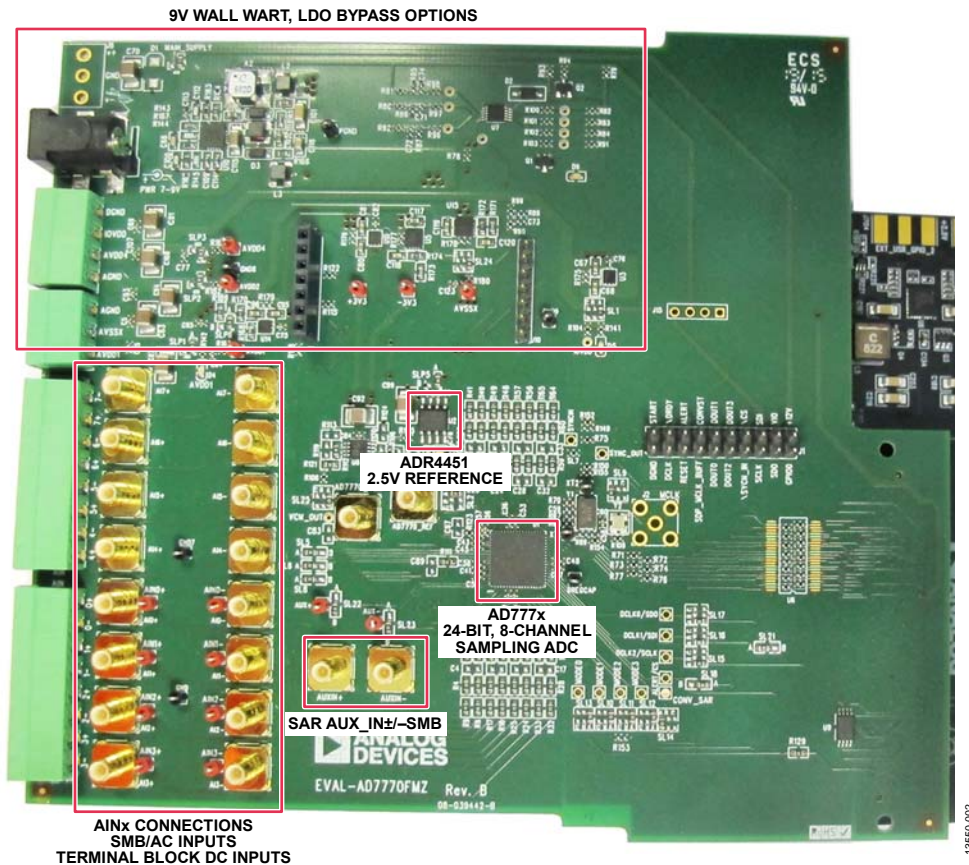


Figure 2. Hardware Configuration—Setting Up the [EVAL-AD7779FMCZ](#)

## ANALOG INPUTS AND FRONT-END CIRCUIT

As shown in Figure 2, the  $AIN0_{\pm}$  to  $AIN7_{\pm}$  analog  $\Sigma$ - $\Delta$  inputs are available on SMB or terminal block inputs. The  $AUXIN_{\pm}$  inputs to the auxiliary SAR converter are available through the SMB inputs.

Figure 2 shows these connectors to the ADC input terminals. Each analog input differential pair has a second-order RC filter option and common-mode option to center the input signal at  $AVDD1A/2$ . An option is available to place an additional VCM buffer in U8 to add drive strength and also gain, attenuation, or filtering to this VCM signal. Channel 7 has the option to evaluate an external drive amplifier on J7/J10 using the analog device amplifier surfboard. The SL3, SL4, SL19, and SL20 solder link options select between applying the  $AIN_{\pm 7}$  analog inputs directly to the RC filter and ADC, or to the surfboard inputs. The evaluation board includes a buffer ([AD8659](#)) connected to  $AIN_{\pm 0}$  and  $AIN_{\pm 2}$ , and a multiplexer that can be connected to

the  $AIN0_{\pm}$  to  $AIN7_{\pm}$   $\Sigma$ - $\Delta$  inputs when the SAR is used for redundancy. If this function is required, solder a  $0\ \Omega$ , 0402 size resistor to the unpopulated resistor footprints (see Figure 16 for more details), and move SL22 and SL23 to Position A.

The default configuration of the board is as follows:

- Connect the input signal from the input terminals through the second-order RC filter (do not populate) to the ADC channels.
- The board accepts ac signals from  $-1.25\text{ V}$  to  $+1.25\text{ V}$ .
- The [ADR441](#) 2.5 V, low noise reference is used by default, allowing an absolute input range of  $0\text{ V}$  to  $2.5\text{ V}$  on each input.
- No external buffers are populated.

## EVALUATION BOARD HARDWARE

### DEVICE DESCRIPTION

The [AD7779](#) is an 8-channel, simultaneously sampled, 24-bit,  $\Sigma$ - $\Delta$  ADC with an additional diagnostics 12-bit SAR. The [AD7779](#) offers an ADC per channel with synchronized sampling.

To cater to application specific ADC power scaling requirements, the user can select either the high resolution mode or low power mode. In high resolution mode, the ADC operates at 16 kSPS maximum, with 111 dB signal-to-noise ratio (SNR), and consumes 16 mW per channel. In low power mode, the ADC operates at 4 kSPS maximum, with 111 dB of SNR, and consumes 5.5 mW per channel.

The [AD7779](#) also provide a low latency, sinc3 filter for digital filtering. The notches of the digital filter are automatically set to remove harmonics at the sampling frequency and the PGA chopping frequency.

The sample rate converter allows the user to fine tune the decimation rate to maintain a number of samples per line cycle for varying input frequencies. Choosing a low output data rate increases the dynamic range, reducing the noise. Decimation rates can be programmed via the [AD7779](#) evaluation software.

Embedded analog functionality on each ADC channel eases system design. The [AD7779](#) has a fully buffered PGA on each channel to reduce analog input current. The [AD7779](#) also has a reference buffer on each channel, which provides a high impedance input reference to the external precision reference.

Complete specifications for the [AD7779](#) are provided in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board. Full details about the [EVAL-SDP-CH1Z](#) are available on the Analog Devices, Inc., website at [www.analog.com/SDP-H1](http://www.analog.com/SDP-H1).

### HARDWARE LINK OPTIONS

The default power link options are listed in Table 1, Table 2, and Table 3. The evaluation board can be powered by different sources, as described in Table 1. By default, the supply required for the evaluation board comes from the SDP-H1 controller board. The supply is regulated by the on-board [ADP5070](#) SMPS, which generates the dual supply, and the [ADP7118](#) and the [ADP7182](#) low dropout (LDO) regulators reduce noise and generate the low noise, regulated, positive and negative rails.

**Table 1. Default Link and Solder Link Options for Power Supply**

Link No.	Default Option	Description
MAIN_SUPPLY	A	Unregulated input voltage source selection. Position A: the unregulated supply to the on-board LDOs is taken from the SDP-H1 12 V supply. Position B: the unregulated external supply to the on-board LDOs is taken from the J5 9V wall wart input or from the J6 connector.
SL1	A	IOVDD supply selection. Position A: IOVDD is supplied from the SDP-H1 board. Set to 3.3 V by default. Position B: IOVDD is supplied from <a href="#">ADP7118</a> 3.3 V, precision LDO. Position C: EXT_IOVDD. IOVDD can be supplied from the J17-3 terminal block (1.8 V to 3.3 V). The SDP-H1 only supports 3.3 V logic. If IOVDD is operated below 3.3 V, populate the U6 buffer to avoid electrical problems.
SLP1	A	AVDD1 supply selection. Position A: AVDD1 is taken from U14, the <a href="#">ADP7118</a> LDO. See SLP6 for more options. Position B: AVDD1 is taken from the J3-1, AVDD1 external supply.
SLP2	A	AVDD2 supply selection. Position A: AVDD2 is taken from U14, the <a href="#">ADP7118</a> LDO. See SLP6 for more options. Position B: AVDD2 is taken from the J17-1 external source.
SLP3	A	AVDD4 supply selection. Position A: AVDD4 is taken from U14, the <a href="#">ADP7118</a> LDO. See SLP6 for more options. Position B: AVDD4 is taken from the J17-2 external source.
SLP6	A	On-board regulated positive rail selection. Position A: 1.65 V. Use this option for dual-supply operation. Position B: 3.3 V. Use this option for single-supply operation.
SL24	A	Regulated negative rail selection. Position A: AVSSx is taken from U15, the <a href="#">ADP7182</a> 1.65 V LDO. Use this option for dual-supply operation. Position B: AGND. Use this option for single-supply operation. Position C: AVSSx is supplied by J3-2, the AVSSx external supply.

**Table 2. AFE Options**

Link No.	Default Option	Description
SL22	B	SAR AUX+ input selection. Position A: AUXIN+ is connected to the on-board multiplexer, which is controlled by the <a href="#">AD7779</a> GPIO pins. If the multiplexer needs to be used, solder the unpopulated resistor that connects the multiplexer inputs to the $\Sigma$ - $\Delta$ ADC inputs. The evaluation board includes an op amp connected to Channel 0 and Channel 2 of the $\Sigma$ - $\Delta$ ADC. Position B: direct connection from source to AUXIN+ SMB connector.
SL23	B	SAR AUX- input selection. Position A: AUXIN- is connected to the on-board multiplexer which is controlled by the <a href="#">AD7779</a> GPIO pins. If the multiplexer needs to be used, solder the unpopulated resistor that connects the multiplexer inputs to the $\Sigma$ - $\Delta$ ADC inputs. The evaluation board includes an op amp connected to Channel 0 and Channel 2 of the $\Sigma$ - $\Delta$ ADC. Position B: direct connection from source to AUXIN- SMB connector.
SL3, SL19	A	AIN7+ input driver selection. Position A: direct connection from source to AIN7+. Position B: surfboard connection J7/J10 drives the analog inputs.
SL4, SL20	A	AIN7- input driver selection. Position A: direct connection from source to AIN7-. Position B: surfboard connection J7/J10 drives the analog inputs.
SLP5	A	ADR441 external voltage reference supply selection. Position A: the reference is powered by the <a href="#">ADP5070</a> . Use this option if the board is powered by the on-board regulators. Position B: the reference is powered by the AVDD1 supply. Use this option if the board is powered by J3 and J17.
SL2	A	Voltage reference selection. Position A: the <a href="#">ADR441</a> is used as a voltage reference. Position B: the <a href="#">AD7779</a> internal reference is used. Position C: the <a href="#">ADR441</a> is buffered and used as a reference. Open: an external voltage reference can be connected to the AD7779_REF SMB connector.
SL25	A	Common-mode voltage output ( $V_{CM}$ ) selection. Position A: $V_{CM}$ signal to analog front-end signal is AGND. Use this option for dual-supply operation. Position B: the VCM pin is buffered through the U8 output. Position C: the $V_{CM}$ signal to the analog front end is taken directly from the <a href="#">AD7779</a> VCM pin. Open: an external $V_{CM}$ signal can be connected to the AD7779_VCM SMB connector.

**Table 3. Digital Connections**

Link No.	Default Option	Description
K0 to K15	Inserted	Digital input/output solder links. These links are inserted by default for unbuffered digital input/output connection between the controller board and the evaluation board. Remove and insert U6 for buffered digital inputs/outputs.
SL5, SL6	A	Data interface format pins. The evaluation software only supports SPI control mode. The default condition is SPI configuration. See the <a href="#">AD7779</a> data sheet for more information.
SL7	Inserted	SL7 provides a path between SYNC_OUT and SYNC_IN. The user can provide an asynchronous start signal to the device. On the next MCLK falling edge, the <a href="#">AD7779</a> outputs a SYNC_OUT signal, which is synchronous to the MCLK. This signal synchronizes multiple <a href="#">AD7779</a> devices or resets the SD modulators when phase compensation is used.
SL8	A	Clock select option. Position A: the CLK_SEL pin is pulled low and selects the CMOS clock option. Position B: the CLK_SEL pin is pulled high and selects the crystal oscillator placed in Y1. To select this crystal oscillator, remove the SL9 connections and insert R69 and R70.
SL9	A	CMOS clock input selection: Position A: the on-board CMOS clock is selected (Y2). Position B: J2 can be used to provide an external CMOS clock through the SMB input terminal. Position C: MCLK is supplied from the J1 connector.

Link No.	Default Option	Description
SL10, SL11, SL13	A	<p>GPIO/mode pins.</p> <p>In SPI control mode, Pin 13 to Pin 16 act as GPIOs. See the <a href="#">AD7779</a> data sheet for more information about additional functionality of these pins for hardware sample rate update source.</p> <p>Position A: Pin 13 to Pin 16 are connected to the GPIOx net that controls the on-board multiplexer, or can be used to update the SRC (R153 needs to be populated with a 0 <math>\Omega</math> resistor).</p> <p>In pin control mode, Pin 13 to Pin 16 (along with SL12) are used to set up the configuration of the device. For more information on GPIO configuration or pin mode, see the <a href="#">AD7779</a> data sheet.</p> <p>Position B: Pin 13 to Pin 16 are connected to IOVDD.</p> <p>Position C: Pin 13 to Pin 16 are connected to DGND.</p>
SL12	A	<p>Alert/mode.</p> <p>In SPI control mode, this pin operates as an alert flag.</p> <p>Position A: error flag. This pin is connected to the J1 and J4 connectors. See SL21 for more details.</p> <p>In pin control mode, this pin becomes the Mode 3 input pin. Used in conjunction with the GPIO/mode pins to set up the device configuration. See the <a href="#">AD7779</a> datasheet for more details.</p> <p>Position B: the pin is connected to IOVDD.</p> <p>Position C: the pin is connected to DGND.</p>
SL14	A	<p>CONVST_SAR selection.</p> <p>In SPI control mode, this link selects the conversion signal source.</p> <p>Position A: the SAR ADC is controlled through the J1 connector.</p> <p>In pin control mode, CONVST_SAR (Pin 17), along with SL5 and SL6, set up the serial interface used to read back the conversions from the <math>\Sigma</math>-<math>\Delta</math> ADC.</p> <p>Position A: CONVST_SAR (Pin 17) is connected to IOVDD.</p> <p>Position B: CONVST_SAR (Pin 17) is connected to DGND.</p>
SL15, SL16, SL17	A	<p>SPI data interface lines.</p> <p>In SPI mode configuration, SCLK, SDI, and SDO are used as digital interface pins.</p> <p>Position A: the SPI data interface lines are connected to the FMC-LPC connector.</p> <p>In pin control mode, these pins define the DCLK frequency used to read back the <math>\Sigma</math>-<math>\Delta</math> data through the DOUT interface. See the <a href="#">AD7779</a> data sheet for more details.</p> <p>Position B: IOVDD.</p> <p>Position C: DGND.</p>
SL18	A	<p>SPI data interface line.</p> <p>In SPI mode configuration, <math>\overline{CS}</math> (Pin 18) is used as a digital interface pin.</p> <p>Position A: <math>\overline{CS}</math> (Pin 18) is connected to the FMC-LPC connector.</p> <p>In pin control mode, <math>\overline{CS}</math> (Pin 18) acts as an alert pin.</p> <p>Position B: error flag, <math>\overline{CS}</math> (Pin 18) is connected to the J1 and J4 connectors. See SL21 for more details.</p>
SL21	A	<p>Alert connection.</p> <p>Position A: SPI control mode.</p> <p>Position B: pin control mode.</p>



**On-Board Connectors**

Table 4 provides information about the external connectors on the [EVAL-AD7779FMCZ](#).

**Table 4. On-Board Connectors**

Connector	Function
J1	General connector for debugging purpose or to connect an external controller
J2	MCLK connector, supplies the external square wave clock
J3	External power supply connector
J4	FMC connector
J5	External power supply connector
J6	External 9 V wall wart connection
J7	Channel 7 surfboard evaluation header
J8, J9	8-pin connector for input to Channel 0 through Channel 3
J10	Channel 7 surfboard evaluation header
J13, J14	8-pin connector for input to Channel 4 through Channel 7
J15	External power supply, supplies all rails independent of LDO supplies

**SERIAL CONFIGURATION INTERFACE**

The [AD7779](#) can be configured by the FPGA via a 4-wire SPI interface. Format 0 and Format 1 must be shorted to Position A for this mode to be active.

To operate the [EVAL-AD7779FMCZ](#) evaluation board in standalone mode,

1. Connect a power supply (see Table 1 for options).
2. Connect the DSP, microcontroller, or FPGA to the J1 interface connector.

# EVALUATION BOARD SOFTWARE

## SOFTWARE INSTALLATION

The [EVAL-AD7779FMCZ](#) evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the installer. The default installation location for the software is **C:\Program Files\Analog Devices\EVAL-AD7779FMCZ**.

Install the evaluation software before connecting the evaluation board and SDP-H1 board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

There are two sections to the installation:

- [AD7779](#) evaluation software installation
- SDP-H1 board drivers installation

Place the software and drivers in the appropriate locations by proceeding through all of the installation steps. Connect the SDP-H1 board to the PC only after the software and drivers are installed. The installer may prompt for permission to make changes to the computer. Click **Yes** to proceed (see Figure 4).

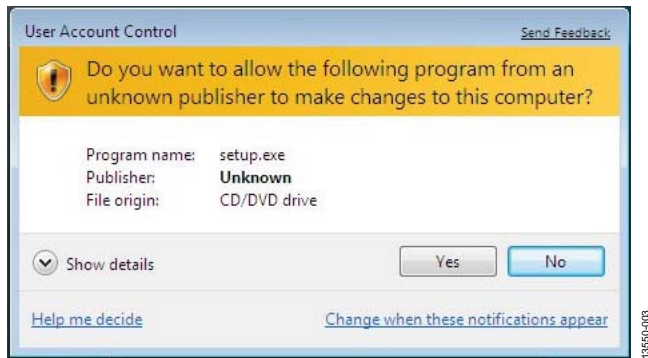


Figure 3. User Account Control Permission Dialog Box

A security warning may appear as part of the SDP-H1 controller board driver installation. Click **Install** to proceed with the installation of the driver (see Figure 5). Without this confirmation, the software cannot operate correctly.

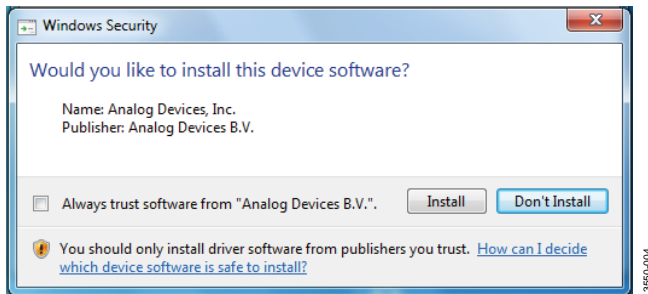


Figure 4. EVAL-SDP-CB1Z Drivers Installation Confirmation Dialog Box

After installation is complete, connect the evaluation board to the SDP-H1 controller board. Connect the SDP-H1 controller board via the USB cable to the computer. Follow these steps to verify that the SDP-H1 controller board driver are installed and working correctly:

1. Allow the **Found New Hardware Wizard** to run.
2. After the drivers are installed, check that the board has connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be found by right clicking **My Computer**, selecting **Manage**, then **Device Manager** from the list of **System Tools** (see Figure 6).
3. The SDP-H1 board appears under **ADI Development Tools** as **Analog Devices SDP-H1** or similar. The installation is complete.



Figure 5. Device Manager

## LAUNCHING THE SOFTWARE

The [AD7779](#) evaluation software can be launched when the evaluation board and the SDP-H1 controller board are correctly connected to the PC.

To launch the software, take the following steps:

1. From the **Start** menu, click **Programs, Analog Devices**, then **EVAL-AD7779FMCZ**. The main window of the software then displays (see Figure 8).
2. If the [AD7779](#) evaluation system is not connected to the USB port via the SDP-H1 board when the software is launched, the **Select Interface...** dialog box appears. Connect the evaluation board to the USB port of the PC, wait a few seconds, and then click the green arrows to rescan the USB ports. When the connection is established, click **Work Online** to proceed.

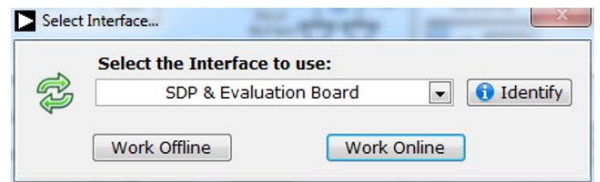


Figure 6. Select Interface Dialog Box

## SOFTWARE OPERATION

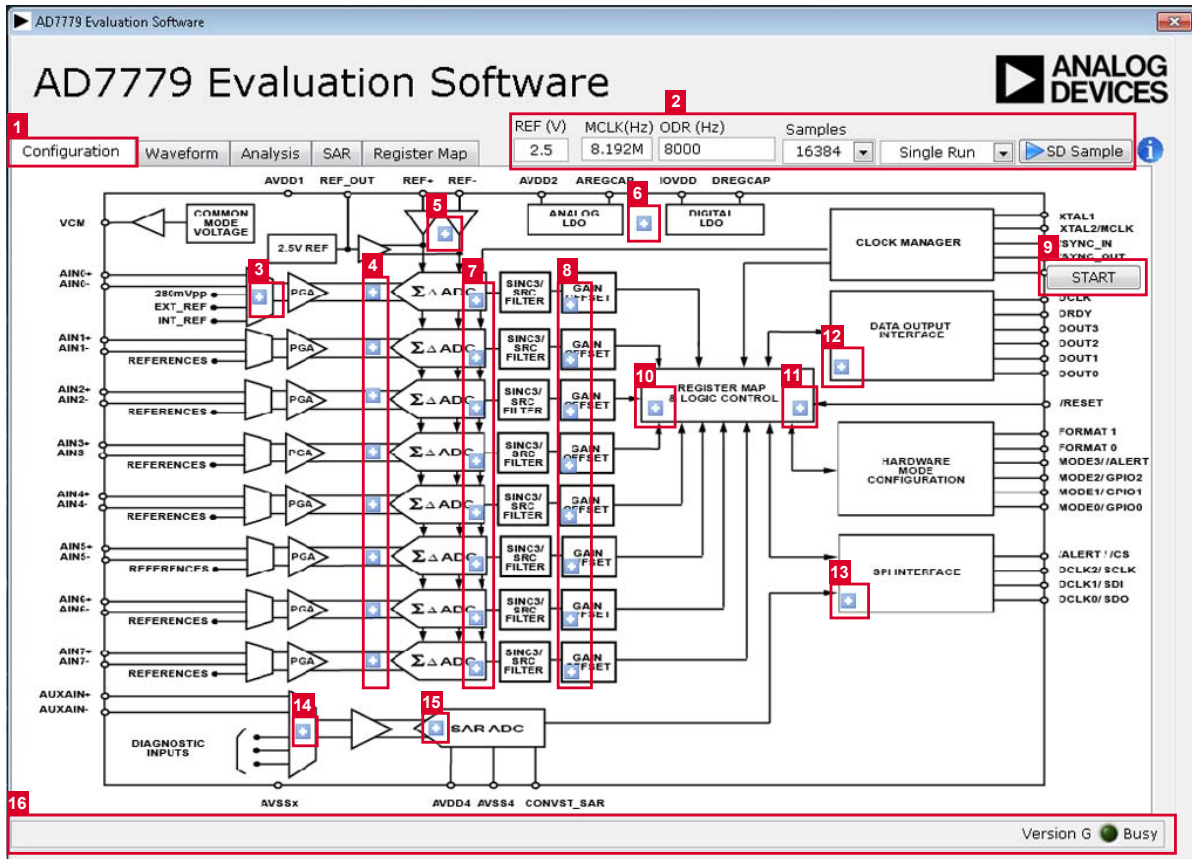


Figure 7. Configuration Tab of the AD7779 Evaluation Software

### OVERVIEW OF THE MAIN WINDOW

The main window of the software displays the significant control buttons and analysis indicators of the EVAL-AD7779FMCZ evaluation board software (see Figure 7). This window is divided into five tabs.

### CONFIGURATION TAB

#### General Configuration

The general configuration controls (Label 2 in Figure 7) define the voltage reference, external clock, the output data rate, number of samples, and if the SD is read continuously or one time only.

When changing the ODR (Hz) value, click away from the field to process the update. The software programs the SRC registers accordingly.

Click **SD Sample** to acquire samples from the AD7779.

#### Σ-Δ ADC Diagnostic Pop-Up Button

The Σ-Δ ADC diagnostic pop-up button (Label 3) selects the internal diagnostic inputs from the multiplexer. This input is common for all eight ADCs.

#### SD Input Configuration Pop-Up Buttons

The SD input configuration pop-up buttons (Label 4) select the ADC gain, enable the diagnostic mux to be the input for the channel (Rx), disable the SD channel, or configure the channel to monitor the voltage reference. Clicking this button selects the SD reference as VDD3/AVSSx for all channels and the input diagnostic mux as the input for this channel.

#### Reference Voltage Pop-Up Buttons

The reference voltage pop-up buttons (Label 5) set the reference voltage used for calculating the results in the **Waveform** and **Histogram** tabs. The evaluation board has an external 2.5 V ADR441 reference; however, this reference can be bypassed using this pop-up button, and the user can change the external reference voltage value to ensure correct calculation of results in the **Waveform** and **Histogram** tabs. Internal reference and reference buffers can be selected using these pop-up buttons. If AVDD3/AVSSx is selected as the reference, the REF (V) value must be updated accordingly.

#### Regulators Pop-Up Button

The regulators pop-up button (Label 6) allows the user to overdrive the internal LDOs externally, and also provides information about the error detected on the regulators.

**SD Errors Pop-up Buttons**

The SD errors pop-up buttons (Label 7) show the errors detected on the SD channel.

**Gain, Offset, and Phase Pop-up Buttons**

The gain, offset, and phase pop-up buttons (Label 8) allow the user to calibrate the offset and gain of each specific SD channel. After the phase compensation is updated, click **START** to apply the change.

**START Button**

Clicking **START** (Label 9) generates a pulse on the START pin to reset the internal sinc filter, which ensures that any update on the phase compensation register is correctly applied.

**Control Configuration Pop-Up Button**

The control configuration pop-up button (Label 10) allows the user to configure features such as the power mode (must be set to high power mode, unless a different clock is provided), the common-mode voltage (VCM), the internal oscillator, and the mode to update the ODR (SRC registers).

It is recommended not to change the SRC load source (Bit 7 in the SRC load source and load update register, Address 0x64[7]), because the GUI only support software updates. Selecting SRC\_LOAD\_SOURCE 0x64 [7] is not supported on the evaluation board.

The SRC register can be updated manually; however, the update is not reflected in the **ODR (Hz)** field.

Errors related to the memory map appear in this pop-up.

**Error Test Pop-Up Button**

The error test pop-up button (Label 11) enables and disables the different error checkers implemented in the [AD7779](#).

**Data Output Interface Pop-Up Button**

The data output interface pop-up button (Label 12) adjusts the DOUT header and driver strength.

**SPI Interface Pop-Up Button**

The SPI interface pop-up button (Label 13) adjusts the various parameters for the SPI and shows any SPI errors.

**SAR Input Pop-Up Button**

The SAR input pop-up button (Label 14) allows the user to select the input signal for the SAR ADC.

**SAR Power Pop-Up Button**

The SAR power pop-up button (Label 15) enables and disables the SAR ADC. If the SAR is disabled, the SAR input mux is disabled as well.

**Status Bar**

The status bar (Label 16) displays the status of the board and indicates if the board is busy and cannot perform any other action.

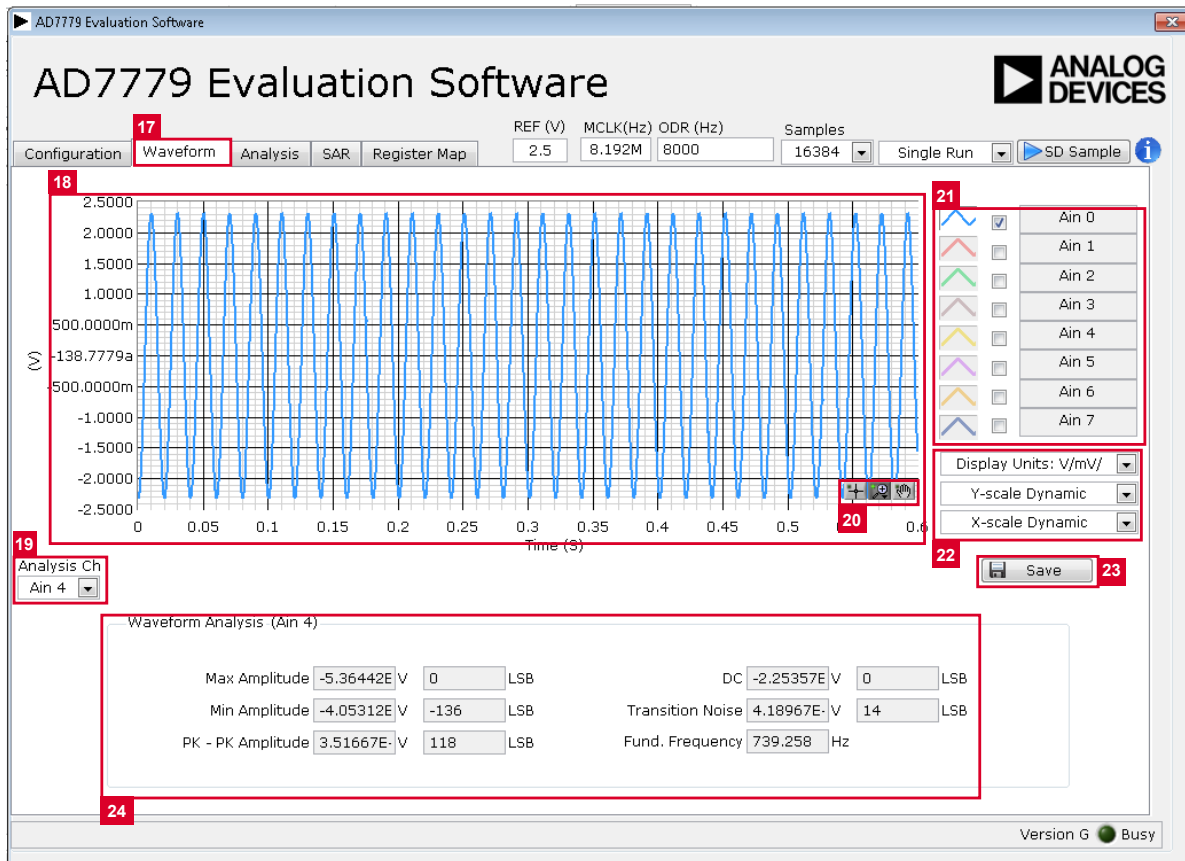


Figure 8. **Waveform** Tab of the **AD7779** Evaluation Software

**WAVEFORM TAB**

**Waveform Graph and Controls**

The data waveform (Label 18) shows each successive sample of the ADC output. The control tools (Label 20) in the graph allow the user to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

**Analysis Channel**

The noise/waveform analysis section (Label 24) and histogram graph show the analysis of the channel selected via the **Analysis Ch** drop-down box (Label 19).

**Channel Selection**

The channel selection control (Label 21) allows the user to choose which channels display on the data waveform. It also shows the analog inputs for that channel labeled next to the on and off controls. These controls only affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

**Display Units and Axis Controls**

Use the **Display Units** drop-down box (Label 22) to select whether the data graph displays in units of voltages or codes. This affects both the waveform graph and the histogram graph. The axis controls can be switched between dynamic and fixed. When dynamic is selected, the axis automatically adjusts to show the entire range of the ADC results after each batch of samples. When fixed is selected, the user can program the axis ranges manually, and the ranges do not adjust automatically after each sample batch.

If the value is selected as hex, the x-axis of the graph shows the original data (second complement). Due to the limitations of the software, the number shows as signed 32 bits rather than signed 24 bits.

**Save Data**

Click **Save** (Label 23) to save the samples to an external file.

**Waveform Analysis**

The **Waveform Analysis** section (Label 24) displays the results of the noise analysis for the selected analysis channel. The rms noise is only applicable with a constant dc value.

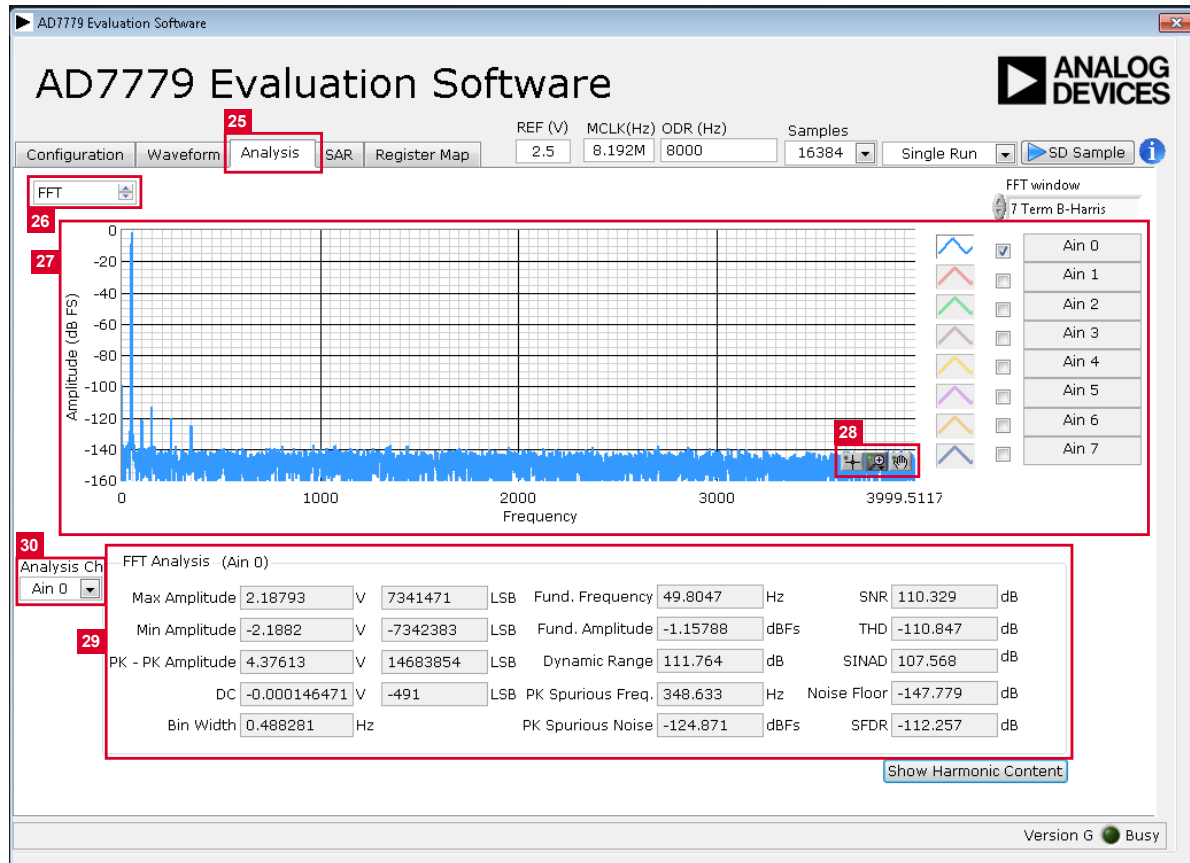


Figure 9. Analysis Tab of the AD7779 Evaluation Software

## ANALYSIS TAB

### FFT Graph and Histogram Selection

Use the FFT/histogram selection box (Label 26) to select between histogram and frequency analysis of the data.

### FFT Graph and Controls

The FFT graph (Label 27) shows the fast Fourier transform of the sampled signal. Note that the windows applied is the 7-term Blackman Harris. The frequency is displayed on the x-axis and the amplitude is graphed on the y-axis. Use the control tools (Label 28) to zoom in on the data. Harmonic content can be selected by clicking **Show Harmonic Content**.

### Analysis Channel

The noise/waveform analysis section (Label 29) and the FFT graph show the analysis of the channel selected via the **Analysis Ch** control (Label 30).

### Channel Selection

The **Analysis Ch** control (Label 30) allows the user to choose which channels display on the data waveform. It also shows the analog inputs for that channel labeled next to the on and off controls. These controls only affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

### FFT Window Selection

The **FFT window** control allows the user to choose which external windowing method to apply to calculate the discrete Fourier transform.

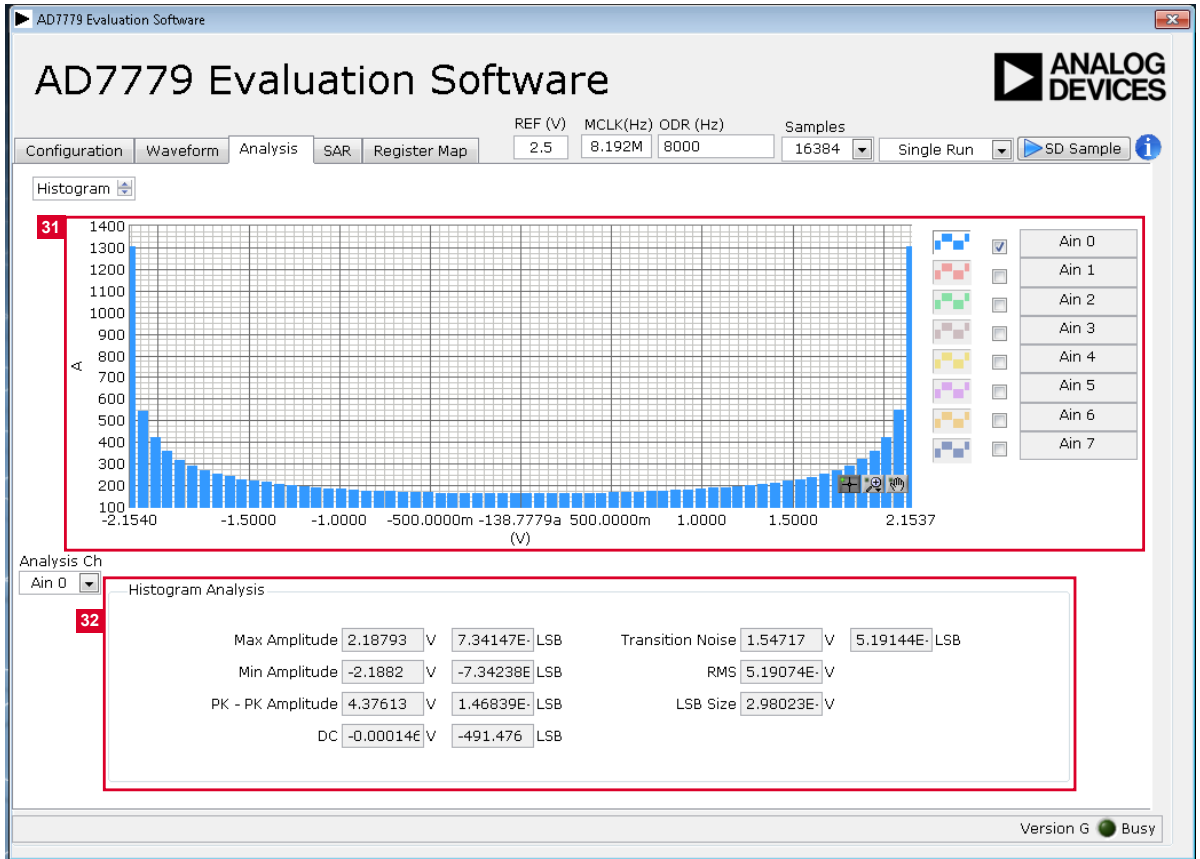


Figure 10. Histogram Tab of the AD7779 Evaluation Board Software

**Histogram and Controls**

The data histogram (Label 31) shows the number of times each sample of the ADC output occurs. The control tools in the graph allow the user to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

**Histogram Analysis**

The **Histogram Analysis** section (Label 32) shows the analysis of the channel selected via the **Analysis Ch** control.

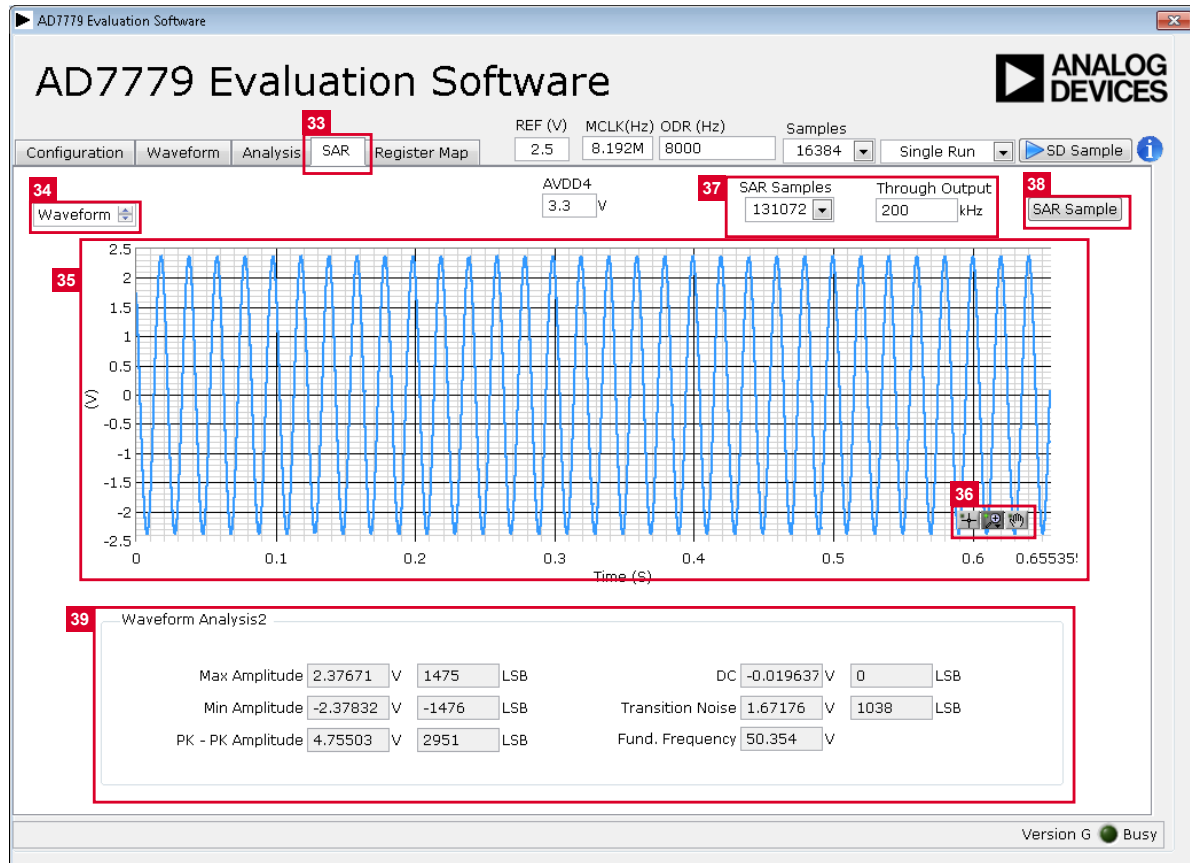


Figure 11. SAR Waveform Tab of the AD7779 Evaluation Software

## SAR TAB

When the SAR ADC is enabled through the SAR power pop-up button (Label 15 in Figure 7), the SAR tab allows the user to sample and analyze data from the SAR ADC.

### FFT Graph and Waveform Selection

Use the FFT/waveform selection box (Label 34) to select between waveform and frequency analysis of the data.

### Waveform Graph and Controls

The data waveform (Label 35) shows each successive sample of the ADC output. The control tools (Label 36) in the graph allow the user to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

### Analysis Channel

The noise/waveform analysis section (Label 39) and histogram graph analysis show the analysis of the channel selected via the Analysis Ch control.

### SAR Configuration

The SAR configuration controls (Label 37) allow the user to define the number of samples and the through output channel.

### SAR sample

Click SAR Sample (Label 38) to gather samples from the SAR.



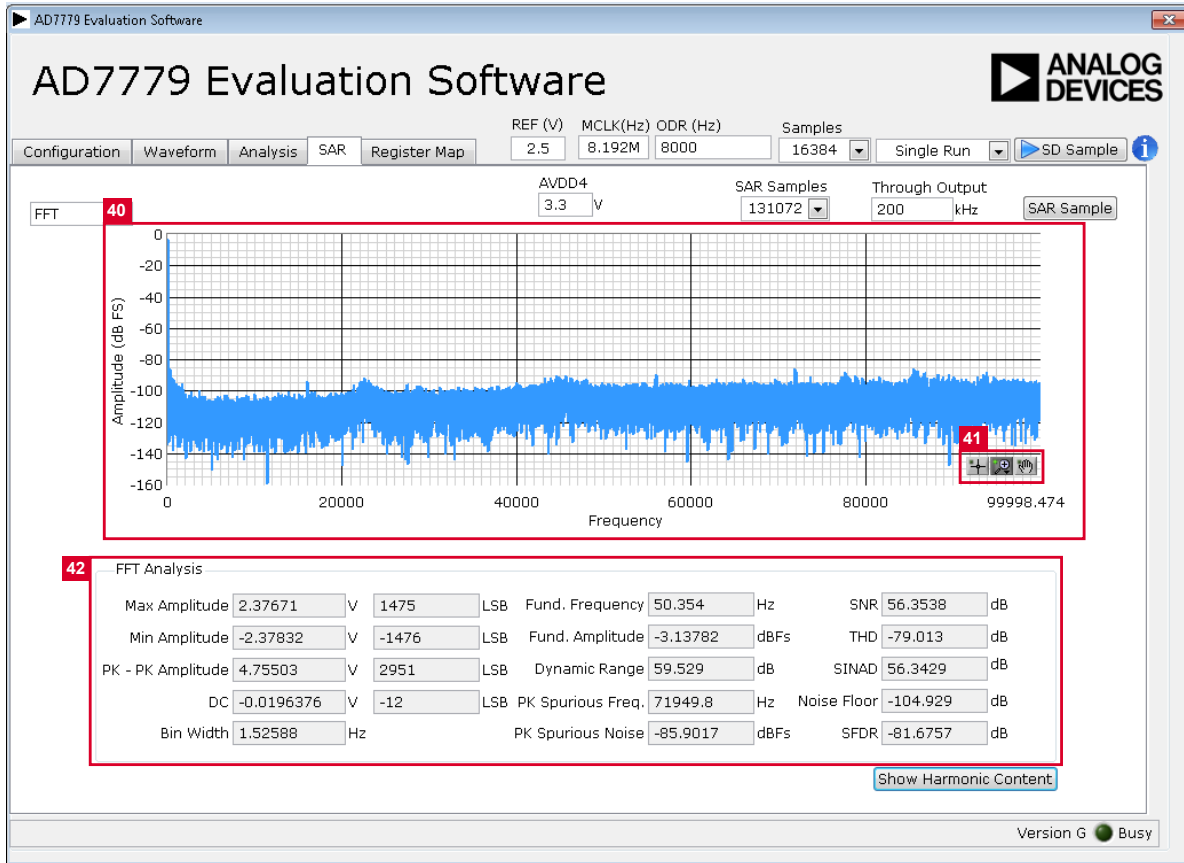


Figure 12. SAR FFT Tab of the AD7779 Evaluation Software

**FFT Graph and Controls**

The FFT graph (Label 40) shows the fast Fourier transform of the sampled signal. The frequency is displayed on the x-axis and the amplitude is graphed on the y-axis. Use the control tools (Label 41) to zoom in on the data. Harmonic content can be selected by clicking **Show Harmonic Content**.

**Analysis Channel**

The noise/waveform analysis section (Label 42) and FFT graph show the analysis of the channel selected via the **Analysis Ch** control.

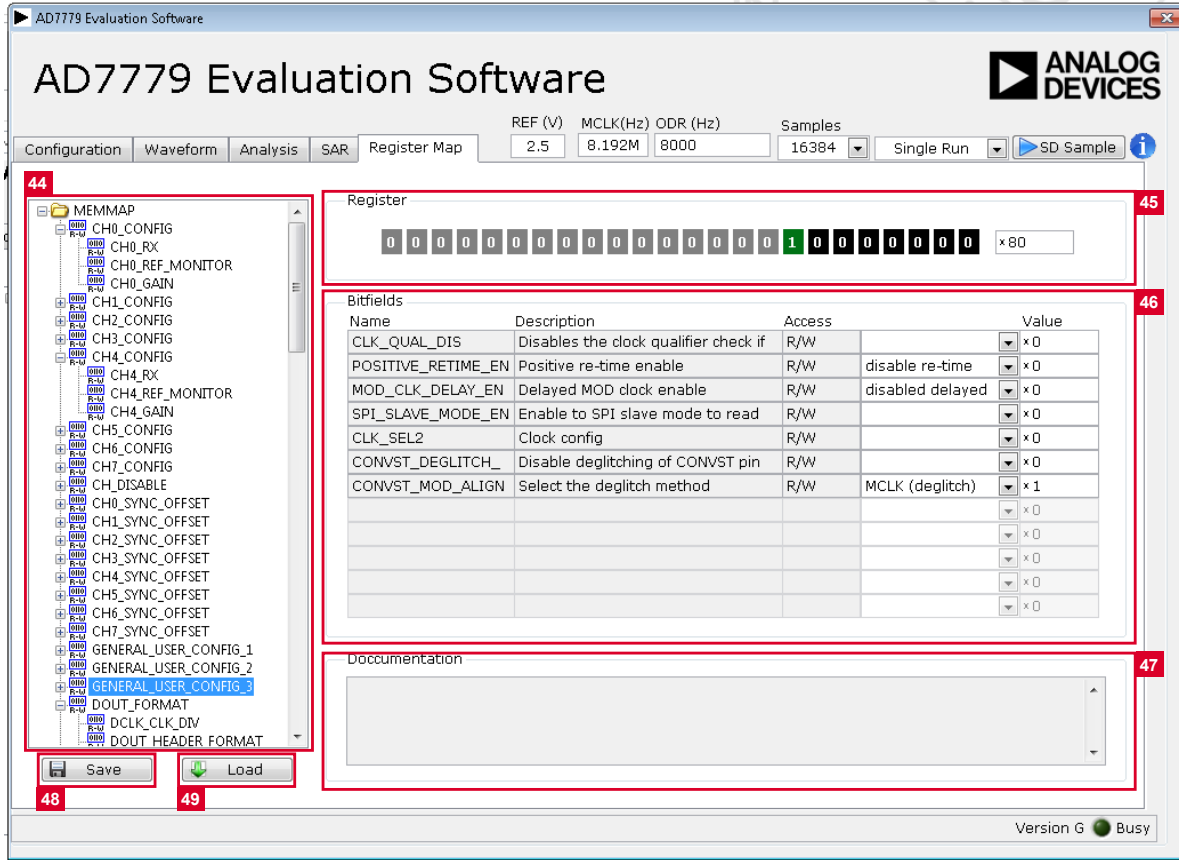


Figure 13. Register Map and Configuration

**REGISTER MAP TAB**

**Register Tree**

The register tree (Label 44) shows the full register map in a tree control. Each register is shown. Click the expand button next to each register to show all the bitfields contained within that register.

**Register Control**

The Register control (Label 45) allows the user to change the individual bits of the register selected in the register tree (Label 44). Click on each bit to toggle the value, or program the register value directly into the number control field on the right.

**Bitfields List**

The Bitfields list (Label 46) shows all the bitfields of the register selected in the register tree (Label 44). The values can be changed using the drop-down box or by entering a value directly into the number control on the right.

**Documentation**

The Documentation section (Label 47) contains the documentation for the register and bitfield selected in the register tree (Label 44).

**Save and Load**

The Save and Load buttons (Label 48 and Label 49) allow the user to save the current register map setting to a file and load the setting from the same file.

**EXITING THE SOFTWARE**

To exit the software, click the close button at the top, right corner of the main window.

# EVALUATION BOARD SCHEMATICS AND LAYOUT

13550-014

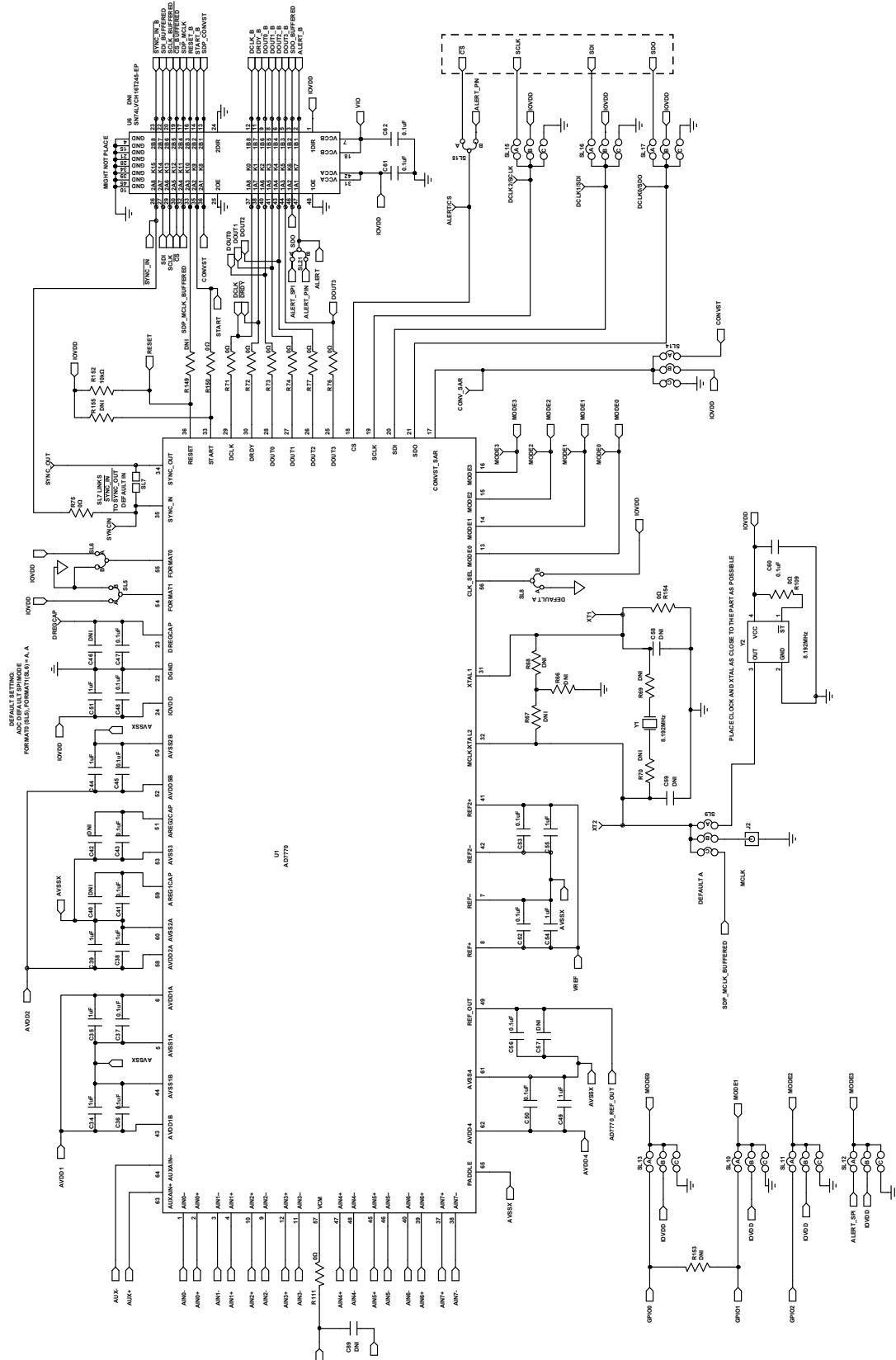


Figure 14. Evaluation Board Schematic—Page 1

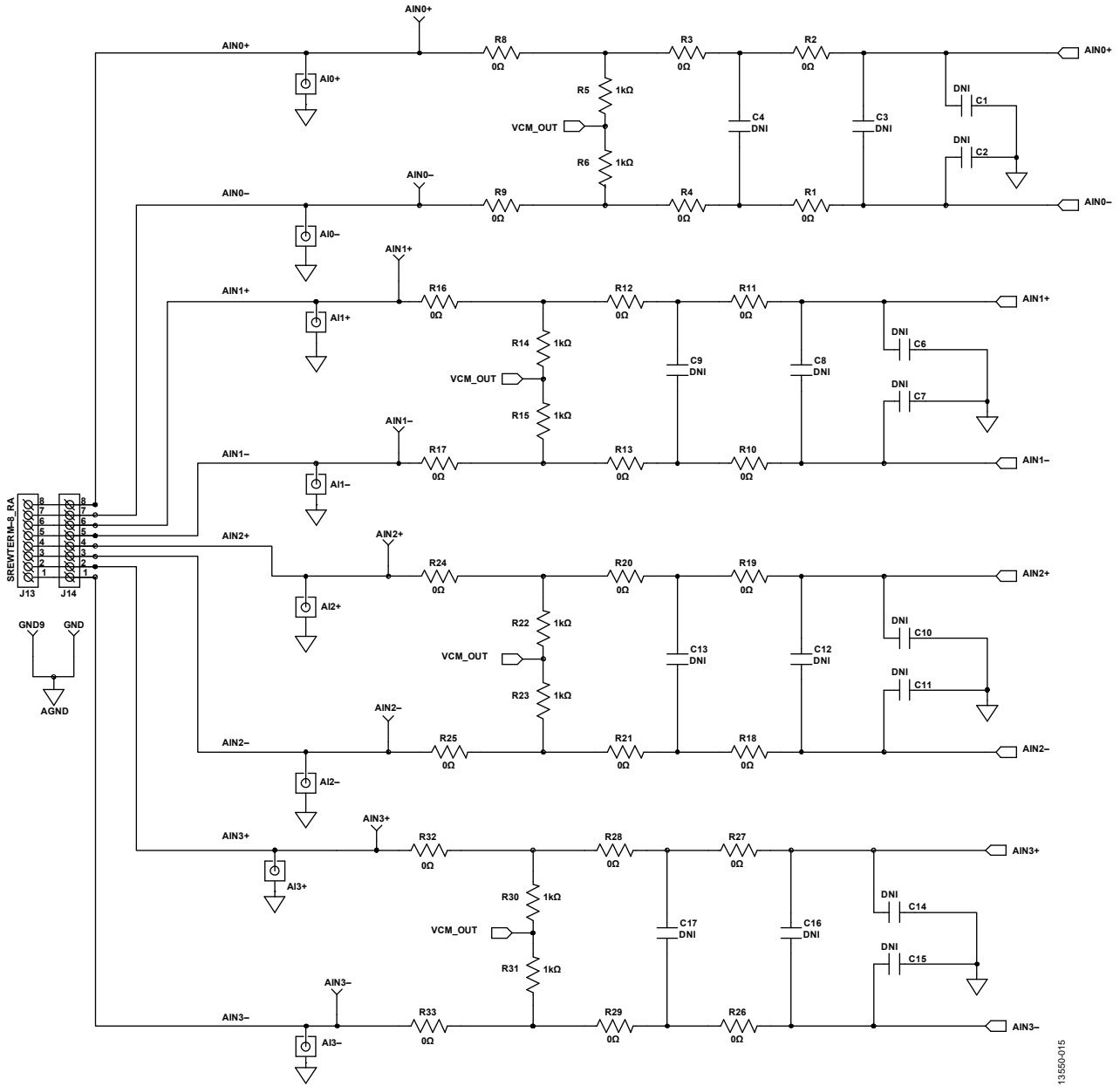


Figure 15. Evaluation Board Schematic—Page 2

13550-015

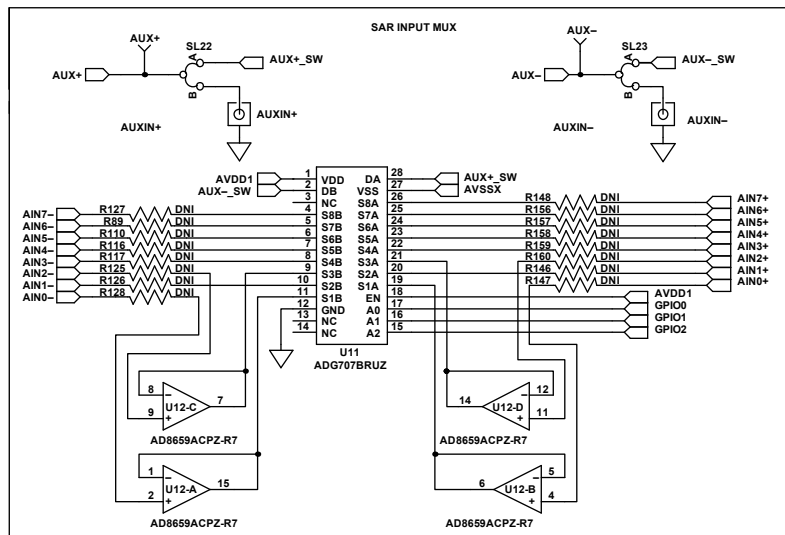
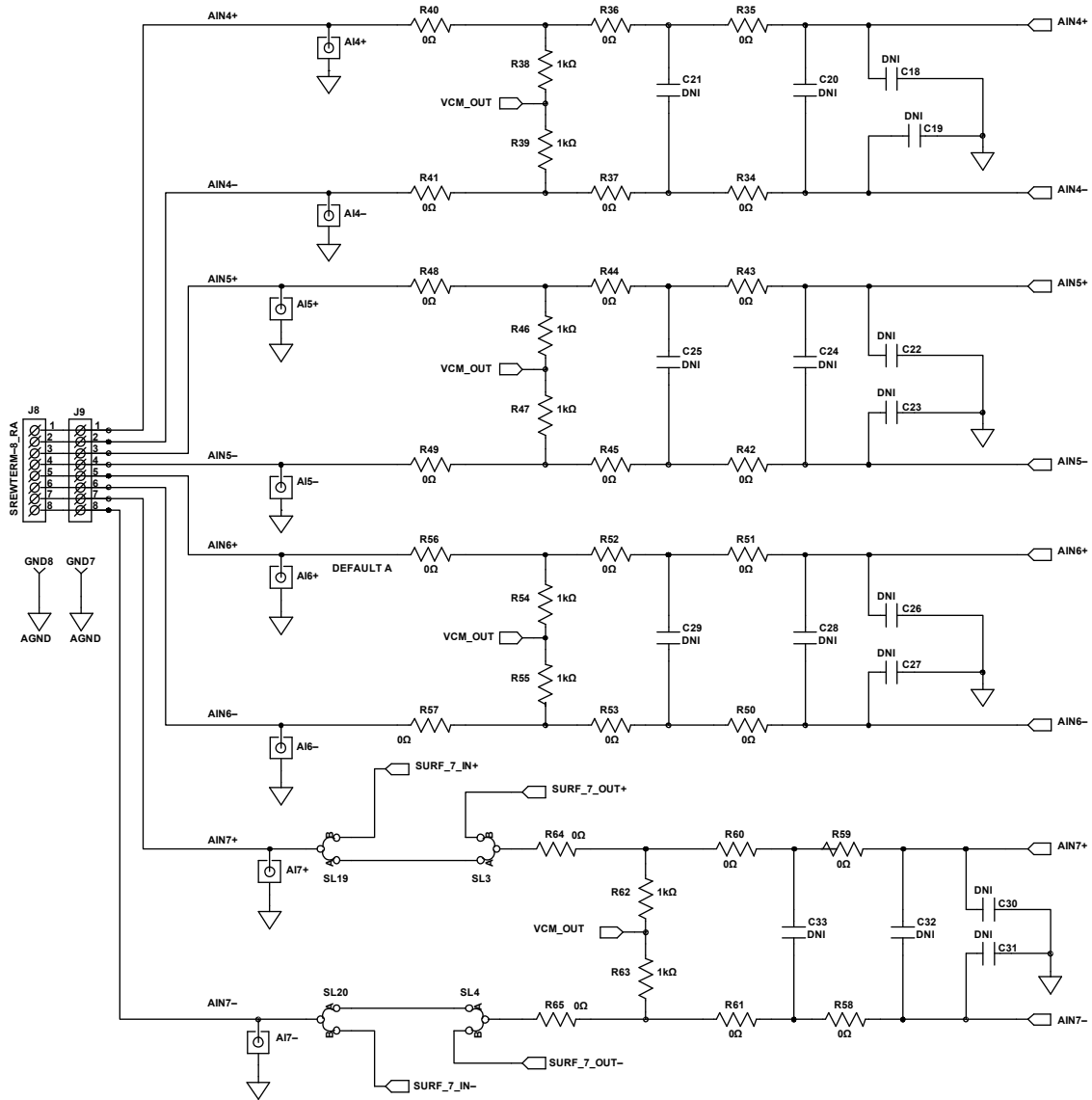


Figure 16. Evaluation Board Schematic—Page 3

13550-017

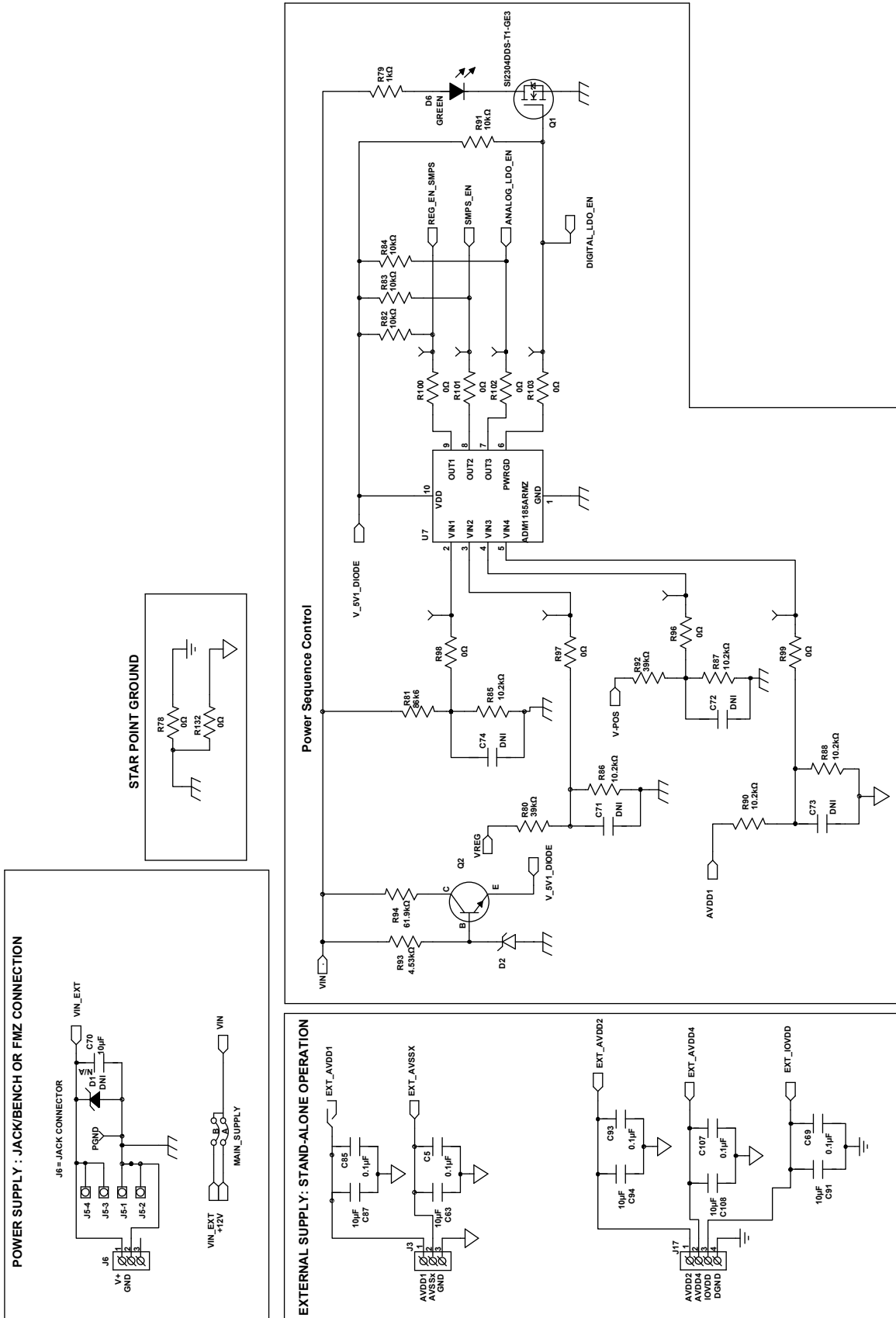


Figure 17. Evaluation Board Schematic—Page 4

810-05513

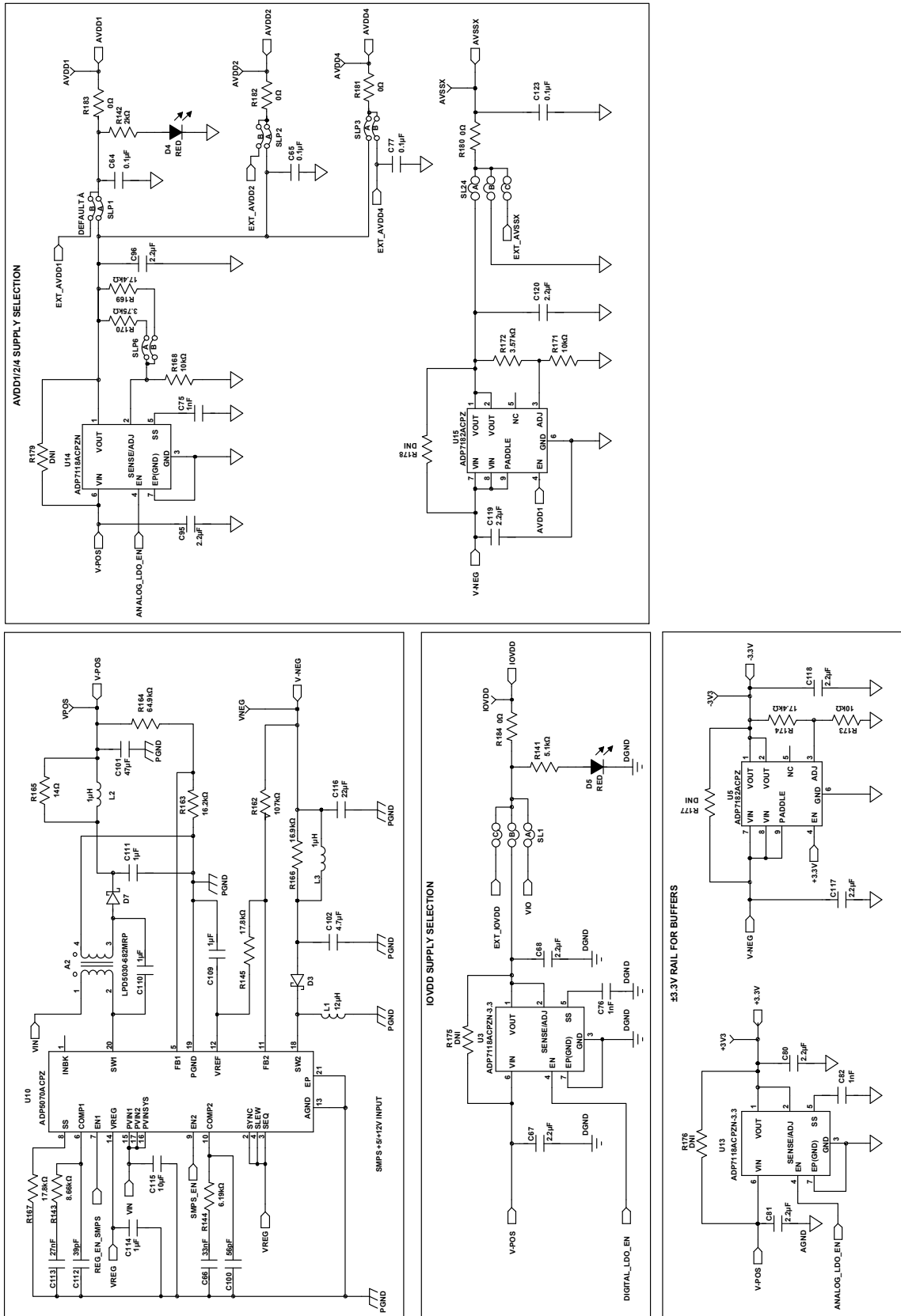


Figure 18. Evaluation Board Schematic—Page 5





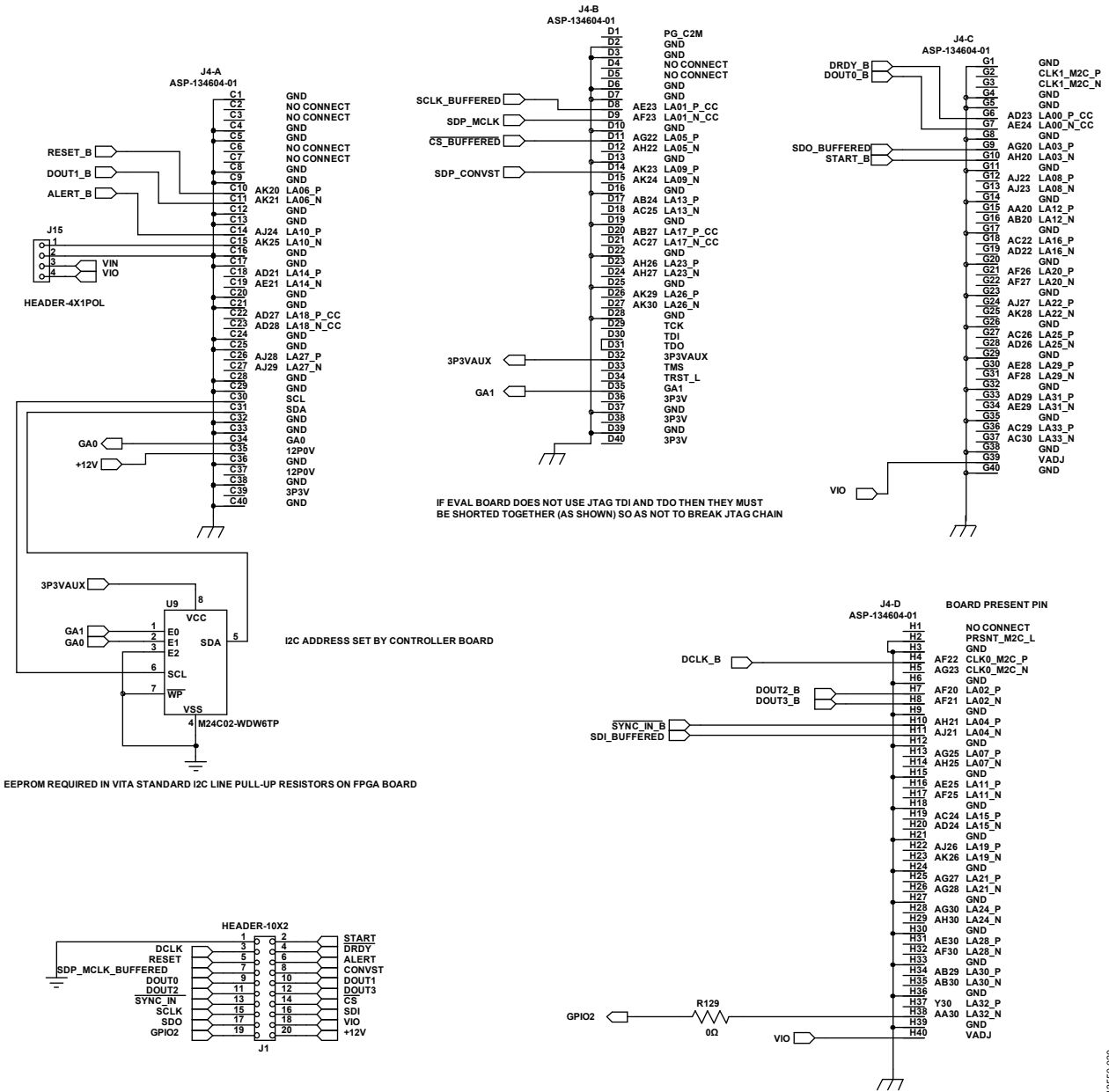


Figure 20. Evaluation Board Schematic—Page 7

135560-020

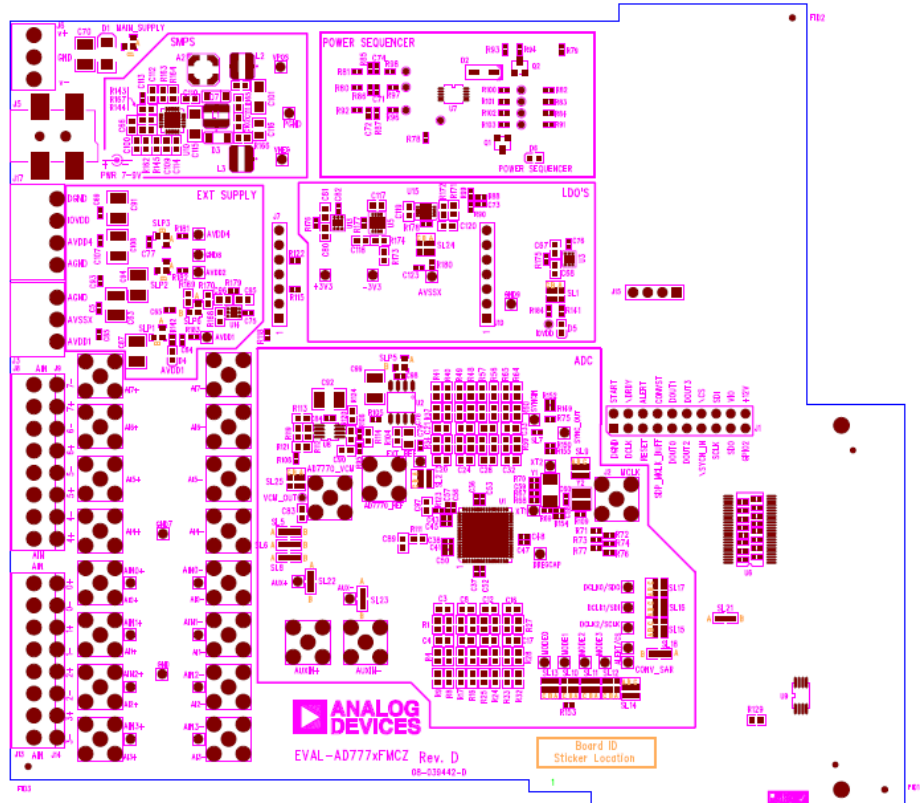


Figure 21. Evaluation Board Layout, Component Side (Top)

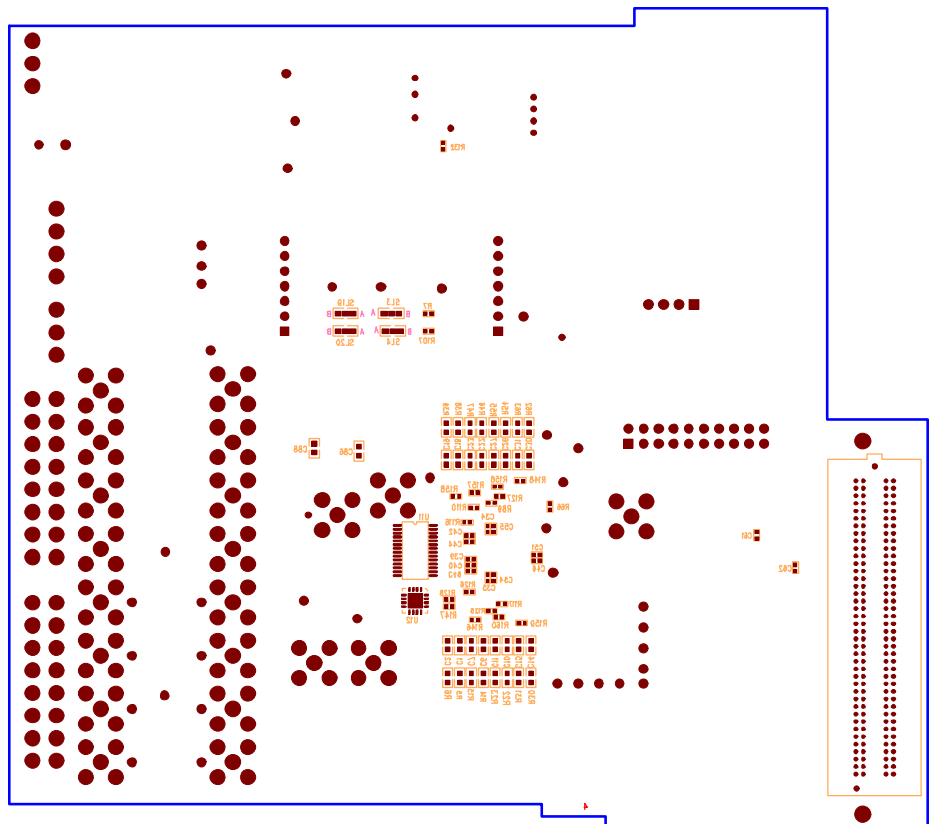


Figure 22. Evaluation Board Layout, Component Side (Bottom)

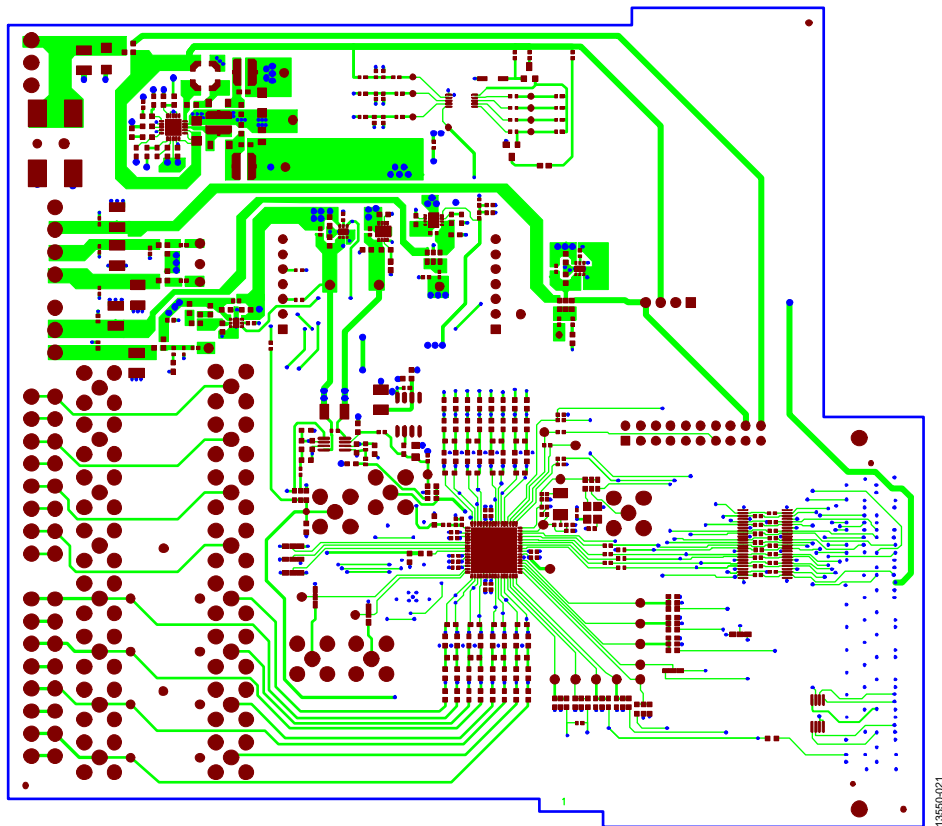


Figure 23. Evaluation Board Layout, Layer 1, Component Side

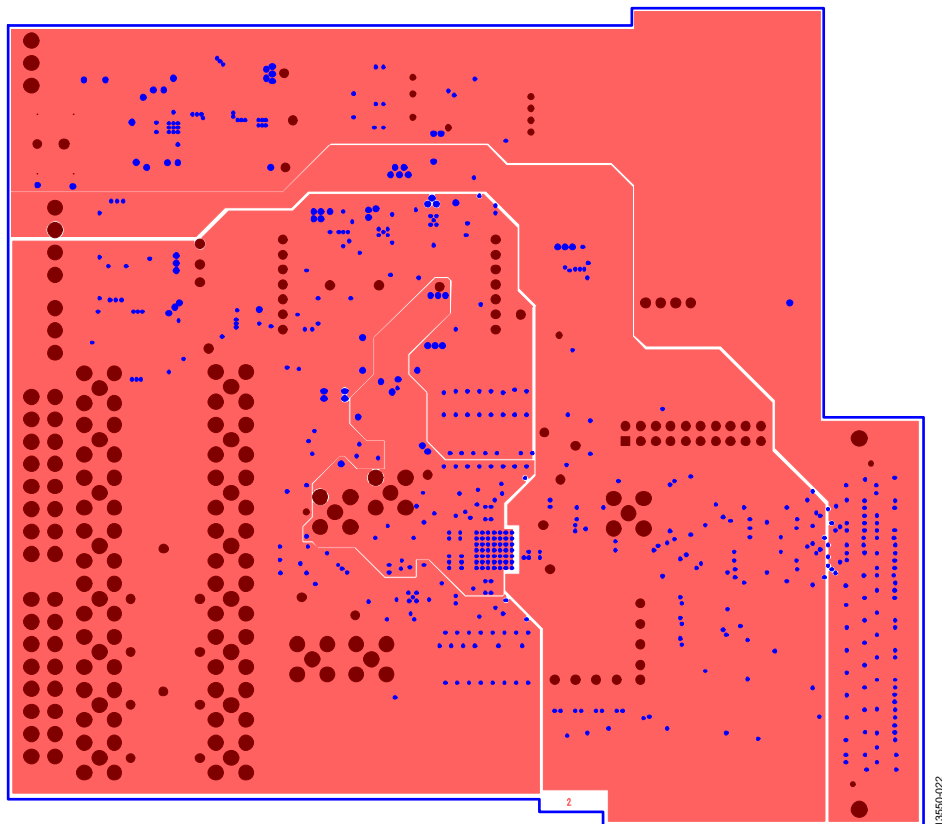


Figure 24. Evaluation Board Layout, Layer 2, GND Planes

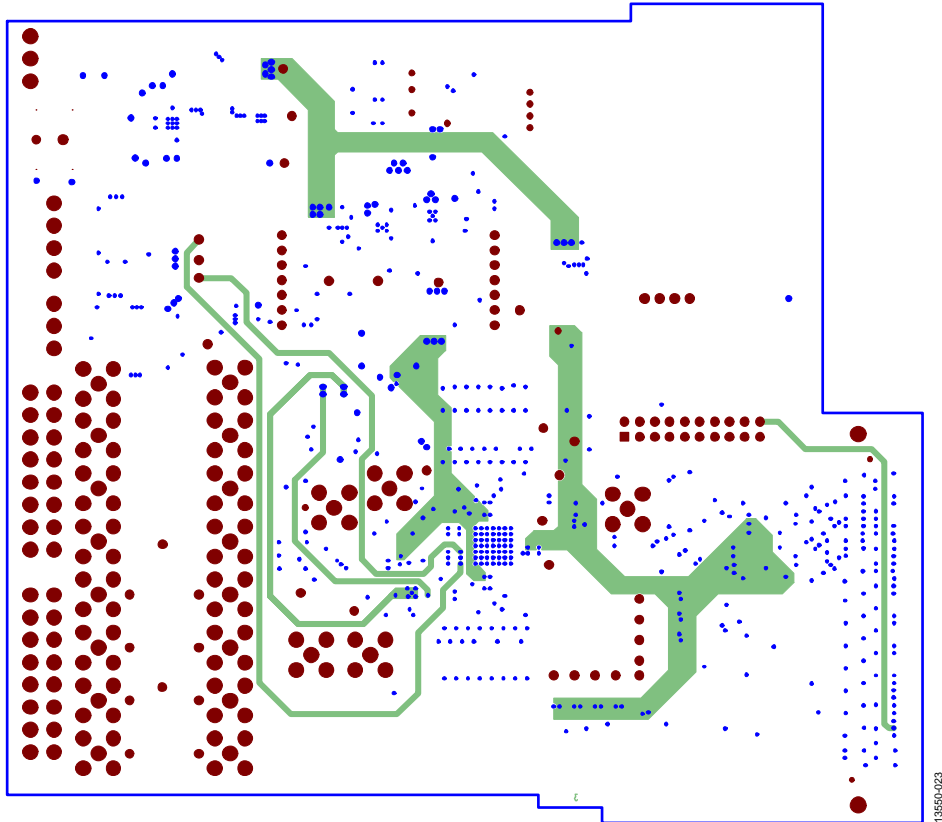


Figure 25. Evaluation Board Layout, Layer 3, Power Traces and GND Planes

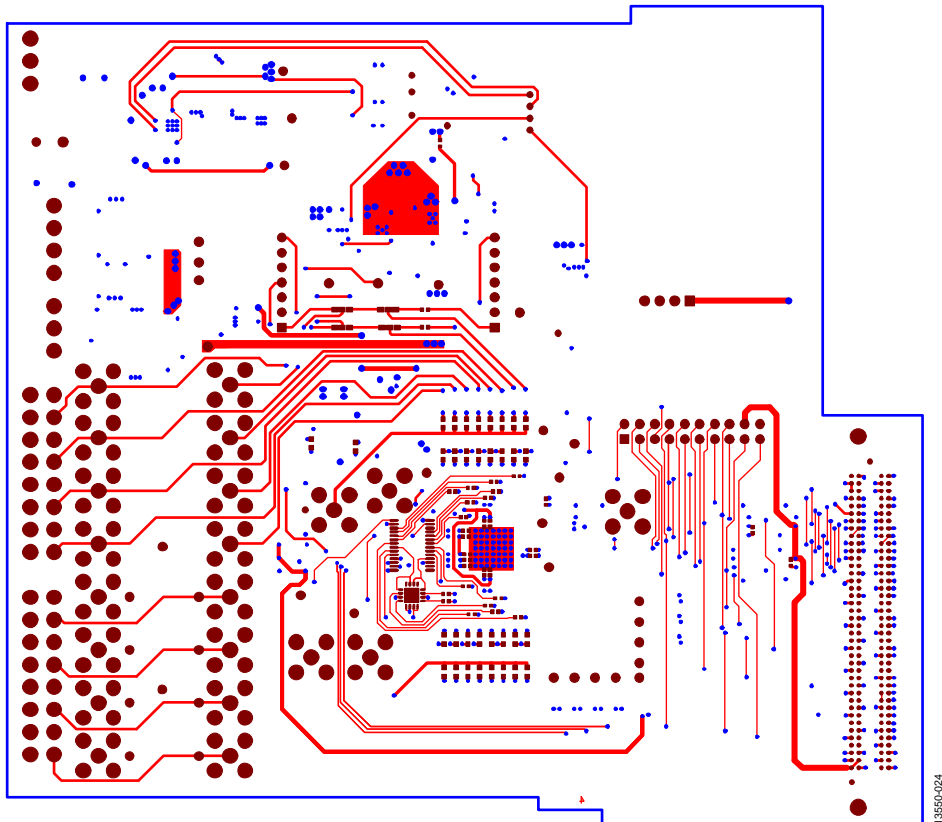


Figure 26. Evaluation Board Layout, Layer 4, Solder Side

# ORDERING INFORMATION

## BILL OF MATERIALS

Table 5.

Reference Designator	Value	Description	Part Number
+3V3, -3V3, AIN0+, AIN0-, AIN1+, AIN1-, AIN2+, AIN2-, AIN3+, AIN3-, AUX+, AUX-, AVDD1, AVDD2, AVDD4, AVSSX, CONV_SAR, DCLK0/SDO, DCLK1/SDI, EXT_REF, MODE0 to MODE3		Red test point	20-313137
A2		Coupled inductor, 6.8 µH, 1.2 A, 20% Straight PCB mount SMB jack	LPD5030-682MRB 1-1337482-0
AD7779_REF, AD7779_VCM, AI0+, AI0-, AI1+, AI1-, AI2+, AI2-, AI3+, AI3-, AI4+, AI4-, AI5+, AI5-, AI6+, AI6-, AI7+, AI7-, AUXIN+, AUXIN-		Black test point	20-3131
ALERT/CS, DCLK2/SCLK, DREGCAP, GND, GND7, GND8, GND9, PGND, XT1, XT2, SYNCIN, SYNC_OUT			
C1 to C4, C6 to C33, C86, C88, C89	Do not insert	Ceramic capacitor, not inserted, 0603	Not applicable
C5, C36 to C38, C41, C43, C45, C47, C48, C50, C52, C53, C56, C60 to C62, C64, C65, C69, C77, C79, C84, C85, C93, C98, C107, C123	0.1 µF	Capacitor ceramic, 16 V, X7R, 0402	MC0402B104K160CT
C34, C35, C39, C44, C49, C51, C54, C55	1 µF	Capacitor, 0402, 1 µF, 6.3 V, X5R	04026D105KAT2A
C40, C42, C46	Do not insert	0402 capacitor location	Not applicable
C57 to C59, C71 to C74	Do not insert	Ceramic capacitor, not inserted, 0402	Not applicable
C63, C70, C87, C91, C92, C94, C99, C108	10 µF	Capacitor, ceramic, 50 V, X5R, 1210	GRM32ER61H106K
C66	33 nF	SMD capacitor	MC0603B333K500CT
C67 C68, C80, C81, C95, C96, C117 to C120	2.2 µF	Capacitor, 0603, 2.2 µF, 6.3 V	MC0603X225K6R3CT
C75, C76, C82	1 nF	50 V, X7R, multilayer ceramic capacitor	MC0402B102K500CT
C78	22 µF	22 µF, SMD, tantalum, 0805, capacitor	TACR226M010XTA
C83, C90, C97	Do not insert	Ceramic capacitor, 0603	Do not insert
C100	56 pF	SMD capacitor	MC0603N560J500CT
C101	47 µF	SMD capacitor	GRM31CR60J476ME19L
C102	4.7 µF	SMD capacitor	C1608X5R0J475K/0.80
C109, C114	1 µF	SMD capacitor	C1005X5R1C105K050BC
C110	1 µF	SMD capacitor	GRM188R61C105KA93D
C111	1 µF	SMD capacitor	C1005X5R0J105M050BB
C112	39 pF	SMD capacitor	MC0603N390J500CT
C113	27 nF	SMD capacitor	C0402C273K3RACTU
C115	10 µF	SMD capacitor	C3216X5R1C106M160AA
C116	22 µF	SMD capacitor	GRM21BR60J226ME49L
D1	Do not insert	Do not insert	Not applicable
D2		Diode, Zener, 0.5 W, 4.7 V, SOD-123	MMSZ5230B-7-F
D3, D7	20 V, 0.5 A	Schottky, 0.5 A, 20 V, SOD-123FL	MBR0520LT1G
D4, D5	Red	LED, SMD, red	HSMC-C191
D6	Green	LED, SMD, green	LGQ971
IOVDD, S1, S3, S5, S5'2, S6'2, S7, S7'2, S8'2, VCM_OUT, VNEG, VPOS	Do not insert	Test point, not inserted, keep hole clear of solder	Not applicable
J1		20-pin (2 × 10), 0.1" pitch, header	M20-9981046
J3		Power socket block, 3-way, 3.81 mm	MC1.5/3-G-3.81
J4		160-pin, 10 mm, male, VITA 57, connector	ASP-134604-01
J5		DC power connectors, 2 mm, SMT, power jack	KLDX-SMT2-0202-A
J6	Do not insert	Socket terminal block, pitch 3.81 mm	MC 1.5/3-G-3.81

Reference Designator	Value	Description	Part Number
J7		7-way, SSW, 2.54 mm, vertical socket (make sure that socket lines up with connector on surfboard)	SSW-107-01-T-S
J8, J13	Do not insert	8-pin screw terminal, pitch 3.81 mm, vertical	1727078
J9, J14		8-pin terminal header, pitch 3.81 mm, vertical	MC 1,5/ 8-G-3,81
J10		7-way, SIP, 2.54 mm, TH header (make sure that header lines up with connector on surfboard)	TLW-107-05-G-S
J15	1 × 4-pin	Header, vertical, not inserted	Not applicable
J17		Power socket block, 4-way, pitch 3.81mm	MC1.5/4-G-3.81
K0 to K15		Resistor, 0402, 1%, 0 Ω	0 Ω
L1	12 μH	Inductor	ME3220-123KLB
L2, L3	1 μH	Inductor	ME3220-102MLB
MAIN_SUPPLY		2-way solder link (use 0 Ω 0603 resistor)	Insert in Link Position A
Q1		MOSFET, N-channel, 30 V, 3.6 A, diode, SOT-23	SI2304DDS-T1-GE3
Q2		Transistor, NPN, SOT-23	MMBT3904LT1G
R1 to R4, R8 to R13, R16 to R21, R24 to R29, R32 to R37, R40 to R45, R48 to R53, R56 to R61, R64, R65, R111, R112, R121, R129	0 Ω	Resistor, 0603, 1%, 0 Ω	MC0063W06030R
R5, R6, R14, R15, R22, R23, R30, R31, R38, R39, R46, R47, R54, R55, R62, R63	1 kΩ	Resistor, 1 kΩ, 0.063 W, 1%, 0603	MC0063W060311K
R7, R71 to R78, R95 to R103, R105 to R109, R115, R118, R122, R123, R132, R150	0 Ω	Resistor, 0402, 1%, 0 Ω	MC00625W040210R
R66 to R70, R89, R110, R116, R117, R125 to R128, R146 to R148, R153, R156 to R160, R175 to R179	Do not insert	Resistor, not inserted, 0402	Not applicable
R79	1 kΩ	Resistor, thick film, 1 kΩ, 0402, 63 mW, 1%	CRCW04021K00FKED
R80, R92	39 kΩ	Resistor, 0402, 1%, 39 kΩ	MC 0.0625W 0402 1% 39K
R81	86.6 kΩ	Resistor, 0402, 1%, 86.6 kΩ	MC 0.0625W 0402 1% 86K6
R82 to R84, R91, R152	10 kΩ	Resistor, 10 kΩ, 0.063 W, 1%, 0402	MC00625W0402110K
R85 to R88, R90	10.2 kΩ	SMD resistor	MC 0.0625W 0402 1% 10K2
R93	4.53 kΩ	Resistor, thick film, 4.53 kΩ, 63 mW, 1%	CRCW04024K53FKED
R94	61.9 Ω	Resistor, 0402, 1%, 61.9 Ω	MC 0.0625W 0402 1% 61R9
R104	15 Ω	Resistor, 15 Ω, 0.063 W, 1%, 0603	MC0063W0603115R
R113, R114, R119, R120, R124	Do not insert	Resistor, not inserted, 0603	Not applicable
R141	5.1 kΩ	Resistor, 5.1 kΩ, 0.063 W, 1%, 0402	MC00625W040215K1
R142	2 kΩ	Resistor, MC series, 2 kΩ, 62.5 mW, ±1%, 50 V, 0402	MC00625W040212K
R143	8.66 kΩ	Resistor, 8.66 kΩ, 0.063 W, 1%, 0603	MC0063W060318K66
R144	6.19 kΩ	Resistor, thick film, 6.19 kΩ, 0.2 W, 1%	ERJP03F6191V
R145, R167	17.8 kΩ	Resistor, thick film, 17.8 kΩ, 1%, 0603	MCT 0603-50 1% P5 17K8
R149, R155	Do not insert	SMD, resistor, 0402	Not applicable
R154	0 Ω	Resistor, 0402, 1%, 0 Ω	MC00625W040210R
R162	107 kΩ	Resistor, 0603, 107 kΩ, 1%	CRCW0603107KFKEA
R163	16.2 kΩ	Resistor, 0603, 16.2 kΩ 1%, 0.1 W	ERJ3EKF1622V
R164	64.9 kΩ	Resistor, 0603, 64.9 kΩ, 1%	CRCW060364K9FKEA
R165	14 Ω	Resistor, 14 Ω, 0.063 W, 1%, 0603	MC0063W0603114R
R166	16.9 Ω	Resistor, 16.9 Ω, 0.063 W, 1%, 0603	MC0063W0603116R9
R168	10 kΩ	Resistor, thick film, 10 kΩ, 0.1 W, 1%	RC0603FR-0710KL
R169	17.4 kΩ	Resistor, 0603, 17.4 kΩ, 1%	CRCW060317K4FKEA
R170	3.74 kΩ	Thick film resistor, 3. 3.74 kΩ, 100 mW, 1%	CRCW06033K74FKEA
R171	10 kΩ	Resistor, thick film, 10 kΩ, 0.1 W, 1%	RC0603FR-0710KL
R172	3.57 kΩ	Resistor, 0603, 3.57 kΩ, 1%	CRCW06033K57FKEA
R173	10 kΩ	Resistor, thick film, 10 kΩ, 0.1W, 1%	RC0603FR-0710KL
R174	17.4 kΩ	Resistor, 0603, 17.4 kΩ, 1%	CRCW060317K4FKEA
R180 to R184, SL7	0 Ω	Resistor, 0402 1%, 0 Ω	MC00625W040210R

Reference Designator	Value	Description	Part Number
SL1, SL2, SL9 to SL17, SL24, SL25	Do not insert	3-way link option, insert 0 $\Omega$ in Position A	MC 0.063W 0603 0R
SL3 to SL6, SL19, SL20, SL22, SL23		2-way resistor link option (insert in Position A)	MC 0.063W 0603 0R
SL8, SL18, SL21		2-way resistor link option, default Position A	MC 0.063W 0603 0R
SLP1 to SLP6		2-way solder link (use 0 $\Omega$ , 0603 resistor)	Insert in Link Position A
U1		8-channel, 24-bit, simultaneous sampling ADC	<a href="#">AD7779ACPZ</a>
U2		2.5 V reference	<a href="#">ADR441BRZ</a>
U3		Linear regulator, 3.3 V, ultralow noise, CMOS	<a href="#">ADP7118ACPZN-3.3</a>
U5		-28 V, -200 mA, low noise, linear regulator	<a href="#">ADP7182ACPZ</a>
U6		16-channel level shifter	SN74LVCH16T245
U7		Quad voltage monitor and sequencer	<a href="#">ADM1185ARMZ-1</a>
U8		IC, SM, dual low noise op amp, ADA4896, MSOP-8	<a href="#">ADA4896-2ARMZ</a>
U9		IC, EEPROM, 2 kb, 400 kHz, TSSOP-8	M24C02-WDW6TP
U10		1 A/0.6 A dc-to-dc switching regulator with positive and negative outputs	<a href="#">ADP5070ACPZ</a>
U11		8-channel multiplexer	<a href="#">ADG707BRUZ</a>
U12		Operational amplifier	<a href="#">AD8659ACPZ-R7</a>
U13	Linear regulator, 3.3 V, ultralow noise, CMOS	<a href="#">ADP7118ACPZN-3.3</a>	
U14	Linear regulator, adjustable voltage, ultralow noise, CMOS	<a href="#">ADP7118ACPZN</a>	
U15	-28 V, -200 mA, low noise, linear regulator	<a href="#">ADP7182ACPZ</a>	
Y1	8.192 MHz	8.192 MHz crystal, 12 pF, SMD	AA-8.192MAGE-T
Y2	8.192 MHz	Oscillator, SG-210 series, 8.192 MHz	SG-210STF 8.1920ML

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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