Single-chip Type with Built-in FET Switching Regulators

Simple Step-down Switching Regulators with Built-in Power MOSFET

Pb Free
ROHM Electronic Components

RoHS
Directive Compliance

BD9325FJ,BD9326EFJ,BD9327EFJ

No.10027ECT06

● Description

The BD9325FJ, BD9326EFJ and BD9327EFJ are step-down regulators that integrate a low resistance high side N-channel MOSFET.
It achieves 2A / 3A / 4A continuous output current over a wide input supply range.
Current mode operation provides fast transient response and easy phase compensation.

● Features

1) Wide operating INPUT Range 4.75V～18.0V
2) Selectable 2A / 3A / 4A Output Current
3) Selectable 0.16Ω / 0.12Ω / 0.11ΩInternal MOSFET Switch
4) Low ESR Output Ceramic Capacitors are Available
5) Low Stanby Current during Shutdown Mode
6) 380kHz Operating Frequency
7) Feedback voltage 0.9V ±1.5% Accuracy at room temp. (±3.0% for -40℃ to 85℃ temperature range)
8) Protection circuit: UnderVoltage lockout protection circuit
   Thermal shutdown circuit
   OverCurrent protection circuit
9) SOP-J8 Package for 2A model, HTSOP-J8 Package for 3A, 4A models (with Exposed thermal PAD)

● Applications

Distributed Power System
Pre-Regulator for Linear Regulator

● Line up matrix

LINE-UP	BD9325FJ	BD9326EFJ	BD9327EFJ
FET ON-RESISTANCE	0.16 Ω	0.12 Ω	0.11 Ω
OUTPUT CURRENT	2.0 A	3.0A	4.0 A
Package	SOP-J8	HTSOP-J8	HTSOP-J8

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{IN}	20	V
Switch Voltage	V_{SW}	20	V
Power Dissipation for HTSOP-J8	Pd1	3760 [*1]	mW
Power Dissipation for SOP-J8	Pd2	675 [*2]	mW
Operating Temperature Range	Topr	-40～+85	°C
Storage Temperature Range	Tstg	-55～+150	°C
Junction Temperature	Tjmax	150	°C
BST Voltage	V_{BST}	V_{SW}+7	V
EN Voltage	V_{EN}	20	V
All other pins	V_{OTH}	7	V

*1 Derating in done 30.08 mW/°C for operating above Ta≧25°C(Mount on 4-layer 70.0mm×70.0mm×1.6mm board)
*2 Derating in done 5.4 mW/°C for operating above Ta≧25°C(Mount on 1-layer 70.0mm×70.0mm×1.6mm board)

●Operation Range (Ta= -40～85°C)

Parameter	Symbol	Ratings			Unit
		Min	Typ	Max	
Supply Voltage	V_{IN}	4.75	12	18	V
SW Voltage	V_{SW}	-0.5	-	18	V
Output current for BD9325FJ	I_{SW2}	-	-	2**	A
Output current for BD9326EFJ	I_{SW3}	-	-	3**	A
Output current for BD9327EFJ	I_{SW4}	-	-	4**	A

** Pd, ASO should not be exceeded

●Electrical characteristics (Unless otherwise specified V_{IN}=12V Ta=25°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Error amplifier block						
FB input bias current	I_{FB}	-	0.1	2	µA	
Feedback voltage1	V_{FB1}	0.886	0.900	0.914	V	Voltage follower
Feedback voltage2	V_{FB2}	0.873	0.900	0.927	V	Ta=-40°C～85°C
SW block – SW						
Hi-side FET On-resistance for BD9325FJ	R_{ON2}	-	0.16	-	Ω	I_{SW}= -0.8A ***
Hi-side FET On-resistance for BD9326EFJ	R_{ON3}	-	0.12	-	Ω	I_{SW}= -0.8A ***
Hi-side FET On-resistance for BD9327EFJ	R_{ON4}	-	0.11	-	Ω	I_{SW}= -0.8A ***
Lo-side FET On-resistance	R_{ONL}	-	10	-	Ω	I_{SW}= 0.1A
Leak current N-channel	I_{LEAKN}	-	0	10	µA	V_{IN}= 18V, V_{SW} = 0V
Switch Current Limit for BD9325FJ	I_{LIMIT2}	2.5	-	-	A	***
Switch Current Limit for BD9326EFJ	I_{LIMIT3}	3.5	-	-	A	***
Switch Current Limit for BD9327EFJ	I_{LIMIT4}	4.5	-	-	A	***
Maximum duty cycle	M_{DUTY}	-	90	-	%	V_{FB}= 0V
General						
Enable Sink current	I_{EN}	86	181	275	µA	V_{EN}= 12V
Enable Threshold voltage	V_{EN}	1.1	1.18	1.4	V	
Under Voltage Lockout threshold	V_{UVLO}	4.05	4.40	4.75	V	V_{IN} rising
Under Voltage Lockout Hysteresis	V_{HYS}	-	0.1	-	V	
Soft Start Current	I_{SS}	23	41	62	uA	V_{SS}= 0 V
Soft Start Time	T_{SS}	-	1.6	-	ms	C_{SS}= 0.1 µF
Operating Frequency	F_{OSC}	300	380	460	kHz	
Circuit Current	I_{CC}	-	2.1	4.3	mA	V_{FB}= 1.5V, V_{EN}= 12V
Quiescent Current	I_{QUI}	-	80	170	µA	V_{EN}= 0V

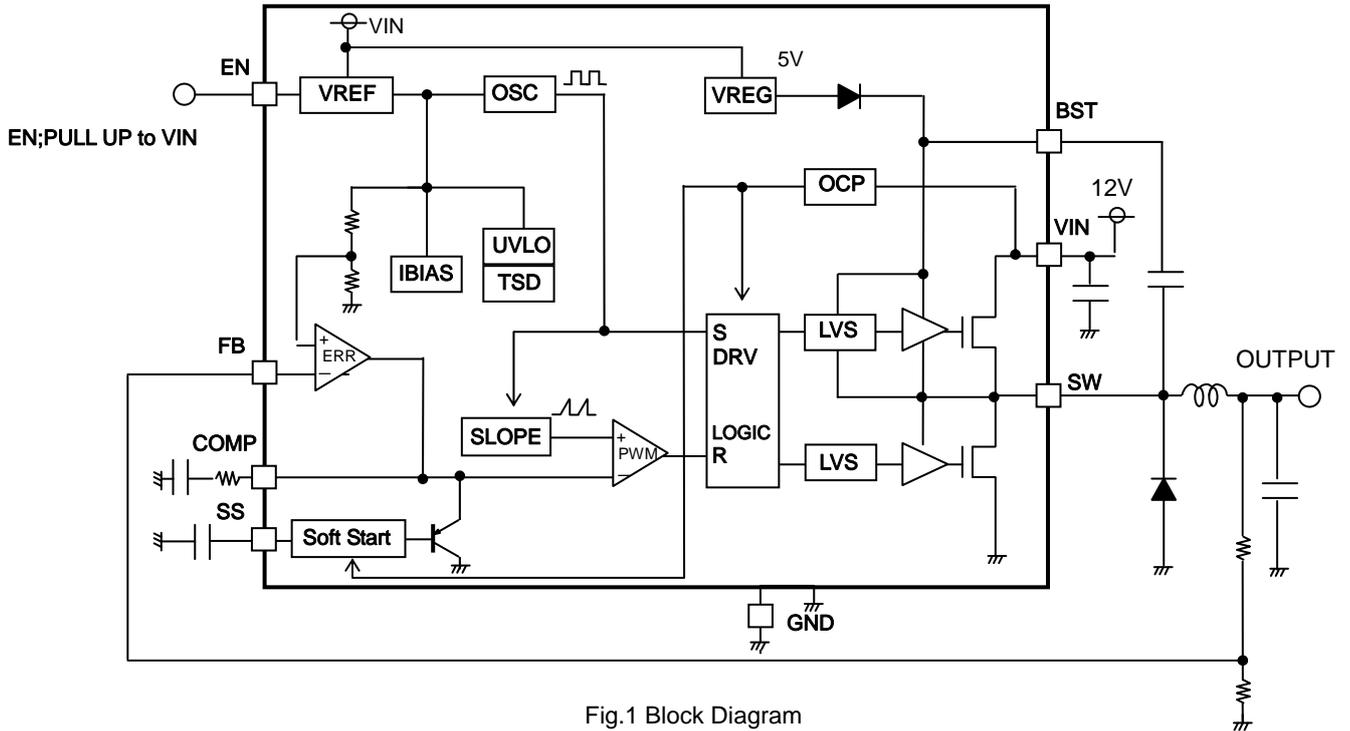*** See the series line-up table below.

● Block diagram
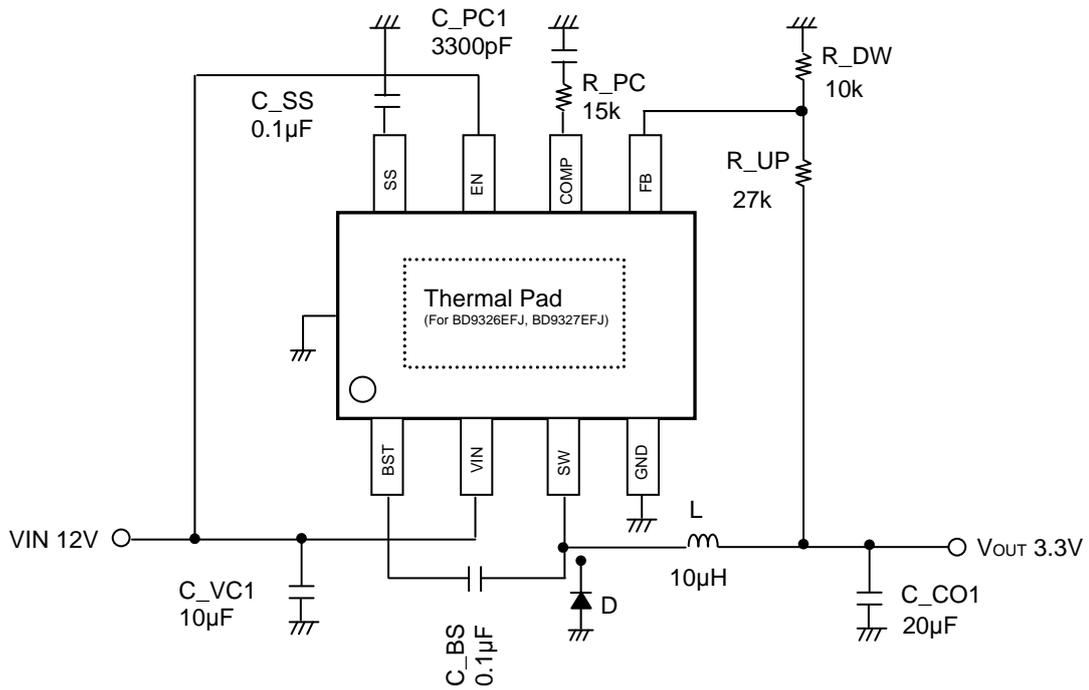

Fig.1 Block Diagram

● Typical application circuit

Fig.2 Application Circuit

●Block operation

・VREG
A block to generate constant-voltage for DC/DC boosting.

・VREF
A block that generates internal reference voltage of 2.9 V (Typ.).

・TSD/UVLO
TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) protection block. The TSD circuit shuts down IC at 175℃ (Typ.)
The UVLO circuit shuts down the IC when the VCC is Low Voltage.

・Error amp block (ERR)
This is the circuit to compare the reference voltage and the feedback voltage of output voltage. The COMP pin voltage
resulting from this comparison determines the switching duty. At the time of startup, since the soft start is operated by the
SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

・Oscillator block (OSC)
This block generates the oscillating frequency.

・SLOPE block
This block generates the triangular waveform from the clock created by OSC. Generated triangular waveform is sent to the
PWM comparator.

・PWM block
The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the
switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not
become 100%.

・DRV block
A DC/DC driver block. A signal from the PWM is input to drive the power FETs.

・Soft start circuit
Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the
output voltage overshoot or the rush current.

●Pin assignment and pin function

Pin No.	Pin name	Function
1	BST	High-Side Gate Drive Boost Input
2	VIN	Power Input
3	SW	Power Switching Output
4	GND	Ground
5	FB	Feed Back Input
6	COMP	Compensation Node
7	EN	Enable Input
8	SS	Soft Start Control Input

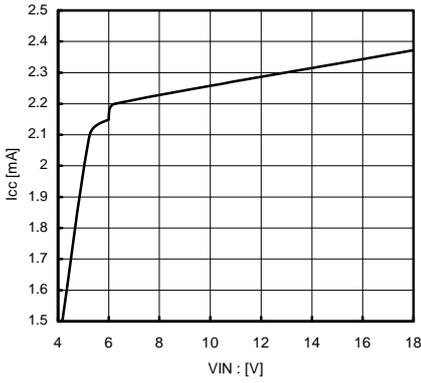●Typical performance characteristics (Unless otherwise specified, V_{IN}= 12V Ta = 25°C)

Fig.3 Circuit Current
(No switching)
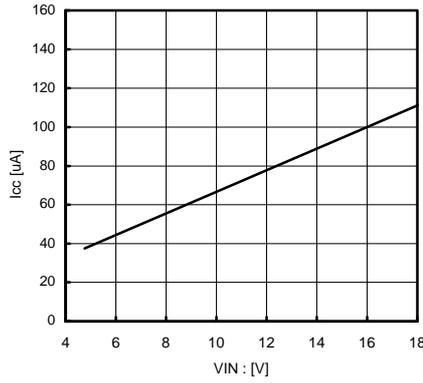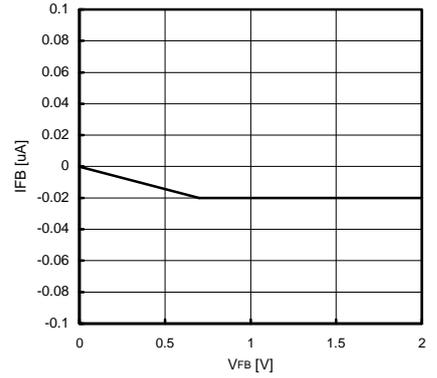
Fig.4 Quiescent Current
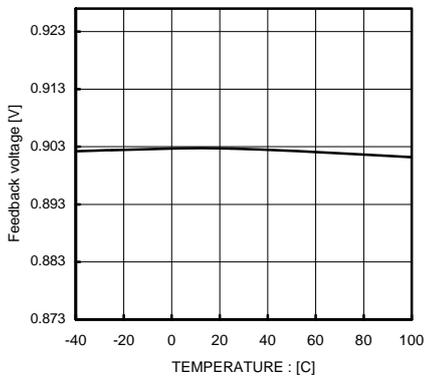(IC not active)

Fig.5 Input Bias Current

Fig.6 Feedback voltage

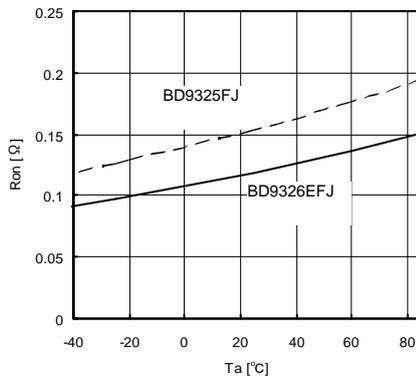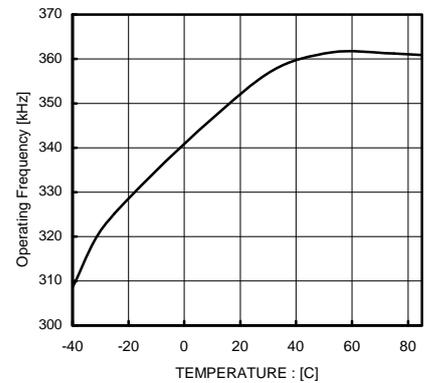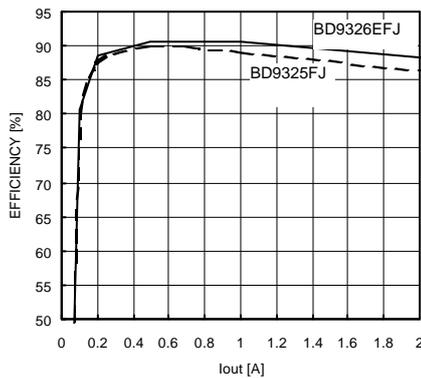Fig.7 Hi-Side On-resistance

Fig.8 Operating Frequency
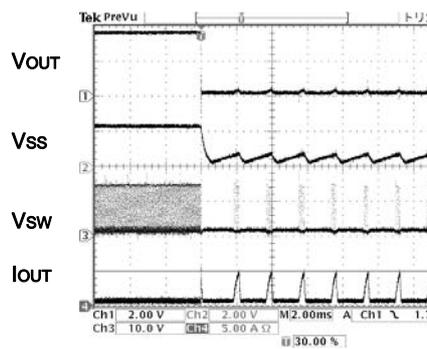
Fig.9 STEP Down Efficiency
(VIN= 12V VOUT= 3.3V L=10μH)

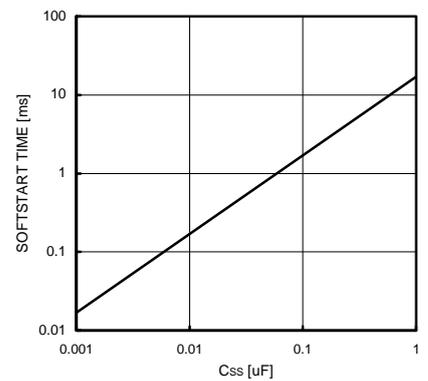Fig.10 OverCurrent Protection
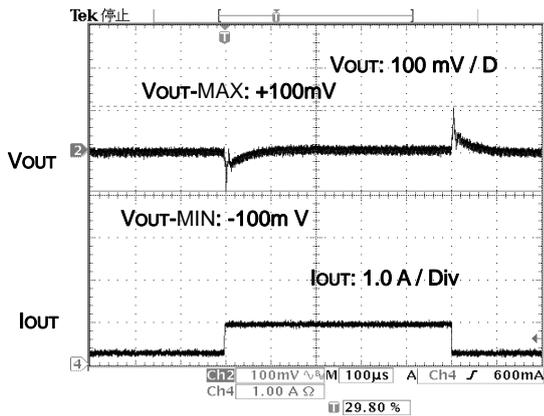(VOUT is shorted to GND)

Fig.11 Soft Start Time

Fig.12 Transient Response
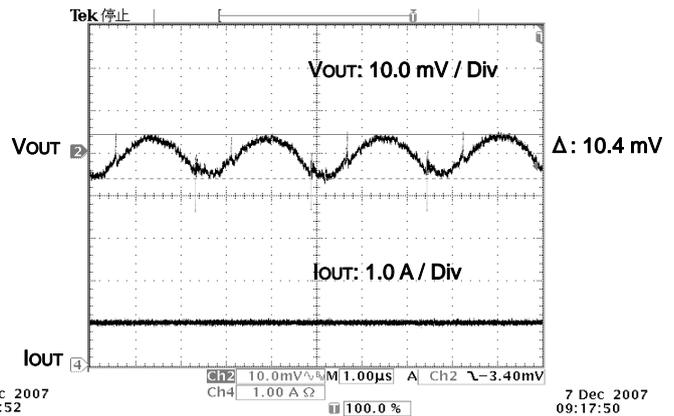(VIN= 12V VOUT= 3.3V L= 10µH Cout =22µF Iout= 0.2-1.0A)

Fig.13 Output Ripple Voltage
(VIN= 12V VOUT= 3.3V L= 10µH Cout =22µF I out= 1.0A)
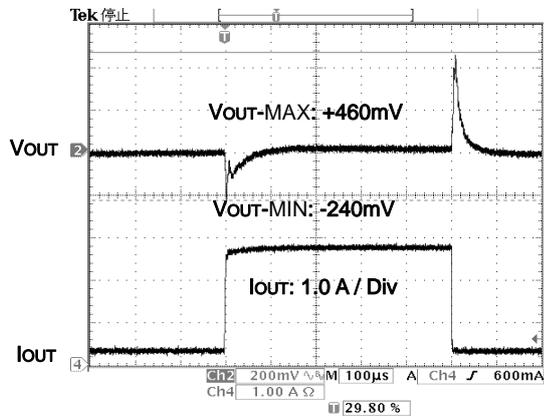

Fig.14 Transient Response
(VIN= 12V V$_{out}$= 3.3V L= 10µH Cout =22µF Iout= 0.2-3.0A)
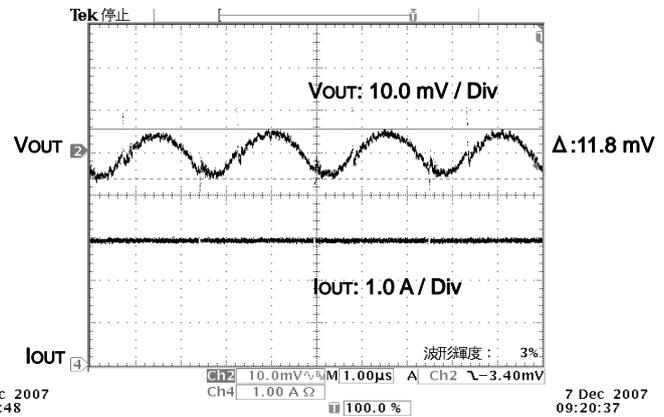

Fig.15 Output Ripple Voltage
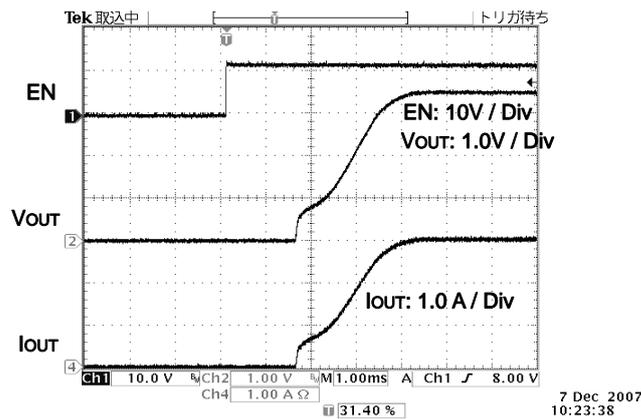(VIN= 12V VOUT= 3.3V L= 10µH Cout =22µF Iout= 3.0A)

Fig.16 Start Up waveform
(VIN= 12V VOUT= 3.3V L= 22µH CSS= 0.1µF Iout= 0A)

●Selecting application components

(1) Output LC constant (Buck Converter)
The inductance L to use for output is decided by the rated current ILR and input current maximum value IOMAX of the inductance.
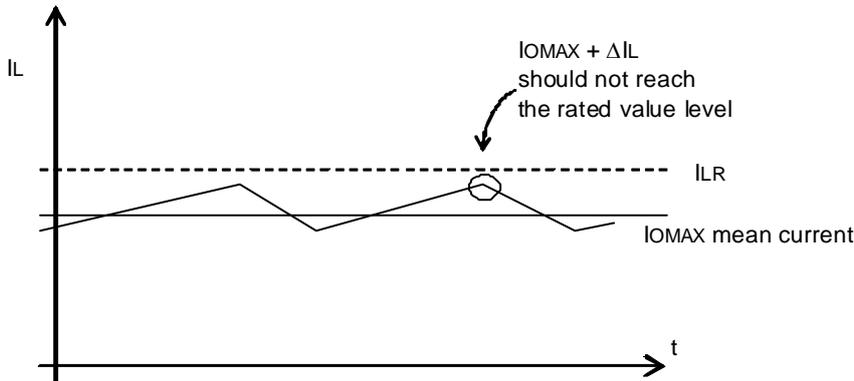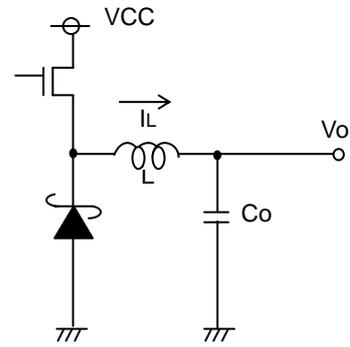

Fig.17

Fig.18

Adjust so that IOMAX + ΔIL does not reach the rated current value ILR. At this time, ΔIL can be obtained by the following equation.

$$\Delta IL = \frac{1}{L} \times (V_{CC} - V_o) \times \frac{V_o}{V_{CC}} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage V$_{PP}$ permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \Delta IL \times R_{ESR} + \frac{\Delta IL}{2Co} \times \frac{V_o}{V_{CC}} \times \frac{1}{f} \quad [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.
For the drop voltage VDR during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta IL}{Co} \times 10 \ \mu s \quad [V]$$

However, 10µs is the rough calculation value of the DC/DC response speed.
Make Co settings so that these two values will be within the limit values.

(2) Loop Compensation
   Choosing compensation capacitor C1 and resistor R3

   The example of DC/DC converter application bode plot is shown below. The compensation resistor R3 will set the cross over frequency FC that decides the stability and response speed of DC/DC converter. So compensation resistor R3 has to be adjusted to adequate value for good stability and response speed.

   The cross over frequency FC can be adjusted by changing the compensation resistor R3 connected to COMP terminal. The higher cross over frequency achieves good response speed, but less stability. And the lower cross over frequency shows good stability, but worse response speed.
   Usually, the 1/10 of DC/DC converter operating frequency is used for cross over frequency FC. So please decide the compensation resistor and capacitor using the following formula on setting FC to 1/10 of operating frequency at first.
   After that, please measure and adjust the cross over frequency on your set (on the actual application) to meet the enough response speed and phase-margin.

(i) Choosing phase compensation resistor R3

   Please decide the compensation resistor R3 on following formula.

   Compensation Resistor $R3 = 5800 \times C_{OUT} \times F_C \times V_{OUT}$ [Ω]

                                          Where
                                          C_{OUT} :   Output capacitor connected to DC/DC output
                                          V_{OUT} :   Output voltage
                                          F_C :   Desired cross over frequency (38kHz)

(ii) Choosing phase compensation capacitor C1

   The stability of DC/DC converter needs to cancel the phase delay that is from output LC filter by inserting the phase advance.
   The phase advance can be added by the zero on compensation resistor and capacitor.
   The LC resonant frequency FLC and the zero on compensation resistor and capacitor are expressed below.

   LC resonant frequency $F_{LC} = \dfrac{1}{2\pi\sqrt{LC_{OUT}}}$ [Hz]

   Zero by C1 and R3 $F_Z = \dfrac{1}{2\pi C_1 R_3}$ [Hz]

   Please choose C1 to make FZ to 1 / 3 of FLC .

   Compensation Capacitor $C_1 = \dfrac{3}{2\pi F_{LC} R_3}$ [F]

(iii) The condition of the loop compensation stability
   The stability of DC/DC converter is important. To secure the operating stability, please check the loop compensation has the enough phase-margin. For the condition of loop compensation stability, the phase-delay must be less than 150 degree where Gain is 0 dB. Namely over 30 degree phase-margin is needed.
   Lastly after the calculation above, please measure and adjust the phase-margin to secure over 30 degree.
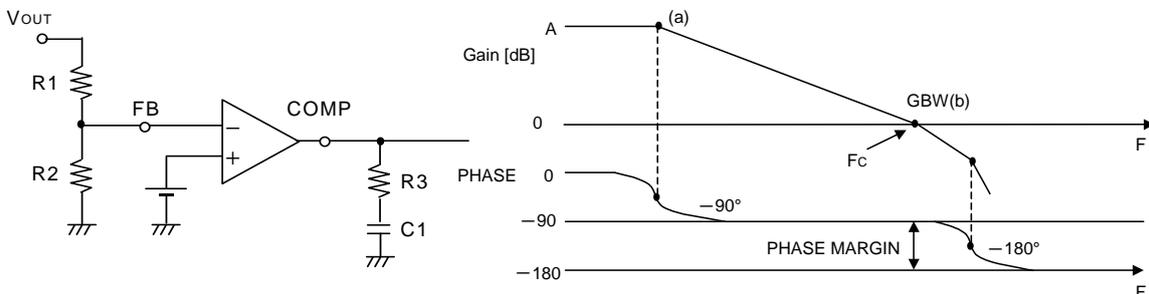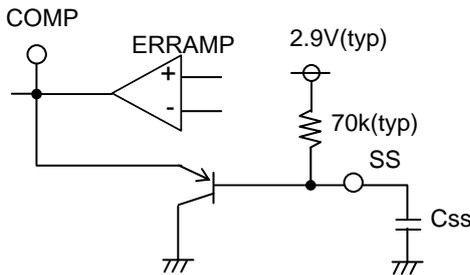
(3) Design of Feedback Resistance constant

Set the feedback resistance as shown below.
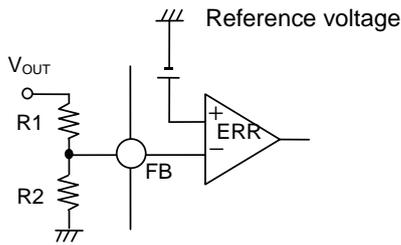
$$V_{OUT} = \frac{R1 + R2}{R2} \times \text{Reference Voltage} \quad [V]$$

● Soft Start Function

The buck converter has an adjustable Soft Start function to prevent high inrush current during start up.
The soft-start time is set by the external capacitor connected to SS pin.
The soft start time is given by;

$$T_{ss} \text{ [ms]} = 16.2 \cdot C \text{ [μF]}$$

Please confirm the overshoot of the output voltage and inrush current when deciding the SS capacitor value.
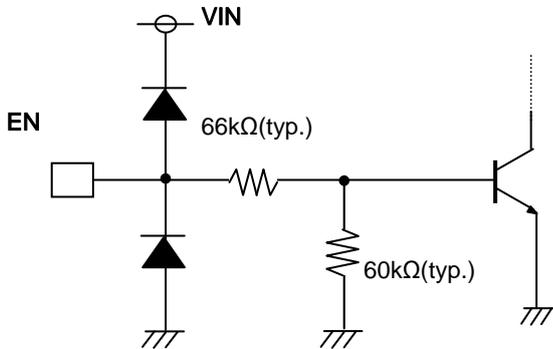
● EN Function

Fig.19 The equivalent internal circuit.

The EN terminal controls IC's shut down.
Leaving EN terminal open makes IC shutdown.
To start the IC, EN terminal should be connected to V_{IN} or the other power source output.
When the EN voltage exceed 1.2V (typ.), the IC start operating.

●Layout Pattern Consideration

Two high pulsing current flowing loops exist in the buck regulator system.

The first loop, when FET is ON, starts from the input capacitors, to the VIN terminal, to the SW terminal, to the inductor, to the output capacitors, and then returns to the input capacitor through GND.

The second loop, when FET is OFF, starts from the shotkey diode, to the inductor, to the output capacitor, and then returns to the shotkey diode through GND.

To reduce the noise and improve the efficiency, please minimize these two loop area.

Especially input capacitor, output capacitor and shotkey diode should be connected to GND plain.

PCB Layout may affect the thermal performance, noise and efficiency greatly. So please take extra care when designing PCB Layout patterns.
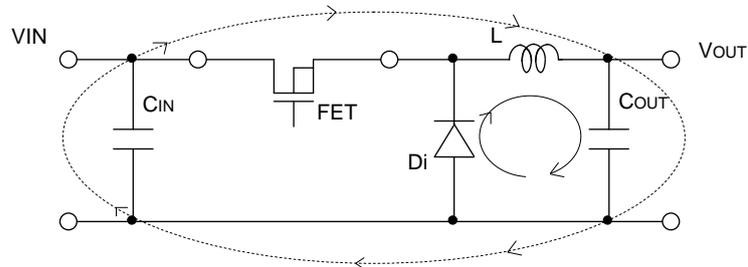
Fig.20 Current loop in Buck regulator system

・The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective.

・The input capacitors should be connected as close as possible to the VIN terminal.

・Keep sensitive signal traces such as trace connected FB and COMP away from SW pin.

・The inductor, the shot key diode and the output capacitors should be placed close to SW pin as much as possible.

Fig.21 The example of PCB layout pattern

●**Operation Notes**

1) Absolute maximum ratings
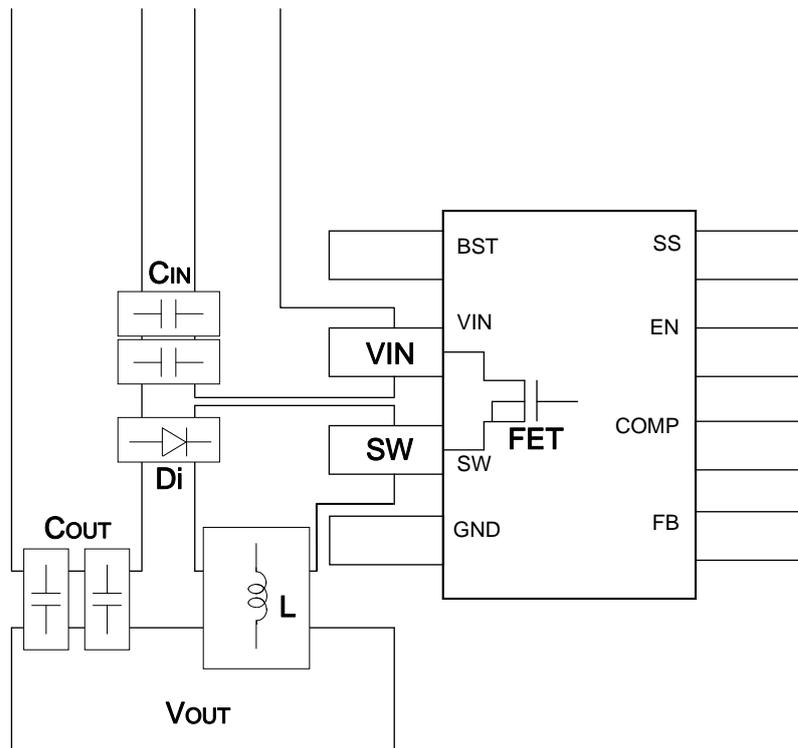Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when the resistors and transistors are connected to the pins as shown in Fig.22 , a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.
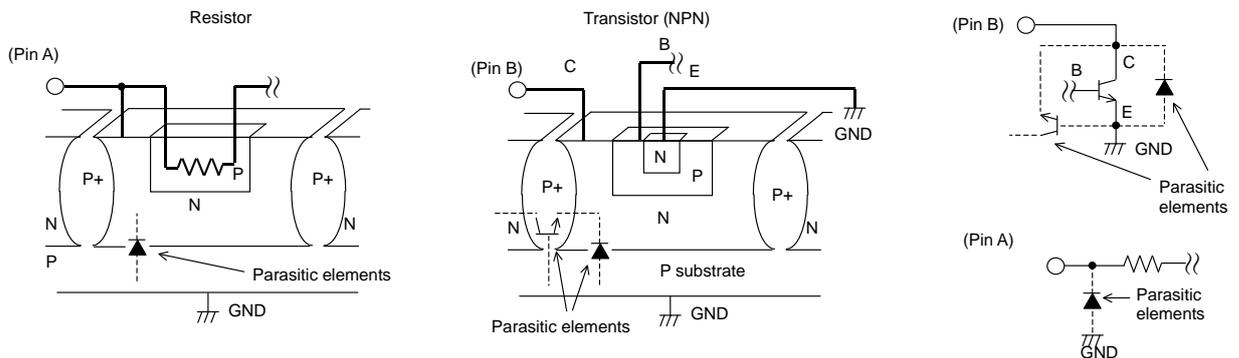

Fig.22   Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits
An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)
   This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the
   IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards
   At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

●I/O Equivalent Circuit Diagram
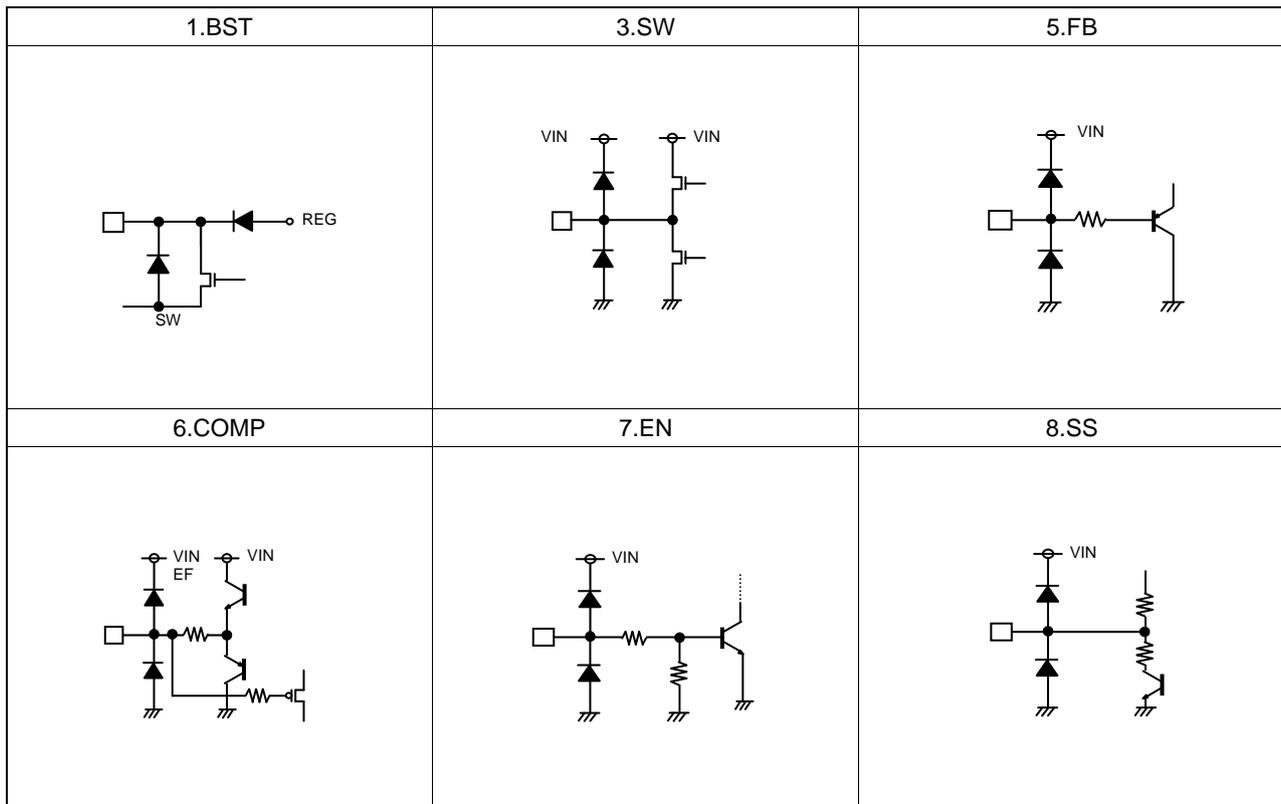
●Power Dissipation
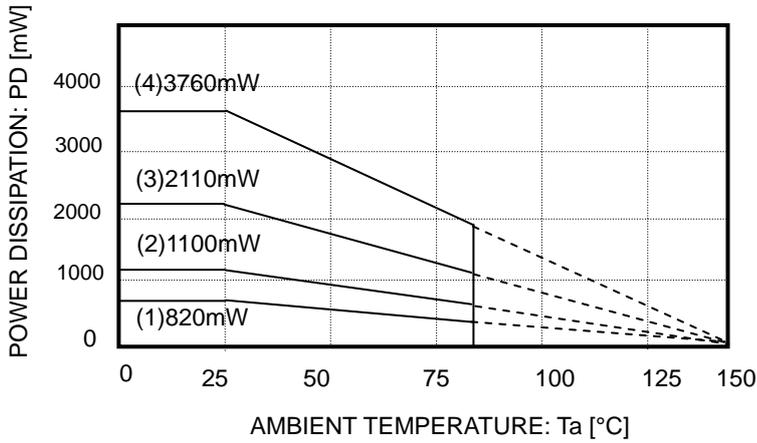
HTSOP-J8 Package
On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)
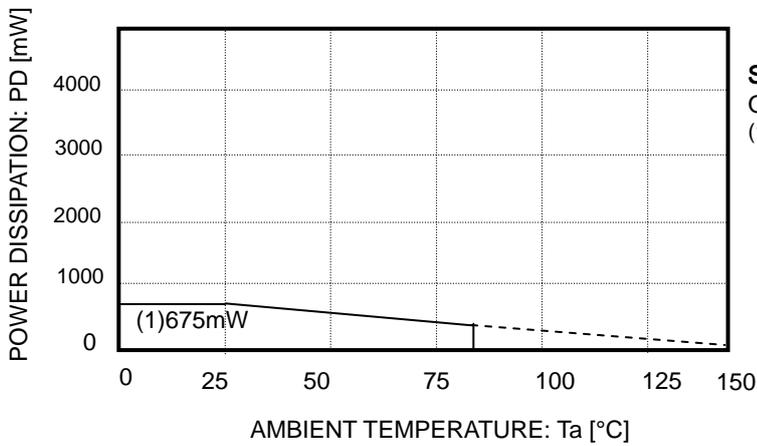

SOP-J8 Package
On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)

●Ordering part number

| B | D | | 9 | 3 | 2 | 5 | | F | J | - | E | 2 |

Part No.

Part No.
9325
9326
9327

Package
FJ   : SOP-J8
EFJ : HTSOP-J8

Packaging and forming specification
E2: Embossed tape and reel

SOP-J8

4.9±0.2
(MAX 5.25 include BURR)

4° +6° −4°

0.45MIN

6.0±0.3
3.9±0.2

0.545

0.2±0.1

S

1.375±0.1
0.175
1.27
0.42±0.1
0.1 S

(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel

1pin

Direction of feed

＊Order quantity needs to be multiple of the minimum quantity.

HTSOP-J8

4.9±0.1
(MAX 5.25 include BURR)

(3.2)

4° +6° −4°

6.0±0.2
3.9±0.1

(2.4)

0.65±0.15
1.05±0.2

0.545

1PIN MARK

0.17 +0.05 −0.03

S

1.0MAX
0.85±0.05
0.08±0.08
1.27
0.42 +0.05 −0.04   ⊕ 0.08 Ⓜ
0.08 S

(Unit : mm)
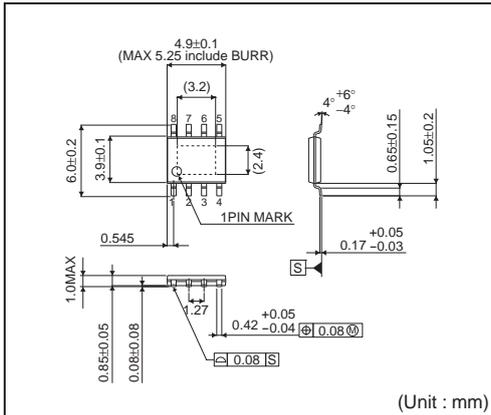
<Tape and Reel information>

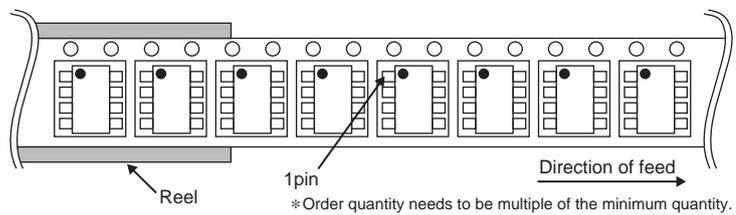| Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel

1pin

Direction of feed

＊Order quantity needs to be multiple of the minimum quantity.

N o t e s

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