TDF8599B

I2C-bus controlled dual channel 43 W/2 Ohm, single channel 85 W/1 Ohm class-D power amplifier with load diagnostics

Rev. 2 — 23 August 2016 **Product data sheet**

1 General description

The TDF8599B is a dual Bridge-Tied Load (BTL) car audio amplifier comprising an NDMOST-NDMOST output stage based on SOI BCDMOS technology. Low power dissipation enables the TDF8599B high-efficiency, class-D amplifier to be used with a smaller heat sink than those normally used with standard class-AB amplifiers.

The TDF8599B can operate in either non-I^{2}C-bus mode or I^{2}C-bus mode. When in I^{2}C-bus mode, DC load detection results and fault conditions can be easily read back from the device. Up to 15 I^{2}C-bus addresses can be selected depending on the value of the external resistor connected to pins ADS and MOD.

When pin ADS is short circuited to ground, the TDF8599B operates in non-I^{2}C-bus mode. Switching between Operating mode and Mute mode in non-I^{2}C-bus mode is only possible using pins EN and SEL_MUTE.
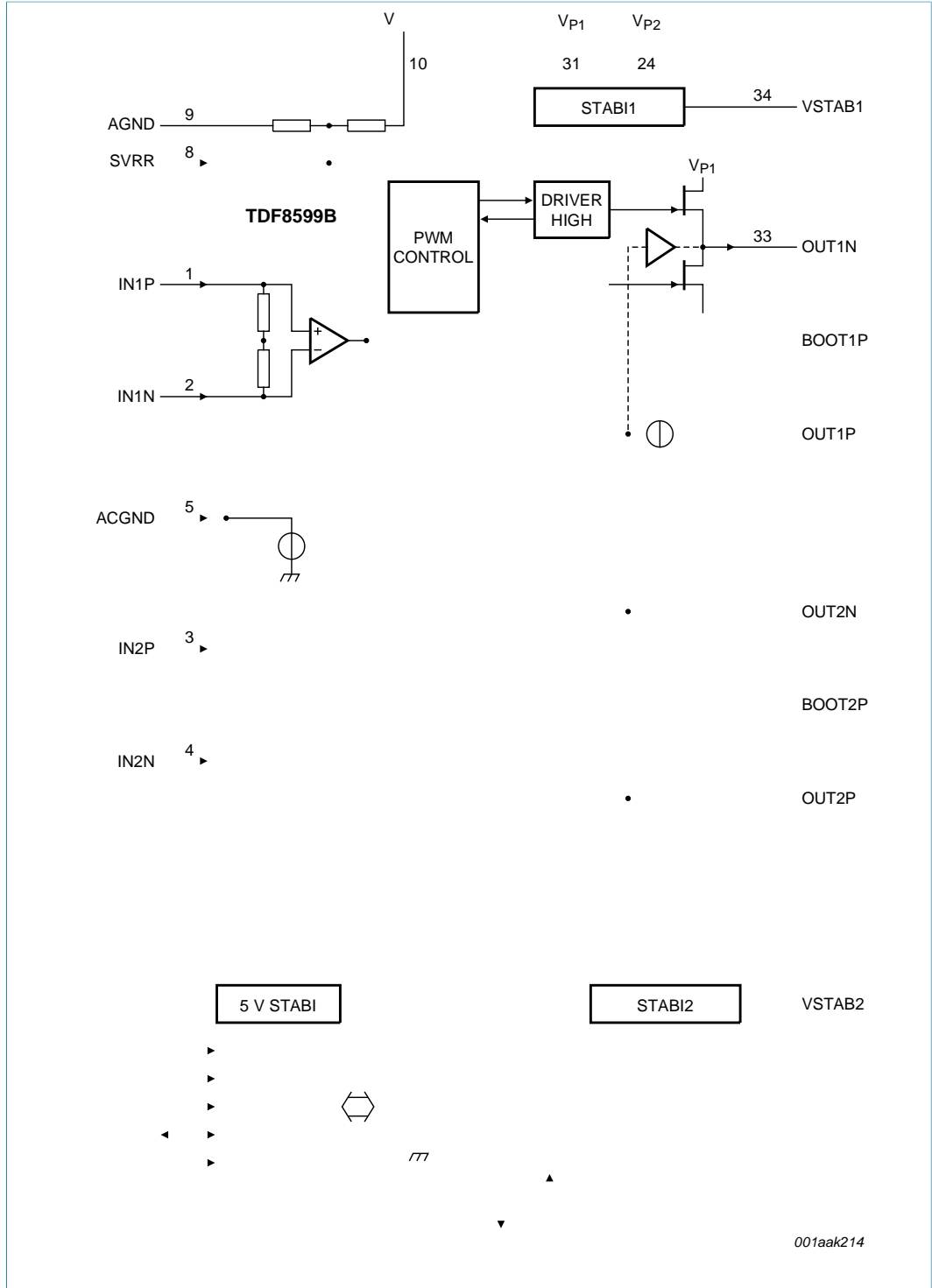
2 Features

- High-efficiency
- Low quiescent current
- Operating voltage from 8 V to 24 V
- Two 4 /2 capable BTL channels or one 1 capable BTL channel
- Differential inputs
- I^{2}C-bus mode with 15 I^{2}C-bus addresses or non-I^{2}C-bus mode operation
- Clip detect
- Independent short circuit protection for each channel
- Advanced short circuit protection for load, GND and supply
- Load dump protection
- Thermal foldback and thermal protection
- DC offset protection
- Selectable AD or BD modulation
- Parallel channel mode for high-current drive capability
- Advanced clocking:
  - Switchable oscillator clock source: internal for Master mode or external for Slave mode
  - Spread spectrum mode
  - Phase staggering
  - Frequency hopping
- No 'pop noise' caused by DC output offset voltage
- I^{2}C-bus mode:
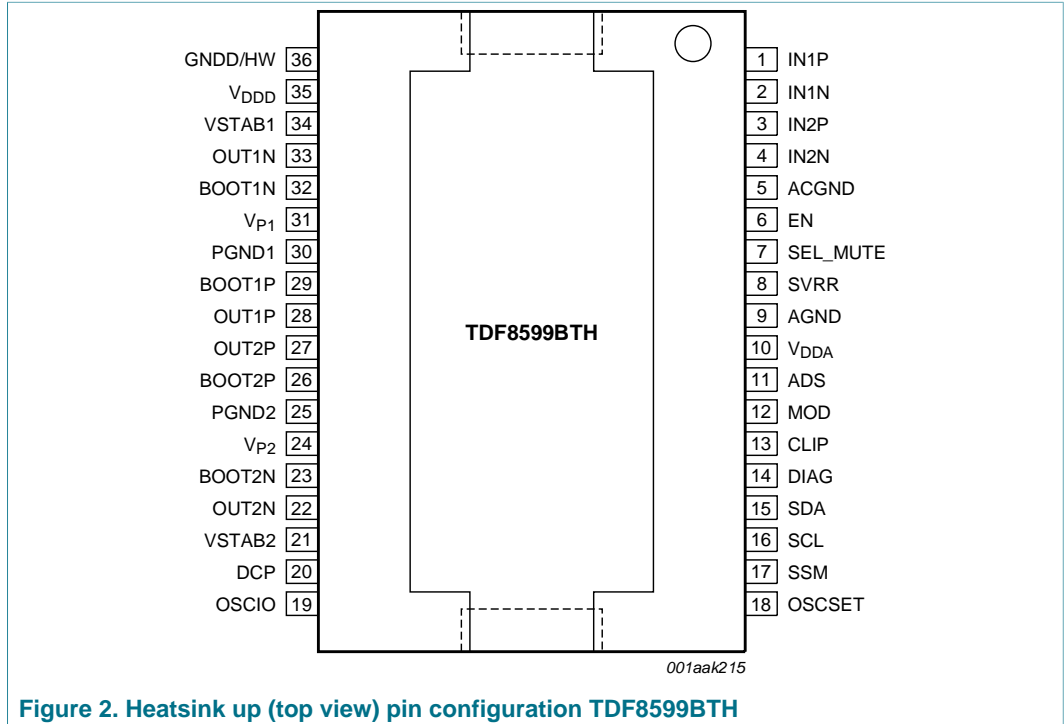 - DC load detection
  - AC load detection

6 Block diagram

001aak214

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

3 / 54

7 Pinning information

7.1 Pinning

Figure 2. Heatsink up (top view) pin configuration TDF8599BTH

7.2 Pin description

Table 3. Table 3. Pin description

Symbol	Pin	Type[1]	Description
IN1P	1	I	channel 1 positive audio input
IN1N	2	I	channel 1 negative audio input
IN2P	3	I	channel 2 positive audio input
IN2N	4	I	channel 2 negative audio input
ACGND	5	I	decoupling for input reference voltage
EN	6	I	enable input: non-I^2C-bus mode: switch between off and Mute mode I^2C-bus mode: off and Standby mode
SEL_MUTE	7	I	select mute or unmute
SVRR	8	I	decoupling for internal half supply reference voltage
AGND	9	G	analog supply ground
V_{DDA}	10	P	analog supply voltage
ADS	11	I	non-I^2C-bus mode: connected to ground I^2C-bus mode: selection and address selection pin

TDF8599B

Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 2 — 23 August 2016

© NXP Semiconductors N.V. 2016. All rights reserved.

4 / 54

Symbol	Pin	Type[1]	Description
MOD	12	I	modulation mode, phase shift and parallel mode select
CLIP	13	O	clip output; open-drain
DIAG	14	O	diagnostic output; open-drain
SDA	15	I/O	I^{2}C-bus data input and output
SCL	16	I	I^{2}C-bus clock input

TDF8599B

Product data sheet　　　　　　　　　　**Rev. 2 — 23 August 2016**

5 / 54

circuits for both high-side and low-side enabling the DMOS power output transistors to be driven. An external 2nd order low-pass filter converts the PWM signal into an analog audio signal across the loudspeakers.

The TDF8599B includes integrated common circuits for all channels such as the oscillator, all reference sources, mode functionality and a digital timing manager. In addition, the built-in protection includes thermal foldback, temperature, overcurrent and overvoltage (load dump).

The TDF8599B operates in either I^2C-bus mode or non-I^2C-bus mode. In I^2C-bus mode, DC load detection, frequency hopping and extended configuration functions are provided together with enhanced diagnostic information.

8.2 Mode selection

The mode pins EN, ADS and SEL_MUTE enable mute state, I^2C-bus mode and Operating mode switching.

Pin SEL_MUTE is used to mute and unmute the device and must be connected to an external capacitor (C_{ON}). This capacitor generates a time constant which is used to ensure smooth fade-in and fade-out of the input signal.

The TDF8599B is enabled when pin EN is HIGH. When pin EN is LOW, the TDF8599B is off and the supply current is at its lowest value (typically 2 µA). When off, the TDF8599B is completely deactivated and will not react to I^2C-bus commands.

I^2C-bus mode is selected by connecting a resistor between pins ADS and AGND. In I^2C-bus mode with pin EN HIGH, the TDF8599B waits for further commands (see Table 4). I^2C-bus mode is described in Section 9.

Non-I^2C-bus mode is selected by connecting pin ADS to pin AGND. In non-I^2C-bus mode, the default TDF8599B state is Mute mode. The amplifiers switch idle (50 % duty cycle) and the audio signal is suppressed at the output. In addition, the capacitor (C_{SVRR}) is charged to half the supply voltage. To enter Operating mode, pin SEL_MUTE must be HIGH with S1 open, enabling capacitor (C_{ON}) charged by an internal pull-up (see Figure 3). In addition, pin EN must be driven HIGH.

Figure 3. Mode selection
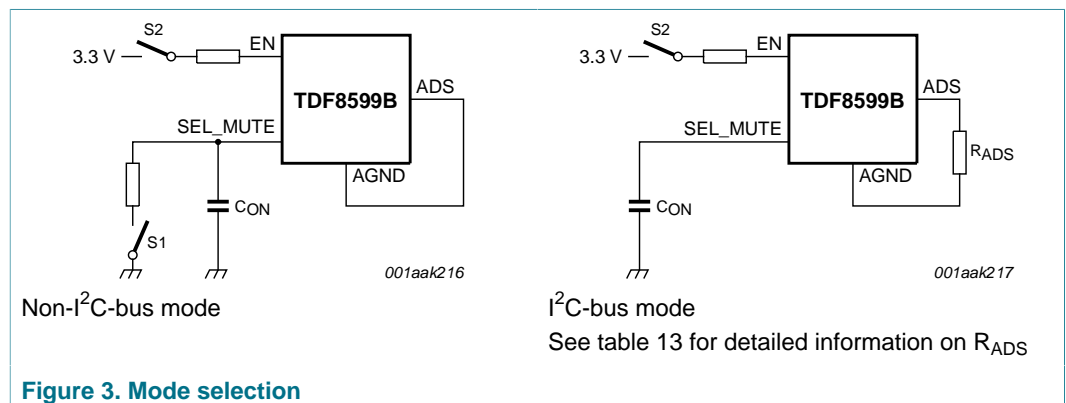
I^2C-bus mode and non-I2C-bus mode control are described in Table 4 and Table 5. Switches S1 and S2 are shown in Figure 3.

TDF8599B

Product data sheet **Rev. 2 — 23 August 2016**

6 / 54

Table 4. I^{2}C-bus mode operation

Pin EN	Pin SEL_MUTE

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

7 / 54

Table 6. Mode setting pin OSCIO

Mode	Settings	
	Pin OSCSET	**Pin OSCIO**
Master	R_{osc} > 26 k	output
Slave	R_{osc} = 0 ; shorted to pin AGND	input

The value of the resistor R_{osc} sets the clock frequency based on equation1:

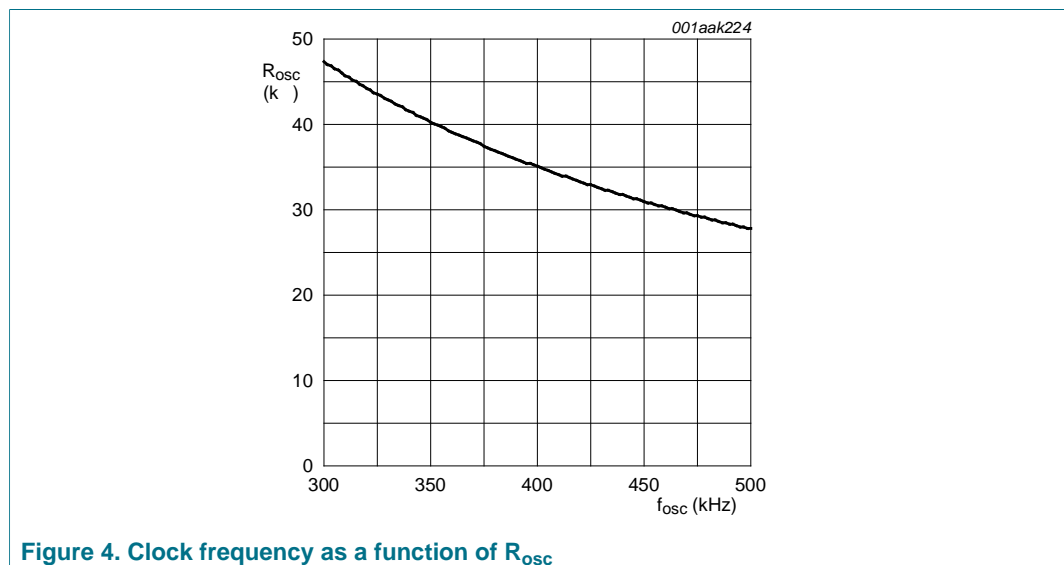$$f_{osc} = \frac{12.45 \times 10^9}{R_{osc}} \; Hz \tag{1}$$

001aak224

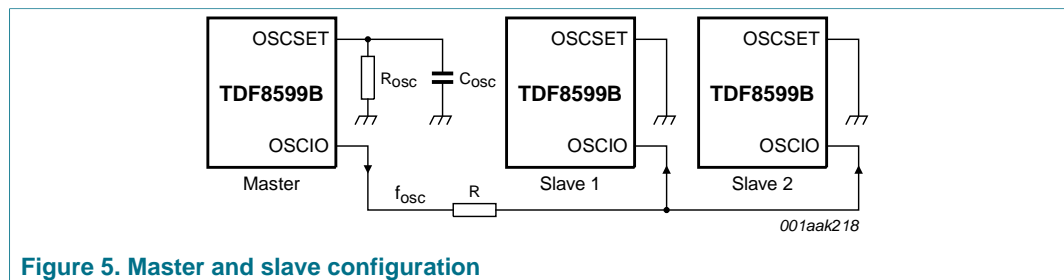**Figure 4. Clock frequency as a function of R$_{osc}$**

001aak218

Figure 5. Master and slave configuration

In Master mode, Spread spectrum mode and frequency hopping can be enabled. In Slave mode, phase staggering and phase lock operation can be selected. An external clock can be used as the master-clock on pin OSCIO of the slave devices. When using an external clock, it must remain active during the shutdown sequence to ensure that all devices are switched off and able to enter the off state as described in Section 8.2.

In Slave mode, an internal watchdog timer on pin OSCIO is triggered when the TDF8599B is switched off by pulling down pin EN. If the external clock fails, the watchdog timer forces the TDF8599B to switch off.

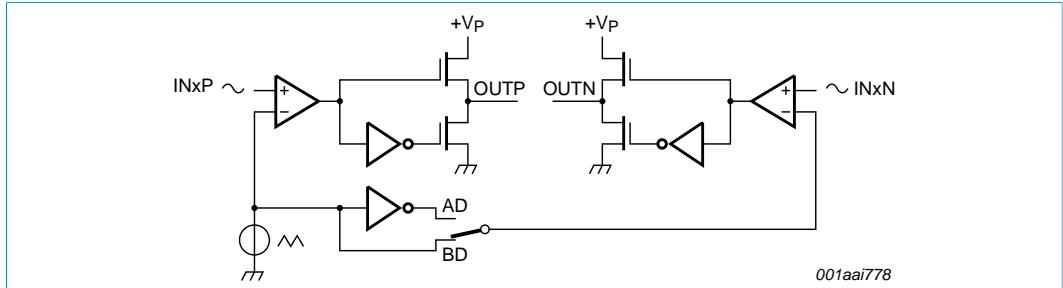| OSCSET pin	OSCIO pin	SSM pin	Oscillator modes
$R_{osc} = 0$	input	C_{PLL} + R_{PLL} to pin AGND	slave, PLL enabled
$R_{osc} = 0$	input	shorted to pin AGND	slave, PLL disabled

8.4 Operation mode selection

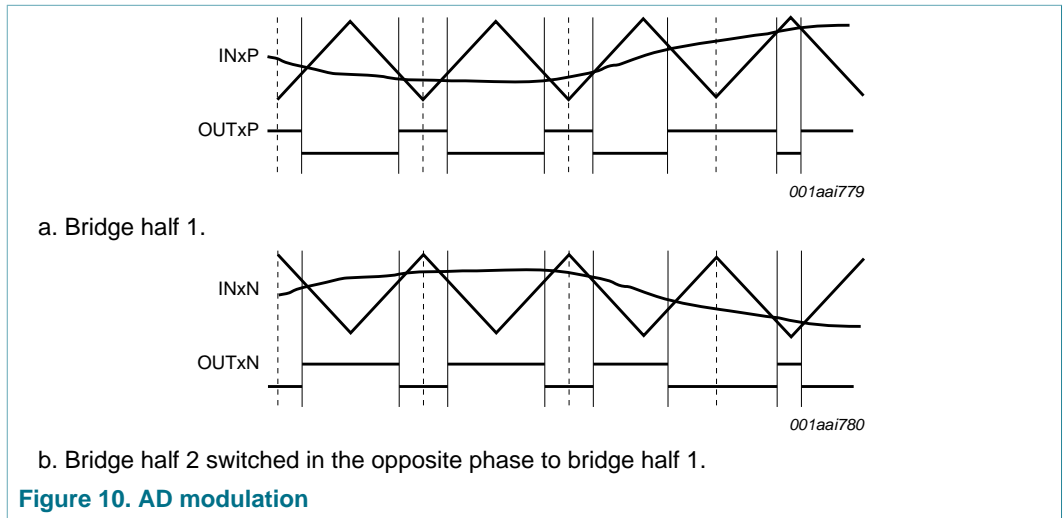*001aai778*

Figure 9. AD/BD modulation switching circuit
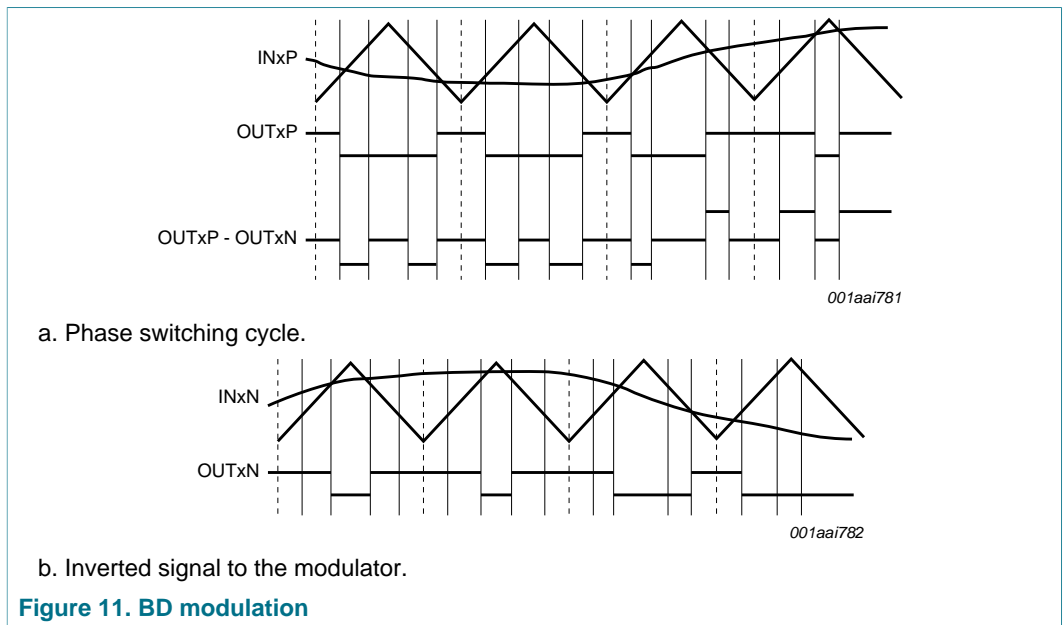
001aai779

a. Bridge half 1.

001aai780

b. Bridge half 2 switched in the opposite phase to bridge half 1.

Figure 10. AD modulation

001aai781

a. Phase switching cycle.

001aai782

b. Inverted signal to the modulator.

Figure 11. BD modulation

TDF8599B

All information provided in this document is subject to legal disclaimers.

8.5 Protection

The TDF8599B includes a range of built-in protection functions. How the TDF8599B manages the various possible fault conditions for each protection is described in the following sections:

Table 9. Overview of protection types

Protection type	Reference
Thermal foldback	Section 8.5.1
Overtemperature	Section 8.5.2
Overcurrent	Section 8.5.3
Window	Section 8.5.4
DC Offset	Section 8.5.5
Undervoltage	Section 8.5.6
Overvoltage	Section 8.5.6

8.5.1 Thermal foldback

Thermal Foldback Protection (TFP) is activated when the average junction temperature exceeds the threshold level (145 °C). TFP decreases amplifier gain such that the combination of power dissipation and $R_{th(j-a)}$ create a junction temperature around the threshold level. The device will not completely switch off but remains operational at the lower output power levels. If the average junction temperature continues to increase, a second built-in temperature protection threshold level shuts down the amplifier completely.

8.5.2 Overtemperature protection

If the average junction temperature T_j > 160 °C, OverTemperature Protection (OTP) is activated and the power stage shuts down immediately.

8.5.3 Overcurrent protection

OverCurrent Protection (OCP) is activated when the output current exceeds the maximum output current of 8 A. OCP regulates the output voltage such that the maximum output current is limited to 8 A. The amplifier outputs keep switching and the amplifier is NOT shutdown completely. This is called current limiting.

OCP also detects when the loudspeaker terminals are short circuited or one of the amplifier's demodulated outputs is short circuited to one of the supply lines. In either case, the shorted channel(s) are switched off.

The amplifier can distinguish between loudspeaker impedance drops and a low-ohmic short across the load or one of the supply lines. This impedance threshold depends on the supply voltage used. When a short is made across the load causing the impedance to drop below the threshold level, the shorted channel(s) are switched off. They try to restart every 50 ms. If the short circuit condition is still present after 50 ms, the cycle repeats. The average power dissipation will be low because of this reduced duty cycle.

When a channel is switched off due to a short circuit on one of the supply lines, Window Protection (WP) is activated. WP ensures the amplifier does not start-up after 50 ms until the supply line short circuit is removed.

8.5.4 Window protection

Window Protection (WP) checks the PWM output voltage before switching from Standby mode to Mute mode (with both outputs switching) and is activated as follows:

- During the start-up sequence:
  - When the TDF8599B is switched from standby to mute ($t_{d(stb-mute)}$). When a short circuit on one of the output terminals (i.e. between V_P or GND) is detected, the start-up procedure is interrupted and the TDF8599B waits for open circuit outputs. No large currents flow in the event of a short circuit to the supply lines because the check is performed before the power stages are enabled.
- During operation:
  - A short to one of the supply lines activates OCP causing the amplifier channel to shutdown. After 50 ms the amplifier channel restarts and WP is activated. However, the corresponding amplifier channel will not start-up until the supply line short circuit has been removed.

8.5.5 DC offset protection

DC offset Protection (DCP) is activated when the DC content in the demodulated output voltage exceeds a set threshold (typically 2 V). DCP is active in both Mute mode and Operating mode. Figure 14 shows how false triggering of the DCP by low frequencies in the audio signal is prevented using the external capacitor (C_F) to generate a cut-off frequency.
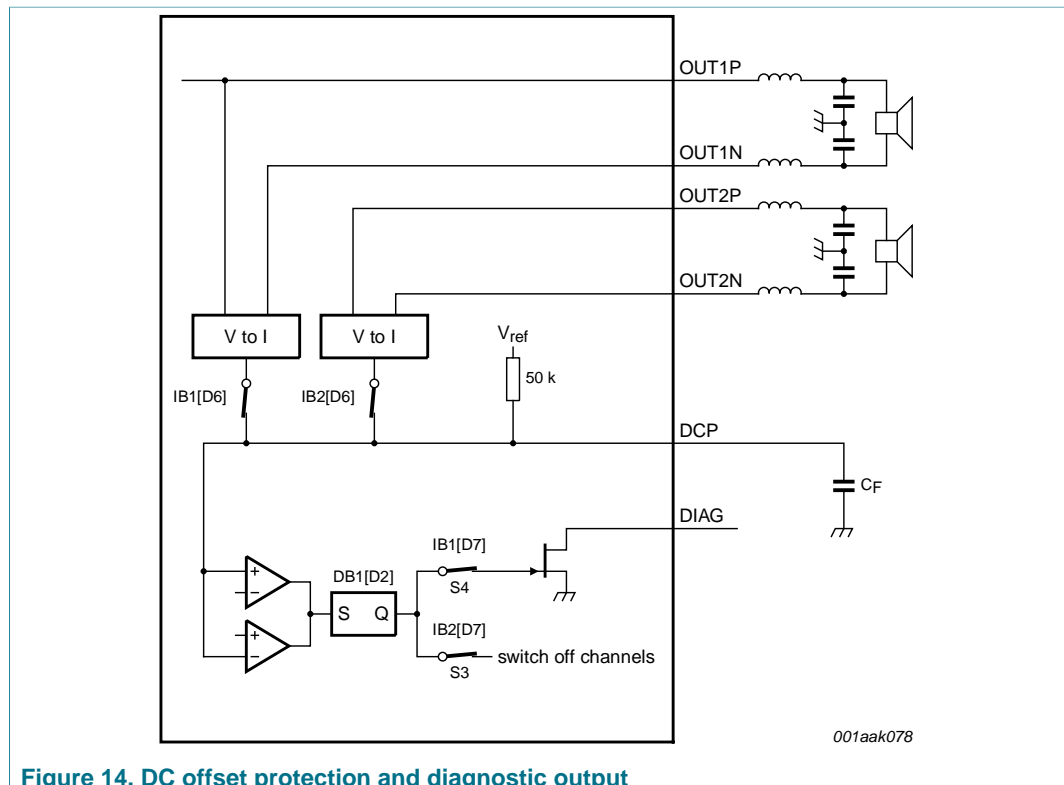

Figure 14. DC offset protection and diagnostic output

TDF8599B

Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 2 — 23 August 2016

© NXP Semiconductors N.V. 2016. All rights reserved.

16 /

8.6 Diagnostic output

8.6.1 Diagnostic table

The diagnostic information for I^{2}C-bus mode and non-I^{2}C-bus mode is shown in Table 11. The instruction bitmap and data bytes are described in Table 14 and Table 15.

Pins DIAG and CLIP have an open-drain output which must have an external pull-up resistor connected to an external voltage. Pins CLIP and DIAG can show both fixed and I^{2}C-bus selectable information.

Pin DIAG goes LOW when a short circuit to one of the amplifier outputs occurs. The microprocessor reads the failure information using the I^{2}C-bus. The I^{2}C-bus bits are set for a short circuit. These bits can be reset with the I^{2}C-bus read command.
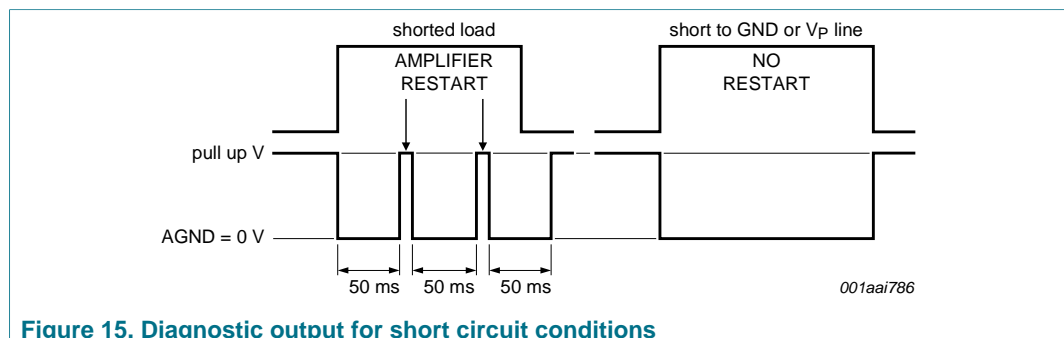
Even after the short has been removed, the microprocessor knows what was wrong after reading the I^{2}C-bus. Old information is read when a single I^{2}C-bus read command is used. To read the current information, two read commands must be sent, one after another.

When selected, pin DIAG gives the current diagnostic information. Pin DIAG is released instantly when the failure is removed, independent of the I^{2}C-bus latches.

Table 11. Available data on pins DIAG and CLIP

Diagnostic	I^{2}C-bus mode		Non-I^{2}C-bus mode	
	Pin DIAG	**Pin CLIP**	**Pin DIAG**	**Pin CLIP**
Power-on reset	yes	yes	yes	yes
UVP or OVP	yes	no	yes	no
Clip detection	no	selectable	no	yes
Temperature pre-warning	no	selectable	no	yes
OCP/WP	yes	no	yes	no
DCP	selectable	no	yes	no
OTP	yes	no	yes	no

When OCP is triggered, the open-drain DIAG output is activated. The diagnostic output signal during different short circuit conditions is illustrated in Figure 15.

Figure 15. Diagnostic output for short circuit conditions

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

17 / 54

8.6.2 Load identification (I²C-bus mode only)

8.6.2.1 DC load detection

DC load detection is only available in I²C-bus mode and is controlled using bit IB2[D2]. The default setting is logic 0 for bit IB2[D2] which disables DC load detection. DC load detection is enabled when bit IB2[D2] = 1. Load detection takes place before the class-D amplifier output stage starts switching in Mute mode and the start-up time from Standby mode to Mute mode is increased by $t_{det(DCload)}$ (see Figure 16).

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

18 / 54
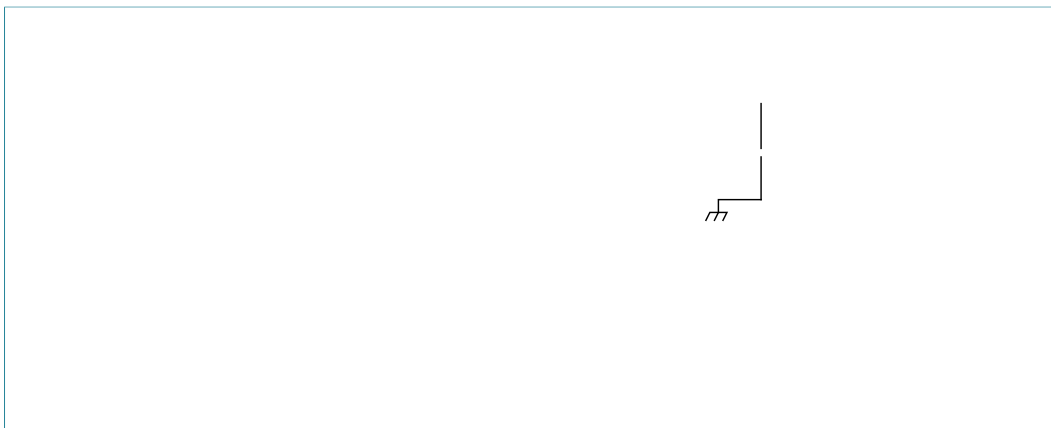
Table 12. Interpretation of DC load detection bits

DC load bits DB1[D4] and DB2[D4]	OCP bits DB1[D3] and DB2[D3]	Description
0	0	speaker load
0	1	shorted load
1	0	open load

Remark: After DC load detection has been performed, the DC load valid bit DB1[D6] must be set. The DC load data bits are only valid when bit DB1[D6] = 1. When DC load detection is interrupted by a sudden large change in supply voltage (triggered by UVP or OVP) or if the amplifier hangs up, the DC load valid bit is reset to DB1[D6] = 0. The DC load detection enable bit IB2[D2] must be reset after the DC load protection cycle to release any amplifier hang-up. Once the DC load detection cycle has finished, DC load detection can be restarted by toggling the DC load detection enable bit IB2[D2]. However, this can only be used if both amplifier channels have not been enabled with bit IB1[D1] or bit IB2[D1]. See Section 8.6.2.2 "Recommended start-up sequence with DC load detection enabled"Section 8.6.2.2 for detailed information.

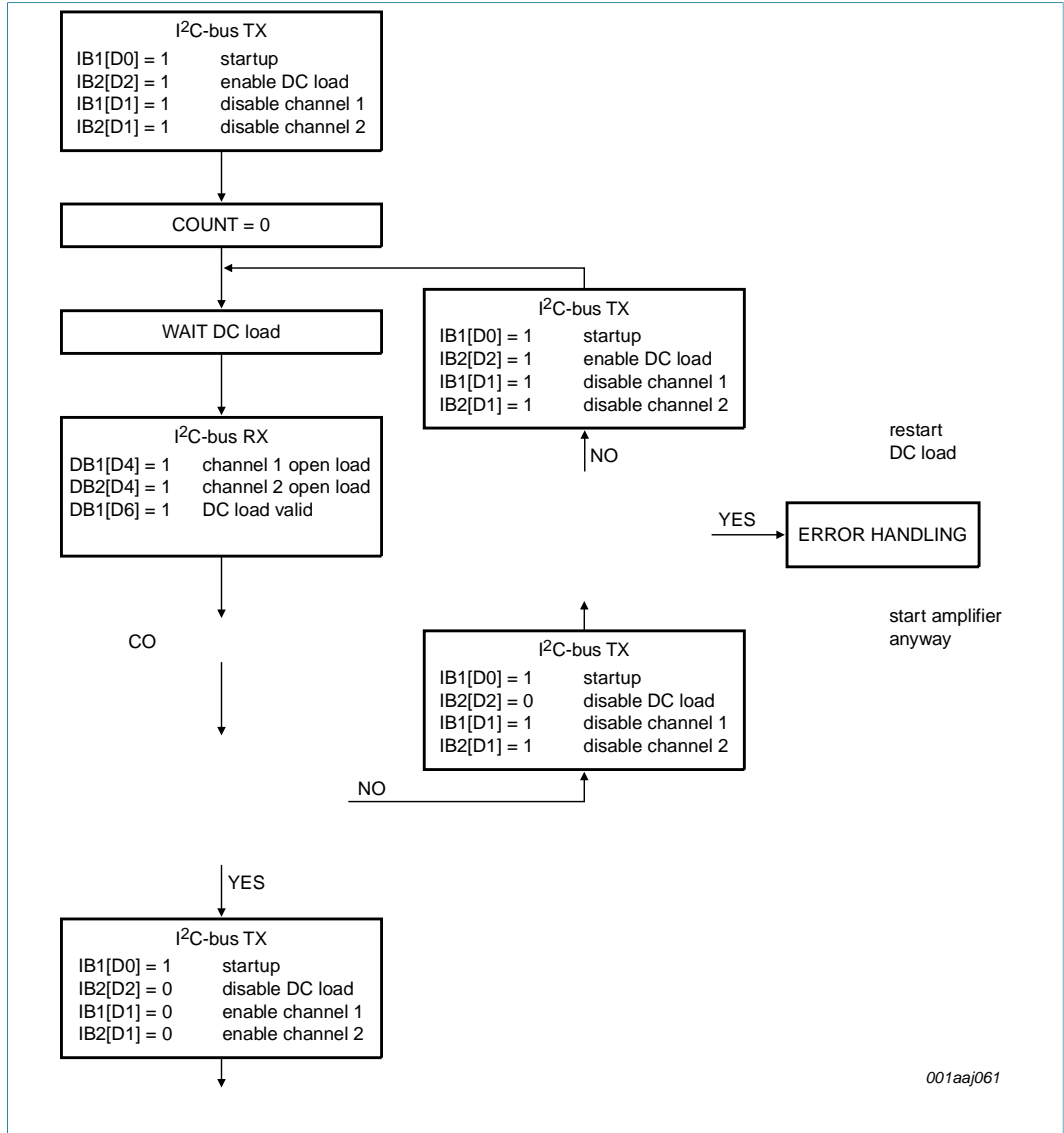### 8.6.2.2 Recommended start-up sequence with DC load detection enabled

The flow diagram (Figure 19) illustrates the TDF8599B's ability to perform a DC load detection without starting the amplifiers. After a DC load detection cycle finishes without setting the DC load valid bit DB1[D6], DC load detection is repeated (when bit IB2[D2] is toggled).

To limit the maximum number of DC load detection cycle loops, a counter and limit have been added. The loop exits after the predefined number of cycles (COUNTMAX), if the DC load detection cycle finishes with an invalid detection.

Depending on the application needs, the invalid DC load detection cycle can be handled as follows:

• the amplifier can be started without DC load detection
• the DC load detection loop can be executed again

I^{2}C-bus TX

IB1[D0] = 1	startup
IB2[D2] = 1	enable DC load
IB1[D1] = 1	disable channel 1
IB2[D1] = 1	disable channel 2

COUNT = 0

WAIT DC load

I^{2}C-bus RX

DB1[D4] = 1	channel 1 open load
DB2[D4] = 1	channel 2 open load
DB1[D6] = 1	DC load valid

CO

I^{2}C-bus TX

IB1[D0] = 1	startup
IB2[D2] = 1	enable DC load
IB1[D1] = 1	disable channel 1
IB2[D1] = 1	disable channel 2

NO

restart
DC load

YES

ERROR HANDLING

start amplifier
anyway

I^{2}C-bus TX

IB1[D0] = 1	startup
IB2[D2] = 0	disable DC load
IB1[D1] = 1	disable channel 1
IB2[D1] = 1	disable channel 2

NO

YES

I^{2}C-bus TX

IB1[D0] = 1	startup
IB2[D2] = 0	disable DC load
IB1[D1] = 0	enable channel 1
IB2[D1] = 0	enable channel 2

001aaj061

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet **Rev. 2 — 23 August 2016** **20 / 54**

8.6.3 Start-up and shutdown sequence

To prevent switch on or switch off 'pop noise', a capacitor (C_{SVRR}) connected to pin SVRR is used to smooth start-up and shutdown. During start-up and shutdown, the output voltage tracks the voltage on pin SVRR. Increasing C_{SVRR} results in a longer start-up and shutdown time. Enhanced pop noise performance is achieved by muting the amplifier until the SVRR voltage reaches its final value and the outputs start switching. The value of capacitor connected to pin SEL_MUTE (C_{ON}) determines the unmute and mute timing. The voltage on pin SEL_MUTE determines the amplifier gain. Increasing C_{ON} increases the unmute and mute times. In addition, a larger C_{ON} value increases the DC load detection cycle.

When the amplifier is switched off with an I^2C-bus command or by pulling pin EN LOW, the amplifier is first muted and then capacitor (C_{SVRR}) is discharged.

In Slave mode, the device enters the off state immediately after capacitor (C_{SVRR}) is discharged. In Master mode, the clock is kept active by an additional delay ($t_d^{(2)}$) of approximately 50 ms to allow slave devices to enter the off state.

When an external clock is connected to pin OSCIO (in Slave mode), the clock must remain active during the shutdown sequence for delay ($t_d^{(1)}$) to ensure that the slaved TDF8599B devices are able to enter the off state.
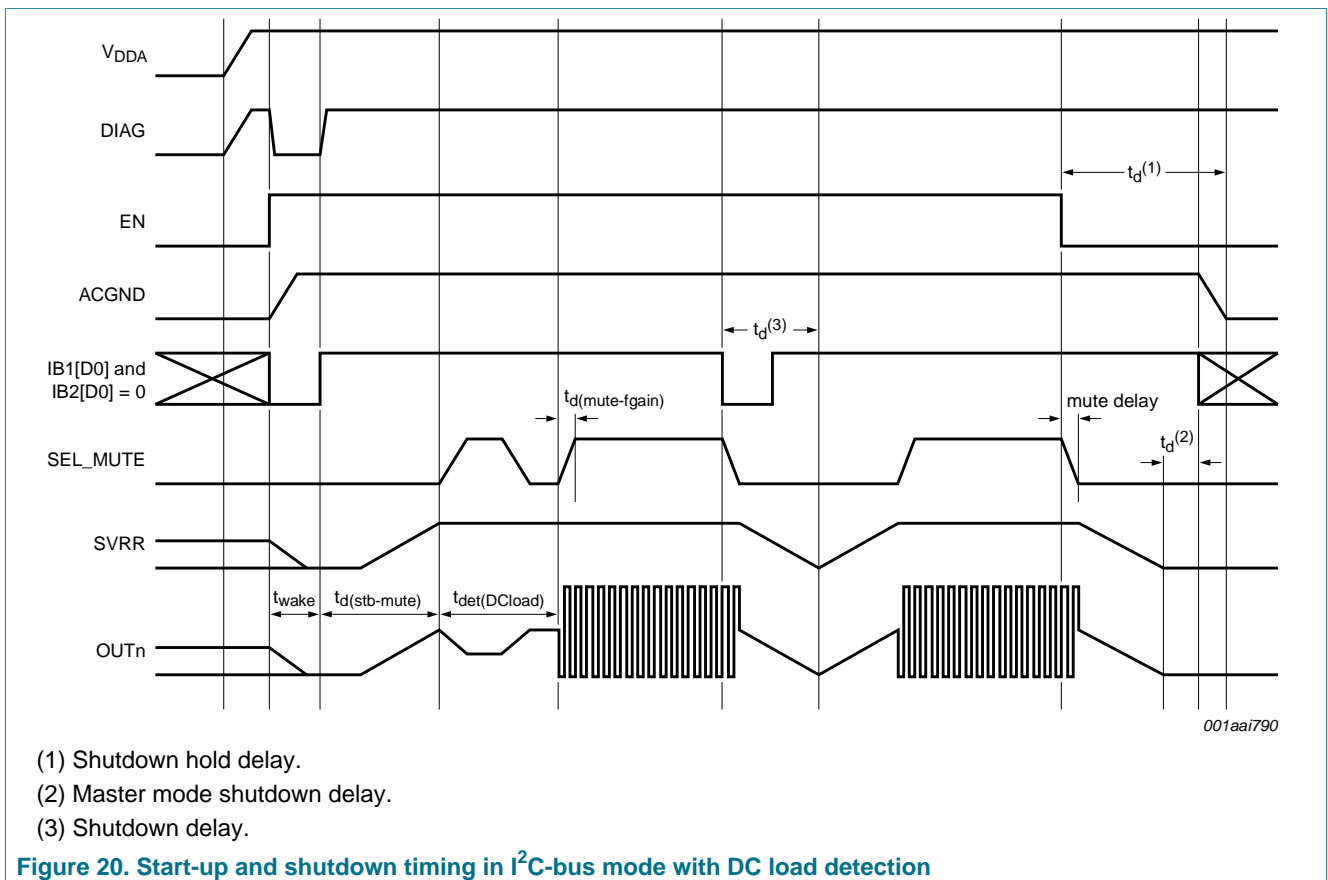
(1) Shutdown hold delay.
(2) Master mode shutdown delay.
(3) Shutdown delay.

Figure 20. Start-up and shutdown timing in I^2C-bus mode with DC load detection

(1) Shutdown hold delay.

(2) Shutdown delay.

(3) Master mode shutdown delay.

Figure 21. Start-up and shutdown timing in non-I²C-bus mode
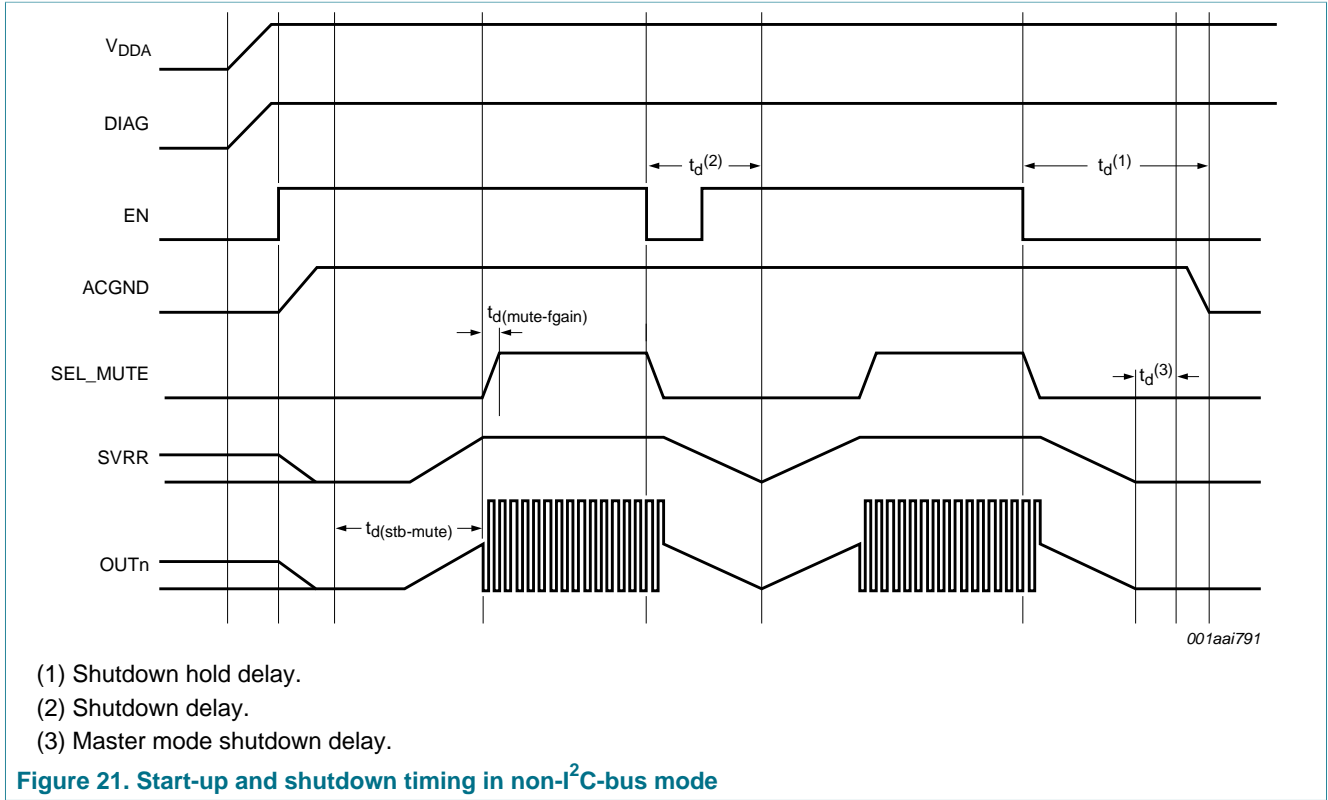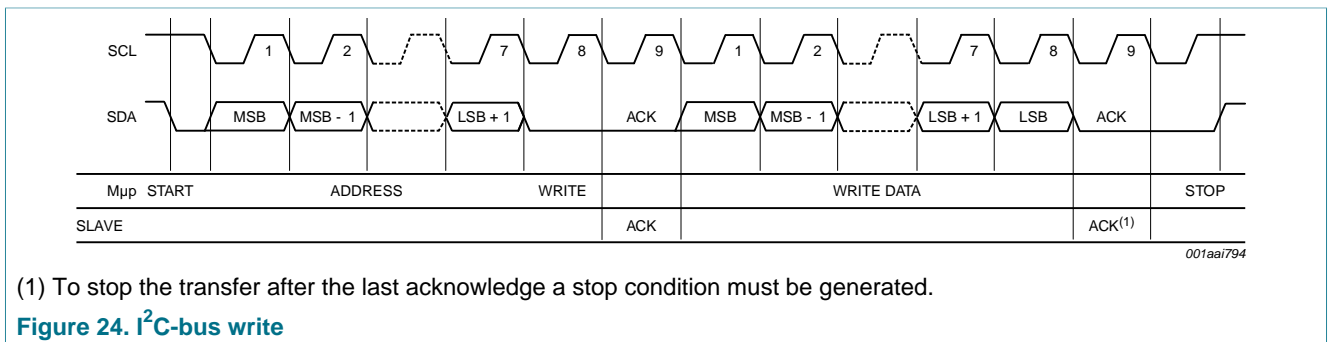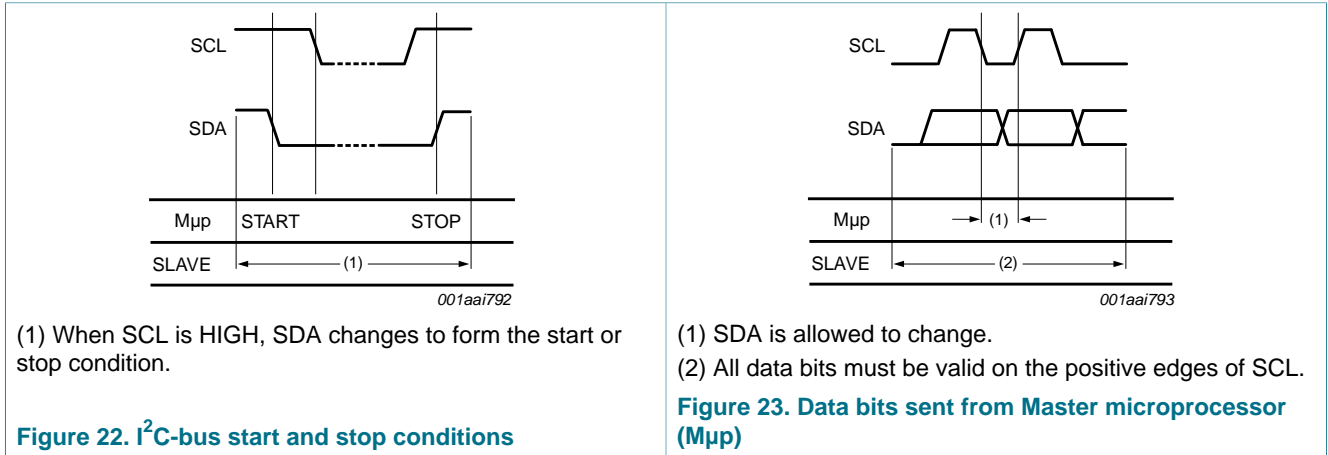
9   I²C-bus specification

TDF8599B address with hardware address select.

Table 13. I²C-bus write address selection using pins MOD and ADS

R$_{ADS}$[1] (k)	R$_{MOD}$[1] (k)		R/W

TDF8599B

Product data sheet **Rev. 2 — 23 August 2016**

22 / 54

In non-I^{2}C mode or when IB3[D7] = 0, the information on the MOD and ADS pins is latched when one of the TDF8599B's outputs starts switching.

(1) When SCL is HIGH, SDA changes to form the start or stop condition.

Figure 22. I^{2}C-bus start and stop conditions

(1) SDA is allowed to change.

(2) All data bits must be valid on the positive edges of SCL.

Figure 23. Data bits sent from Master microprocessor (Mμp)

(1) To stop the transfer after the last acknowledge a stop condition must be generated.

Figure 24. I^{2}C-bus write

(1) To stop the transfer, the last byte must not be acknowledged (SDA is HIGH) and a stop condition must be generated.

Figure 25. I^{2}C-bus read

9.1 Instruction bytes

If R/W bit = 0, the TDF8599B expects three instruction bytes: IB1, IB2 and IB3. After a power-on reset, all unspecified instruction bits must be set to zero.

Table 14. Instruction byte descriptions

Bit	Value	Description		
		Instruction byte IB1	**Instruction byte IB2**	**Instruction byte IB3**
D7	0	offset detection on pin DIAG	offset protection on	latch information on pins ADS and MOD when the amplifier starts switching
	1	no offset detection on pin DIAG	offset protection off	latch information on pins ADS and MOD; see Section 9
D6	0	channel 1 offset monitoring on	channel 2 offset monitoring on	

9.2 Data bytes

If R/W = 1, the TDF8599B sends two data bytes to the microprocessor (DB1 and DB2). All short diagnostic and offset protection bits are latched. In addition, all bits are reset after a read operation except the DC load detection bits (DBx[D4], DB1[D6]). The default setting for all bits is logic 0.

In Parallel mode, the diagnostic information is stored in byte DB1.

Table 16. Description of data bytes

Bit	Value	DB1 channel 1	DB2 channel 2
D7	0	at least 1 instruction bit set to logic 1	below maximum temperature
	1	all instruction bits are set to logic 0	maximum temperature protection activated
D6	0	invalid DC load data	no temperature warning
	1	valid DC load data	temperature pre-warning active
D5	0	no overvoltage	no undervoltage
	1	overvoltage protection active	undervoltage protection active
D4	0	speaker load channel 1	speaker load channel 2
	1	open load channel 1	open load channel 2
D3	0	no shorted load channel 1	no shorted load channel 2
	1	shorted load channel 1	shorted load channel 2
D2	0	no offset	reserved
	1	offset detected	reserved
D1	0	no short to V_P channel 1	no short to V_P channel 2
	1	short to V_P channel 1	short to V_P channel 2
D0	0	no short to ground channel 1	no short to ground channel 2
	1	short to ground channel 1	short to ground channel 2

Data byte DB1[D7] indicates whether the instruction bits have been set to logic 0. In principle, DB1[D7] is set after a POR or when all the instruction bits are programmed to logic 0. Pin DIAG is driven HIGH when bit DB1[D7] = 1.

10 Limiting values

Table 17. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage	Operating mode		-	29	V
		off state	[1]	−1	+50	V

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet   **Rev. 2 — 23 August 2016**

26 / 54

11 Thermal characteristics

Table 18. Table 18. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	35	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W

12 Static characteristics

Table 19. Static characteristics

$V_P = V_{DDA} = 14.4$ V; $f_{osc} = 320$ kHz; -40 °C $< T_{amb} < +85$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_P	supply voltage		8	14.4	24	V
I_P	supply current	off state; T_j 85 °C; $V_P = 14.4$ V	-	2	10	µA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, snubbers and filter connected	-	90	120	mA
Series resistance output switches						
R_{DSon}	drain-source on-state resistance	power switch;				
		$T_j = 25$ °C	-	140	150	m
		$T_j = 100$ °C	-	190	205	m
I^{2}C-bus interface: pins SCL and SDA						
V_{IL}	LOW-level input voltage		0	-	1.5	V
V_{IH}	HIGH-level input voltage		2.3	-	5.5	V
V_{OL}	LOW-level output voltage	pin SDA; $I_{load} = 5$ mA	0	-	0.4	V
Address, phase shift and modulation mode select: pins ADS and MOD						
V_i	input voltage	pins not connected [1]	1.5	2	2.7	V
I_i	input current	pins shorted to GND [1]	80	105	160	µA
Enable and SEL_MUTE input: pins EN and SEL_MUTE						

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet **Rev. 2 — 23 August 2016**

27 / 54

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		pin SEL_MUTE; Operating mode; 0.8 V	-	-	50	µA
Diagnostic output						
THD_{clip}	total harmonic distortion clip detection level		-	0.2	-	%
$V_{th(offset)}$	threshold voltage for offset detection	[2] [3]	1	2	3	V
V_{OL}	LOW-level output voltage	DIAG or CLIP pins activated; $I_o = 1$ mA	-	-	0.3	V
I_L	leakage current	DIAG and CLIP pins; diagnostic not activated	-	-	50	µA
Audio inputs; pins IN1N, IN1P, IN2N and IN2P						
V_i	input voltage		-	2.45	-	V
SVRR voltage and ACGND input bias voltage in Mute and Operating modes						
V_{ref}	reference voltage	input ACGND pin	2	2.45	3	V
		half supply reference SVRR pin	6.9	7.2	7.5	V
Amplifier outputs; pins OUT1N, OUT1P, OUT2N and OUT2P						
$V_{O(offset)}$	output offset voltage	BTL; Mute mode	-	-	25	mV
		BTL; Operating mode [4] [5]	-	-	70	mV
Stabilizer output; pins VSTAB1 and VSTAB2						
V_o	output voltage	stabilizer output in Mute mode and Operating mode	8	10	12	V
Voltage protections						
$V_{(prot)}$	protection voltage	undervoltage; amplifier is muted	6.8	7.2	8	V
		overvoltage; load dump protection is activated	26.2	27	-	V
		V_P that a POR occurs at	3	3.7	4.6	V
Current protection						
$I_{O(ocp)}$	overcurrent protection output current	current limiting concept				

TDF8599B

Product data sheet **Rev. 2 — 23 August 2016** **28 / 54**

I2C-bus controlled dual channel 43 W/2 Ohm, single channel 85 W/1 Ohm class-D power amplifier with load diagnostics

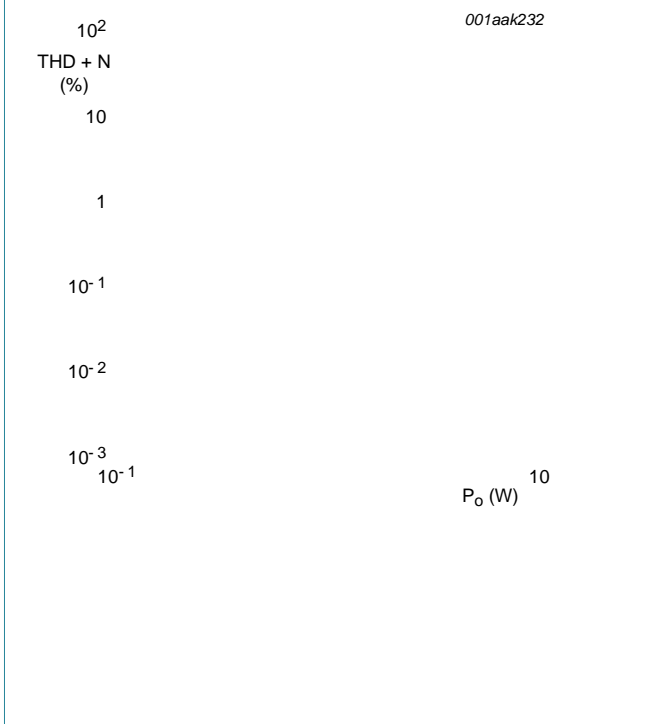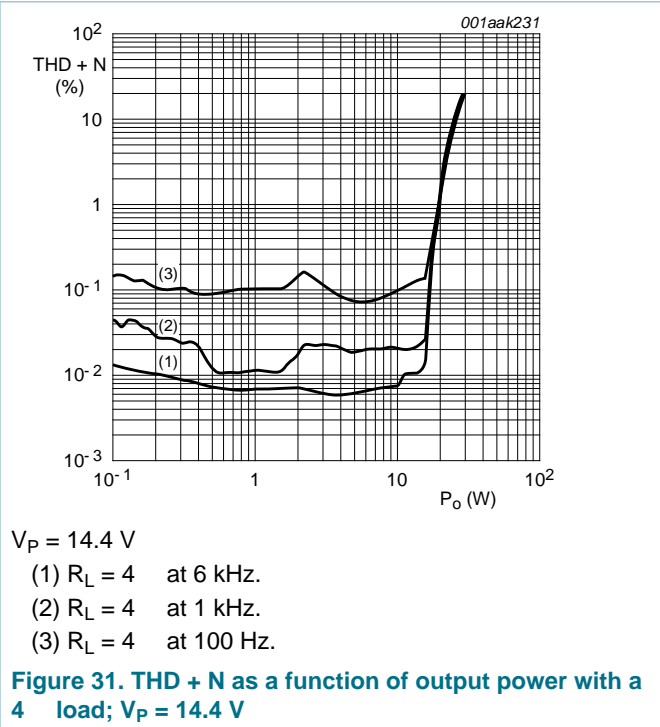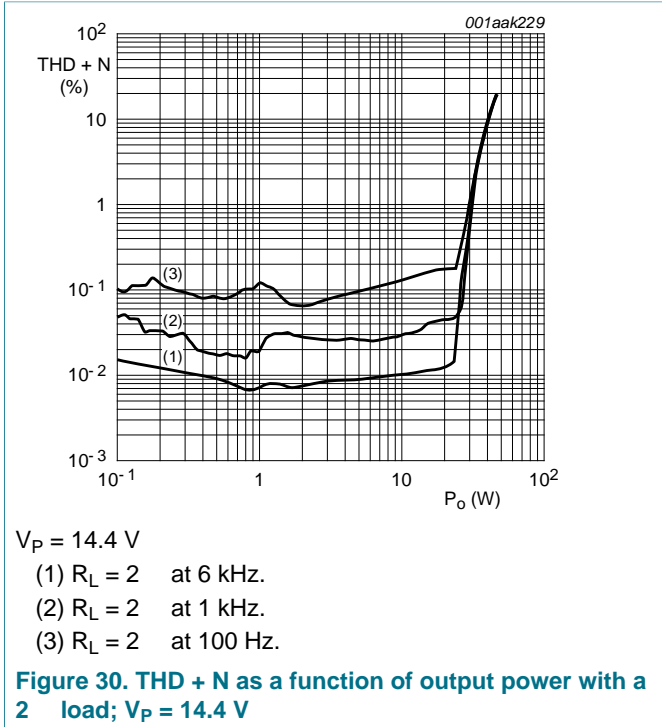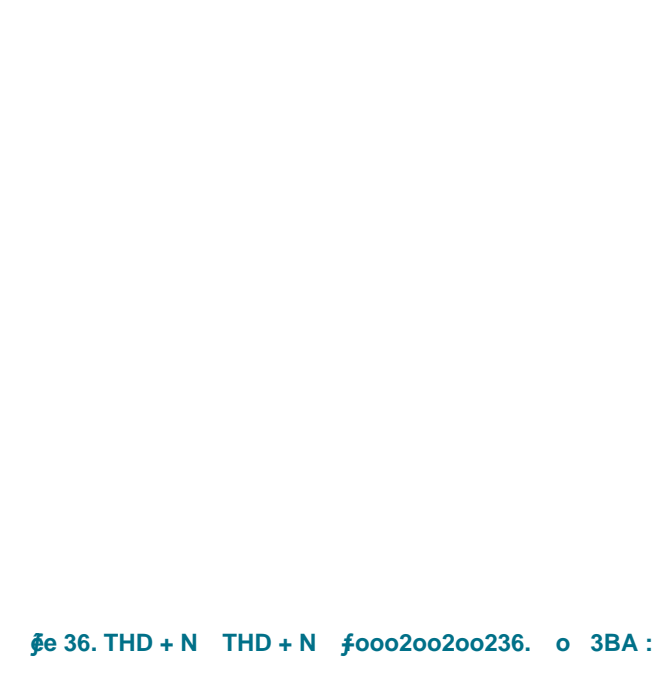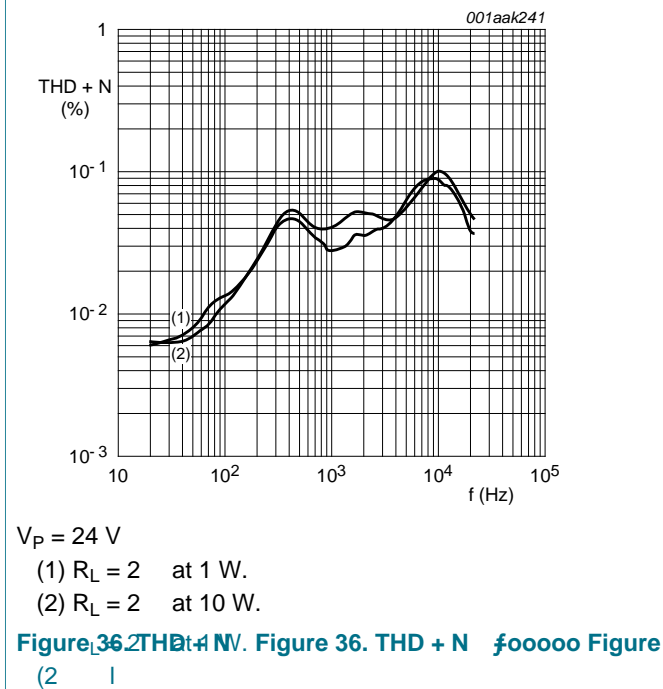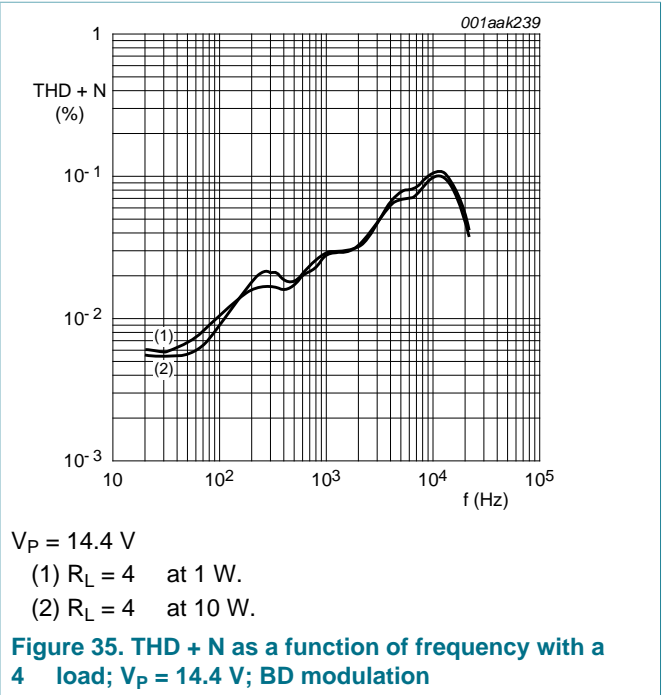| Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Z_{th(load)}$	load detection threshold impedance	for normal speaker load; DB1[D4] = 0; DB2[D4] = 0	-	-	25	
$Z_{th(open)}$	open load detection threshold impedance	DB1[D4] = 1; DB2[D4] = 1	350	-	-	
AC load detection levels: I²C-bus mode only						
$I_{th(o)det(load)AC}$	AC load detection output threshold current		250	500	700	mA
Start-up/shut-down/mute timing						
t_{wake}	wake-up time	on pin EN before first I²C-bus transmission is recognized [7]	-	-	500	µs
$t_{det(DCload)}$	DC load detection time	C_{ON} = 470 nF [7]	-	380	-	ms
$t_{d(stb-mute)}$	delay time from standby to mute	measured from amplifier enabling to start of unmute (no DC load detection); C_{SVRR} = 47 µF C_{ON} = 470 nF	-	140	-	ms
$t_{d(mute-fgain)}$	mute to full gain delay time	C_{ON} = 470 nF [5]	-	15	-	ms
t_d	delay time	shutdown delay time from EN pin LOW to SVRR LOW; voltage on pin SVRR < 0.1 V; C_{SVRR} = 47 µF	200	350	550	ms
		shutdown delay time from EN pin LOW to SVRR LOW; voltage on pin SVRR < 0.1 V; C_{SVRR} = 47 µF; V_P = 35 V	300	400	700	ms
		shutdown hold delay time from pin EN LOW to ACGND LOW; voltage on pin ACGND < 0.1 V; Master mode	-	370	-	ms
		hold delay in Master mode to allow slaved devices to shutdown f_{osc} = 320 kHz	-	50	-	ms
Speaker load impedance						
R_L	load resistance	at supply voltage equal to or below 24 V				
		stereo mode	1.6	4	-	
		parallel mode	0.8	-	-	

[1]   Required resistor accuracy for pins ADS and MOD is 1 %; see Section 9.
[2]   Maximum leakage current from DCP pin to ground = 3 µA
[3]   The output offset values can be either positive or negative. The Vth(offset) limit values (excluding Typ) are the valid absolute values.
[4]   DC output offset voltage is applied to the output gradually during the transition between Mute mode and Operating mode.
[5]   The transition time between Mute mode and Operating mode is determined by the time constant on the SEL_MUTE pin.
[6]   The DC load valid bit DB1[D6] must be used; Section 8.6.2.1. The DC load enable bit IB2[D2] must be reset after each load detection cycle to prevent amplifier hang-up incidents.
[7]   I2C-bus mode only.

13 Dynamic characteristics

Table 21. Dynamic characteristics

$V_P = V_{DDA} = 14.4$ V; $R_L = 4$; $f_i = 1$ kHz; $f_{osc} = 320$ kHz; $R_{s(L)} < 0.04$ [1]; -40 °C $< T_{amb} < +85$ °C; Stereo mode; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	Stereo mode:	[2]				
		$V_P = 14.4$ V; THD = 1 %; $R_L = 4$		18	20	-	W
		$V_P = 14.4$ V; THD = 10 %; $R_L = 4$		24	26	-	W
		square wave (EIAJ); $R_L = 4$		-	40	-	W
		$V_P = 24$ V; THD = 10 %; $R_L = 4$		-	70	-	W
		$V_P = 14.4$ V; THD = 1 %; $R_L = 2$		29	32	-	W
		$V_P = 14.4$ V; THD = 10 %; $R_L = 2$		39	43	-	W
		square wave (EIAJ); $R_L = 2$		-	70	-	W
		Parallel mode:	[2]				
		$V_P = 14.4$ V; THD = 10 %; $R_L = 1$		-	85	-	W
		$V_P = 24$ V; THD = 10 %; $R_L = 2$		-	138	-	W
		$V_P = 24$ V; THD = 1 %; $R_L = 1$		135	150	-	W
THD		$f_i = 1$ kHz; $P_o = 1$ W	[3]	-	0.02	0.1	%

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

31 / 54

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
po	output power efficiency	P_o = 20 W	-	90	-	%

[1] $R_{s(L)}$ is the sum of the inductor series resistance from the low-pass LC filter in the application together with all resistance from PCB traces or wiring between the output pin of the TDF8599B and the inductor to the measurement point. LC filter dimensioning is L = 10 µH, C = 1 µF for 4   load and L = 5 µH, C = 2.2 µF for 2   load.

[2]   Output power is measured indirectly based on R_{DSon} measurement.

[3]   Total harmonic distortion is measured at the bandwidth of 22 Hz to 20 kHz, AES brick wall. The maximum limit is guaranteed but may not be 100 % tested.

[4] V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); R_s = 0   .

[5]   B = 22 Hz to 20 kHz, AES brick wall, R_s = 0   .

[6]   B = 22 Hz to 20 kHz, AES brick wall, independent of R_s.

[7] V_i = $V_{i(max)}$ = 0.5 V RMS.

14 Application information

14.1 Output power estimation (Stereo mode)

The output power, just before clipping, can be estimated using Equation 5:

$$P_o = \frac{\left(\left(\frac{R_L}{R_L+}\right.\right.}{}$$
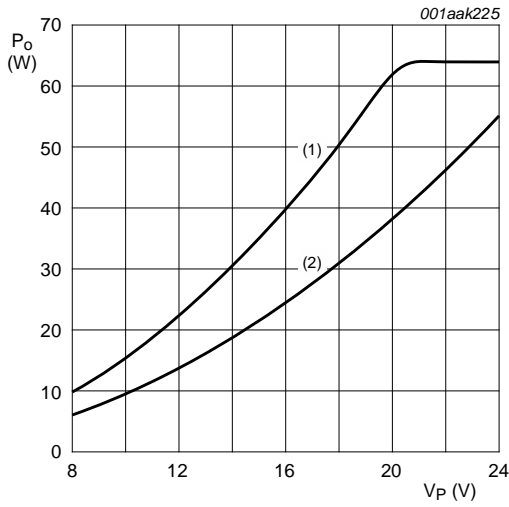
THD = 0.5 %

R_{DSon} = 0.19   (at Tj = 100 °C), R_s = 0.05 ,

$t_{w(min)}$ = 190 ns and $I_{O(ocp)}$ = 8 A (minimum).

(1) R_L = 2 .

(2) R_L = 4 .

Figure 26. P_o as a function of VP in stereo mode with THD = 0.5 %
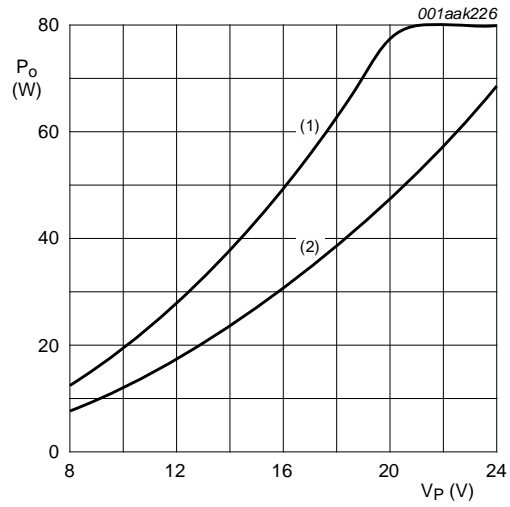
THD = 10 %

R_{DSon} = 0.19   (at Tj = 100 °C), R_s = 0.05 ,

$t_{w(min)}$ = 190 ns and $I_{O(ocp)}$ = 8 A (minimum).

(1) R_L = 2 .

(2) R_L = 4 .

Figure 27. P_o as a function of V_P in stereo mode with THD = 10 %

14.2 Output power estimation (Parallel mode)

Figure 28 and Figure 29 show the estimated output power at THD = 0.5 % and THD = 10 % as a function of the supply voltage for different load impedances in parallel mode.

TDF8599B

Product data sheet **Rev. 2 — 23 August 2016**

33 / 54

TDF8599B

Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 2 — 23 August 2016

© NXP Semiconductors N.V. 2016. All rights reserved.

34 / 54

Table 22. Filter component values

Load impedance ( )	L_{LC} (µH)	C_{LC} (µF)
1	2.5	4.4
2		

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

35 / 54

14.6 Curves measured in reference design

V_P = 14.4 V
  (1) R_L = 2   at 6 kHz.
  (2) R_L = 2   at 1 kHz.
  (3) R_L = 2   at 100 Hz.

Figure 30. THD + N as a function of output power with a 2   load; V_P = 14.4 V

V_P = 14.4 V
  (1) R_L = 4   at 6 kHz.
  (2) R_L = 4   at 1 kHz.
  (3) R_L = 4   at 100 Hz.

Figure 31. THD + N as a function of output power with a 4   load; V_P = 14.4 V

I2C-bus controlled dual channel 43 W/2 Ohm, single channel 85 W/1 Ohm class-D power amplifier with load diagnostics

V_P = 14.4 V
(1) R_L = 2   at 1 W.
(2) R_L = 2   at 10 W.

Figure 34. THD + N as a function of frequency with a 2   load; V_P = 14.4 V; BD modulation

V_P = 14.4 V
(1) R_L = 4   at 1 W.
(2) R_L = 4   at 10 W.

Figure 35. THD + N as a function of frequency with a 4   load; V_P = 14.4 V; BD modulation

V_P = 24 V
(1) R_L = 2   at 1 W.
(2) R_L = 2   at 10 W.

Figure 36. THD + N $f$ooooo Figure   ŧe 36. THD + N   THD + N $f$ooo2oo2oo236.   o   3BA :

TDF8599B

Product data sheet **Rev. 2 — 23 August 2016**

37 / 54
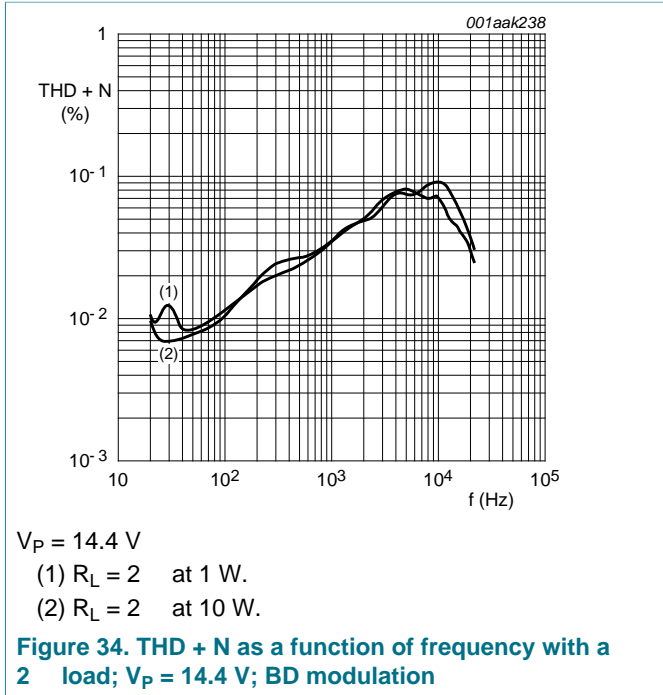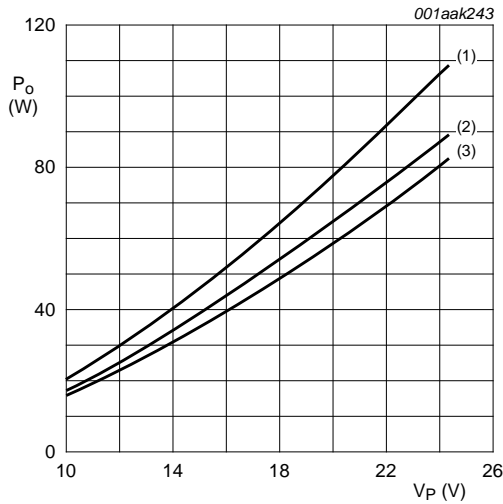
f = 1 kHz; R_L = 2
(1) THD = 10 %
(2) THD = 3 %
(3) THD = 1 %

Figure 38. Output power as a function of supply voltage with a 2 load
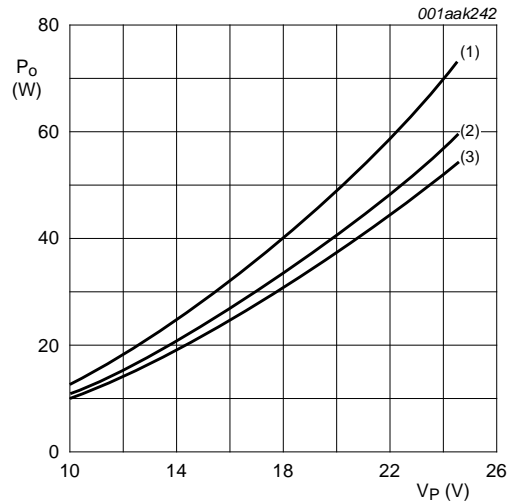
f = 1 kHz; R_L = 4
(1) THD = 10 %
(2) THD = 3 %
(3) THD = 1 %

Figure 39. Output power as a function of supply voltage with a 4 load
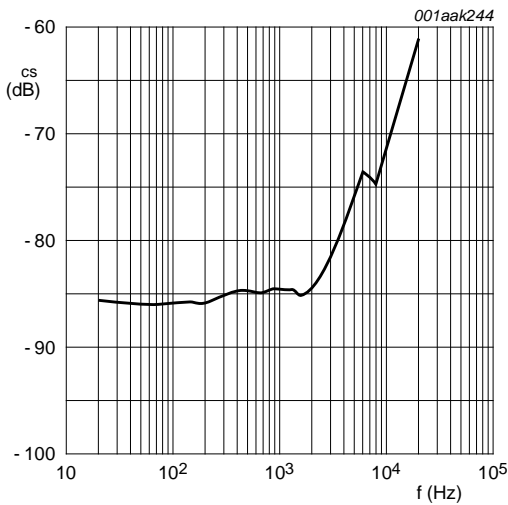
V_P = 14.4 V; R_L = 4 at 1 W

Figure 40. Channel separation as a function of frequency with 1 W output power, BD modulation
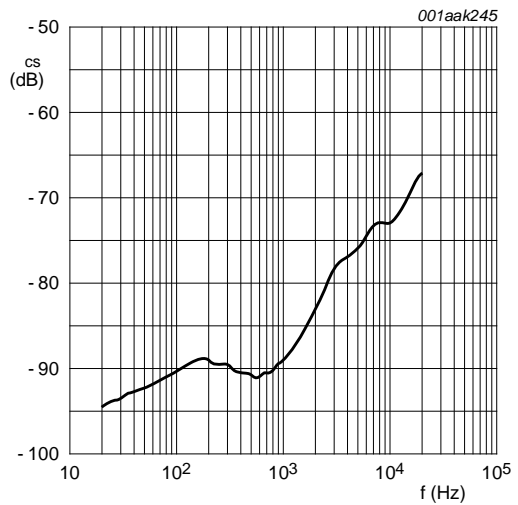
V_P = 14.4 V; R_L = 4 at 10 W

Figure 41. Channel separation as a function of frequency with 10 W output power, BD modulation

001aak246
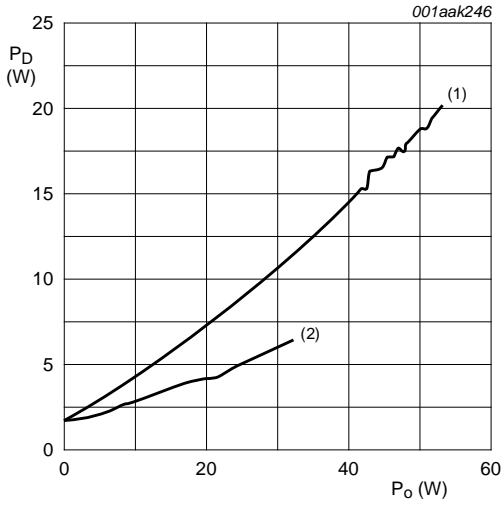
V_P = 14.4 V
(1) R_L = 2
(2) R_L = 4

Figure 42. Power dissipation as a function of total output power with both channels driven; V_P = 14.4 V

001aak247
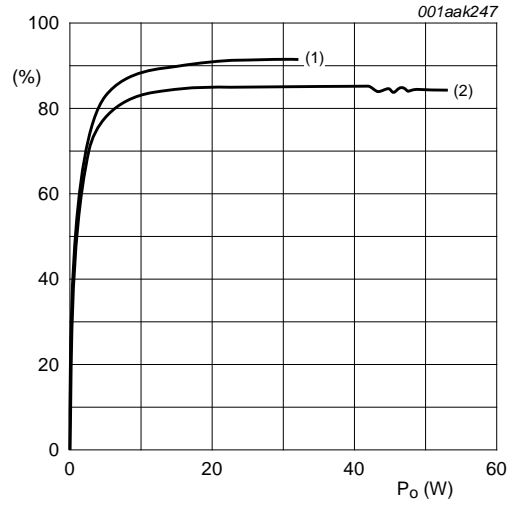
V_P = 14.4 V
(1) R_L = 4
(2) R_L = 2

Figure 43. Efficiency as a function of total output power with both channels driven; V_P = 14.4 V

001aak248
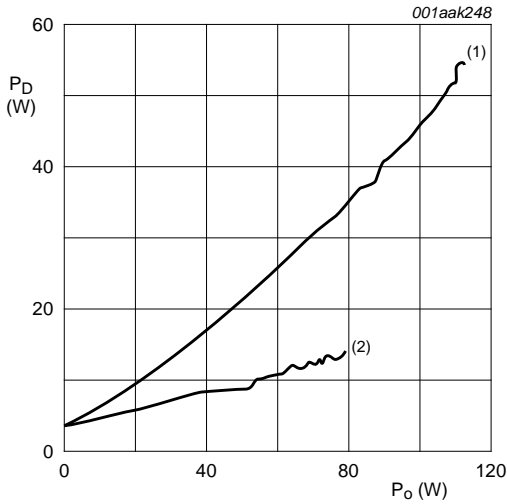
V_P = 24 V
(1) R_L = 2
(2) R_L = 4

Figure 44. Power dissipation as a function of total output power with both channels driven; V_P = 24 V

001aak249
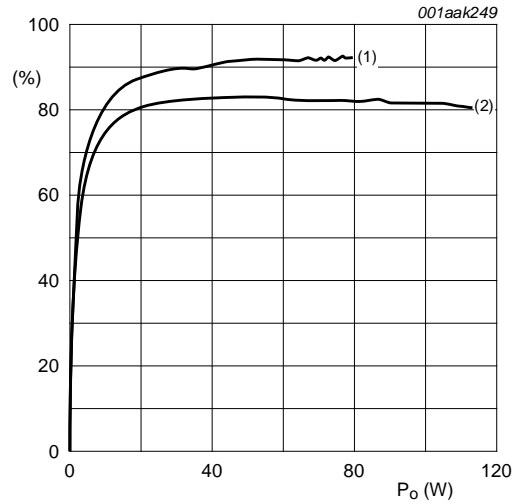
V_P = 24 V
(1) R_L = 4
(2) R_L = 2

Figure 45. Efficiency as a function of total output power with both channels driven; V_P = 24 V

TDF8599B

Product data sheet **Rev. 2 — 23 August 2016**

39 / 54

001aak250

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

40 / 54

14.7 Typical application schematics

001aak220

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

41 / 54

Dual BTL mode (stereo) in I²C-bus mode with DC offset protection enabled; Spread spectrum mode disabled.

(1) See Figure 3 for a diagram of the connection for pins EN and SEL_MUTE.

(2) See Section 8.3.2 for detailed information.

(3) See Section 8.5.5 for detailed information on DC offset protection.

Figure 48. Example application diagram for dual BTL in I²C-bus mode

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet **Rev. 2 — 23 August 2016**

42 / 54

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

43 / 54

15 Package outline

HSOP36: plastic, heatsink small outline package; 36 leads; low stand-off height

SOT851-2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT851-2						04-05-04

16 Handling information

In accordance with SNW-FQ-611-D. The number of the quality specification can be found in the Quality Reference Handbook. The handbook can be ordered using the code 9398 510 63011.

17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 "Surface mount reflow soldering description".

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

• Through-hole components
• Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

• Board specifications, including the board finish, solder masks and vias
• Package footprints, including solder thieves and orientation
• The moisture sensitivity level of the packages
• Package placement
• Inspection and repair
• Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 52) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 23 and Table 24

Table 23. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C) Volume (mm^3)	
	< 350	**350**
< 2.5	235	220
2.5	220	220

Table 24. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C) Volume (mm^3)		
	< 350	**350 to 2 000**	**> 2 000**
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 52.

TDF8599B

Product data sheet

Rev. 2 — 23 August 2016

47 / 54

18 Abbreviations

Table 25. Table 25. Abbreviations

Abbreviation	Description
BCDMOS	Bipolar Complementary and double Diffused Metal-Oxide Semiconductor
BTL	Bridge-Tied Load
DCP	DC offset Protection
DMOST	double Diffused Metal-Oxide Semiconductor Transistor
EMI	ElectroMagnetic Interference
I^{2}C	Inter-Integrated Circuit
LSB	Least Significant Bit
Mµp	Master microprocessor
MSB	Most Significant Bit
NDMOST	N-type double Diffused Metal-Oxide Semiconductor Transistor
OCP	OverCurrent Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
POR	Power-On Reset
PWM	Pulse-Width Modulation
SOI	Silicon On Insulator
TFP	Thermal Foldback Protection
UVP	UnderVoltage Protection
WP	Window Protection

19 Revision history

Table 26. Table 26. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8599B v.2	20160823	Product data sheet	-	TDF8599B v.1
Modifications:	• corrected "2 Ohm" typo in title			
TDF8599B v.1	20090729	Product data sheet	-	-

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

49 / 54

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of

dmation included herein and s
Xu[Xzuded here Xǿd heuý heherecy z)h Xc<mn ig   he u8use̸ ÿ   e

the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP Semiconductors N.V.

Tables

Figures

TDF8599B

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2016. All rights reserved.

Product data sheet

Rev. 2 — 23 August 2016

53 / 54

Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.   **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 23 August 2016
Document identifier: TDF8599B