SY58051AU

Ultra-Precision CML AnyGate® with Internal Input and Output Termination

Revision 1.0

General Description

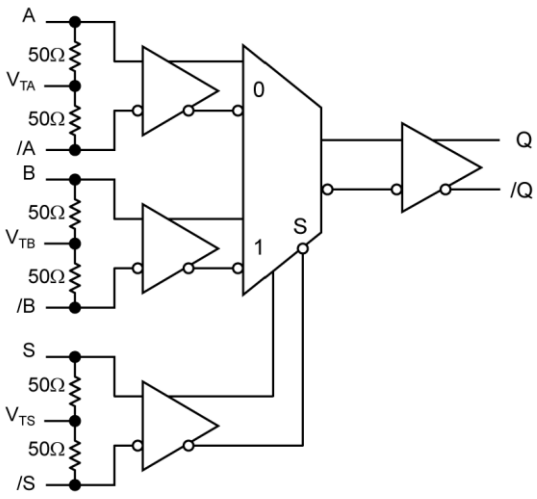
The SY58051AU is an ultra-fast, low jitter universal logic gate with a guaranteed maximum data or clock throughput of 10.7Gbps or 8GHz, respectively. This AnyGate® differential logic device will produce many logic functions of two Boolean variables, such as AND, NAND, OR, NOR, DELAY, or NEGATION.

The SY58051AU differential inputs include a unique internal termination design that allows access to the termination network throughout a VT pin. This feature allows the device to easily interface to different logic standards, both AC- and DC-coupled, without external resistor-bias and termination networks. The result is a clean, stub-free, low-jitter interface solution. The differential CML output is optimized for environments with internal 50Ω source termination and a 400mV output swing.

The SY58051AU operates from a 2.5V or 3.3V supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY58051AU is part of Micrel's Precision Edge® product family.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Precision Edge®

Features

- Three matched-delay input pairs provide any logic function: AND, NAND, OR, NOR
- Guaranteed AC performance over temperature and voltage:
  - DC to >10.7Gbps data rate throughput
  - DC to >8GHz clock f_{MAX}
  - <160ps Any In-to-Out t_{pd}
  - 20ps typical t_r/t_f
- Ultra-low jitter design:
  - 0.2ps$_{RMS}$ typical random jitter (data)
  - 2ps$_{PP}$ typical deterministic jitter (data)
  - 5ps$_{PP}$ typical total jitter (clock)
  - 46fs$_{RMS}$ typical additive phase jitter (clock)
- Unique input termination and VT pin accepts AC- and DC-coupled inputs (CML, PECL)
- Internal 50Ω output source termination
- Typical 400mV CML output swing (R_L = 50Ω)
- Internal 50Ω input termination
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C industrial temperature range
- Available in a 16-pin 3mm × 3mm QFN package

Applications

- Data communciation systems
- OC-192, OC-192+FEC data-to-clock
- All SONETOC-3 – OC-768 applications
- Fibre Channel
- Gigabit Ethernet
- ATE
- Test and measurement

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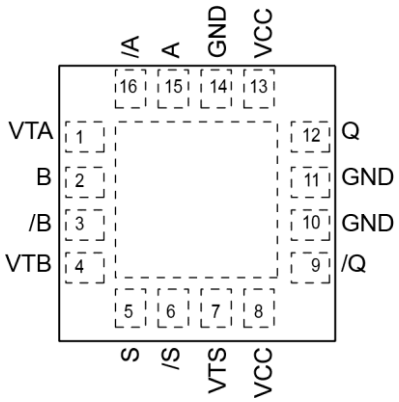
Ordering Information

Part Number	Package Type	Temperature Range	Package Marking	Lead Finish
SY58051AUMG[1]	Pb-Free QFN-16	Industrial	051A with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY58051AUMG TR[1, 2]	Pb-Free QFN-16	Industrial	051A with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Pb-Free package recommended for new designs.
2. Tape and Reel

Pin Configuration



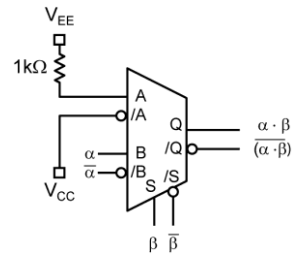
16-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	VTA	Input termination center tap: Each of the two inputs (A, /A) terminates to this pin through a 50Ω resistor. The VTA pin provides a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section for more details.
15, 16 2, 3	A, /A B, /B	Differential input: These input pairs are the two data inputs to the device. Each pin of a pair (A, /A) and (B, /B) internally terminates to the VTA or VTB pin to 50Ω. Note that these inputs will default to an indeterminate state if left open. See the Input Interface Applications section for more details.
4	VTB	Input termination center tap: Each of the two inputs (B, /B) terminates to this pin through a 50Ω resistor. The VTB pin provides a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section for more details.
5, 6	S, /S	Differential input: This input pair is the select input to the device. Each pin of this pair internally terminates to the VTS pin to 50Ω. Note that this input will default to an indeterminate state if left open. See the Input Interface Applications section for more details.
7	VTS	Input termination center tap: Each of the two inputs (S, /S) terminates to this pin. The VTS pin provides a center-tap to a termination network for maximum interface flexibility.
8, 13	VCC	Positive power supply. Bypass with 0.1µF‖0.01µF low ESR capacitors.
12, 9	Q, /Q	Differential output: This CML output pair is the output of the device. It is a logic function of the A, B, and S inputs. See the Truth Tables for details.
10, 11, 14	GND	Ground. Exposed pad must be connected to the same potential as GND pin.

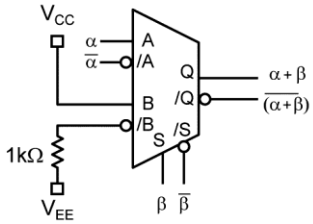
Truth Tables

A	/A	B	/B	S	/S	Q	/Q
0	1	X	X	0	1	0	1
1	0	X	X	0	1	1	0
X	X	0	1	1	0	0	1
X	X	1	0	1	0	1	0



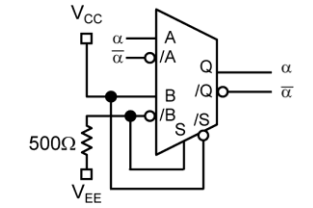
AND/NAND

A α B	α B	β S	α • β Q	$\overline{(\alpha \bullet \beta)}$ /Q
L L L L	L H L H	L L H H	L L L H	H H H L



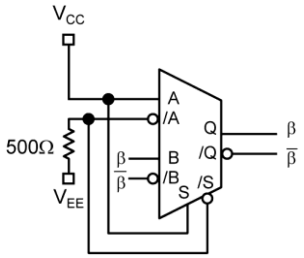
OR/NOR

α A	B	β S	α + β Q	$\overline{(\alpha + \beta)}$ /Q
L H L H	H H H H	L L H H	L H H H	H L L L



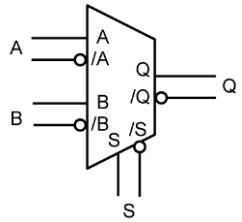
DELAY/NEGATION

α A	B	S	α Q	$\overline{\alpha}$ /Q
L H		L L	L H	H L



DELAY/NEGATION

A	β B	S	β Q	$\overline{\beta}$ /Q
	L H	H H	L H	H L



2:1 MUX

S	Q	/Q
L H	A B	$\overline{A}$ $\overline{B}$

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Absolute Maximum Ratings[3]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... V_{CC} – 1.0V to V_{CC} + 0.5V
Termination Current[5]
Source or Sink Current on V_{TA}, V_{TB}, V_{TS} ..... ±60mA
Input Current
Source or Sink Current on A, /A, B, /B, S, /S ..... ±30mA
Lead Temperature (soldering, 20s) ..... 260°C
Storage Temperature (Ts) ..... –65°C to +150°C

Operating Ratings[4]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
..... or +2.97V to +3.63V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[6]
QFN (θ_{JA}) Still-Air ..... 61°C/W
QFN (ψ_{JB}) ..... 38°C/W

DC Electrical Characteristics[7, 8]

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply		2.375 2.97	2.5 3.3	2.625 3.63	V
I_{CC}	Power supply current	With load for either 2.5V or 3.3V supply		42	60	mA
R_{DIFF_IN}	Differential input resistance (A-to-/A), (B-to-/B), or (S-to-/S)		90	100	110	Ω
R_{IN}	Input resistance (A-to-V_{TA}, B-to-V_{TB}, or S-to-V_{TS})		45	50	55	Ω
V_{IH}	Input HIGH voltage (A, /A), (B, /B), or (S, /S)	Note 9	1.2		V_{CC}	V
V_{IL}	Input LOW voltage (A, /A), (B, /B), or (S, /S)	Note 9	0		V_{IH} + 0.1	mV
V_{IN}	Input voltage swing (A, /A), (B, /B), or (S, /S)	Note 9 See Figure 3	100			mV
V_{DIFF_IN}	Differential input voltage swing (A, /A), (B, /B), or (S, /S)	Note 9 See Figure 4	200			mV
I_{IN}	Input current (A, /A), (B, /B), or (S, /S)	Note 9			21	mA

Notes:

3. Exceeding the absolute maximum ratings may damage the device.
4. The device is not guaranteed to function outside its operating ratings.
5. Due to the limited drive capability use for input of the same package only.
6. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air, unless otherwise stated.
7. Specification for packaged product only.
8. The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.
9. Due to the internal termination (see “Input Structures” section), the input current depends upon the applied voltages at A, /A, and V_{TA} inputs, the B, /B, and V_{TB} inputs, or the S, /S, and V_{TS} inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

CML Electrical Characteristics[10]

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L =100Ω across output pair or equivalent; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH voltage (Q, /Q)	R_L = 50Ω to V_{CC}	V_{CC}-0.020		V_{CC}	V
V_{OUT}	Output voltage swing (Q, /Q)	See Figure 3	325	400		mV
V_{DIFF_OUT}	Differential output voltage swing (Q, /Q)	See Figure 4	650	800		mV
R_{OUT}	Output source impedance (Q, /Q)		45	50	55	Ω

AC Electrical Characteristics[10, 11]

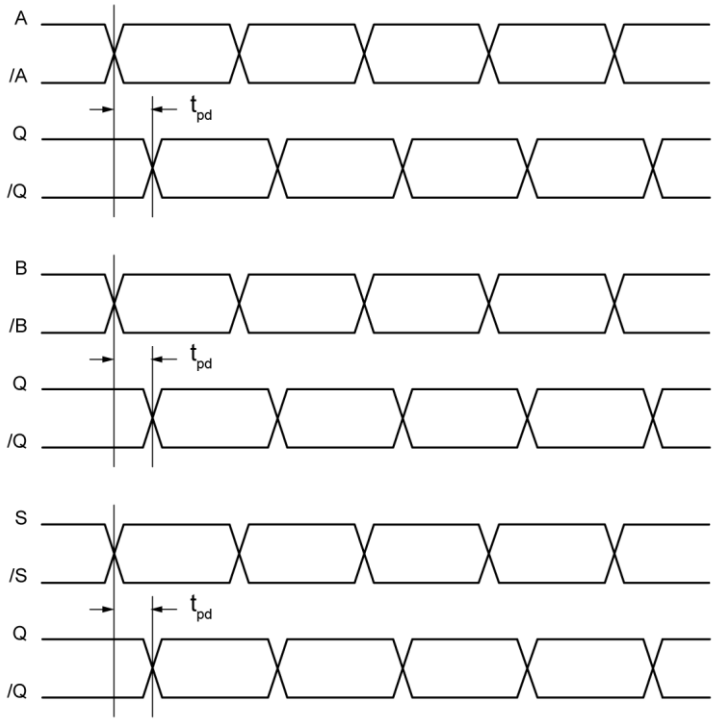
V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L =100Ω across output pair or equivalent; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum operating frequency	Clock NRZ data	8 10.7			GHz Gbps
t_{pd}	Propagation delay any input (A, B, S)-to-Q		70		160	ps
t_{SKEW}	Part-to-part skew	Note 12			100	ps
t_{JITTER}	**Data**					
	Random jitter (RJ)	Note 13		0.2	1	ps_{RMS}
	Deterministic jitter (DJ)	Note 14		2	5	ps_{PP}
	Clock					
	Cycle-to-cycle jitter (RJ)	Note 15		0.5	1	ps_{RMS}
	Total jitter (TJ)	Note 16		5	10	ps_{PP}
	Additive phase jitter	622MHz input integrated over 12kHz – 20MHz		46		fs_{RMS}
t_r/t_f	Output rise/fall times (20% to 80%)	At full output swing		20	50	ps

Notes:

10. Specification for packaged product only.
11. Measured with 100mV input swing. See the Timing Diagrams section for definition of parameters. High-frequency AC parameters are guaranteed by design and characterization.
12. Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
13. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.
14. Deterministic jitter is measured at 2.5Gbps/3.2Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
15. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_n$–1 where Tn is the time between rising edges of the output signal.
16. Total jitter definition: with an ideal clock input of frequency ≤f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Timing Diagram



Input and Output Stage Internal Termination

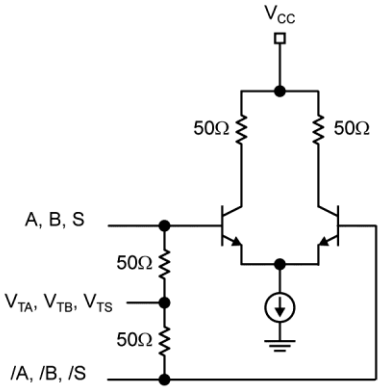


Figure 1. Simplified Differential Input Stage

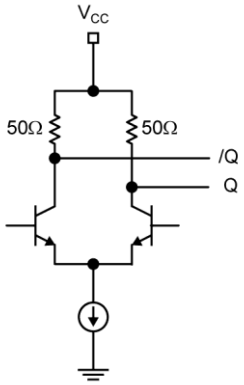


Figure 2. Simplified Differential Output Stage

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Definition of Single-Ended and Differential Swings

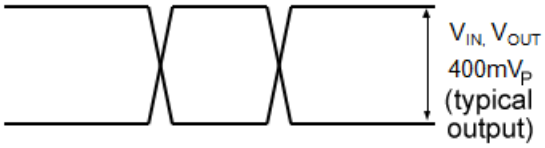


Figure 3. Single-Ended Swing

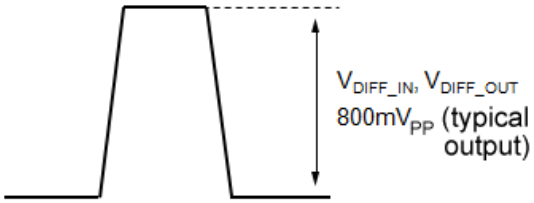
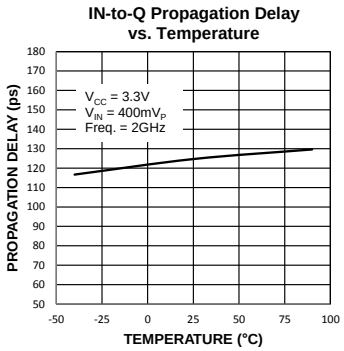
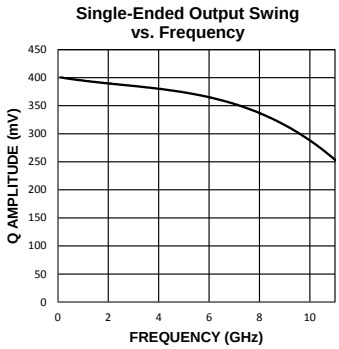
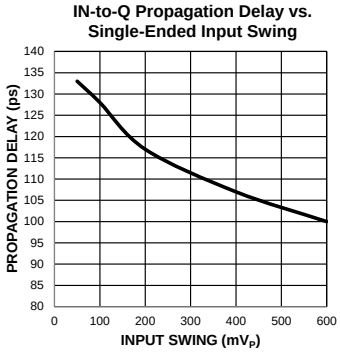


Figure 4. Differential Swing

Typical Operating Characteristics



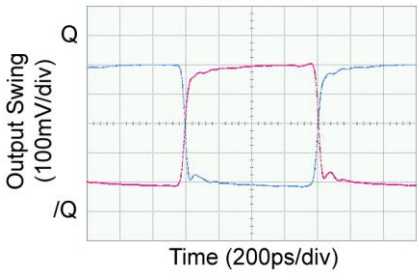




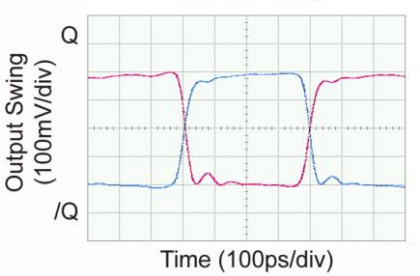
Functional Characteristics

V_{IN} = 400mV, 3.3V supply.

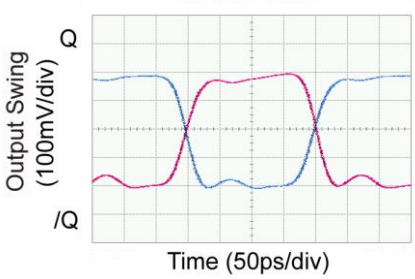
622MHz Clock



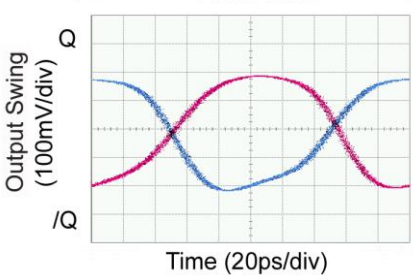
1.25GHz Clock



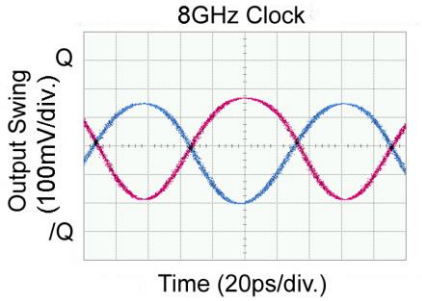
2.5GHz Clock



5GHz Clock



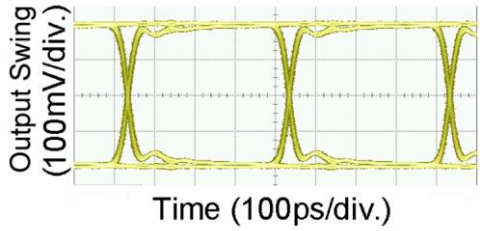
8GHz Clock



Functional Characteristics (Continued)

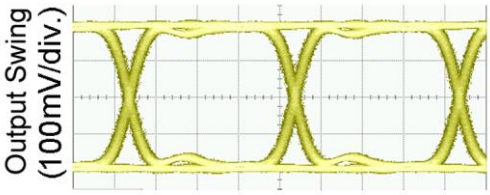
V_{IN} = 400mV, 3.3V supply.

2.5Gbps Data



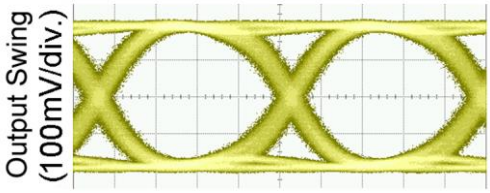
Time (100ps/div.)

5Gbps Data



Time (50ps/div.)

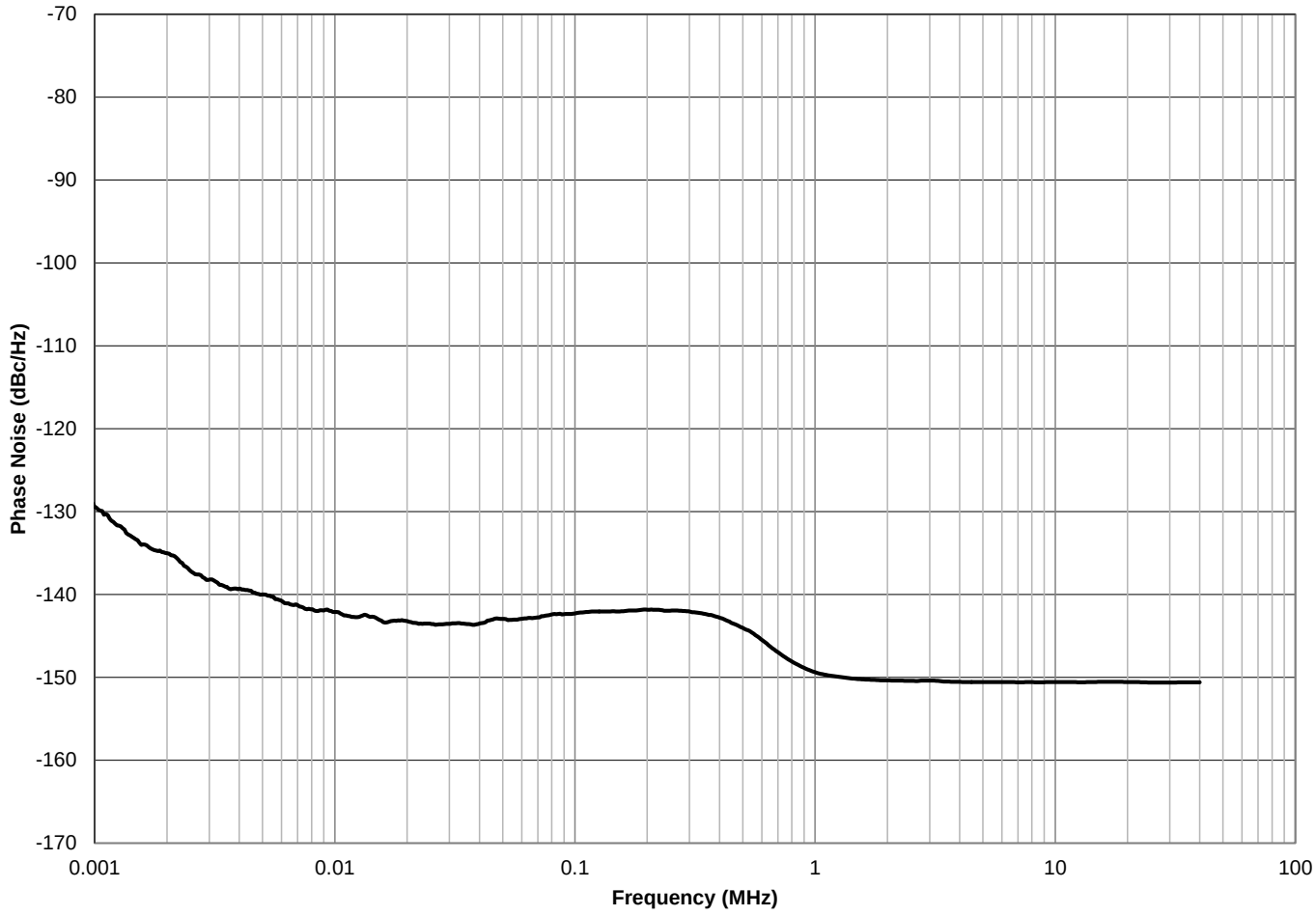
10.7Gbps Data



Time (50ps/div.)

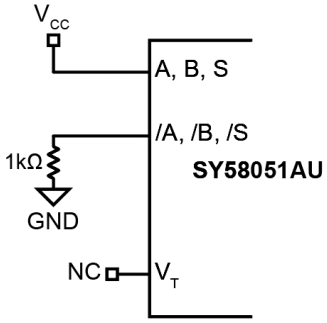
Phase Noise Plot

V_{CC} = 3.0V, CML Input, Temperature = 25°C



Phase Noise at 622MHz over 12kHz to 20MHz
Additive RMS Phase Jitter: 46fs$_{RMS}$

Input Interface Applications



NOTE: INPUT HIGH LEVEL SHOWN

Figure 5. Static Input Level

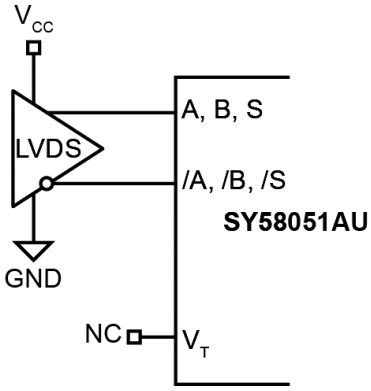
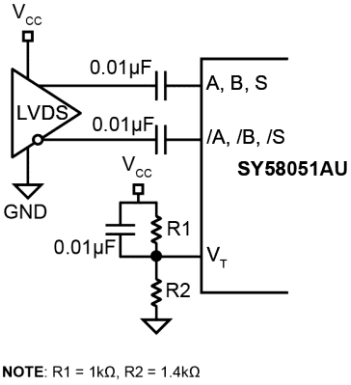


Figure 6. LVDS Interface (DC-Coupled)



NOTE: R1 = 1kΩ, R2 = 1.4kΩ

Figure 7. LVDS Interface (AC-Coupled)
Note: Be certain that the LVDS driver can be AC-coupled.

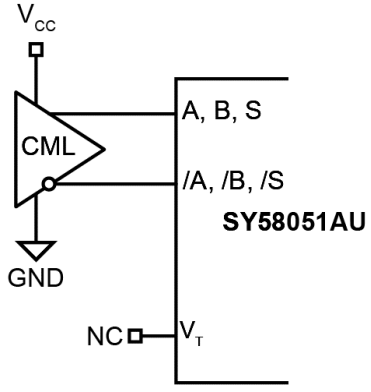
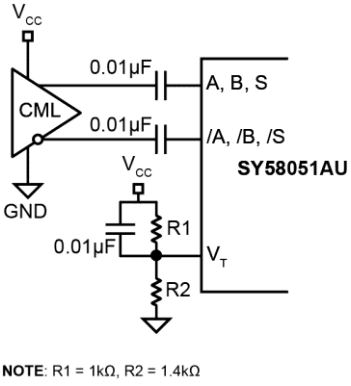


Figure 8. CML Interface (DC-Coupled)



NOTE: R1 = 1kΩ, R2 = 1.4kΩ

Figure 9. CML Interface (AC-Coupled)

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Input Interface Applications (Continued)

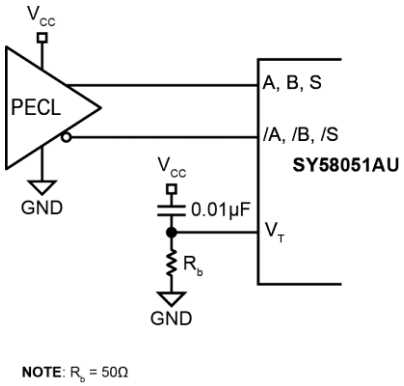


Figure 10. PECL Interface (DC-Coupled)

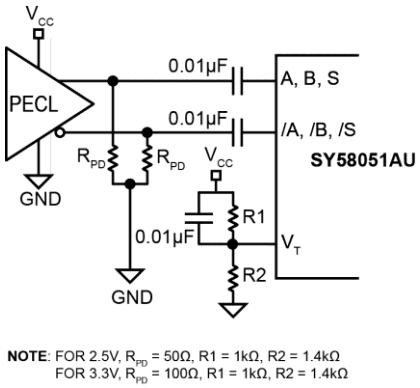
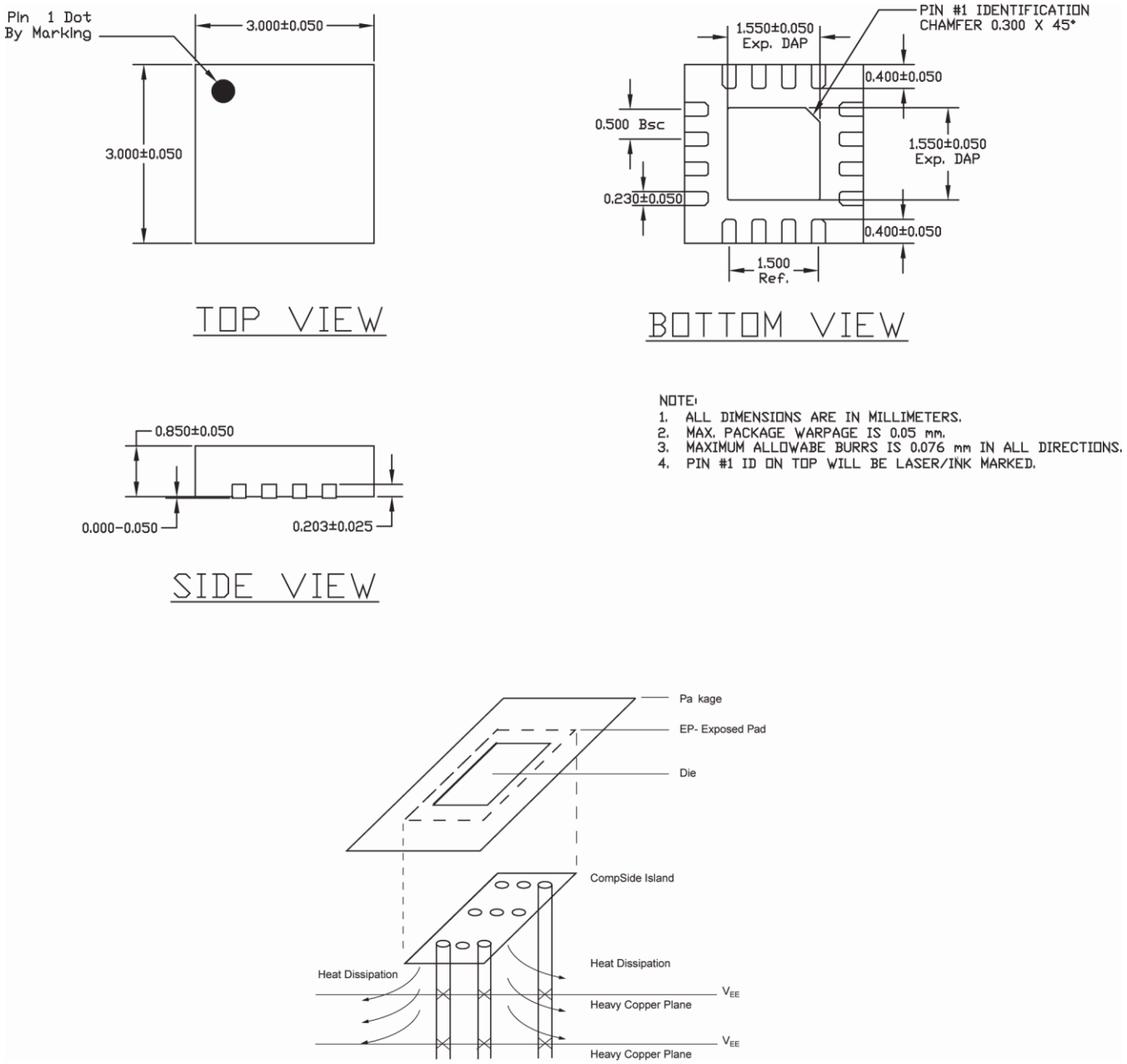


Figure 11. PECL Interface (AC-Coupled)

Related Product and Support Documentation

Part Number	Function	Datasheet Link
SY58016L	3.3V 10Gbps Differential CML Line Driver/Receiver with Internal Termination	http://www.micrel.com/_PDF/HBW/sy58016l.pdf
SY58052AU	10.7Gbps Clock/Data Retimer with 50Ω Input Termination	http://www.micrel.com/_PDF/HBW/SY58052AU.pdf
TCG Solutions	New Products and Applications	http://www.micrel.com/index.php/en/products/clock-timing.html

Package Information[17]



16-Pin QFN

Note:

17. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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