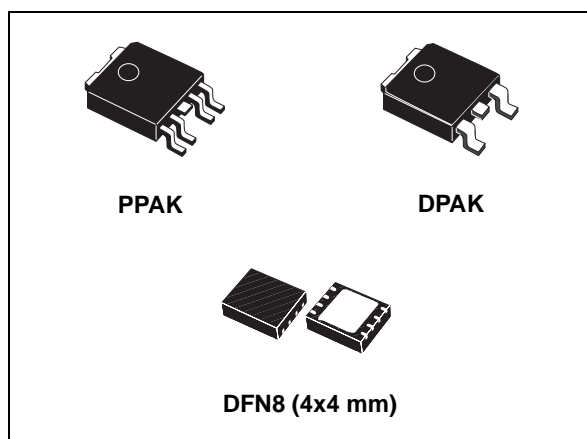


## Ultra low drop BiCMOS voltage regulator

Datasheet - production data



- Temperature range: -40 to 125 °C
- Fast dynamic response to line and load changes
- Stable with ceramic capacitor
- Available in PPAK, DPAK and DFN8 (4x4 mm)

### Applications

- Microprocessor power supply
- DSP power supply
- Post regulators for switching suppliers
- High efficiency linear regulator

### Features

- 0.8 A guaranteed output current
- Ultra low-dropout voltage (150 mV typ. @ 0.8 A load, 20 mV typ. @ 150 mA load)
- Very low quiescent current (1 mA typ. @ 0.8 A load, 1  $\mu$ A max. @ 25 °C in off mode)
- Logic-controlled electronic shutdown
- Current and thermal internal limit
- $\pm 1.5\%$  output voltage tolerance @ 25 °C
- Fixed and ADJ output voltages: 1.22 V, 1.8 V, 2.5 V, 3.3 V, ADJ

### Description

The LD39080 is a fast, ultra low drop linear regulator which operates from 2.5 V to 6 V input supply.

A wide range of output options is available. The low drop voltage, low noise, and ultra low quiescent current make it suitable for low voltage microprocessors and memory applications. The device is developed on the BiCMOS process which allows the low quiescent current operation regardless of the output load current.

Table 1. Device summary

Part numbers			Output voltage
DPAK (tape and reel)	PPAK (tape and reel)	DFN8 (4x4 mm) <sup>(1)</sup>	
LD39080DT12-R		LD39080PU12R	1.22 V
LD39080DT18-R	LD39080PT18-R	LD39080PU18R	1.8 V
LD39080DT25-R	LD39080PT25-R	LD39080PU25R	2.5 V
LD39080DT33-R	LD39080PT33-R	LD39080PU33R	3.3 V
	LD39080PT-R	LD39080PU-R	ADJ from 1.22 to 5.0 V

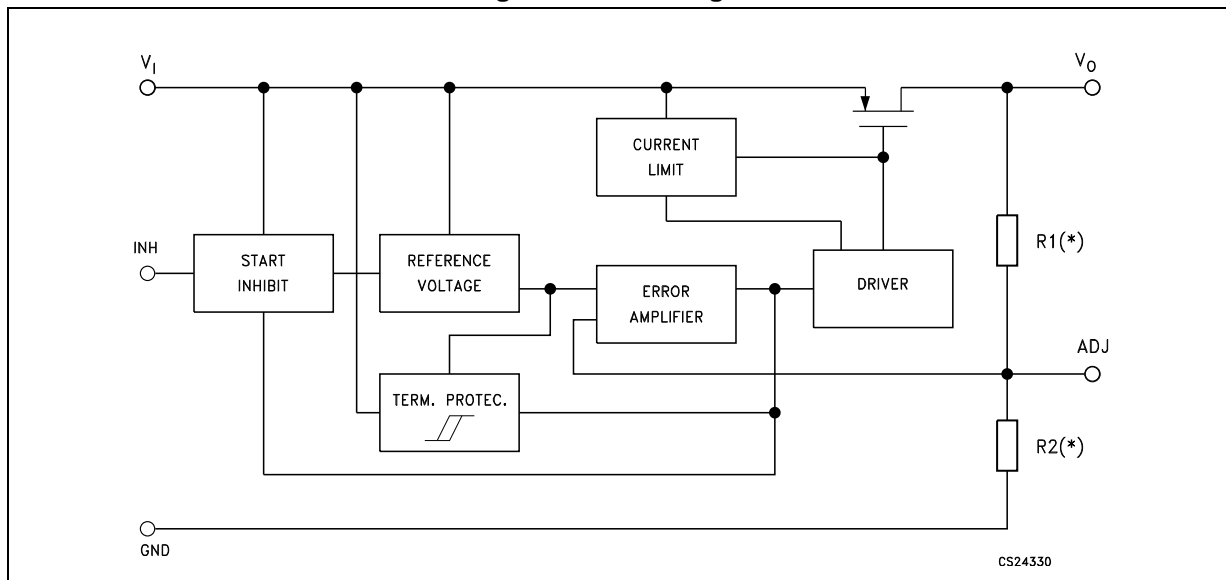
1. Available on request.

# Contents

<b>1</b>	<b>Diagram</b> .....	<b>3</b>
<b>2</b>	<b>Pin configuration</b> .....	<b>4</b>
<b>3</b>	<b>Typical application circuits</b> .....	<b>5</b>
<b>4</b>	<b>Maximum ratings</b> .....	<b>7</b>
<b>5</b>	<b>Electrical characteristics</b> .....	<b>8</b>
<b>6</b>	<b>Typical performance characteristics</b> .....	<b>10</b>
<b>7</b>	<b>Application notes</b> .....	<b>13</b>
	7.1 External capacitor .....	13
	7.2 Input capacitor .....	13
	7.3 Output capacitor .....	13
	7.4 Thermal note .....	13
	7.5 Inhibit input operation .....	13
<b>8</b>	<b>Package mechanical data</b> .....	<b>14</b>
<b>9</b>	<b>Packaging mechanical data</b> .....	<b>21</b>
<b>10</b>	<b>Revision history</b> .....	<b>24</b>

# 1 Diagram

Figure 1. Block diagram



(\*) Not present on ADJ version.

## 2 Pin configuration

Figure 2. Pin connections (top view for DPAK and PPAK, bottom view for DFN8)

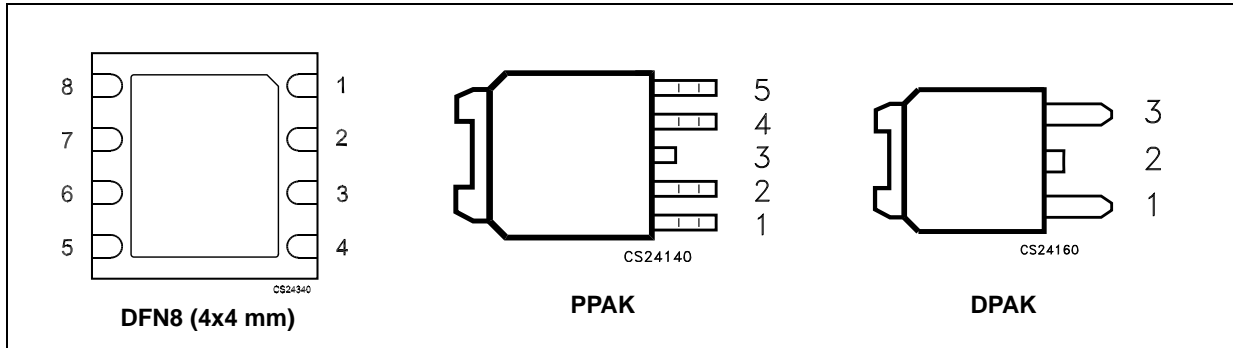


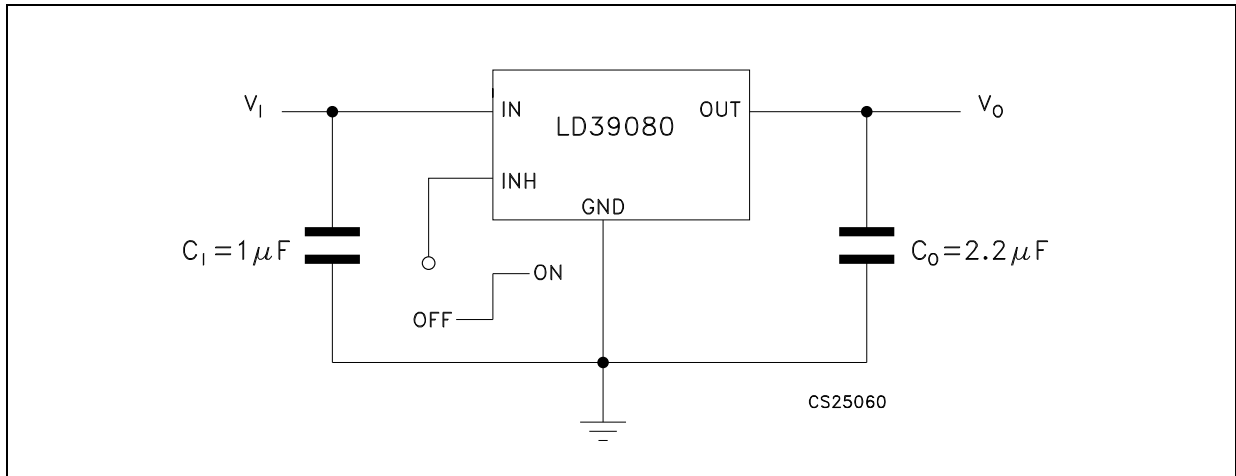
Table 2. Pin description

Pin			Symbol	Note
DFN8 (4x4 mm)	PPAK	DPAK		
8	5		$V_{SENSE}/N.C.$	Fixed version: to be connected to LDO output voltage pins for DFN package and not connected on PPAK
			ADJ	Adjustable version: error amplifier input pin for $V_O$ from 1.22 to 5.0 V
3, 4	2	1	$V_I$	LDO input voltage: $V_I$ from 2.5 V to 6 V, $C_I=1 \mu F$ not farther than 1 cm from input pin
6, 7	4	3	$V_O$	LDO output voltage pins, with minimum $C_O = 2.2 \mu F$ needed for stability (refer to $C_O$ vs ESR stability chart)
2	1		$V_{INH}$	Inhibit input voltage: on mode when $V_{INH} \geq 2 V$ , off mode when $V_{INH} \leq 0.3 V$ (do not leave it floating, not internally pulled down/up)
1	3	2	GND	Common ground
5			N.C.	Not connected

### 3 Typical application circuits

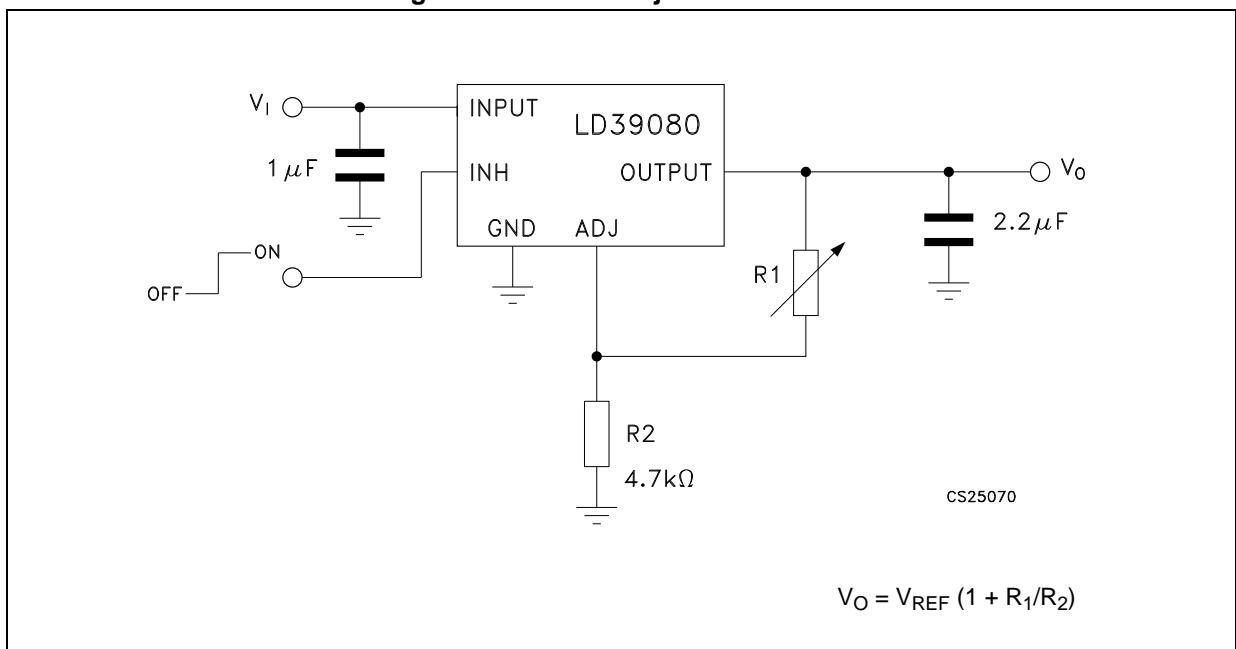
( $C_I$  and  $C_O$  capacitors have to be placed as closer as possible to the IC pin)

Figure 3. LD39080 fixed version with inhibit



Note: The inhibit pin is not internally pulled down/up, therefore it must not be left floating. The device has to be disabled when it is connected to GND or to a positive voltage less than 0.3 V.

Figure 4. LD39080 adjustable version



Note: Set  $R_2$  as closer as possible to 4.7 K $\Omega$ .

Figure 5. LD39080 DPAK

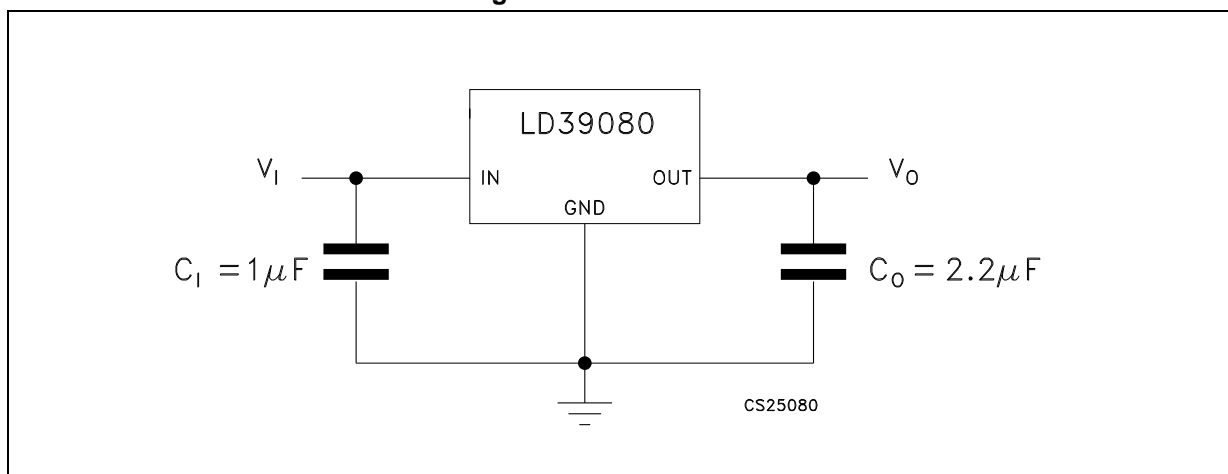
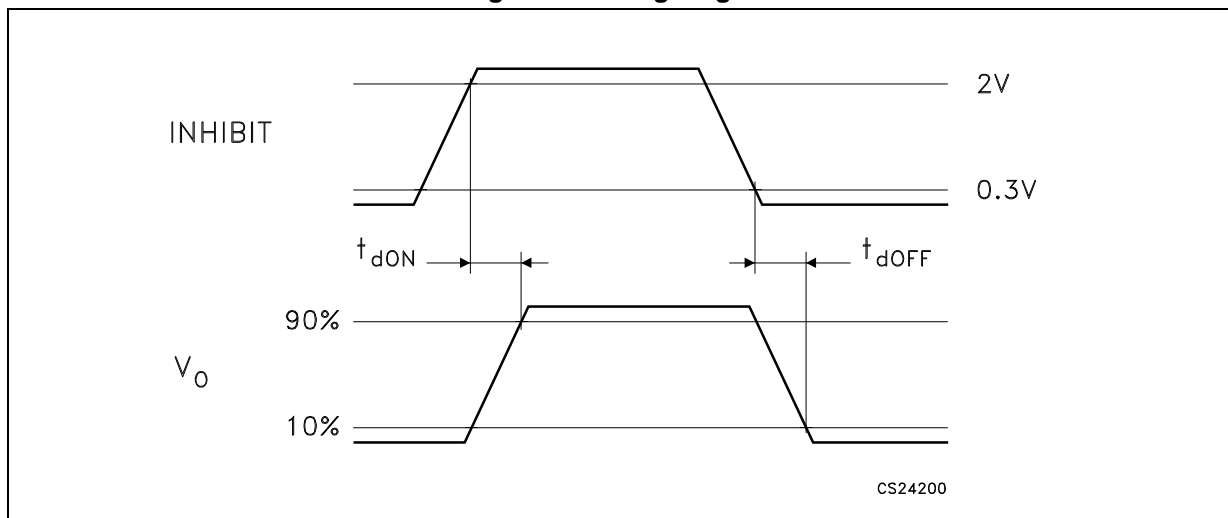


Figure 6. Timing diagram



## 4 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_I$	DC input voltage	-0.3 to 6.5	V
$V_{INH}$	Inhibit input voltage	-0.3 to $V_I + 0.3$ (6.5 V max.)	V
$V_O$	DC output voltage	-0.3 to $V_I + 0.3$ (6.5 V max.)	V
$V_{ADJ}$	ADJ pin voltage	-0.3 to $V_I + 0.3$ (6.5 V max.)	V
$I_O$	Output current	Internally limited	mA
$P_D$	Power dissipation	Internally limited	mW
$T_{STG}$	Storage temperature range	-50 to 150	°C
$T_{OP}$	Operating junction temperature range	-40 to 125	°C

*Note:* Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

**Table 4. Thermal data**

Symbol	Parameter	PPAK	DPAK	DFN8 (4x4 mm) <sup>(1)</sup>	Unit
$R_{thJA}$	Thermal resistance junction-ambient	100	100	40	°C/W
$R_{thJC}$	Thermal resistance junction-case	8	8	10	°C/W

1. With a PCB ground plane and heatsink.

## 5 Electrical characteristics

$T_J = 25\text{ °C}$ ,  $V_I = V_O + 1\text{ V}$ ,  $C_I = 1\text{ }\mu\text{F}$ ,  $C_O = 2.2\text{ }\mu\text{F}$ ,  $I_{LOAD} = 10\text{ mA}$ ,  $V_{INH} = 2\text{ V}$ , unless otherwise specified.

**Table 5. Electrical characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_I$	Operating input voltage		2.5		6	V
$V_O$	Output voltage tolerance	$V_I = V_O + 1\text{ V}$ , $I_{LOAD} = 10\text{ mA to }0.8\text{ A}$	-1.5		1.5	% of $V_{O(NOM)}$
		$V_I = V_O + 1\text{ V to }6\text{ V}$ , $I_{LOAD} = 10\text{ mA to }0.8\text{ A}$ $T_J = -40\text{ to }125\text{ °C}$	-3		3	
$V_{REF}$	Reference voltage			1.22		V
$\Delta V_O$	Output voltage line regulation	$V_I = V_O + 1\text{ V to }6\text{ V}$		0.04		%
		$V_I = V_O + 1\text{ V to }6\text{ V}$ , $T_J = -40\text{ to }125\text{ °C}$		0.1	0.2	%
$\Delta V_O / \Delta I_{LOAD}$	Output voltage load regulation	$I_{LOAD} = 10\text{ mA to }0.8\text{ A}$		0.06		% / A
		$I_{LOAD} = 10\text{ mA to }0.8\text{ A}$ , $T_J = -40\text{ to }125\text{ °C}$		0.2	0.4	
$V_{DROP}$	Dropout voltage ( $V_I - V_O$ )	$I_{LOAD} = 150\text{ mA}$ , $T_J = -40\text{ to }125\text{ °C}$		20	40	mV
		$I_{LOAD} = 0.8\text{ A}$ , $T_J = -40\text{ to }125\text{ °C}$		150	300	
$I_Q$	Quiescent current: on mode	$I_{LOAD} = 10\text{ mA to }0.8\text{ A}$ , $V_{INH} = 2\text{ V}$ $T_J = -40\text{ to }125\text{ °C}$		1	2.5	mA
	Quiescent current: off mode	$V_{INH} = 0.3\text{ V}$			1	$\mu\text{A}$
		$V_{INH} = 0.3\text{ V}$ , $T_J = -40\text{ to }125\text{ °C}$			5	
<b>Short-circuit protection</b>						
$I_{SC}$	Short-circuit protection	$R_L = 0$		1.6		A
<b>Inhibit Input</b>						
$V_{INH}$	Inhibit threshold low	$V_I = 2.5\text{ to }6\text{ V off}$ $T_J = -40\text{ to }125\text{ °C}$			0.3	V
	Inhibit threshold high		2			



Table 5. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{D-OFF}$	Current limit	$I_{LOAD} = 0.8 \text{ A}$ , $V_O = 3.3 \text{ V}$		15		$\mu\text{s}$
$T_{D-ON}$	Current limit	$I_{LOAD} = 0.8 \text{ A}$ , $V_O = 3.3 \text{ V}$		15		
$I_{INH}$	Inhibit input current <sup>(1)</sup>	$V_I = 6 \text{ V}$ , $V_{INH} = 0 \text{ to } 6 \text{ V}$		$\pm 0.1$	$\pm 1$	$\mu\text{A}$
<b>AC parameters</b>						
SVR	Supply voltage rejection	$V_I = 4.5 \pm 1 \text{ V}$ , $V_O = 3.3 \text{ V}$ , $I_{LOAD} = 10 \text{ mA}$ ,	$f = 120 \text{ Hz}$		65	dB
			$f = 1 \text{ kHz}$		55	
$e_N$	Output noise voltage	$B_W = 10 \text{ Hz to } 100 \text{ kHz}$ , $C_O = 2.2 \mu\text{F}$ , $V_O = 2.5 \text{ V}$		100		$\mu\text{V}_{RMS}$
$T_{SHDN}$	Thermal shutdown off			170		$^{\circ}\text{C}$
	Hysteresis			10		

1. Guaranteed by design.

## 6 Typical performance characteristics

$T_J = 25\text{ }^\circ\text{C}$ ,  $V_I = V_O + 1\text{ V}$ ,  $C_I = 1\text{ }\mu\text{F}$ ,  $C_O = 2.2\text{ }\mu\text{F}$ ,  $I_{LOAD} = 10\text{ mA}$ ,  $V_{INH} = V_I$ , unless otherwise specified.

Figure 7. Output voltage vs temperature

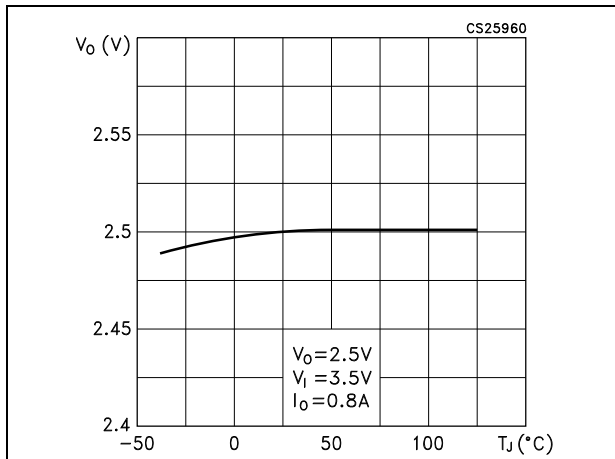


Figure 8. Dropout voltage vs temperature

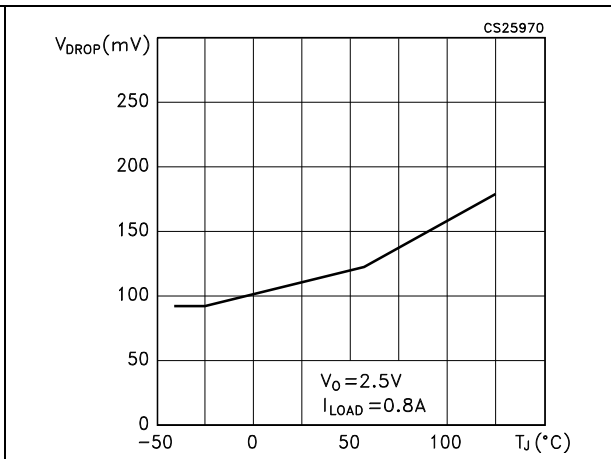


Figure 9. Dropout voltage vs output current

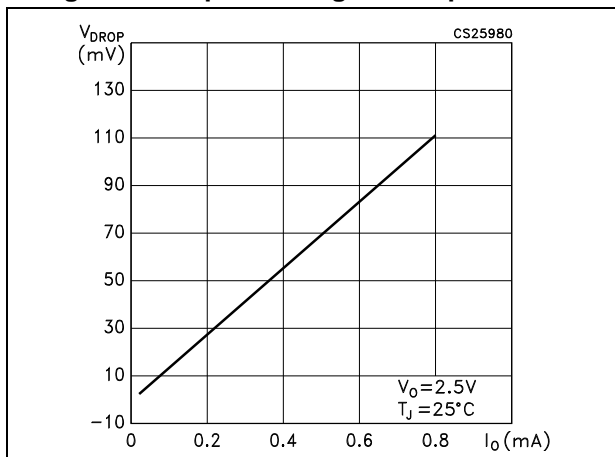


Figure 10. Quiescent current vs output current

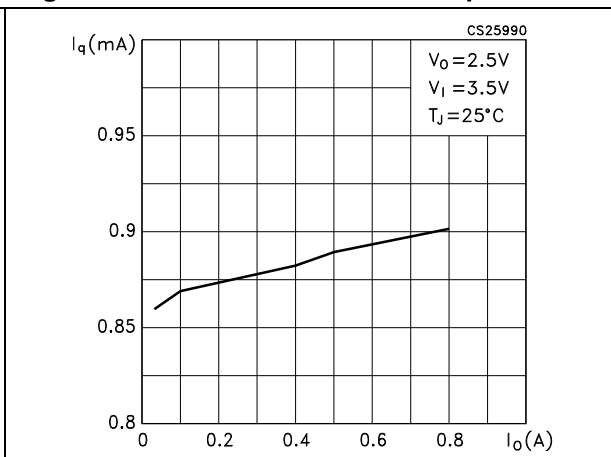


Figure 11. Quiescent current vs supply voltage

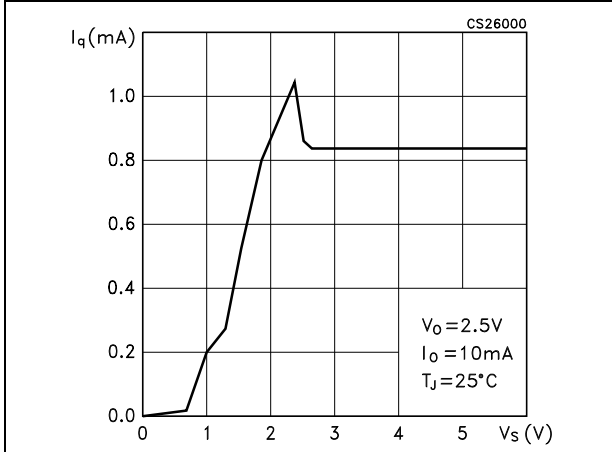


Figure 12. Off-state current vs temperature

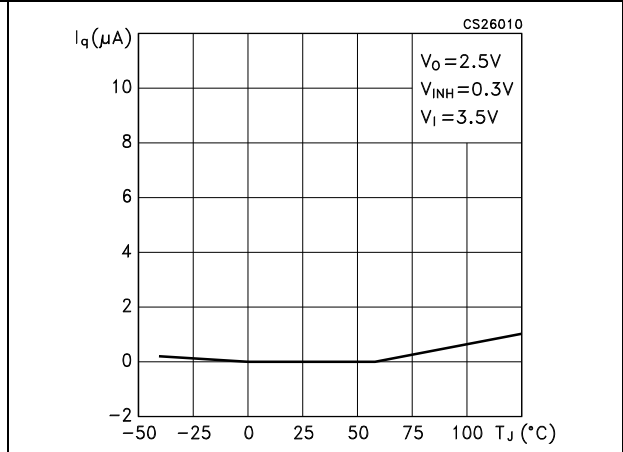


Figure 13. Quiescent current vs temperature

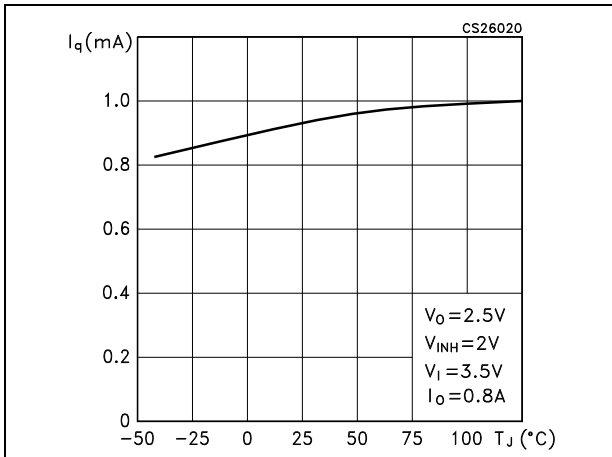


Figure 14. Short-circuit current vs temperature

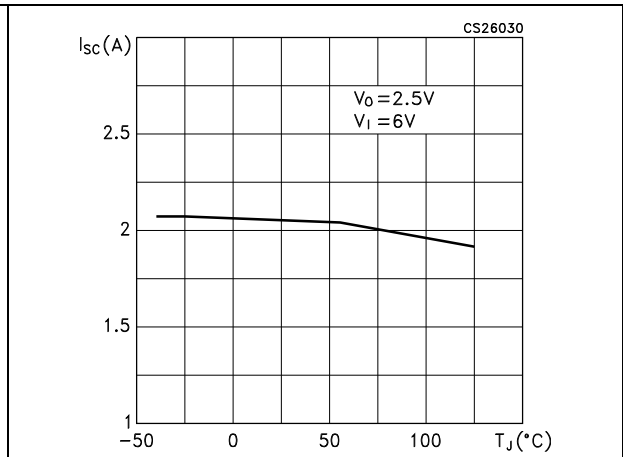


Figure 15. Output voltage vs input voltage

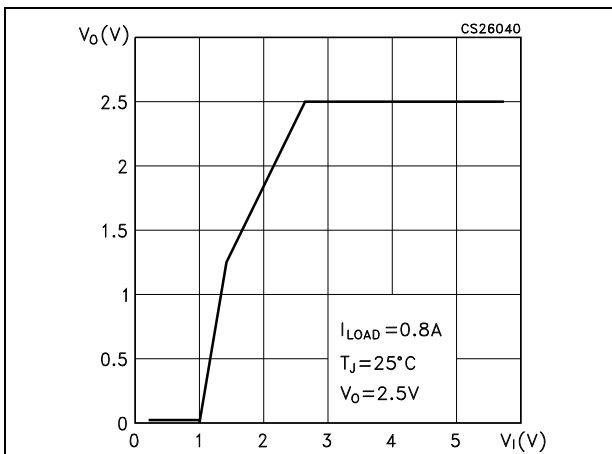


Figure 16. Supply voltage rejection vs temperature

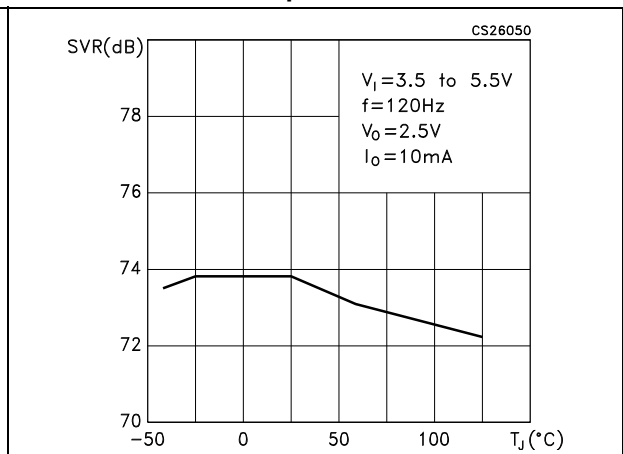


Figure 17. Stability region vs  $C_O$  and ESR (at 100 kHz)

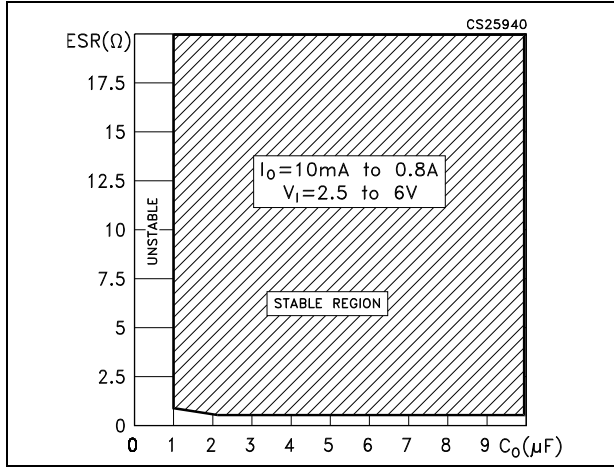


Figure 18. Stability region vs  $C_O$  and low ESR (at 100 kHz)

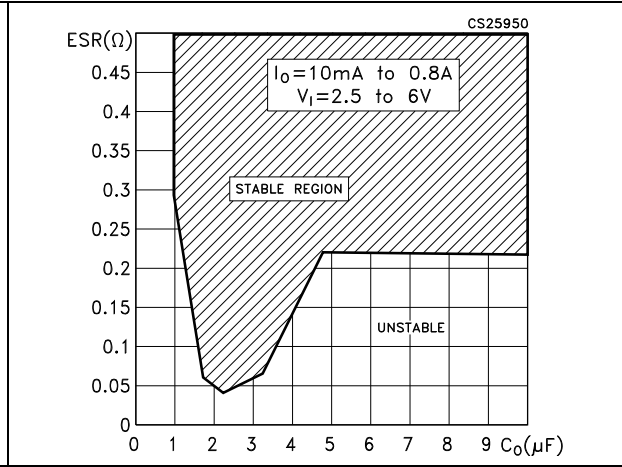


Figure 19. Load transient

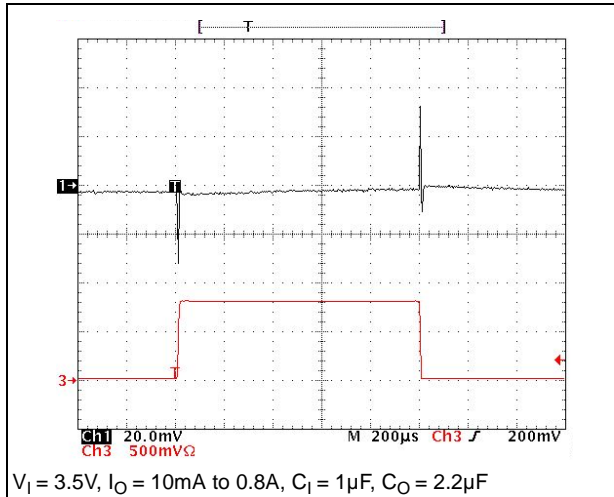
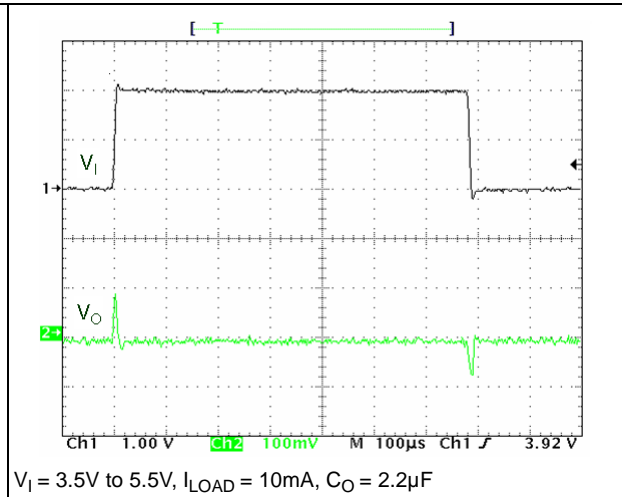


Figure 20. Line transient



## 7 Application notes

### 7.1 External capacitor

The LD39080 requires external capacitors to assure the stability. These capacitors have to meet the requirements of minimum capacitance and equivalent series resistance (see [Figure 17](#) [Figure 18](#)). The input/output capacitors cannot be farther than 1 cm from the relative pins and have to be connected directly to the input/output ground pins using traces without any current flowing through them. Ceramic or electrolytic capacitors can be used.

### 7.2 Input capacitor

An input capacitor, whose minimum value is 1  $\mu\text{F}$ , is required (the amount of capacitance can be increased without any limit). This capacitor cannot be farther than 1 cm from the input pin of the device and has to return to clean analog ground. Ceramic, tantalum or film capacitors can be used.

### 7.3 Output capacitor

Ceramic or tantalum capacitors can be used but the output capacitor has to meet the requirements of minimum capacitance and ESR (equivalent series resistance) value. A minimum capacitance of 2.2  $\mu\text{F}$  is a good choice to guarantee the stability of the regulator. Anyway, other  $C_O$  values can be used as per [Figure 17](#) [Figure 18](#), where the allowable ESR range is seen as a function of the output capacitance. The curve represents the stability region over the full temperature and  $I_O$  range.

### 7.4 Thermal note

The output capacitor has to maintain its ESR in the stable region over the operating temperature range to assure the stability. Besides, capacitor tolerance and temperature variation have to be taken into account to assure the minimum amount of capacitance all time.

### 7.5 Inhibit input operation

The inhibit pin can be used to turn off the regulator when pulled down, therefore by reducing the current consumption below 1  $\mu\text{A}$ . When the inhibit feature is not used, this pin has to be tied to  $V_I$  to turn on the regulator output all the time. To assure the right operation, the signal source, used to drive the inhibit pin, has to swing above and below the specified thresholds listed in [Section 5: Electrical characteristics](#) ( $V_{IH}$   $V_{IL}$ ). The inhibit pin must not be left floating because it is not internally pulled down/up.

# 8 Package mechanical data

Figure 21. PPAK drawings

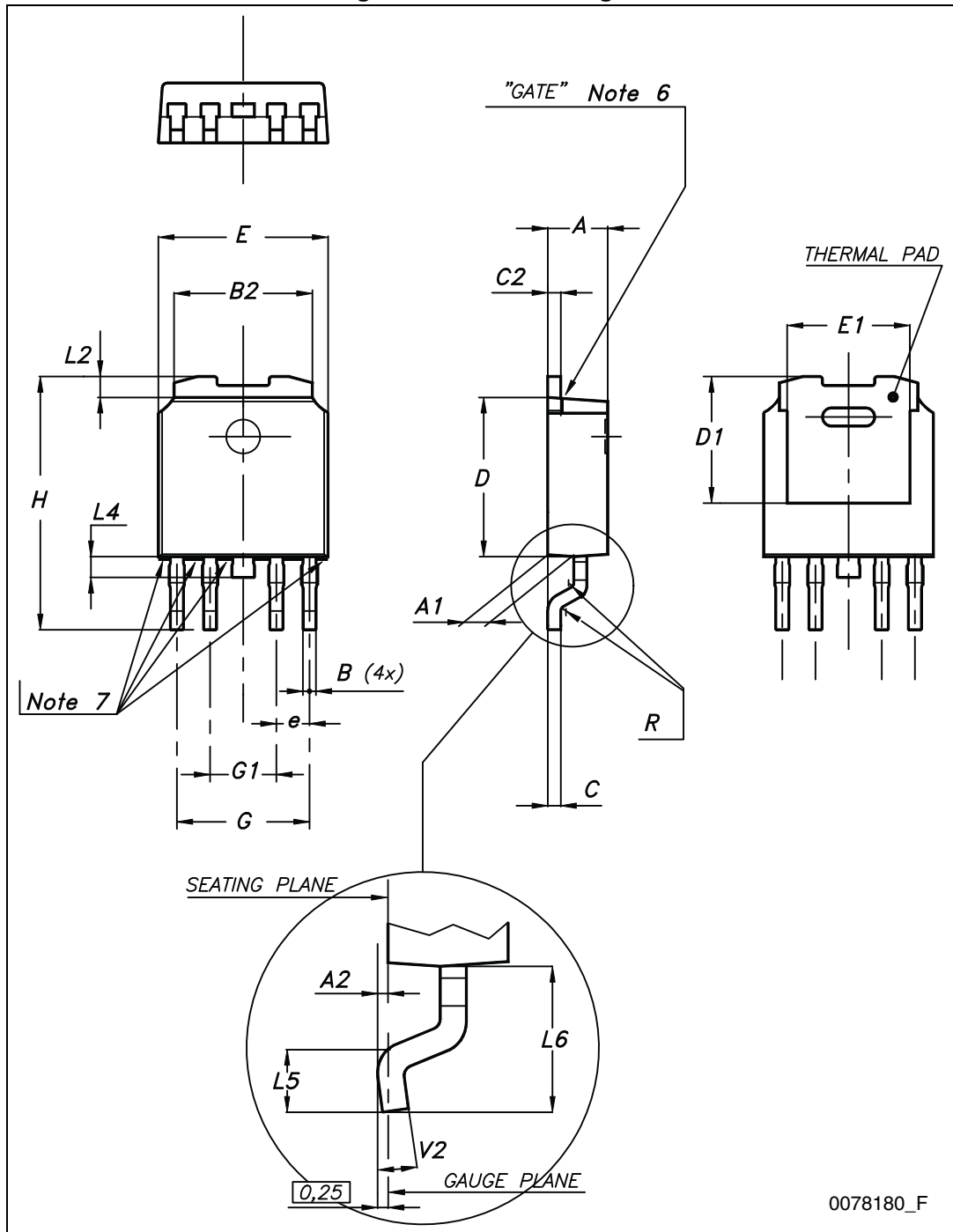
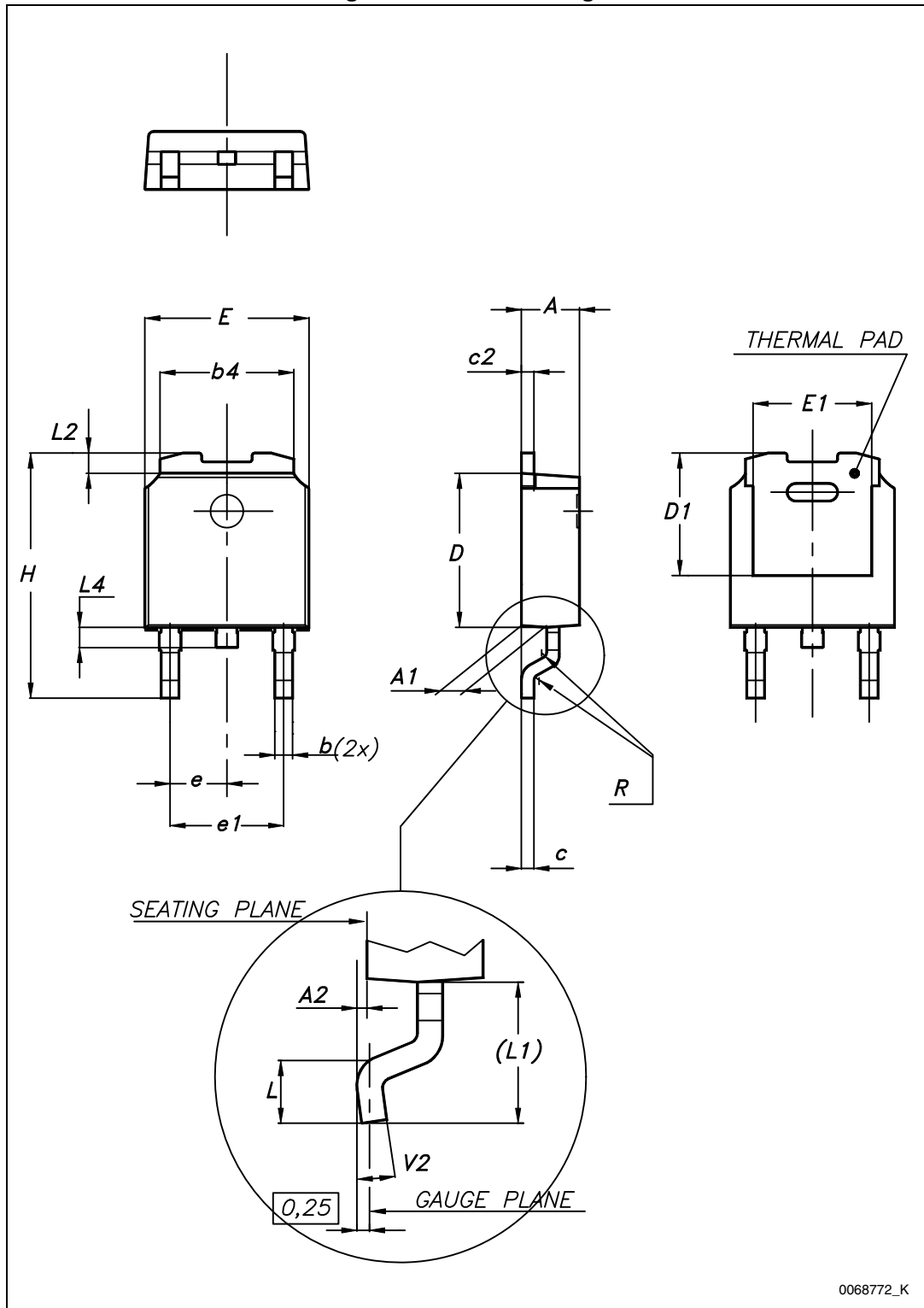


Table 6. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

Figure 22. DPAK drawings



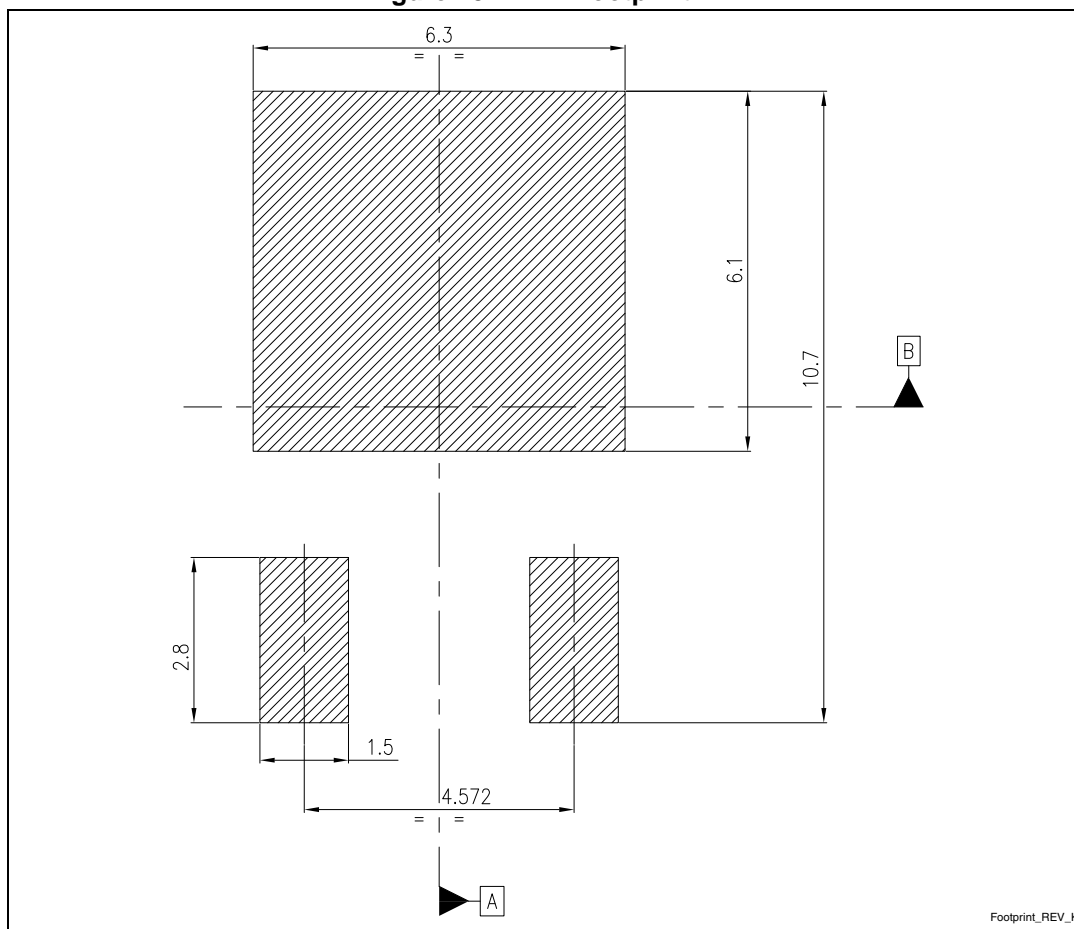
0068772\_K



Table 7. DPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 23. DPAK footprint (a)



a. All dimensions are in millimeters.

Figure 24. DFN8 (4x4 mm) drawings

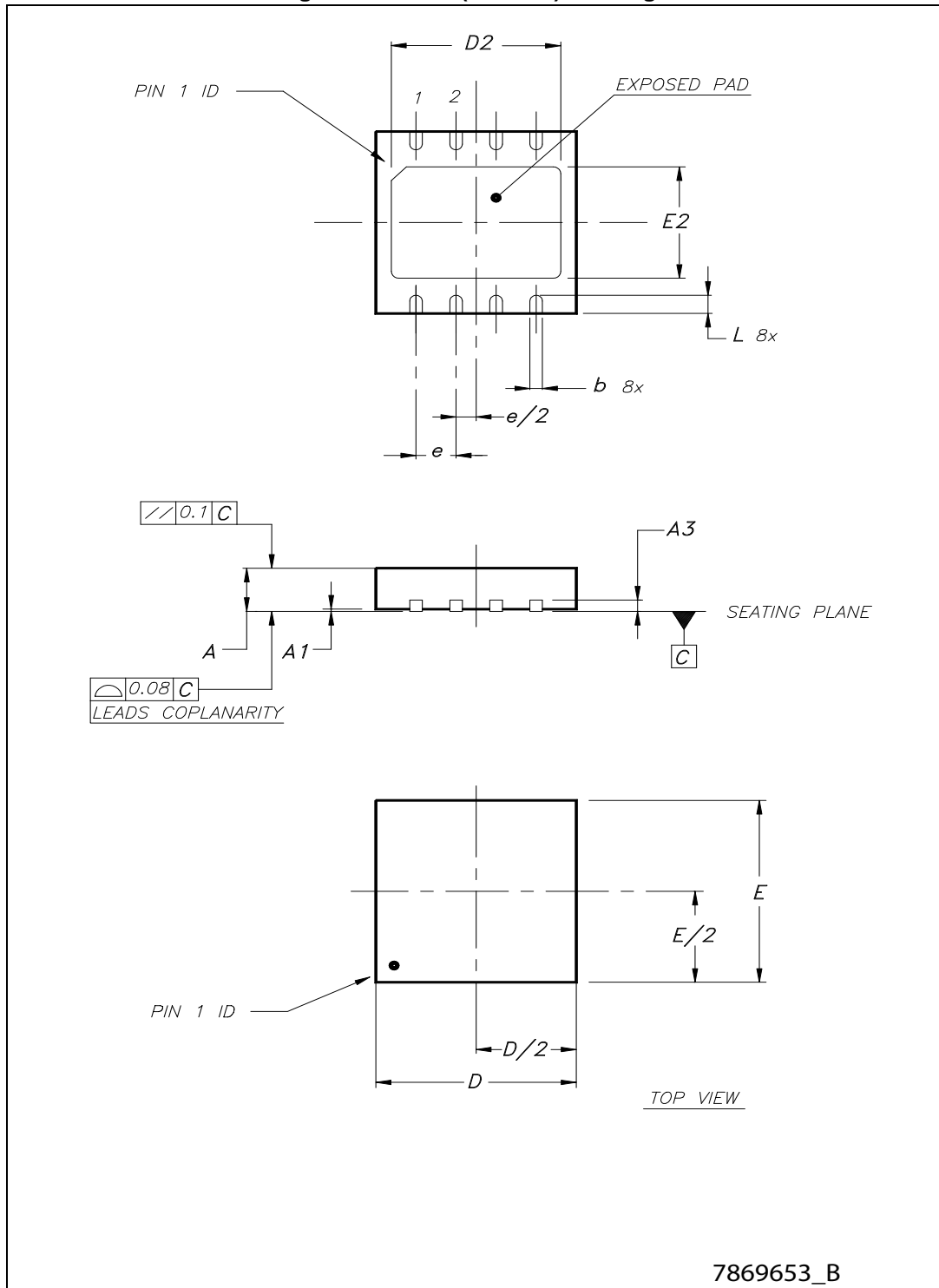
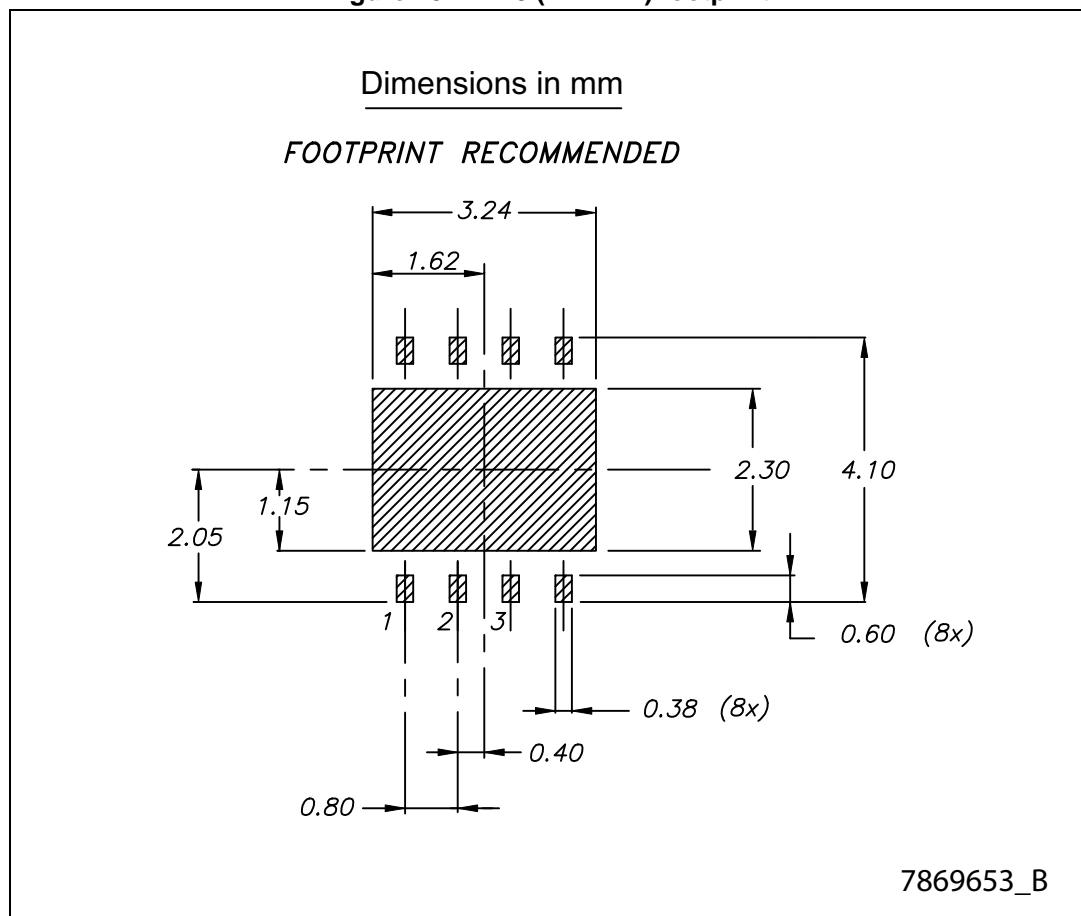


Table 8. DFN8 (4x4 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1
A1	0	0.02	0.05
A3		0.20	
b	0.23	0.30	0.38
D	3.90	4	4.10
D2	2.82	3	3.23
E	3.90	4	4.10
E2	2.05	2.20	2.30
e		0.80	
L	0.40	0.50	0.60

Figure 25. DFN8 (4x4 mm) footprint



# 9 Packaging mechanical data

Figure 26. Tape for PPAK and DPAK

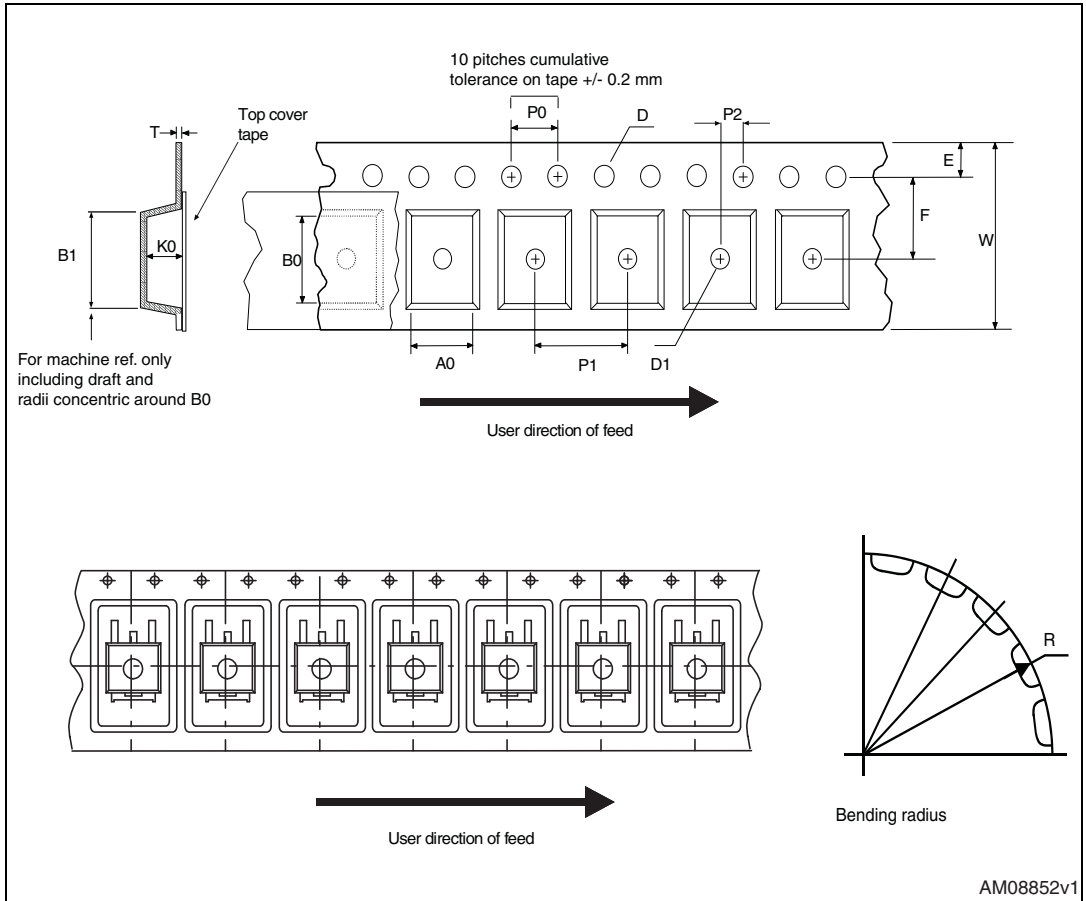


Figure 27. Reel for PPAK and DPAK

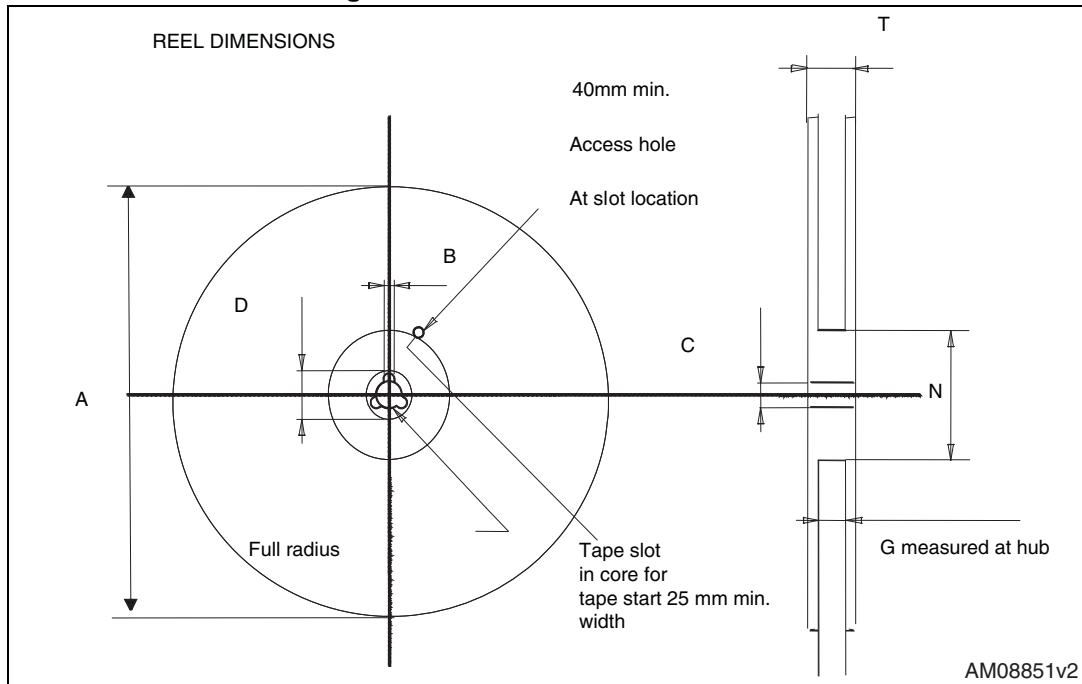


Table 9. PPAK and DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 28. DFN8 (4x4 mm) tape and reel mechanical data

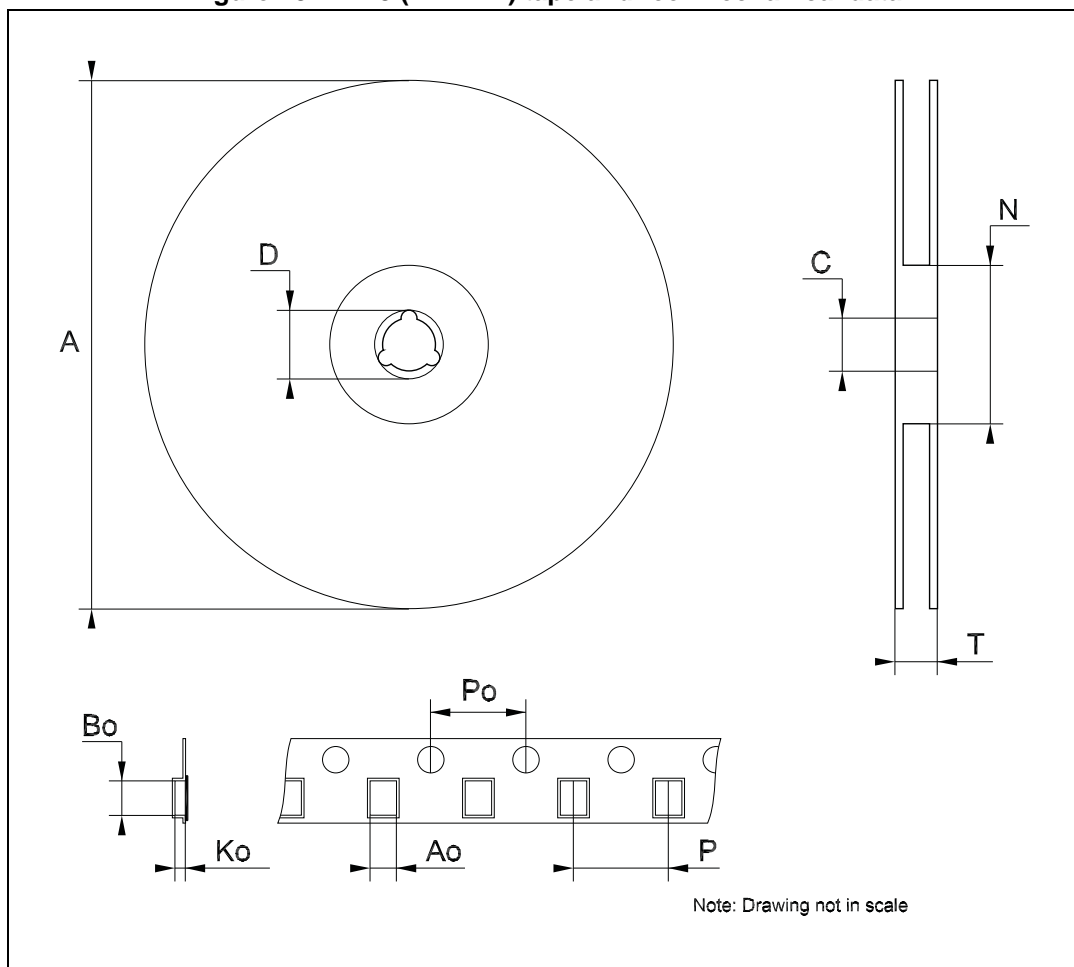


Table 10. DFN8 (4x4 mm) tape and reel dimensions

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	99		101
T			14.4
Ao		4.35	
Bo		4.35	
Ko		1.1	
Po		4	
P		8	

## 10 Revision history

Table 11. Document revision history

Date	Revision	Changes
26-Jan-2007	1	Initial release.
25-Mar-2014	2	Updated features in cover page, <a href="#">Section 5: Electrical characteristics</a> , <a href="#">Section 6: Typical performance characteristics</a> , <a href="#">Section 7: Application notes</a> , <a href="#">Section 8: Package mechanical data</a> . Added <a href="#">Section 9: Packaging mechanical data</a> . Minor text changes.



**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

