19-0737; Rev 0; 1/07

EVALUATION KIT AVAILABLE

MAXIM

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

MAX8784

General Description

The MAX8784 generates supply rails for the thin-film transistor (TFT) liquid-crystal display (LCD) panels in TVs and monitors. It includes a step-up regulator, a regulated positive and a negative charge-pump, three high-current operational amplifiers, and Dual Mode™, logic-controlled, high-voltage switch control block. HVS mode automatically increases the output voltages of the boost regulator and the positive charge-pump to stress test display panels during production. The MAX8784 can operate from input voltages of 4V to 5.5V and is optimized for LCD TV panel and LCD monitor applications.

The step-up DC-DC regulator provides a regulated supply voltage for TFT source drivers. The step-up regulator is a high-frequency (1.2MHz), high-efficiency, current-mode regulator. The step-up regulator has a built-in 110mΩ (typ) power MOSFET. The high-switching frequency allows the use of ultra-small inductors and ceramic capacitors. The current-mode architecture provides fast transient response and easy compensation. The step-up regulator features output undervoltage protection, soft-start, internal current limit, and adjustable output voltage by an external resistive divider.

The three operational amplifiers drive the LCD backplane and the gamma-correction-divider string. Each operational amplifier has a fast slew rate (45V/µs), a wide bandwidth (20MHz), and a high-output short-circuit current (200mA). Each op amp has rail-to-rail input and rail-to-rail output operation.

The positive charge-pump regulator and the negative charge-pump regulator provide regulated supply voltages for the TFT gate drivers. The positive charge pump is a two-stage charge pump, which requires no external diodes. The output voltages of both charge pumps are resistor adjustable. The logic-controlled high-voltage switch allows the manipulation of the positive TFT gate-driver supply.

The MAX8784 is available in a small (5mm x 5mm), low-profile (0.8mm), 40-pin TQFN package and operates over the -40°C to +85°C temperature range.

Applications

LCD TVs and LCD Monitors

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8784ETL+	-40°C to +85°C	40 TQFN 5mm x 5mm	T4055-1

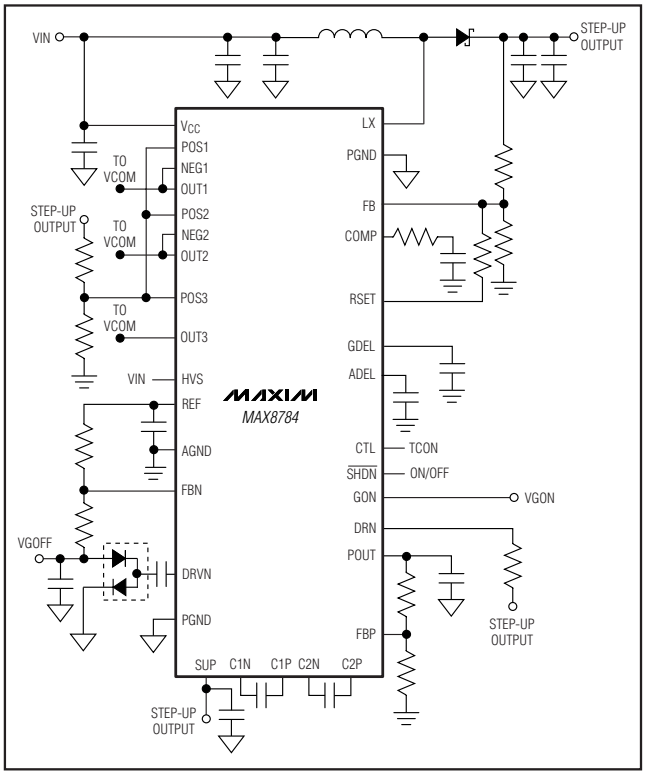
+Denotes a lead(Pb)-free/RoHS-compliant package.

Dual Mode is a trademark of Maxim Integrated Products, Inc.

Features

- **Step-Up Regulator Supply for LCD Panel Source Driver**
  - **Fast Transient Response to Pulsed Load**
  - **Built-In 18V, 4A, 0.11Ω n-Channel Power MOSFET with Lossless Current Sensing**
  - **Cycle-by-Cycle Current-Limit Comparator**
  - **90% Efficiency (5V In to 15V Out)**
  - **1.2MHz Switching Frequency**
- **Three High-Current 19V Operational Amplifiers**
  - **180mA Output Short-Circuit Current**
  - **45V/µs Slew Rate**
  - **20MHz Bandwidth**
  - **Rail-to-Rail Input and Output Operation**
- **Regulated Charge-Pump Tripler with Integrated Diodes for TFT Gate-On Supply**
- **Regulated Charge Pump for TFT Gate-Off Supply**
- **Built-In Sequencing**
  - **Internal Digital Soft-Start**
  - **36V Gate-On Switch**
  - **Startup Timing Capacitors for AVDD and GON**
- **Undervoltage and Thermal Protection**
- **4V to 5.5V Input Operating Range**

Simplified Operating Circuit



Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

ABSOLUTE MAXIMUM RATINGS

V_{CC}, CTL, HVS, $\overline{SHDN}$, ADEL, GDEL to AGND ....-0.3V to +7.5V
REF, COMP, FB, FBN, FBP to AGND .....-0.3V to (V_{CC} + 0.3V)
POS1, NEG1, POS2, NEG2, POS3, OUT1, OUT2,
OUT3 to AGND .....-0.3V to (V_{SUP} + 0.3)
PGND, BGND to AGND.....-0.3V to +0.3V
LX, RSET to PGND .....-0.3V to +22V
SUP to AGND .....-0.3V to +22V
DRVN to AGND.....-0.3V to (V_{SUP} + 0.3V)
C1N, C2N to AGND .....-0.3V to (V_{SUP} + 0.3V)
C1P to AGND .....-0.3V to +30V
POUT to C2P, C1P to C2P.....-0.3V to +22V
C2P, POUT to AGND.....-0.3V to +40V
GON, DRN to AGND .....-0.3V to +40V
DRN to GON.....-30V to +30V
REF Short Circuit to AGND.....Continuous
RMS V_{CC} Current.....50mA
RMS DRVN Current.....400mA
LX, PGND RMS Current Rating.....2.4A
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 35.7mW/°C above +70°C) 2857mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, Circuit of Figure 1, AVDD = SUP = +14V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Input Supply Range		4.0		5.5	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} rising, typical hysteresis = 50mV	2.4	2.6	2.8	V
V_{CC} Quiescent Current	V_{FB} = 1.3V, not switching		1.0		mA
	V_{FB} = 1.1V, switching, no load, V_{SUP} disconnected, V_{FBP} = V_{CC}, V_{FBN} = 0V		4	6	
	$\overline{SHDN}$ = GND			0.05	
$\overline{SHDN}$ Input Low Voltage				0.8	V
$\overline{SHDN}$ Input High Voltage		1.8			V
$\overline{SHDN}$ Input Current		-1		+1	µA
REFERENCE					
REF Output Voltage	No external load	1.238	1.250	1.262	V
REF Load Regulation	0 < I_{LOAD} < 50µA			10	mV
REF Sink Current	In regulation	10			µA
REF Undervoltage Lockout Threshold	Rising edge, typical hysteresis = 200mV		1.0	1.15	V
OSCILLATOR AND TIMING					
Frequency		1000	1200	1400	kHz
Oscillator Maximum Duty Cycle		87	90	93	%
Duration to Trigger Fault Condition		47	55	65	ms
ADEL, GDEL Capacitor Charge Current		4	5	6	µA
ADEL, GDEL Turn-On Threshold			1.25	1.32	V
STEP-UP REGULATOR					
FB Regulation Voltage	FB = COMP, C_{COMP} = 1nF	1.235	1.246	1.256	V
	FB = COMP, C_{COMP} = 1nF, +25°C to +85°C	1.238	1.246	1.256	
FB Fault-Trip Level	Falling edge	0.96	1.00	1.04	V
FB Load Regulation	0 < I_{LOAD} < full		-1		%
FB Line Regulation	V_{CC} = 4.5V to 5.5V		0.25		%/V
FB Input Bias Current	V_{FB} = 1.25V		100	200	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, Circuit of Figure 1, AVDD = SUP = +14V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FB Transconductance	ΔI_{COMP} = ±2.5µA, FB = COMP	75	160	280	µS
LX Current Limit	V_{FB} = 1.1V, duty cycle = 75%	3.5	4.0	4.6	A
LX On-Resistance	I_{LX} = 1.0A		0.10	0.19	Ω
Current-Sense Transresistance		0.10	0.20	0.26	V/A
Soft-Start Period	7-bit current ramp		3		ms
POSITIVE CHARGE-PUMP REGULATOR					
V_{SUP} Input Supply Range		6		19	V
V_{SUP} Overvoltage Charge-Pump Inhibit	V_{SUP} = rising, typical hysteresis = 200mV	20	21	22	V
FBP Regulation Voltage		1.225	1.25	1.275	V
FBP Line Regulation Error	V_{SUP} = 10V ~ 19V, V_{POUT} = 28V		0.1		%/V
FBP Input Bias Current	V_{FBP} = 1.5V	-100		+100	nA
POUT Output-Voltage Range	I_{VGON} = 0mA			36	V
POUT Fixed Output Voltage	HVS = V_{CC}, I_{POUT} = 0mA	29.1	30	30.9	V
POUT Output Current Limit	Not in dropout, V_{SUP} = 9V, V_{POUT} = 24V	20	50		mA
C1N, C2N High-Side On-Resistance				9.0	Ω
C1N, C2N Low-Side On-Resistance				6.0	Ω
C1P Switch On-Resistance				15.0	Ω
C2P Switch On-Resistance				10.0	Ω
POUT Switch On-Resistance				10.0	Ω
FBP Fault-Trip Level	Falling edge	0.96	1.00	1.04	V
Positive Charge-Pump Soft-Start Period	7-bit voltage ramp		3		ms
NEGATIVE CHARGE-PUMP REGULATOR					
FBN Regulation Voltage	V_{REF} - V_{FBN}	0.985	1.00	1.015	V
FBN Input Bias Current	V_{FBN} = 250mV	-50		+50	nA
FBN Line Regulation Error	V_{SUP} = 11V to 19V, VGOFF = -9V, I_{VGOFF} = -20mA		0.1		%/V
DRVN PCH On-Resistance				10	Ω
DRVN NCH On-Resistance				6	Ω
FBN Fault-Trip Level	Rising edge		450		mV
Negative Charge-Pump Soft-Start Period	7-bit voltage ramp		3		ms
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
CTL Input-Low Voltage				0.8	V
CTL Input-High Voltage		1.8			V
CTL Input Current	CTL = 0V or V_{CC}	-1		+1	µA
CTL-to-GON Rising Propagation Delay			200		ns
CTL-to-GON Falling Propagation Delay			200		ns
GON-to-POUT Switch On-Resistance	V_{GDEL} = 1.5V, CTL = V_{CC}		10	20	Ω
GON-to-POUT Switch Saturation Current	V_{POUT} - V_{GON} > 5V	180			mA
GON-to-DRN Switch On-Resistance	V_{GDEL} = 1.5V, CTL = 0V			60	Ω
GON-to-DRN Switch Saturation Current	V_{GON} - V_{DRN} > 5V	35			mA
GON-to-PGND Switch On-Resistance	V_{GDEL} = 1.0V		100		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, Circuit of Figure 1, AVDD = SUP = +14V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATIONAL AMPLIFIERS					
SUP Supply Range		6		19	V
SUP Overvoltage Fault Threshold	(Note 1)	19.1	20	21.0	V
SUP Supply Current	Buffer configuration, V_{POSx} = V_{SUP} / 2, no load		11	15	mA
Input Offset Voltage	V_{NEGx}, V_{POSx} = V_{SUP} / 2,			12	mV
Input Bias Current	V_{NEGx}, V_{POSx} = V_{SUP} / 2	-1		+1	µA
Input Common-Mode Voltage Range		0		V_{SUP}	V
Input Common-Mode Rejection Ratio	1V < V_{NEGx}, V_{POSx} < (V_{SUP} - 1)		80		dB
Output Voltage-Swing High	I_{OUTx} = 1mA	V_{SUP} - 50			mV
	I_{OUTx} = 25mA	V_{SUP} - 300			
Output Voltage-Swing Low	I_{OUTx} = -1mA			50	mV
	I_{OUTx} = -25mA			300	
Large-Signal Voltage Gain	V_{OUTx} = 1V to V_{SUP} - 1V		80		dB
Slew Rate	C_{LOAD} = 20pF		45		V/µs
-3dB Bandwidth	C_{LOAD} = 20pF		20		MHz
Short-Circuit Current	Short to V_{SUP} / 2, sourcing		140		mA
	Short to V_{SUP} / 2, sinking		220		
HVS FUNCTION					
HVS Input-Low Voltage				0.8	V
HVS Input-High Voltage		1.8			V
HVS Input Pulldown Resistance		5	10	50	kΩ
RSET Output On-Resistance	HVS = V_{CC}		5	20	Ω
RSET Output Leakage	HVS = AGND			1	µA

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, Circuit of Figure 1, AVDD = SUP = +14V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Input Supply Range		4.0		5.5	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} rising, typical hysteresis = 50mV	2.4		2.8	V
V_{CC} Quiescent Current	V_{FB} = 1.1V, switching, no load, AVDD isolated from SUP, V_{FBP} = V_{CC}, V_{FBN} = 0V			6	mA
	$\overline{SHDN}$ = GND			0.05	
$\overline{SHDN}$ Input-Low Voltage				0.8	V
$\overline{SHDN}$ Input-High Voltage		1.8			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, Circuit of Figure 1, AVDD = SUP = +14V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE					
REF Output Voltage	No external load	1.232		1.262	V
REF Load Regulation	$0 < I_{LOAD} < 50\mu A$			10	mV
REF Sink Current	In regulation	10			µA
REF Undervoltage Lockout Threshold	Rising edge, typical hysteresis = 200mV			1.15	V
OSCILLATOR AND TIMING					
Frequency		950		1400	kHz
Oscillator Maximum Duty Cycle		87		93	%
Duration-to-Trigger Fault Condition		47		69	ms
ADEL, GDEL Capacitor Charge Current		4		6	µA
ADEL, GDEL Turn-On Threshold		1.18		1.32	V
STEP-UP REGULATOR					
FB Regulation Voltage	FB = COMP, C_{COMP} = 1nF	1.230		1.262	V
FB Fault Trip Level	Falling edge	0.96		1.04	V
FB Transconductance	ΔI_{COMP} = ±2.5µA, FB = COMP	75		280	µS
LX Current Limit	V_{FB} = 1.1V, duty cycle = 75%	3.0		5.0	A
LX On-Resistance	I_{LX} = 1.0A			0.19	Ω
Current-Sense Transresistance		0.10		0.26	V/A
POSITIVE CHARGE-PUMP REGULATOR					
V_{SUP} Input Supply Range		6		19	V
V_{SUP} Overvoltage Charge-Pump Inhibit	V_{SUP} = rising, typical hysteresis = 200mV	20		22	V
FBP Regulation Voltage		1.225		1.275	nA
POUT Output-Voltage Range	I_{POUT} = 0mA	V_{SUP}		36	V
POUT Fixed-Output Voltage	HVS = V_{CC}, I_{POUT} = 0mA	29.1		30.9	V
POUT Output-Current Limit	Not in dropout, V_{SUP} = 9V V_{POUT} = 24V	20			mA
C1N, C2N High-Side On-Resistance				9	Ω
C1N, C2N Low-Side On-Resistance				6	Ω
C1P Switch On-Resistance				15	Ω
CP2 Switch On-Resistance				10	Ω
POUT Switch On-Resistance				10	Ω
FBP Fault Trip Level	Falling edge	0.96		1.04	V
NEGATIVE CHARGE-PUMP REGULATOR					
FBN Regulation Voltage	V_{REF} - V_{FBN}	0.985		1.015	V
DRVN PCH On-Resistance				10	Ω
DRVN NCH On-Resistance				6	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, Circuit of Figure 1, AVDD = SUP = +14V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
CTL Input-Low Voltage				0.8	V
CTL Input-High Voltage		1.8			V
GON-to-POUT Switch On-Resistance	GDEL = 1.5V, CTL = V_{CC}			20	Ω
GON-to-POUT Switch Saturation	V_{POUT} - V_{GON} > 5V	180			mA
GON-to-DRN Switch On-Resistance	GDEL = 1.5V, CTL = 0V			60	Ω
GON-to-DRN Switch Saturation Current	V_{GON} - V_{DRN} > 5V	35			mA
OPERATIONAL AMPLIFIERS					
SUP Supply Range		6		19	V
SUP Overvoltage Fault Threshold	(Note 1)	19.1		21.0	V
SUP Supply Current	Buffer configuration, V_{POS} = V_{SUP} / 2, no load			15	mA
Input Offset Voltage	V_{NEG}, V_{POS} = V_{SUP} / 2			13	mV
Input Common-Mode Voltage Range		0		V_{SUP}	V
Output-Voltage Swing High	I_{OUT} = 1mA	V_{SUP} - 50			mV
	I_{OUT} = 25mA	V_{SUP} - 300			
Output-Voltage Swing Low	I_{OUT} = -1mA			50	mV
	I_{OUT} = -25mA			300	
HVS FUNCTION					
HVS Input-Low Voltage				0.8	V
HVS Input-High Voltage		1.8			V
HVS Input Pulldown Resistance		5		50	kΩ
RSET Output On-Resistance	HVS = V_{CC}			20	Ω

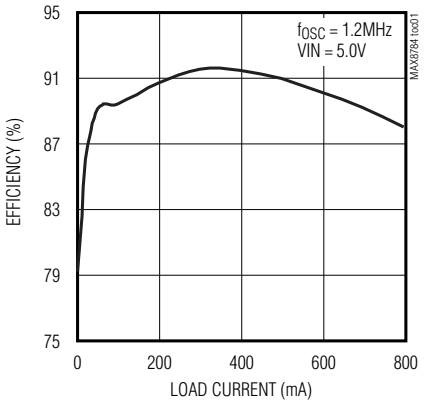
Note 1: Step-up regulator switching is disabled above the threshold. This fault is not latched.
Note 2: -40°C specs are guaranteed by design, not production tested.

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

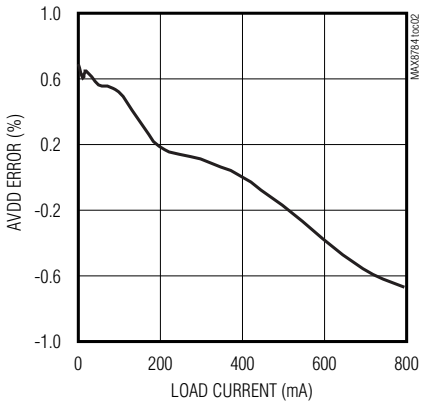
Typical Operating Characteristics

(Circuit of Figure 1, V_{CC} = 5V, AVDD = 14V, V_{POUT} = 28V, VGOFF = -9V, T_A = +25°C, unless otherwise noted.)

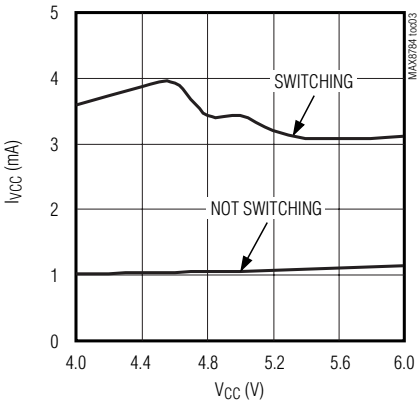
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



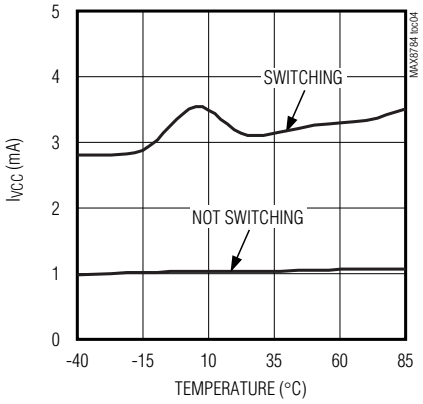
STEP-UP REGULATOR LOAD REGULATION



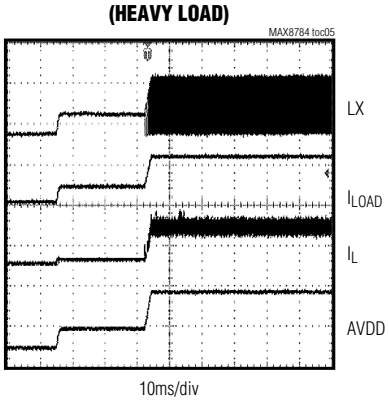
V_{CC} QUIESCENT CURRENT vs. V_{CC}



V_{CC} QUIESCENT CURRENT vs. TEMPERATURE

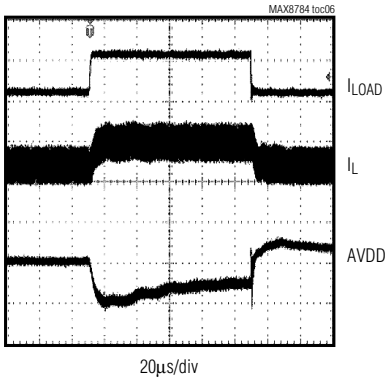


STEP-UP REGULATOR SOFT-START (HEAVY LOAD)



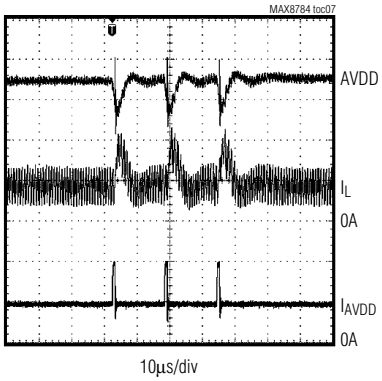
LX: 10V/div
I_{LOAD}: 500mA/div
I_L: 20A/div
AVDD: 10V/div

STEP-UP REGULATOR LOAD TRANSIENT RESPONSE



I_{LOAD}: 200mA/div
I_L: 1A/div
AVDD: 100mV/div (AC-COUPLED)

STEP-UP REGULATOR PULSED LOAD TRANSIENT RESPONSE



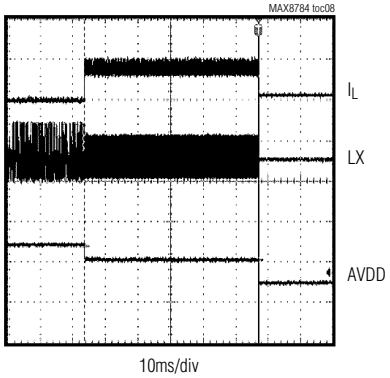
AVDD : 200mV/div (AC-COUPLED)
I_L : 1A/div
I_{AVDD} : 1A/div
I_{AVDD} : 0.3A TO 1.3A, 2µs PULSE

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

Typical Operating Characteristics (continued)

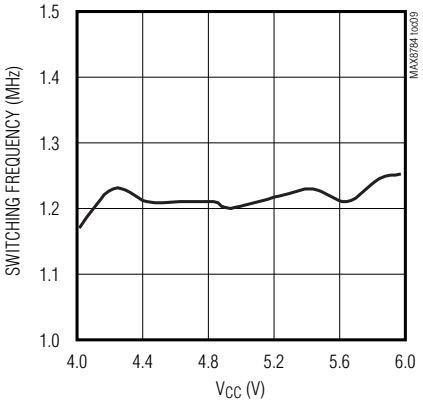
(Circuit of Figure 1, V_{CC} = 5V, AVDD = 14V, V_{POUT} = 28V, VGOFF = -9V, T_A = +25°C, unless otherwise noted.)

TIMER-DELAY LATCH RESPONSE TO OVERLOAD

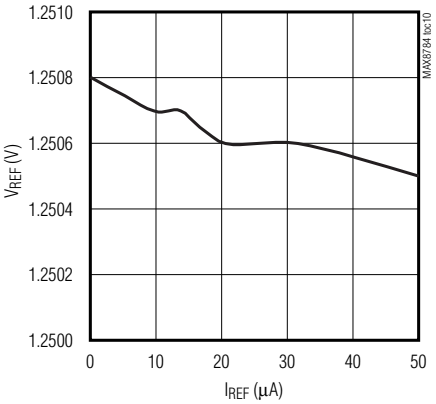


AVDD: 10V/div
LX: 10V/div
I_L: 5A/div

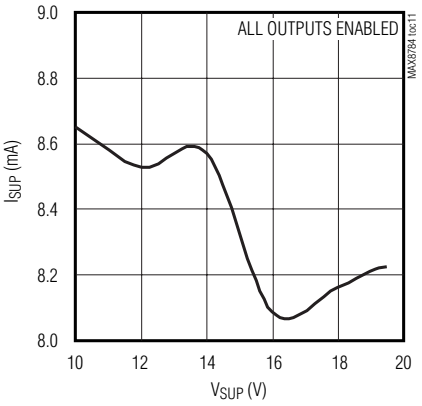
SWITCHING FREQUENCY vs. V_{CC}



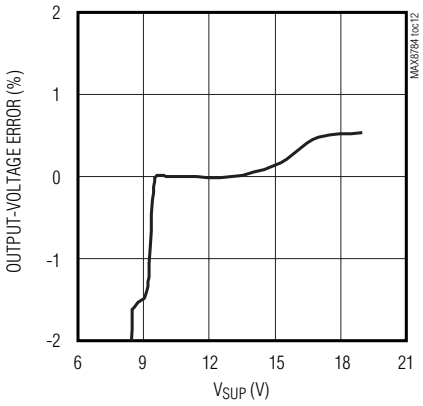
REFERENCE LOAD REGULATION



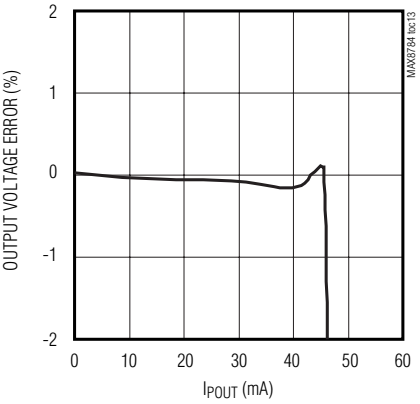
SUP SUPPLY CURRENT vs. SUP VOLTAGE



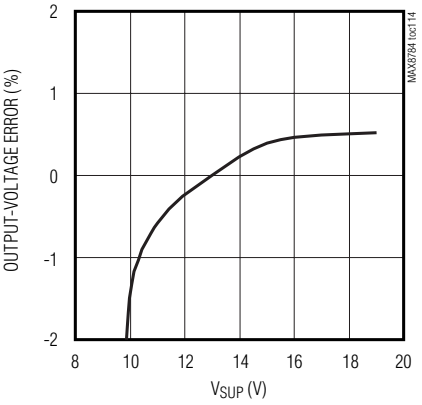
POSITIVE CHARGE-PUMP REGULATOR LINE REGULATION



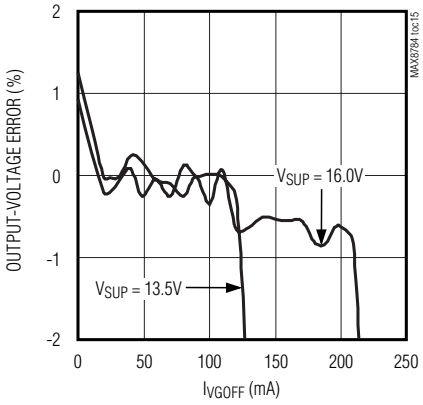
POSITIVE CHARGE-PUMP REGULATOR LOAD REGULATION



NEGATIVE CHARGE-PUMP REGULATOR LINE REGULATION



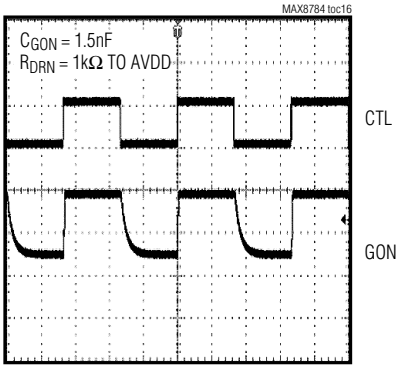
NEGATIVE CHARGE-PUMP REGULATOR LOAD REGULATION



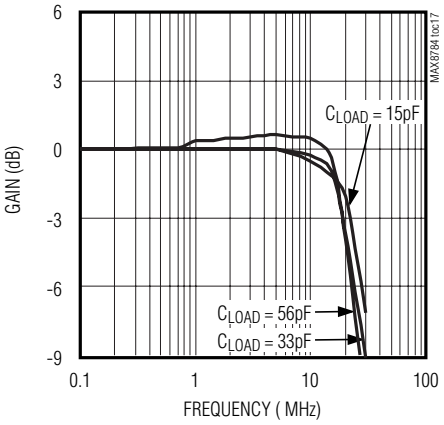
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{CC} = 5V, AVDD = 14V, V_{POUT} = 28V, VGOFF = -9V, T_A = +25°C, unless otherwise noted.)

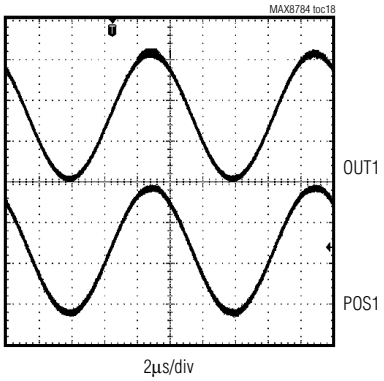
HIGH-VOLTAGE SWITCH CONTROL FUNCTION



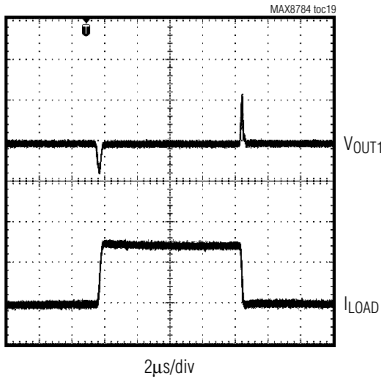
OPERATIONAL AMPLIFIER FREQUENCY RESPONSE



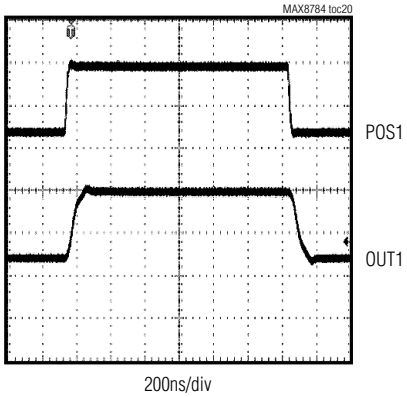
OPERATIONAL AMPLIFIER RAIL-TO-RAIL OPERATION



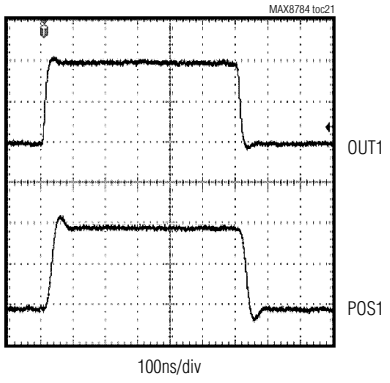
OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



OPERATIONAL AMPLIFIER LARGE-SIGNAL RESPONSE



OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

Pin Description

PIN	NAME	FUNCTION
1	C1N	Negative Terminal of Flying Capacitor C1
2	C1P	Positive Terminal of Flying Capacitor C1
3	BGND	Operational Amplifier and Charge-Pump Supply Ground
4	SUP	Operational Amplifier and Charge-Pump Supply Input. Connect SUP to AVDD. Bypass SUP to BGND with 0.1µF capacitor.
5	POS1	Operational Amplifier Noninverting Input
6	NEG1	Operational Amplifier Inverting Input
7	OUT1	Operational Amplifier Output
8	OUT2	Operational Amplifier Output
9	NEG2	Operational Amplifier Inverting Input
10	POS2	Operational Amplifier Noninverting Input
11	POS3	Operational Amplifier Noninverting Input
12	OUT3	Operational Amplifier Output
13, 19, 20, 26	N.C.	No Connection. Not internally connected.
14	ADEL	Step-Up Regulator Delay Input. Connect a capacitor from ADEL to AGND to set the delay time. A 5µA current source charges C_{ADEL}. ADEL is internally pulled to AGND by a 20Ω resistor in shutdown. For details, see the *Power-Up Sequence* section.
15	GDEL	Positive Charge-Pump Startup Delay and High-Voltage Switch Delay Input. Connect a capacitor from GDEL to AGND to set the delay time. A 5µA current source charges C_{GDEL}. GDEL is internally pulled to AGND by a 20Ω resistor in shutdown. For details, see the *Power-Up Sequence* section.
16	CTL	High-Voltage Switch Control Input. When CTL is high, the switch between GON and POUT is turned on and the switch between GON and DRN is turned off. When CTL is low, the switch between GON and DRN is turned on and the switch between GON and POUT is turned off. For details, see the *High-Voltage Switch Control* section.
17	HVS	HVS Mode Input. Connect HVS to V_{CC} to enable HVS mode. For details, see the *HVS Mode* section.
18	DRVN	Negative Charge-Pump Regulator Output. Connect DRVN to the negative charge-pump flying capacitor(s).
21	FBN	Negative Charge-Pump Regulator Feedback Input. Connect FBN to the center of a resistive voltage-divider between the negative output and REF. Place the resistive voltage-divider within 5mm of FBN. For details, see the *Output-Voltage Selection* section.
22	REF	Reference Output. Connect a 0.22µF capacitor from REF to AGND.
23	AGND	Analog Ground
24	V_{CC}	V_{CC} Supplies the Internal Reference and Other Internal Circuitry. Connect V_{CC} to the input supply voltage and bypass V_{CC} to AGND with a minimum 1µF ceramic capacitor.
25	$\overline{SHDN}$	Active-Low Shutdown. When $\overline{SHDN}$ is low, the device enters its low-power shutdown mode.
27, 28	PGND	Power Ground
29, 30	LX	Step-Up Regulator Switching Node. Connect inductor and Schottky diode to LX and minimize trace area for lowest EMI.

Pin Description (continued)

PIN	NAME	FUNCTION
31	AGND	Analog GND
32	RSET	Open-Drain HVS Mode Output. For details, see the *HVS Mode* section.
33	COMP	Error-Amplifier Output. Connect a series RC network from COMP to AGND for compensation.
34	FB	Step-Up Regulator Feedback Input. Connect FB to the center of a resistive voltage-divider between the step-up regulator output and AGND. Place the resistive voltage-divider within 5mm of FB. For details, see the *Output-Voltage Selection* section.
35	GON	Internal High-Voltage Switch Common Terminal. GON common terminal between the high-side p-channel MOSFET and back-to-back p-channel MOSFET. GON is internally pulled to PGND by a 100kΩ resistor in shutdown.
36	DRN	High-Voltage Switch Drain. Drain of the internal low-side, back-to-back p-channel MOSFET.
37	FBP	Positive Charge-Pump Regulator Feedback Input. Connect FBP to the center of a resistive voltage-divider between POUT and AGND. Place the resistive voltage-divider within 5mm of FBP. For details, see the *Output-Voltage Selection* section.
38	POUT	Positive Charge-Pump Output and High-Voltage Switch Source Input
39	C2P	Positive Terminal of Flying Capacitor C2
40	C2N	Negative Terminal of Flying Capacitor C2

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

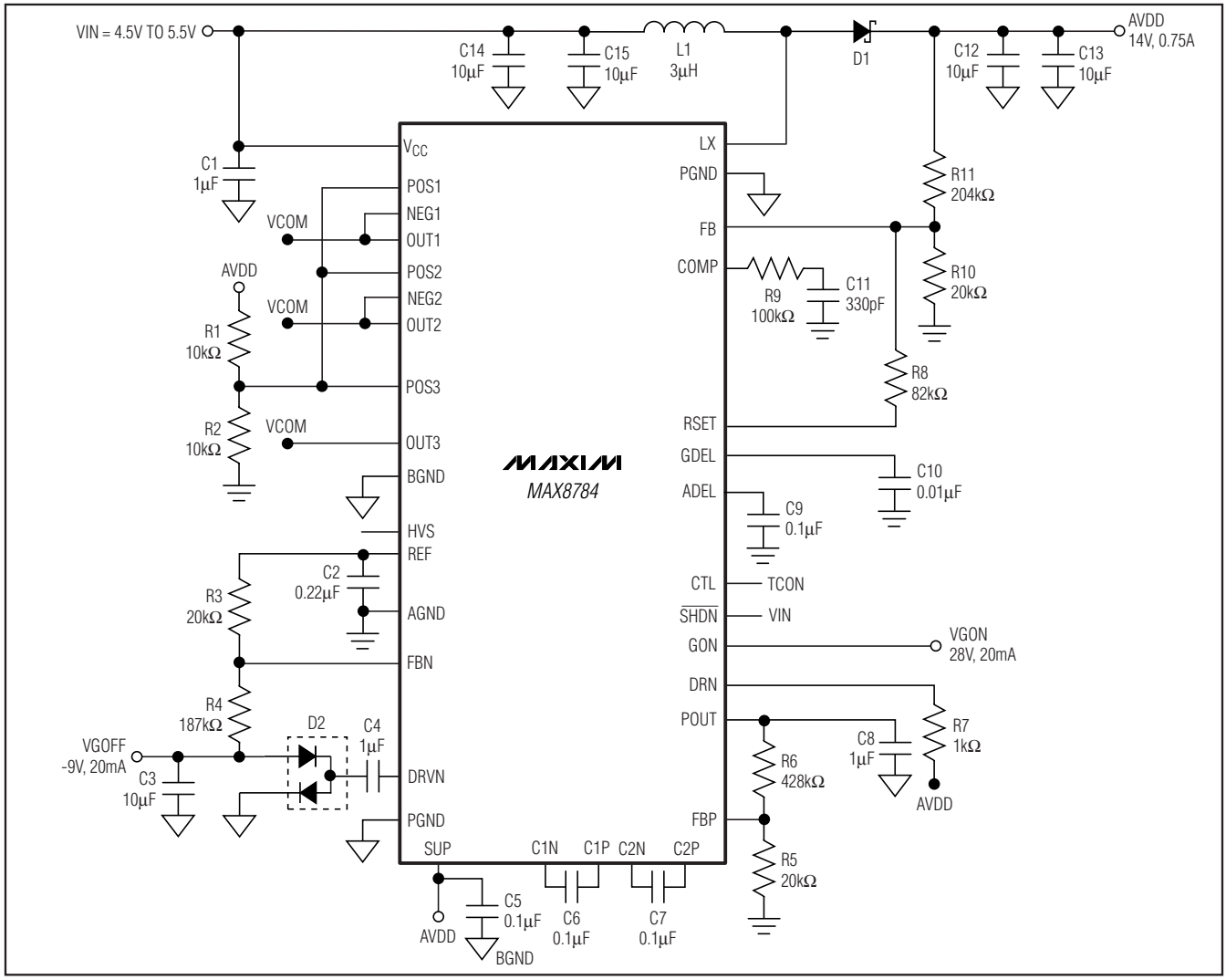


Figure 1. Typical Operating Circuit

Typical Operating Circuit

The typical operating circuit (Figure 1) of the MAX8784 is a power-supply system for TFT-LCD panels in monitors and TVs. The circuit generates a +14V source-driver supply, a +28V positive gate-driver supply, and a -9V negative gate-driver supply from a 5V ±10% input supply. Table 1 lists the selected components and Table 2 lists the contact information of the component suppliers.

Detailed Description

The MAX8784 is a multiple-output power supply designed primarily for TFT-LCD panels used in monitors

Table 1. Component List

C1	1µF ±10%, 6.3V X5R ceramic capacitor (0402) TDK C1005X5R0J105K
C14, C15	10µF ±20%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J106M
C12, C13	10µF ±20%, 16V X5R ceramic capacitors (1206) TDK C3216X5R1C106M
D1	3A, 30V Schottky diode (M-flat) Toshiba CMS02 (top mark S2)
D2	220mA, 100V dual diode (SOT23) Fairchild MMBD4148SE (top mark D4)
L1	3.0µH, $3A_{DC}$ inductor Sumida CDRH6D28-3R0

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild Semiconductor	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec

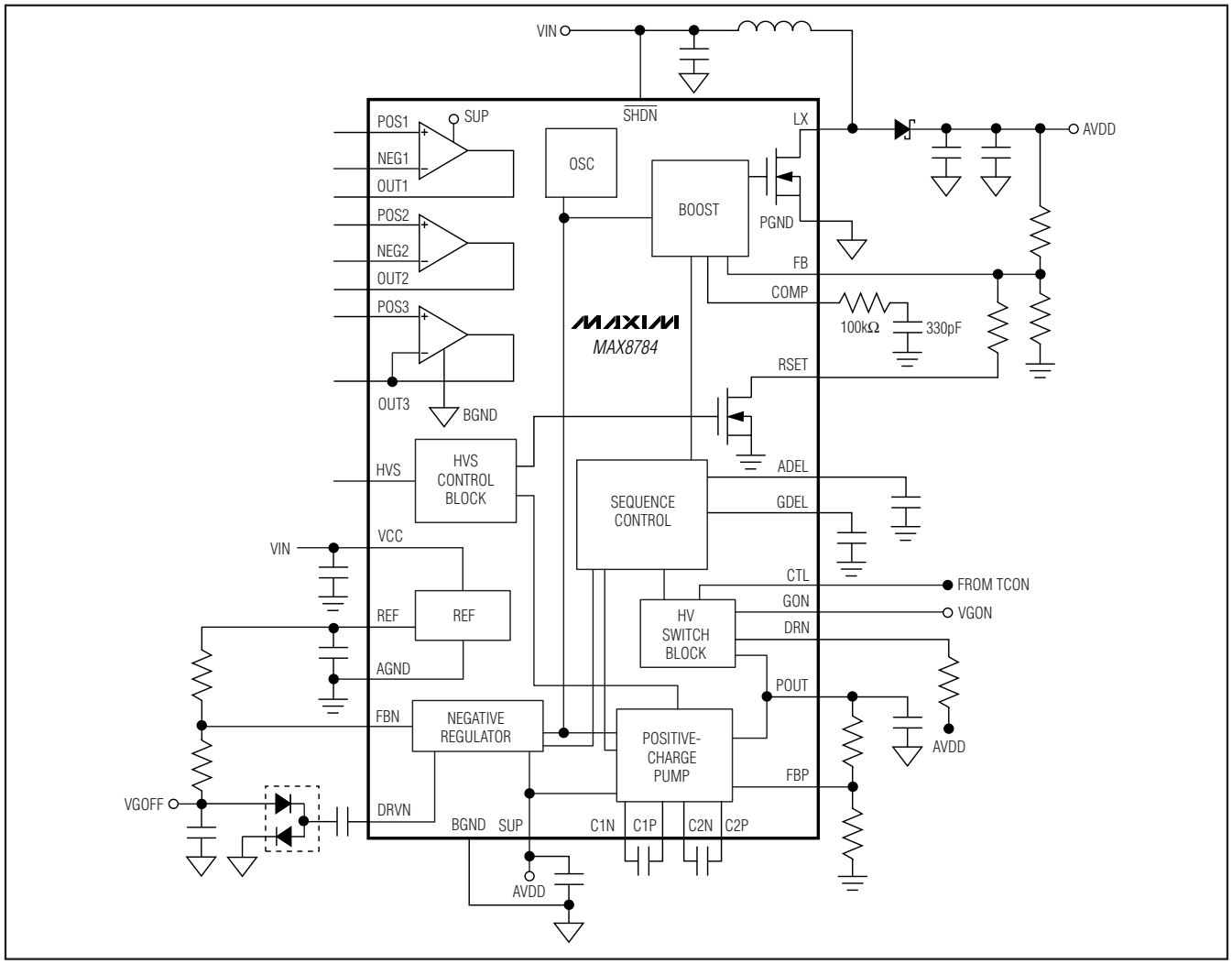


Figure 2. Functional Diagram

and TVs. It has a step-up switching regulator to generate the source-driver supply, two charge-pump regulators to generate the positive and negative gate-driver supplies, and three high-current operational amplifiers. Each regulator features an adjustable output voltage and digital soft-start. The step-up regulator has cycle-by-cycle current limiting and uses a fixed-frequency current-mode control architecture with fast transient response and excellent line regulation.

The MAX8784 features a high-voltage switch-control block, a very stable reference output, well-defined power-up and power-down sequences, and thermal-overload protection. Figure 2 shows the MAX8784 functional block diagram.

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

Step-Up Regulator

The step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and to provide fast-transient response to pulsed loads typical of TFT-LCD panel source drivers. The integrated MOSFET and the built-in digital soft-start function reduce the number of external components required to control inrush currents. The output voltage can be set from VIN to 19V with an external resistive voltage-divider. The regulator controls the output voltage and output power by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{AVDD} - V_{IN}}{V_{AVDD}}$$

where V_{AVDD} is the output voltage of the step-up regulator.

PWM Control Block

Figure 3 is the block diagram of the step-up regulator controller. On the rising edge of the internal oscillator clock, the controller sets a flip-flop, turning on the n-channel MOSFET, which applies the input voltage across the inductor. The current through the inductor ramps up linearly. The transconductance error amplifier compares the FB voltage with the reference voltage. The error amplifier changes the COMP voltage by charging or discharging the COMP capacitor. The COMP voltage is compared with a ramp, which is the sum of the current-sense signal and a slope compensation signal. Once the ramp signal exceeds the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the Schottky diode (D1 in Figure 1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

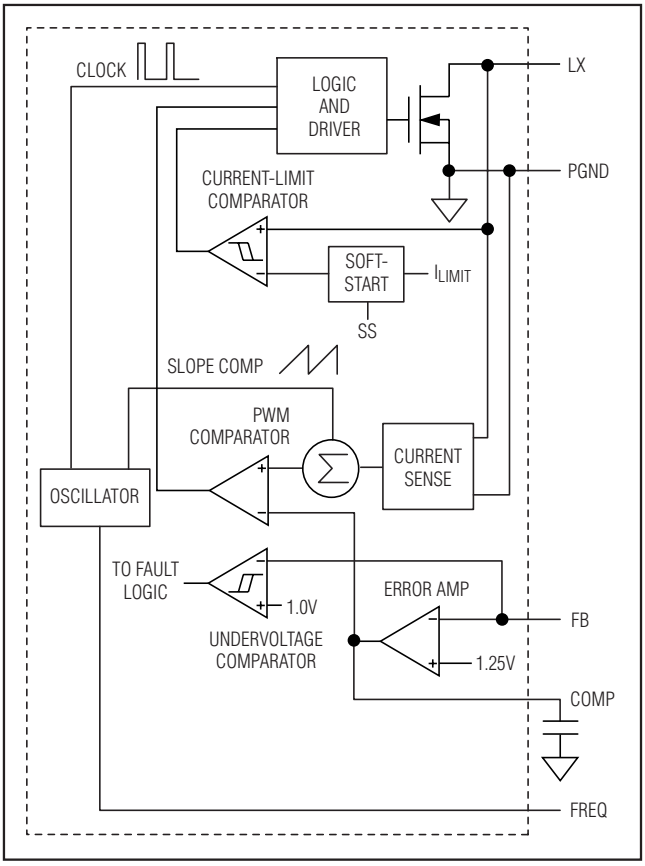


Figure 3. Step-Up Regulator PWM Control Block Diagram

Soft-Start and Fault Protection

The step-up regulator achieves soft-start by linearly ramping up its internal current limit. The soft-start terminates when the output reaches regulation or the full current limit has been reached. The current limit rises from zero to the full current limit in approximately 3ms. The soft-start feature effectively limits the inrush current during startup (see the Step-Up Regulator Soft-Start waveforms in the *Typical Operating Characteristics*). The MAX8784 monitors FB for undervoltage conditions. If the voltage is continuously below 80% of the nominal regulation point for approximately 55ms, the MAX8784 sets the fault latch, shutting down all outputs except the reference and the operational amplifier.

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

Positive Charge-Pump Regulator

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT LCD gate driver ICs. The positive charge pump is a two-stage charge pump with external pump and reservoir capacitors. The output voltage is set with an external resistive voltage-divider from its output to GND with the midpoint connected to FBP. The charge pump includes internal switches with drivers to control the power transfer. Figure 4 shows the block diagram of the positive charge pump.

The controller regulates the positive charge-pump output voltage so that $V_{FBP} = V_{REF}$. If V_{FBP} goes below the reference, P1 and P3 are turned on when the rising edge of the oscillator arrives, while the drivers pull C1N to GND and C2N to SUP. The first stage flying capacitor C6 (Figure 4) is charged by the charge-pump supply input and the second stage flying capacitor C7 is discharged into the reservoir capacitor C8. After a fixed period, P2 is turned on and P1 and P3 are turned off while C1N is pulled to SUP and C2N is pulled to GND. C7 is charged by C6 in preparation for the next pump cycle.

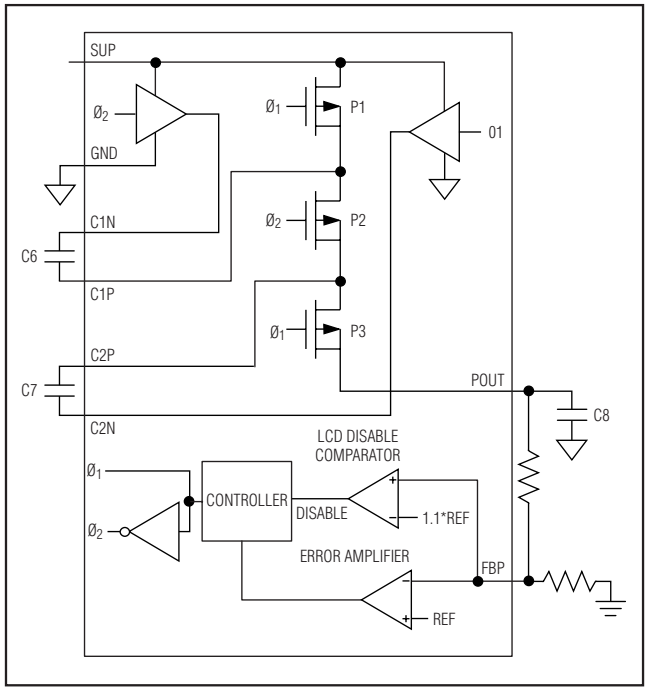


Figure 4. Positive Charge-Pump Regulator Control Block Diagram

The MAX8784 implements a digital variable-resistance algorithm to control the current delivered to the output. The algorithm sets the on-resistance of the positive charge-pump drivers according to the load current. The on-resistance of the drivers is set by counting the number of charging pulses in the previous 12 oscillator cycles. As the number of charging pulses in the previous 12 oscillator cycles increases, the on-resistance of the switch is reduced. The number of charging pulses in the previous 12 oscillator cycles is a measure of the load current. The period of C1N and C2N switching is 1.66µs.

The positive charge-pump regulator's startup can be delayed by connecting an external capacitor from GDEL to GND. An internal constant-current source begins charging the GDEL capacitor when the negative charge pump reaches regulation. When the GDEL voltage exceeds V_{REF}, the positive charge-pump regulator is enabled. Each time it is enabled, the positive charge-pump regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to V_{REF} in 128 steps. The soft-start period is 3ms (typ) and FBP fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

The MAX8784 monitors the FBP and SUP voltage to detect fault conditions. If V_{FBP} is continuously below 80% of its nominal regulation point for approximately 55ms, the MAX8784 sets a fault latch, shutting down all outputs except the reference and operational amplifiers.

If SUP exceeds the SUP overvoltage faut threshold (20V, typ), LX switching is inhibited until SUP decreases. Furthermore, if SUP exceeds its overvoltage charge-pump inhibit level (21V, typ), positive charge-pump switching is inhibited until SUP decreases to prevent damage to the charge pump.

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

Negative Charge-Pump Regulator

The negative charge-pump regulator (see Figure 5) generates the negative supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge-pump stages and the setting of the feedback divider determine the output voltage of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P4) and a low-side n-channel MOSFET (N4) to control the power transfer as shown in Figure 7.

The error comparator compares the feedback signal (FBN) with a 250mV internal reference. If the feedback signal is above the reference, the charge-pump regulator turns on N4 and turns off P4 when the rising edge of the oscillator clock arrives, level shifting $C_{(NEG)}$ in parallel with the reservoir capacitor $C_{OUT(NEG)}$. If the voltage across $C_{OUT(NEG)}$ minus a diode drop (V_{NEG} - V_{DIODE}) is higher than the level-shifted flying capacitor voltage ($-V_{C(NEG)}$), charge flow from $C_{OUT(NEG)}$ to $C_{(NEG)}$ until the diode D2-B turns off. The falling edge of the oscillator clock turns off N4 and turns on P4, allowing V_{SUP} to charge up flying capacitor $C_{(NEG)}$ through diode D2-A. If the feedback signal is below the reference when the rising edge of the oscillator comes, the regulator ignores this clock edge and keeps P4 on and N4 off.

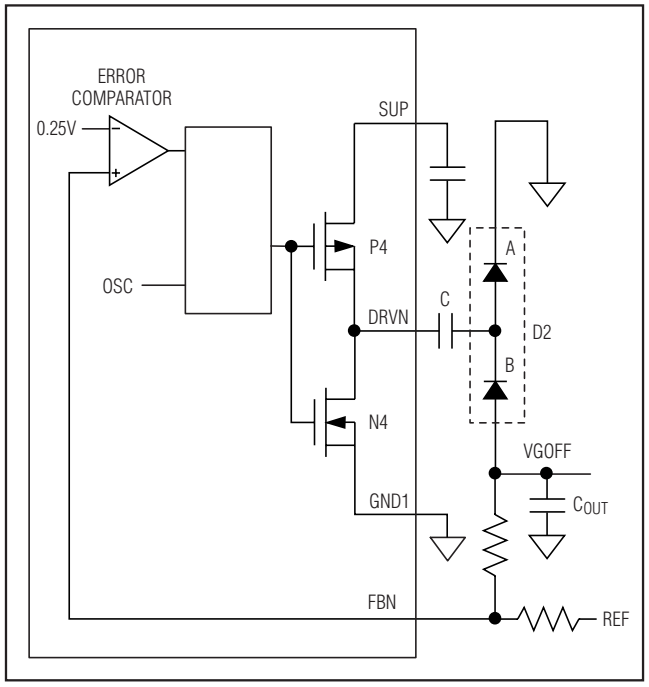


Figure 5. Negative Charge-Pump Regulator Block Diagram

The negative charge-pump regulator is enabled when the step-up regulator reaches regulation. Each time it is enabled, the negative charge-pump regulator goes through a soft-start routine by ramping down its internal reference voltage from 1.25V to 250mV in 128 steps. The soft-start period is 3ms (typ) and FBN fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup. The MAX8784 monitors FBN voltage for undervoltage conditions. If V_{FBN} is continuously above 450mV for approximately 55ms, the MAX8784 sets a fault latch, shutting down all outputs except the reference and the operational amplifiers.

High-Voltage Switch Control

The MAX8784's high-voltage switch control block (Figure 6) consists of three high-voltage p-channel MOSFETs: Q1, between POUT and GON, Q2 and Q3 between GON and DRN. Q2 and Q3 are arranged back-to-back so that GON can be either above or below DRN. The switch control block is enabled when V_{GDEL} goes above V_{REF}.

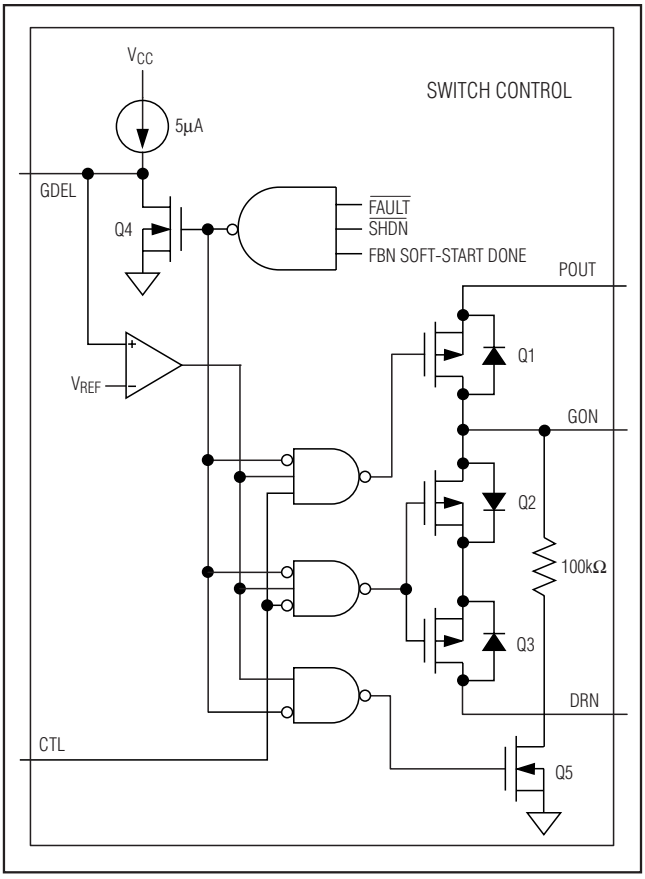


Figure 6. High-Voltage Switch Control Block Diagram

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

When CTL is logic-high, Q1 turns on and Q2 and Q3 turn off, connecting GON to POUT. When CTL is logic-low, Q1 turns off and Q2 and Q3 turn on, connecting GON to DRN. GON can be discharged through a resistor connected between DRN and GND.

The switch control block is enabled when GDEL is charged to V_{REF}. GDEL is charged by a 5µA current after the negative charge pump reaches regulation. The switch control block is disabled during fault mode and during shutdown. When the switch control block is disabled, GON is pulled to PGND with an internal 100kΩ resistor.

Operational Amplifier

The MAX8784 has three operational amplifiers that are typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. Each operational amplifier features 140mA/220mA (source/sink) output short-circuit current, 45V/µs slew rate, and 20MHz bandwidth. While the op amp is a rail-to-rail input and output design, its accuracy is significantly degraded for input voltages within 1V of its supply rails (SUP, BGND).

Short-Circuit Current Limit

The operational amplifier limits short-circuit current to approximately 140mA if the output is shorted to AGND and to approximately -220mA if the output is shorted to AVDD. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal-fault latch, shutting off the main step-up regulator, the charge pumps, the high-voltage switch control block, and the operational amplifier. Those portions of the device remain inactive until the input voltage is cycled.

Driving Pure Capacitive Loads

The operational amplifier is typically used to drive the LCD backplane (VCOM). The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between VCOM and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain.

Reference Voltage

The reference voltage is nominally 1.246V, and can source at least 50µA (see the *Typical Operating Characteristics*). V_{CC} is the input of the internal reference block. Bypass REF with a 0.22µF ceramic capacitor connected between REF and GND.

Power-Up Sequence

The MAX8784 operational amplifier and internal reference are enabled when V_{CC} exceeds its UVLO threshold. A 5µA current charges ADEL after the internal reference reaches regulation. The step-up regulator starts the soft-start sequence after ADEL is charged to V_{REF}. The FB fault-detection circuit is enabled and the negative charge-pump regulator starts up after the step-up regulator reaches regulation. The FBN fault-detection circuit is enabled and a 5µA current charges GDEL after the negative charge pump reaches regulation. The positive charge pump starts its soft-start sequence after GDEL is charged to 1.25V (typ). The FBP fault-detection circuit is enabled after the positive-charge pump reaches regulation.

Power-Down Control

The MAX8784 disables the step-up regulator, positive charge-pump regulator, negative charge-pump regulator, and high-voltage switch control block when $\overline{SHDN}$ is logic low. The operational amplifier depends only upon the supply voltage at SUP.

Fault Protection

During steady-state operation, if any output of the three regulators (step-up regulator, positive charge-pump regulator, and negative charge-pump regulator) is not above its respective fault-detection threshold, the MAX8784 activates an internal fault timer. If any condition or a combination of conditions indicates a continuous fault for the fault-timer duration (55ms typ), the MAX8784 sets the fault latch. The MAX8784 shuts down all the outputs except the reference and operational amplifiers after the fault latch is set. Toggle $\overline{SHDN}$ or cycle the input voltage to clear the fault latch and restart the IC.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the MAX8784. When the junction temperature exceeds T_J = +160°C (typ), a thermal sensor immediately sets its fault latch, which shuts down all the outputs. After the device cools down, input voltage has to be recycled to restart. The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute junction temperature rating of T_J = +150°C.

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

HVS Mode

HVS mode is designed as a special operating mode for end-of-line panel testing. In HVS mode, higher than normal voltages are forced to the power-supply outputs to expose faults in the LCD panel. HVS pin is forced logic-high to enable HVS mode. In HVS mode operation, FBP is ignored and the positive charge-pump regulates to a fixed-output voltage of 30V. To raise the step-up regulator output voltage in HVS operation, the open-drain RSET pin is pulled to GND. In Figure 1, resistor R8 becomes parallel to R10, which reduces the feedback resistance during HVS operation. This special feature allows the customer to select a resistor that sets an appropriate HVS voltage according to the panel requirements. The negative charge pump operates normally. Figure 7 shows the typical application circuit in HVS mode.

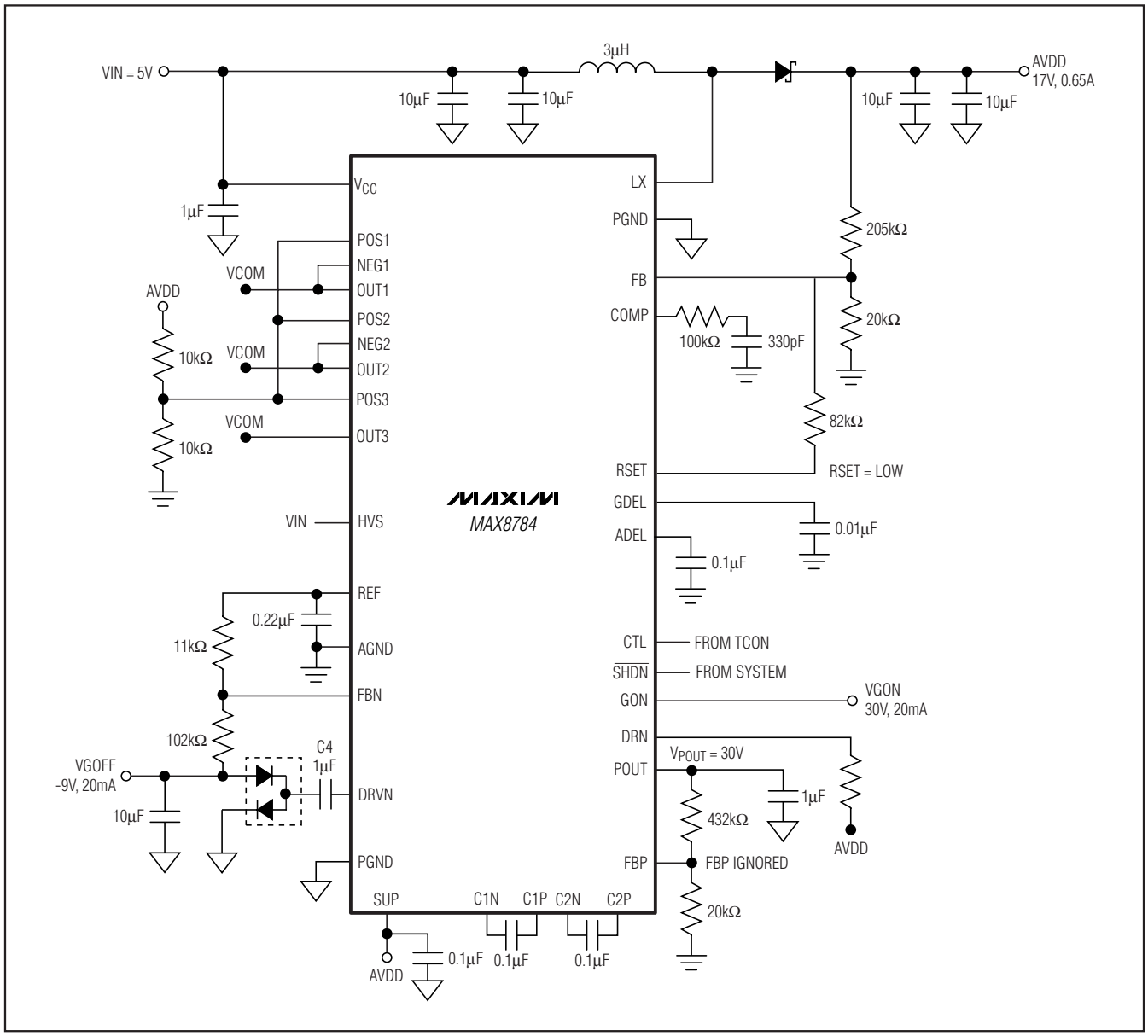


Figure 7. HVS Mode Operation

Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

Design Procedure

Step-Up Regulator

Inductor Selection

The inductance value, peak-current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output-load capability, transient response time, and output voltage ripple. Physical size and cost are also important factors to be considered. The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high-inductance values minimize the current ripple, and therefore, reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low-inductance values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 to 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to the other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (VIN), the maximum output current ($I_{AVDD(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L_I = \left(\frac{V_{IN}}{V_{AVDD}}\right)^2 \left(\frac{V_{AVDD} - V_{IN}}{I_{AVDD(MAX)} \times f_{SW}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{AVDD(MAX)} \times V_{AVDD}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{LI\_RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{AVDD} - V_{IN(MIN)}\right)}{L_I \times V_{AVDD} \times f_{SW}}$$

$$I_{AVDD\_PEAK} = I_{IN(DC,MAX)} + \frac{I_{LI\_RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX8784's LX current limit should exceed I_{LI_PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit in Figure 1, the maximum load current ($I_{AVDD(MAX)}$), with charge-pump loads, is 820mA with a 14V output and a typical input voltage of 5V. Choosing an LIR of 0.35 and estimating efficiency of 85% at this operating point:

$$L_I = \left(\frac{5V}{14V}\right)^2 \left(\frac{14V - 5V}{0.82A \times 1.2MHz}\right)\left(\frac{0.85}{0.35}\right) \approx 3.0\mu H$$

Using the circuit's minimum input voltage (4.5V) and estimating efficiency of 85% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.82A \times 14V}{4.5V \times 0.85} \approx 3.00A$$

The ripple current and the peak current are:

$$I_{LI\_RIPPLE} = \frac{4.5V \times \left(14V - 4.5V\right)}{3.0\mu H \times 14V \times 1.2MHz} \approx 0.69A$$

$$I_{LI\_PEAK} = 3.0A + \frac{0.69A}{2} \approx 3.35A$$

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Output-Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{AVDD\_RIPPLE} = V_{AVDD\_RIPPLE(C)} + V_{AVDD\_RIPPLE(ESR)}$$

$$V_{AVDD\_RIPPLE(C)} \approx \frac{I_{AVDD}}{C_{AVDDT}}\left(\frac{V_{AVDD} - V_{IN}}{V_{AVDD} \times f_{SW}}\right)$$

and:

$$V_{AVDD\_RIPPLE(ESR)} \approx I_{AVDD\_PEAK} \times R_{ESR\_AVDD}$$

where I_{AVDD_PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{AVDD\_RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input-Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 10µF ceramic capacitors are used in the typical operating circuit (Figure 1) because of the high source impedance seen in the typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the values used in Figure 1.

Rectifier Diode

The MAX8784's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 2A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (AVDD) to AGND with the center tap connected to FB1 (see Figure 1). Select R10 in the 10kΩ to 50kΩ range. Calculate R11 with the following equation:

$$R11 = R10 \times \left(\frac{V_{AVDD}}{V_{FB}} - 1\right)$$

where V_{FB} is the step-up regulator's feedback set point. Place R10 and R11 close to the IC.

Loop Compensation

Choose R_{COMP} (R9 in Figure 1) to set the high-frequency integrator gain for fast transient response. Choose C_{COMP} (C11 in Figure 1) to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{251 \times V_{IN} \times V_{AVDD} \times C_{AVDD}}{L_I \times I_{AVDD(MAX)}}$$

$$C_{COMP} \approx \frac{V_{AVDD} \times C_{AVDD}}{10 \times I_{AVDD(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient response waveforms.

If additional noise rejection is desired, add a high-frequency pole by placing a 10pF to 47pF capacitor from COMP to GND.

Charge-Pump Regulators

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement.

The number of negative charge-pump stages is given by:

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT}}{V_{SUP} - 2 \times V_D}$$

where n_{NEG} is the number of negative charge-pump stages, V_{GOFF} is the output of the negative charge-pump regulator, V_{SUP} is the supply voltage of the charge-pump regulators, V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the regulator. Use $V_{DROPOUT}$ = 0.6V.

The above equations are derived based on the assumption that the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to VIN or another available supply. If the first-stage charge pump is powered from VIN, then the above equation becomes:

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT} + V_{IN}}{V_{SUP} - 2 \times V_D}$$

The MAX8784's positive charge-pump regulator is a fixed two-stage charge pump with built-in switches.

Pump Capacitors

Increasing the pump capacitor value (C4, C6, and C7) lowers the effective source impedance and increases the output-current capability. Increasing the capacitance indefinitely has a negligible effect on output current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. For the negative charge pump, the flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n \times V_{SUP}$$

where n is the stage number in which the flying capacitor appears.

For the positive charge pump, the pump capacitor's voltage rating must exceed the following:

$$V_{C6} > V_{SUP}$$
$$V_{C7} > 2 \times V_{SUP}$$

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output-voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT\_CP} \geq \frac{I_{LOAD\_CP}}{2 f_{OSC} V_{RIPPLE\_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the peak-to-peak value of the output ripple.

Output-Voltage Selection

Adjust the positive charge-pump regulator's output voltage by connecting a resistive voltage-divider from POUT to GND with the center tap connected to FBP (Figure 1). Select the lower resistor of divider R5 in the 10kΩ to 30kΩ range. Calculate upper resistor R6 with the following equation:

$$R6 = R5 \times \left(\frac{V_{POUT}}{V_{FBP}} - 1 \right)$$

where V_{FBP} is the positive charge-pump regulator's feedback set point.

Adjust the negative charge-pump regulator's output voltage by connecting a resistive voltage-divider from VGOFF to REF with the center tap connected to FBN (Figure 1). Select R3 in the 20kΩ to 68kΩ range. Calculate R4 with the following equation:

$$R4 = R3 \times \frac{V_{FBN} - V_{GOFF}}{V_{REF} - V_{FBN}}$$

where V_{REF} - V_{FBN} is the negative charge-pump regulator's feedback set point. Note that REF can only source up to 50µA. Using a resistor less than 20kΩ for R2 results in higher bias current than REF can supply.

PCB Layout Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of respective high-current loops by placing step-up regulator's inductor, diode, and output capacitors near its input capacitors and its LX and PGND pins. For the step-up regulator, the high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pins, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power ground island (PGND) for the step-up regulator, consisting of the input and output capacitor grounds and the PGND pin. Connect all these together with short, wide traces or a small ground plane. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the COMP, ADEL, and GDBL capacitor ground connections, and the device's exposed backside pad.
- Place all feedback voltage-divider resistors as close as possible to their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near LX, DRVN, C1N, C1P, C2N, or C2P.

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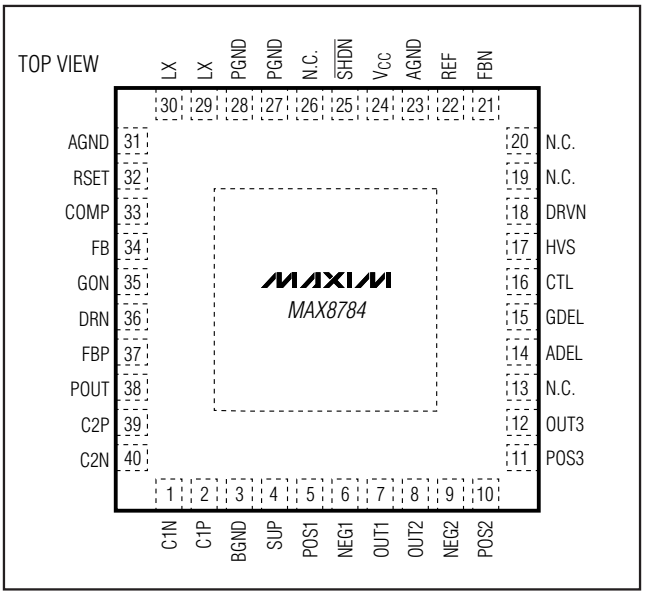
- Place V_{CC} pin and REF pin bypass capacitors as close as possible to the device. The ground connection of the V_{CC} bypass capacitor should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX and charge-pump nodes away from feedback nodes (FB, FBP, and FBN) and analog ground. Use DC traces as a shield if necessary.

Refer to the MAX8784 evaluation kit for an example of proper board layout.

Pin Configuration



Chip Information

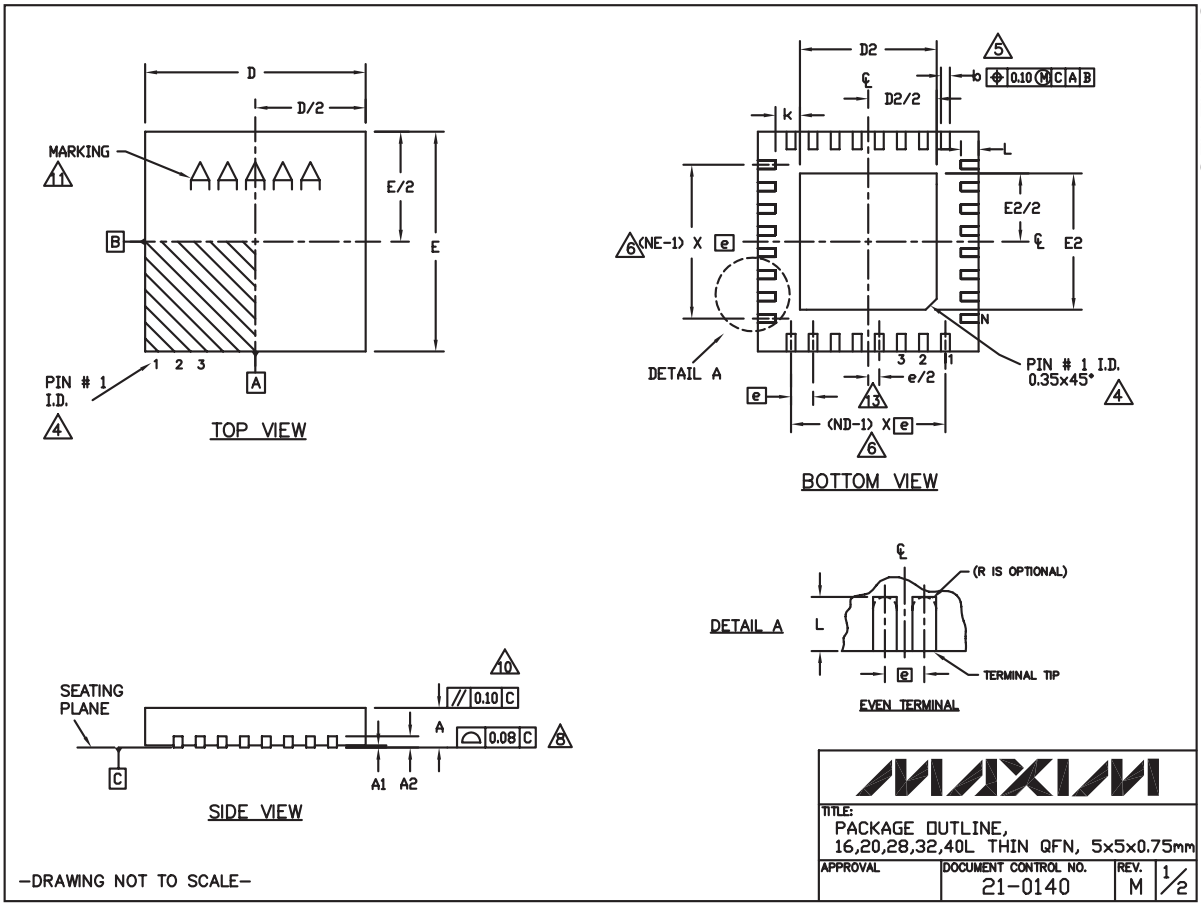
TRANSISTOR COUNT: 11,424

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

QFN THIN.EPS



Step-Up Regulator, Internal Charge Pumps, Switch Control, and Operational Amplifier for TFT LCDs

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655-4	2.19	2.29	2.39	2.19	2.29	2.39
T165N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055N-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	M	2/2