3.3 VOLT CMOS SyncBiFIFO™ WITH BUS-MATCHING

16,384 x 36 x 2 — ***IDT72V3684***

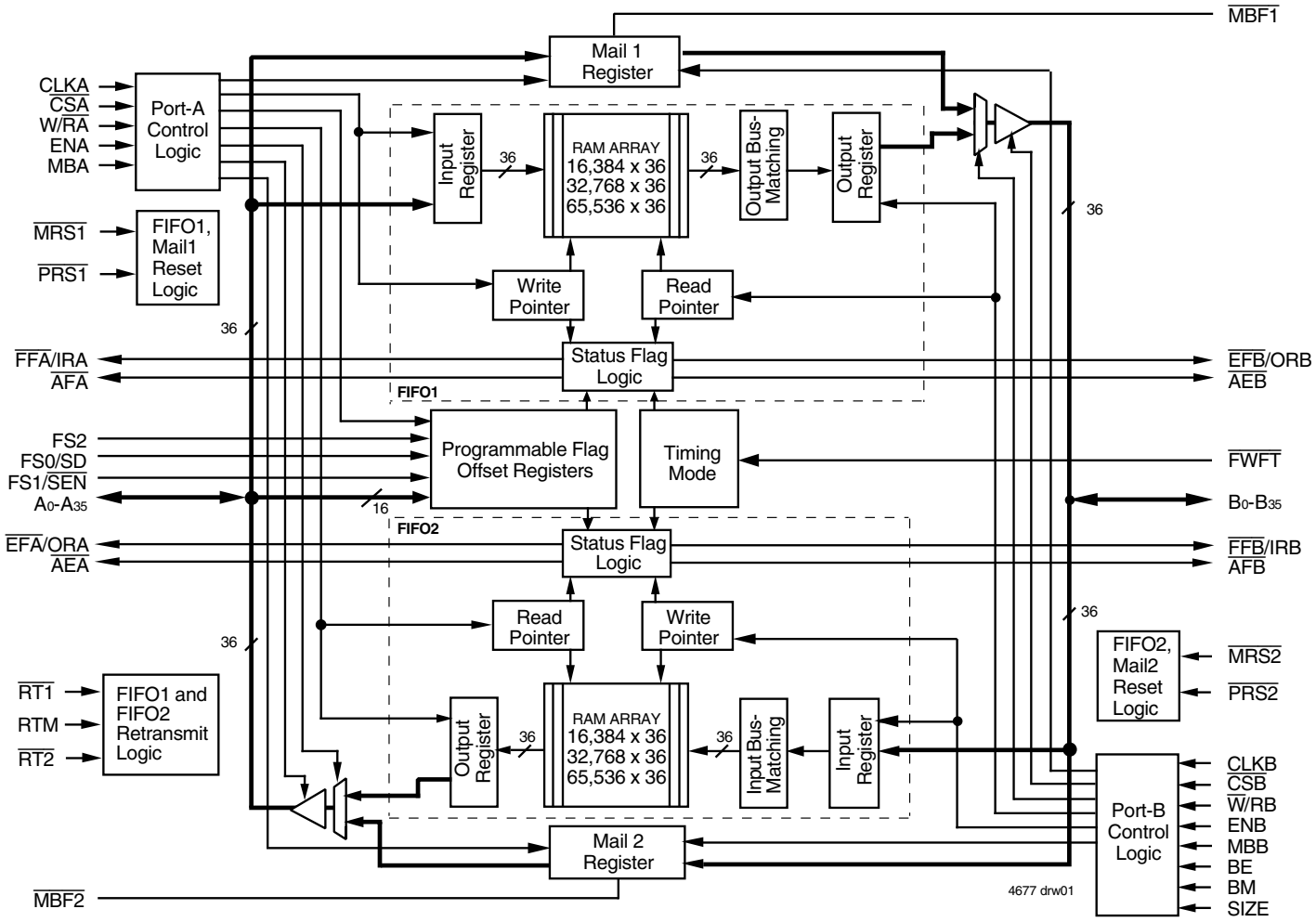
32,768 x 36 x 2 — ***IDT72V3694***

65,536 x 36 x 2 — ***IDT72V36104***

FEATURES

- Memory storage capacity:
  - IDT72V3684 – 16,384 x 36 x 2
  - IDT72V3694 – 32,768 x 36 x 2
  - IDT72V36104 – 65,536 x 36 x 2
- Clock frequencies up to 100 MHz (6.5ns access time)
- Two independent clocked FIFOs buffering data in opposite directions
- Select IDT Standard timing (using $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$ flags functions) or First Word Fall Through Timing (using ORA, ORB, IRA, and IRB flag functions)
- Programmable Almost-Empty and Almost-Full flags; each has five default offsets (8, 16, 64, 256 and 1,024)
- Serial or parallel programming of partial flags
- Retransmit Capability
- Port B bus sizing of 36 bits (long word), 18 bits (word) and 9 bits (byte)
- Big- or Little-Endian format for word and byte bus sizes
- Master Reset clears data and configures FIFO, Partial Reset clears data but retains configuration settings
- Mailbox bypass registers for each FIFO
- Free-running CLKA and CLKB may be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)
- Auto power down minimizes power dissipation
- Available in space saving 128-pin Thin Quad Flatpack (TQFP)
- Pin compatible to the lower density parts, IDT72V3624/72V3634/72V3644/72V3654/72V3664/72V3674
- Industrial temperature range (–40°C to +85°C) is available
- Green parts available, see ordering information

FUNCTIONAL BLOCK DIAGRAM



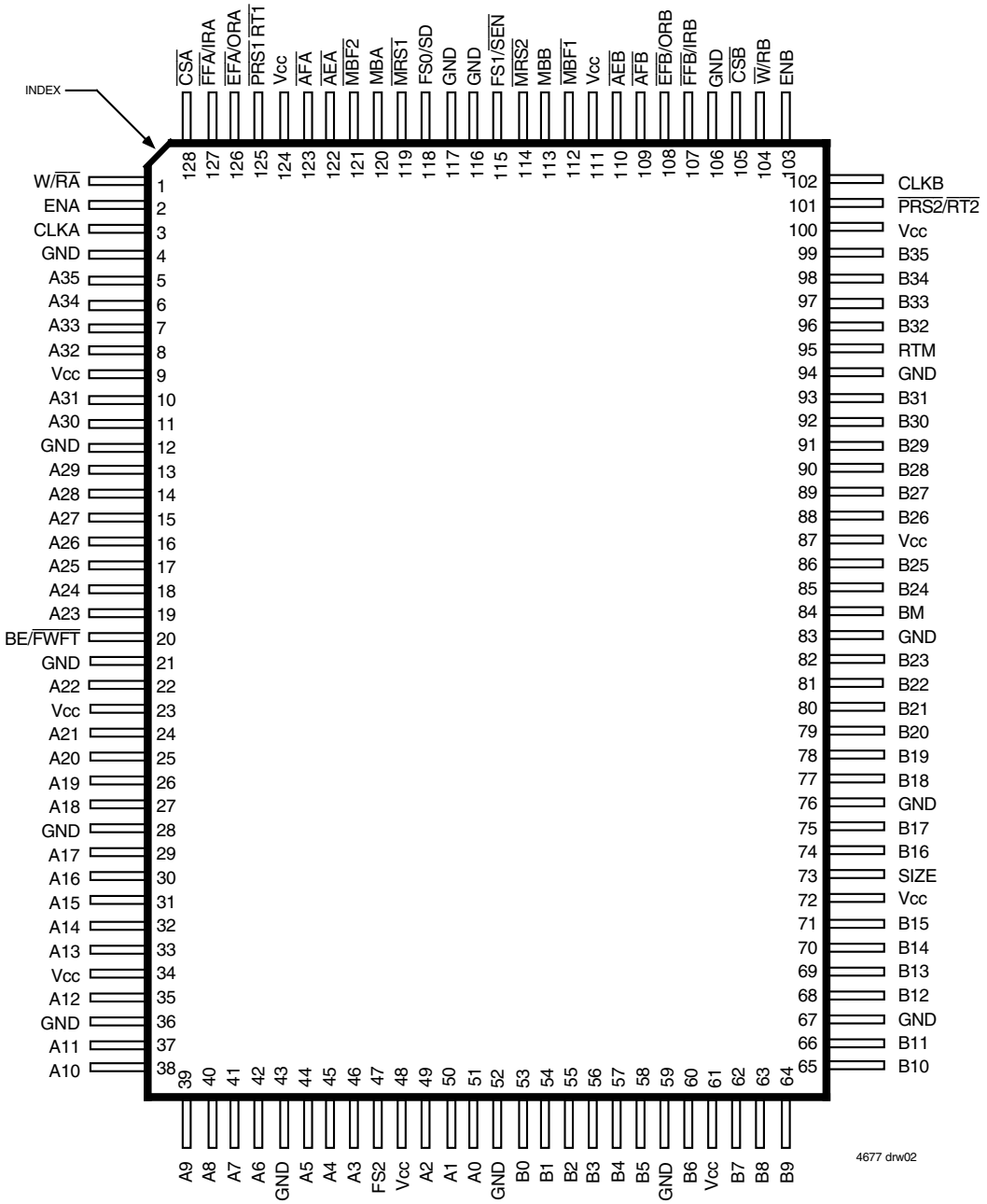
DESCRIPTION

The IDT72V3684/72V3694/72V36104 are designed to run off a 3.3V supply for exceptionally low-power consumption. These devices are monolithic, high-speed, low-power, CMOS bidirectional synchronous (clocked) FIFO memory which supports clock frequencies up to 100 MHz and has read access times as fast as 6.5ns. Two independent 16,384/32,768/65,536 x 36 dual-port SRAM FIFOs on board each chip buffer data in opposite directions. FIFO data on Port B can be input and output in 36-bit, 18-bit, or 9-bit formats with a choice of Big- or Little-Endian configurations.

These devices are a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

Communication between each port may bypass the FIFOs via two mailbox registers. The mailbox registers' width matches the selected Port B bus width.

PIN CONFIGURATION



TQFP (PK128-1, order code: PF)

TOP VIEW

Each Mailbox register has a flag ($\overline{MBF1}$ and $\overline{MBF2}$) to signal when new mail has been stored.

Two kinds of reset are available on these FIFOs: Master Reset and Partial Reset. Master Reset initializes the read and write pointers to the first location of the memory array, configures the FIFO for Big- or Little-Endian byte arrangement and selects serial flag programming, parallel flag programming, or one of five possible default flag offset settings, 8, 16, 64, 256 or 1,024. There are two Master Reset pins, $\overline{MRS1}$ and $\overline{MRS2}$.

Partial Reset also sets the read and write pointers to the first location of the memory. Unlike Master Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings. Each FIFO has its own, independent Partial Reset pin, $\overline{PRS1}$ and $\overline{PRS2}$.

Both FIFO's have Retransmit capability, when a Retransmit is performed on a respective FIFO only the read pointer is reset to the first memory location. A Retransmit is performed by using the Retransmit Mode, RTM pin in conjunction with the Retransmit pins $\overline{RT1}$ or $\overline{RT2}$, for each respective FIFO. Note that the two Retransmit pins $\overline{RT1}$ and $\overline{RT2}$ are muxed with the Partial Reset pins.

These devices have two modes of operation: In the *IDT Standard mode*, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory). In the *First Word Fall Through mode* (FWFT), the first long-word (36-bit wide) written to an empty FIFO appears automatically on the outputs, no read operation is required (Nevertheless, accessing subsequent words does necessitate a formal read request). The state of the BE/$\overline{FWFT}$ pin during FIFO operation determines the mode in use.

Each FIFO has a combined Empty/Output Ready Flag ($\overline{EFA}$/ORA and $\overline{EFB}$/ORB) and a combined Full/Input Ready Flag ($\overline{FFA}$/IRA and $\overline{FFB}$/IRB). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the IDT Standard mode. $\overline{EF}$ indicates whether or not the FIFO memory is empty. $\overline{FF}$ shows whether the memory is full or not. The IR and OR functions are selected in the First Word Fall Through mode. IR indicates whether or not the FIFO has available memory locations. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

Each FIFO has a programmable Almost-Empty flag ($\overline{AEA}$ and $\overline{AEB}$) and a programmable Almost-Full flag ($\overline{AFA}$ and $\overline{AFB}$). $\overline{AEA}$ and $\overline{AEB}$ indicate when a selected number of words remain in the FIFO memory. $\overline{AFA}$ and $\overline{AFB}$ indicate when the FIFO contains more than a selected number of words.

$\overline{FFA}$/IRA, $\overline{FFB}$/IRB, $\overline{AFA}$ and $\overline{AFB}$ are two-stage synchronized to the port clock that writes data into its array. $\overline{EFA}$/ORA, $\overline{EFB}$/ORB, $\overline{AEA}$ and $\overline{AEB}$ are two-stage synchronized to the port clock that reads data from its array. Programmable offsets for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$ and $\overline{AFB}$ are loaded in parallel using Port A or in serial via the SD input. Five default offset settings are also provided. The $\overline{AEA}$ and $\overline{AEB}$ threshold can be set at 8, 16, 64, 256 or 1,024 locations from the empty boundary and the $\overline{AFA}$ and $\overline{AFB}$ threshold can be set at 8, 16, 64, 256 or 1,024 locations from the full boundary. All these choices are made using the FS0, FS1 and FS2 inputs during Master Reset.

Interspersed Parity can also be selected during a Master Reset of the FIFO. If Interspersed Parity is selected then during parallel programming of the flag offset values, the device will ignore data line A8. If Non-Interspersed Parity is selected then data line A8 will become a valid bit.

Two or more devices may be used in parallel to create wider data paths. If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. During the power down state, supply current consumption (I_{CC}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the power down state.

The IDT72V3684/72V3694/72V36104 are characterized for operation from 0°C to 70°C. Industrial temperature range (-40°C to +85°C) is available. They are fabricated using IDT's high speed, submicron CMOS technology.

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port A Almost-Empty Flag	O	Programmable Almost-Empty flag synchronized to CLKA. It is LOW when the number of words in FIFO2 is less than or equal to the value in the Almost-Empty A Offset register, X2.
$\overline{AEB}$	Port B Almost-Empty Flag	O	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in FIFO1 is less than or equal to the value in the Almost-Empty B Offset register, X1.
$\overline{AFA}$	Port A Almost-Full Flag	O	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in FIFO1 is less than or equal to the value in the Almost-Full A Offset register, Y1.
$\overline{AFB}$	Port B Almost-Full Flag	O	Programmable Almost-Full flag synchronized to CLKB. It is LOW when the number of empty locations in FIFO2 is less than or equal to the value in the Almost-Full B Offset register, Y2.
B0-B35	Port A Data	I/O	36-bit bidirectional data port for side B.
BE/$\overline{FWFT}$	Big-Endian/ First Word Fall Through Select	I	This is a dual purpose pin. During Master Reset, a HIGH on BE will select Big Endian operation. In this case, depending on the bus size, the most significant byte or word on Port A is read from Port B first (A-to-B data flow) or written to Port B first (B-to-A data flow). A LOW on BE will select Little-Endian operation. In this case, the least significant byte or word on Port A is read from Port B first (for A-to-B data flow) or written to Port B first (B-to-A data flow). After Master Reset, this pin selects the timing mode. A HIGH on $\overline{FWFT}$ selects IDT Standard mode, a LOW selects First Word Fall Through mode. Once the timing mode has been selected, the level on $\overline{FWFT}$ must be static throughout device operation.
BM[1]	Bus-Match Select (Port B)	I	A HIGH on this pin enables either byte or word bus width on Port B, depending on the state of SIZE. A LOW selects long word operation. BM works with SIZE and BE to select the bus size and endian arrangement for Port B. The level of BM must be static throughout device operation.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through Port A and can be asynchronous or coincident to CLKB. $\overline{FFA}$/IRA, $\overline{EFA}$/ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through Port B and can be asynchronous or coincident to CLKA. $\overline{FFB}$/IRB, $\overline{EFB}$/ORB, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable to LOW-to-HIGH transition of CLKA to read or write on Port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EFA}$/ORA	Port A Empty/ Output Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{EFA}$ function is selected. $\overline{EFA}$ indicates whether or not the FIFO2 memory is empty. In the FWFT mode, the ORA function is selected. ORA indicates the presence of valid data on A0-A35 outputs, available for reading. $\overline{EFA}$/ORA is synchronized to the LOW-to-HIGH transition of CLKA.
$\overline{EFB}$/ORB	Port B Empty/ Output Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{EFB}$ function is selected. $\overline{EFB}$ indicates whether or not the FIFO1 memory is empty. In the FWFT mode, the ORB function is selected. ORB indicates the presence of valid data on the B0-B35 outputs, available for reading. $\overline{EFB}$/ORB is synchronized to the LOW-to-HIGH transition of CLKB.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on Port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B.
$\overline{FFA}$/IRA	Port A Full/ Input Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{FFA}$ function is selected. $\overline{FFA}$ indicates whether or not the FIFO1 memory is full. In the FWFT mode, the IRA function is selected. IRA indicates whether or not there is space available for writing to the FIFO1 memory. $\overline{FFA}$/IRA is synchronized to the LOW-to-HIGH transition of CLKA.
$\overline{FFB}$/IRB	Port B Full/ Input Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{FFB}$ function is selected. $\overline{FFB}$ indicates whether or not the FIFO2 memory is full. In the FWFT mode, the IRB function is selected. IRB indicates whether or not there is space available for writing to the FIFO2 memory. $\overline{FFB}$/IRB is synchronized to the LOW-to-HIGH transition of CLKB.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O	Description
FS0/SD	Flag Offset Select 0/ Serial Data	I	FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag offset register programming. During Master Reset, FS1/$\overline{SEN}$ and FS0/SD, together with FS2, select the flag offset programming method. Three offset register programming methods are available: automatically load one of five preset values (8, 16, 64, 256 or 1,024), parallel load from Port A, and serial load.
FS1/$\overline{SEN}$	Flag Offset Select 1/ Serial Enable,	I	When serial load is selected for flag offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/$\overline{SEN}$ is LOW, a rising edge on CLKA load the bit present on FS0/SD into the X and Y registers. The number of bit writes required to program the offset registers is 56 for the IDT72V3684, 60 for the IDT72V3694, and 64 for the IDT72V36104. The first bit write stores the Y- register (Y1) MSB and the last bit write stores the X-register (X2) LSB.
FS2[1]	Flag Offset Select 2	I	
MBA	Port A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a Port A read or write operation. When the A0-A35 outputs are active, a HIGH level on MBA selects data from the mail2 register for output and a LOW level selects FIFO2 output register data for output.
MBB	Port B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a Port B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output and a LOW level selects FIFO1 output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a Port B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH following either a Master or Partial Reset of FIFO1.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a Port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH following either a Master or Partial Reset of FIFO2.
$\overline{MRS1}$	FIFO1 Master Reset	I	A LOW on this pin initializes the FIFO1 read and write pointers to the first location of memory and sets the Port B output register to all zeroes. A LOW-to-HIGH transition on $\overline{MRS1}$ selects the programming method (serial or parallel) and one of five programmable flag default offsets for FIFO1 and FIFO2. It also configures Port B for bus size and endian arrangement. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{MRS1}$ is LOW.
$\overline{MRS2}$	FIFO2 Master Reset	I	A LOW on this pin initializes the FIFO2 read and write pointers to the first location of memory and sets the Port A output register to all zeroes. A LOW-to-HIGH transition on $\overline{MRS2}$, toggled simultaneously with $\overline{MRS1}$, selects the programming method (serial or parallel) and one of the programmable flag default offsets for FIFO2. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{MRS2}$ is LOW.
$\overline{PRS1}$/ $\overline{RT1}$	Partial Reset/ Retransmit FIFO1	I	This pin is muxed for both Partial Reset and Retransmit operations, it is used in conjunction with the RTM pin. If RTM is in a LOW condition, a LOW on this pin performs a Partial Reset on FIFO1 and initializes the FIFO1 read and write pointers to the first location of memory and sets the Port B output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained. If RTM is HIGH, a LOW on this pin performs a Retransmit and initializes the FIFO1 read pointer only to the first memory location.
$\overline{PRS2}$/ $\overline{RT2}$	Partial Reset/ Retransmit FIFO2	I	This pin is muxed for both Partial Reset and Retransmit operations, it is used in conjunction with the RTM pin. If RTM is in a LOW condition, a LOW on this pin performs a Partial Reset on FIFO2 and initializes the FIFO2 read and write selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained. If RTM is HIGH, a LOW on this pin performs a Retransmit and initializes the FIFO2 read pointer only to the first memory location.
RTM	Retransmit Mode	I	This pin is used in conjunction with the $\overline{RT1}$ and $\overline{RT2}$ pins. When RTM is HIGH a Retransmit is performed on FIFO1 or FIFO2 respectively.
SIZE[1]	Bus Size Select	I	A HIGH on this pin when BM is HIGH selects byte bus (9-bit) size on Port B. A LOW on this pin when BM is HIGH selects word (18-bit) bus size. SIZE works with BM and BE to select the bus size and endian arrangement for Port B. The level of SIZE must be static throughout device operation
W/$\overline{RA}$	Port-A Write/ Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on Port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the HIGH impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port-B Write/ Read Select	I	A LOW selects a write operation and a HIGH selects a read operation on Port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the HIGH impedance state when $\overline{W}$/RB is LOW.

NOTE:
1. FS2, BM and SIZE inputs are not TTL compatible. These inputs should be tied to GND or V_{CC}.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current (V_O = < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±400	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}(1)	Supply Voltage	3.15	3.3	3.45	V
V_{IH}	High-Level Input Voltage	2	—	V_{CC}+0.5	V
V_{IL}	Low-Level Input Voltage	—	—	0.8	V
I_{OH}	High-Level Output Current	—	—	–4	mA
I_{OL}	Low-Level Output Current	—	—	8	mA
T_A	Operating Temperature	0	—	70	°C

NOTE:
1. V_{CC} = 3.3V ± 0.15V, JEDEC JESD8-A compliant

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)

Symbol	Parameter	Test Conditions		IDT72V3684 IDT72V3694 IDT72V36104 Commercial t_{CLK} = 10, 15 ns(2) Min.	Typ.	Max.	Unit
V_{OH}	Output Logic "1" Voltage	V_{CC} = 3.0V,	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage	V_{CC} = 3.0V,	I_{OL} = 8 mA	—	—	0.5	V
I_{LI}	Input Leakage Current (Any Input)	V_{CC} = 3.6V,	V_I = V_{CC} or 0	—	—	±5	µA
I_{LO}	Output Leakage Current	V_{CC} = 3.6V,	V_O = V_{CC} or 0	—	—	±5	µA
I_{CC2}(3)	Standby Current (with CLKA and CLKB running)	V_{CC} = 3.6V,	V_I = V_{CC} - 0.2V or 0	—	—	15	mA
I_{CC3}(3)	Standby Current (no clocks running)	V_{CC} = 3.6V,	V_I = V_{CC} - 0.2V or 0	—	—	5	mA
C_{IN}(4)	Input Capacitance	V_I = 0,	f = 1 MHz	—	4	—	pF
C_{OUT}(4)	Output Capacitance	V_O = 0,	f = 1 MHZ	—	8	—	pF

NOTES:
1. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
2. V_{CC} = 3.3V ± 0.15V, T_A = 0° to +70°; JEDEC JESD8-A compliant
3. For additional I_{CC} information, see Figure 1, *Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)*.
4. Characterized values, not currently tested.

DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 1 was taken while simultaneously reading and writing a FIFO on the IDT72V3684/72V3694/72V36104 with CLKA and CLKB set to fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero capacitance load. Once the capacitance load per data-output channel and the number of these device's inputs driven by TTL HIGH levels are known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC(f)}$ taken from Figure 1, the maximum power dissipation (PT) of these FIFOs may be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \sum_{N}(C_L \times V_{CC}^2 \times f_o)$$

where:

N	=	number of used outputs (36-bit (long word), 18-bit (word) or 9-bit (byte) bus size)
C_L	=	output capacitance load
f_o	=	switching frequency of an output

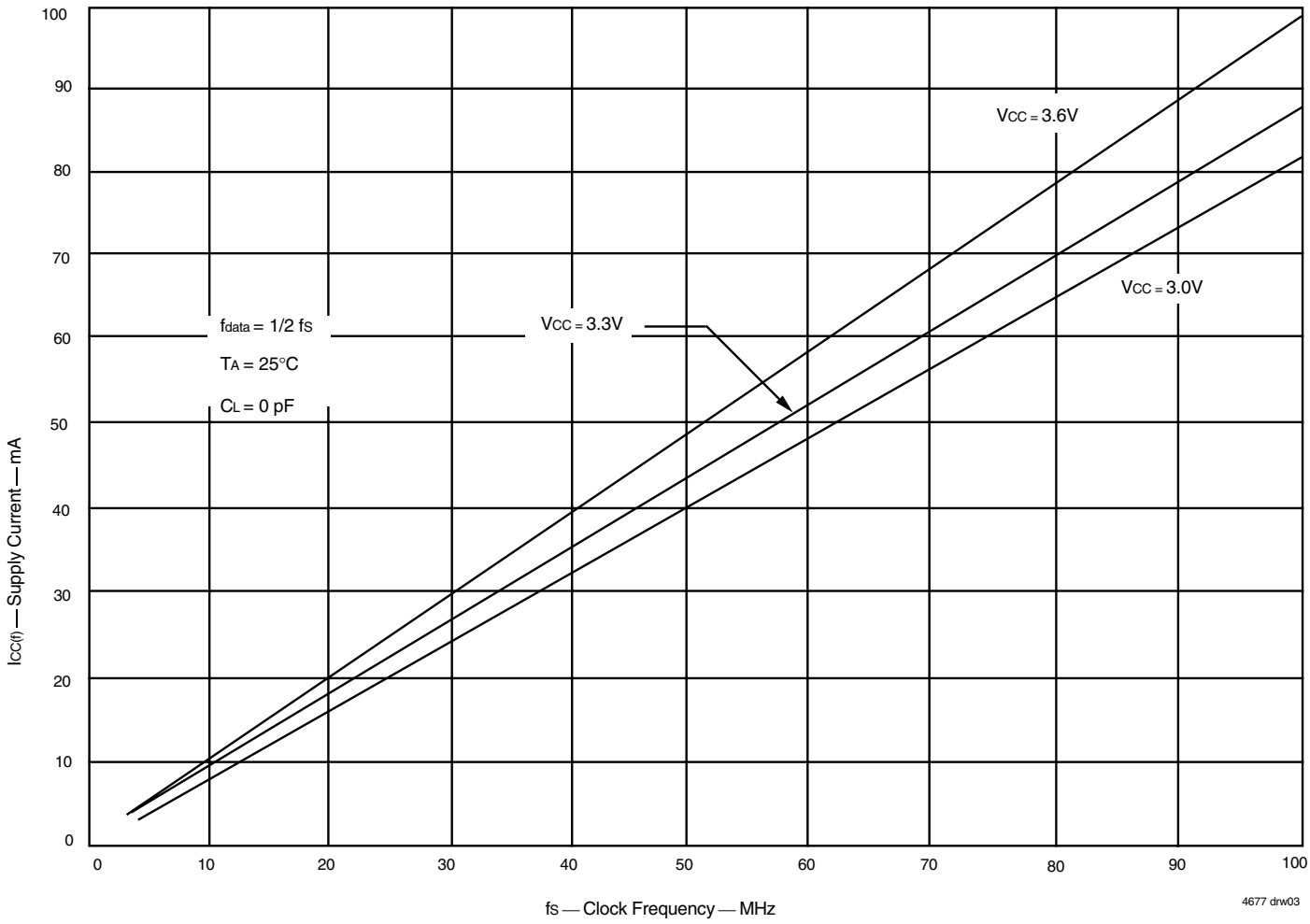


Figure 1. Typical Characteristics: Supply Current (Icc) vs. Clock Frequency (fs)

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

(Vcc = 3.3V ± 0.15V; TA = 0° C to +70° C; JEDEC JESD8-A compliant)

Symbol	Parameter	IDT72V3684L10 IDT72V3694L10 IDT72V36104L10		IDT72V3684L15 IDT72V3694L15 IDT72V36104L15		Unit
		Min.	Max.	Min.	Max.	
fS	Clock Frequency, CLKA or CLKB	—	100	—	66.7	MHz
tCLK	Clock Cycle Time, CLKA or CLKB	10	—	15	—	ns
tCLKH	Pulse Duration, CLKA or CLKB HIGH	4.5	—	6	—	ns
tCLKL	Pulse Duration, CLKA and CLKB LOW	4.5	—	6	—	ns
tDS	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	3	—	4	—	ns
tENS1	Setup Time, $\overline{CSA}$ and W/$\overline{RA}$ before CLKA↑; $\overline{CSB}$ and $\overline{W}$/RB before CLKB↑	4	—	4.5	—	ns
tENS2	Setup Time, ENA, and MBA before CLKA↑; ENB, and MBB before CLKB↑	3	—	4.5	—	ns
tRSTS	Setup Time, $\overline{MRS1}$, $\overline{MRS2}$, $\overline{PRS1}$, or $\overline{PRS2}$ LOW before CLKA↑ or CLKB↑(1)	5	—	5	—	ns
tFSS	Setup Time, FS0, FS1, FS2 before $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	7.5	—	7.5	—	ns
tBES	Setup Time, BE/$\overline{FWFT}$ before $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	7.5	—	7.5	—	ns
tSDS	Setup Time, FS0/SD before CLKA↑	3	—	4	—	ns
tSENS	Setup Time, FS1/$\overline{SEN}$ before CLKA↑	3	—	4	—	ns
tFWS	Setup Time, BE/$\overline{FWFT}$ before CLKA↑	0	—	0	—	ns
tRTMS	Setup Time, RTM before $\overline{RT1}$; RTM before $\overline{RT2}$	5	—	5	—	ns
tDH	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	0.5	—	1	—	ns
tENH	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	0.5	—	1	—	ns
tRSTH	Hold Time, $\overline{MRS1}$, $\overline{MRS2}$, $\overline{PRS1}$ or $\overline{PRS2}$ LOW after CLKA↑ or CLKB↑(1)	4	—	4	—	ns
tFSH	Hold Time, FS0, FS1, FS2 after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	2	—	2	—	ns
tBEH	Hold Time, BE/$\overline{FWFT}$ after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	2	—	2	—	ns
tSDH	Hold Time, FS0/SD after CLKA↑	0.5	—	1	—	ns
tSENH	Hold Time, FS1/$\overline{SEN}$ HIGH after CLKA↑	0.5	—	1	—	ns
tSPH	Hold Time, FS1/$\overline{SEN}$ HIGH after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	2	—	2	—	ns
tRTMH	Hold Time, RTM after $\overline{RT1}$; RTM after $\overline{RT2}$	5	—	5	—	ns
tSKEW1(2)	Skew Time between CLKA↑ and CLKB↑ for $\overline{EFA}$/ORA, $\overline{EFB}$/ORB, $\overline{FFA}$/IRA, and $\overline{FFB}$/IRB	5	—	7.5	—	ns
tSKEW2(2,3)	Skew Time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	12	—	12	—	ns

NOTES:
1. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
2. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.
3. Design simulated, not tested.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30pF

(V_{CC} = 3.3V ± 0.15V; T_A = 0° C to +70° C; JEDEC JESD8-A compliant)

Symbol	Parameter	IDT72V3684L10 IDT72V3694L10 IDT72V36104L10		IDT72V3684L15 IDT72V3694L15 IDT72V36104L15		Unit
		Min.	Max.	Min.	Max.	
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	2	6.5	2	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FFA}$/IRA and CLKB↑ to $\overline{FFB}$/IRB	2	6.5	2	8	ns
t_{REF}	Propagation Delay Time, CLKA↑ to $\overline{EFA}$/ORA and CLKB↑ to $\overline{EFB}$/ORB	1	6.5	1	8	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	6.5	1	8	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	1	6.5	1	8	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	6.5	0	8	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	3	8	2	10	ns
t_{MDV}	Propagation Delay Time, MBA to A0-A35 valid and MBB to B0-B35 valid	3	6.5	2	10	ns
t_{RSF}	Propagation Delay Time, $\overline{MRS1}$ or $\overline{PRS1}$ LOW to $\overline{AEB}$ LOW, $\overline{AFA}$ HIGH, and $\overline{MBF1}$ HIGH and $\overline{MRS2}$ or $\overline{PRS2}$ LOW to $\overline{AEA}$ LOW, $\overline{AFB}$ HIGH, and $\overline{MBF2}$ HIGH	1	10	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ or W/$\overline{RA}$ LOW to A0-A35 Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 Active	2	6	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high-impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at high-impedance	1	6	1	8	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.

SIGNAL DESCRIPTION

MASTER RESET ($\overline{MRS1}$, $\overline{MRS2}$)

After power up, a Master Reset operation must be performed by providing a LOW pulse to $\overline{MRS1}$ and $\overline{MRS2}$ simultaneously. Afterwards, each of the two FIFO memories of the IDT72V3684/72V3694/72V36104 undergoes a complete reset by taking its associated Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input LOW for at least four Port A Clock (CLKA) and four Port B Clock (CLKB) LOW-to-HIGH transitions. The Master Reset inputs can switch asynchronously to the clocks. A Master Reset initializes the associated write and read pointers to the first location of the memory and forces the Full/Input Ready flag ($\overline{FFA}$/IRA, $\overline{FFB}$/IRB) LOW, the Empty/Output Ready flag ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB) LOW, the Almost-Empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW and forces the Almost-Full flag ($\overline{AFA}$, $\overline{AFB}$) HIGH. A Master Reset also forces the associated Mailbox Flag ($\overline{MBF1}$, $\overline{MFB2}$) of the parallel mailbox register HIGH. After a Master Reset, the FIFO's Full/Input Ready flag is set HIGH after two write clock cycles. Then the FIFO is ready to be written to.

A LOW-to-HIGH transition on the FIFO1 Master Reset ($\overline{MRS1}$) input latches the values of the Big-Endian (BE) input for determining the order by which bytes are transferred through Port B. It also latches the values of the Flag Select (FS0, FS1 and FS2) inputs for choosing the Almost-Full and Almost-Empty offset programming method.

A LOW-to-HIGH transition on the FIFO2 Master Reset ($\overline{MRS2}$) clears the Flag Offset Registers of FIFO2 (X2, Y2). A LOW-to-HIGH transition on the FIFO2 Master Reset ($\overline{MRS2}$) together with the FIFO1 Master Reset ($\overline{MRS1}$) input latches the value of the Big-Endian (BE) input for Port B and also latches the values of the Flag Select (FS0, FS1 and FS2) inputs for choosing the Almost-Full and Almost-Empty offset programming method. (For details see Table 1, *Flag Programming*, and the *Programming the Almost-Empty and Almost-Full Flags* section). The relevant FIFO Master Reset timing diagram can be found in Figure 3.

PARTIAL RESET ($\overline{PRS1}$, $\overline{PRS2}$)

Each of the two FIFO memories of these devices undergoes a limited reset by taking its associated Partial Reset ($\overline{PRS1}$, $\overline{PRS2}$) input LOW for at least four Port A Clock (CLKA) and four Port B Clock (CLKB) LOW-to-HIGH transitions. The Partial Reset inputs can switch asynchronously to the clocks. A Partial Reset initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FFA}$/IRA, $\overline{FFB}$/IRB) LOW, the Empty/Output Ready flag ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB) LOW, the Almost-Empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW, and the Almost-Full flag ($\overline{AFA}$, $\overline{AFB}$) HIGH. A Partial Reset also forces the Mailbox Flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a Partial Reset, the FIFO's Full/Input Ready flag is set HIGH after two write clock cycles. Then the FIFO is ready to be written to.

Whatever flag offsets, programming method (parallel or serial), and timing mode (FWFT or IDT Standard mode) are currently selected at the time a Partial Reset is initiated, those settings will be remain unchanged upon completion of the reset operation. A Partial Reset may be useful in the case where reprogramming a FIFO following a Master Reset would be inconvenient. See Figure 4 for the Partial Reset timing diagram.

RETRANSMIT ($\overline{RT1}$, $\overline{RT2}$)

The FIFO1 memory of these devices undergoes a Retransmit by taking its associated Retransmit ($\overline{RT1}$) input LOW for at least four Port A Clock (CLKA) and four Port B Clock (CLKB) LOW-to-HIGH transitions. The Retransmit initializes the read pointer of FIFO1 to the first memory location.

The FIFO2 memory undergoes a Retransmit by taking its associated Retransmit ($\overline{RT2}$) input LOW for at least four Port A Clock (CLKA) and four Port C Clock (CLKC) LOW-to-HIGH transitions. The Retransmit initializes the read pointer of FIFO2 to the first memory location.

The RTM pin must be HIGH during the time of Retransmit. Note that the $\overline{RT1}$ input is muxed with the $\overline{PRS1}$ input, the state of the RTM pin determining whether this pin performs a Retransmit or Partial Reset. Also, the $\overline{RT2}$ input is muxed with the $\overline{PRS2}$ input, the state of the RTM pin determining whether this pin performs a Retransmit or Partial Reset.

BIG-ENDIAN/FIRST WORD FALL THROUGH (BE/$\overline{FWFT}$)

— ENDIAN SELECTION

This is a dual purpose pin. At the time of Master Reset, the BE select function is active, permitting a choice of Big or Little-Endian byte arrangement for data written to or read from Port B. This selection determines the order by which bytes (or words) of data are transferred through this port. For the following illustrations, assume that a byte (or word) bus size has been selected for Port B. (Note that when Port B is configured for a long word size, the Big-Endian function has no application and the BE input is a "don't care"[1].)

A HIGH on the BE/$\overline{FWFT}$ input when the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) inputs go from LOW to HIGH will select a Big-Endian arrangement. When data is moving in the direction from Port A to Port B, the most significant byte (word) of the long word written to Port A will be read from Port B first; the least significant byte (word) of the long word written to Port A will be read from Port B last. When data is moving in the direction from Port B to Port A, the byte (word) written to Port B first will be read from Port A as the most significant byte (word) of the long word; the byte (word) written to Port B last will be read from Port A as the least significant byte (word) of the long word.

A LOW on the BE/$\overline{FWFT}$ input when the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) inputs go from LOW to HIGH will select a Little-Endian arrangement. When data is moving in the direction from Port A to Port B, the least significant byte (word) of the long word written to Port A will be read from Port B first; the most significant byte (word) of the long word written to Port A will be read from Port B last. When data is moving in the direction from Port B to Port A, the byte (word) written to Port B first will be read from Port A as the least significant byte (word) of the long word; the byte (word) written to Port B last will be read from Port A as the most significant byte (word) of the long word. Refer to Figure 2 for an illustration of the BE function. See Figure 3 (Master Reset) for the Endian select timing diagram.

— TIMING MODE SELECTION

After Master Reset, the FWFT select function is active, permitting a choice between two possible timing modes: IDT Standard mode or First Word Fall Through (FWFT) mode. Once the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input is HIGH, a HIGH on the BE/$\overline{FWFT}$ input during the next LOW-to-HIGH transition of CLKA (for FIFO1) and CLKB (for FIFO2) will select IDT Standard mode. This mode uses the Empty Flag function ($\overline{EFA}$, $\overline{EFB}$) to indicate whether or not there are any words present in the FIFO memory. It uses the Full Flag function ($\overline{FFA}$, $\overline{FFB}$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using a formal read operation.

NOTE:
1. Either a HIGH or LOW can be applied to a "don't care" input with no change to the logical operation of the FIFO. Nevertheless, inputs that are temporarily "don't care" (along with unused inputs) must not be left open, rather they must be either HIGH or LOW.

Once the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input is HIGH, a LOW on the BE/$\overline{FWFT}$ input during the next LOW-to-HIGH transition of CLKA (for FIFO1) and CLKB (for FIFO2) will select FWFT mode. This mode uses the Output Ready function (ORA, ORB) to indicate whether or not there is valid data at the data outputs (A0-A35 or B0-B35). It also uses the Input Ready function (IRA, IRB) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs, no read request necessary. Subsequent words must be accessed by performing a formal read operation.

Following Master Reset, the level applied to the BE/$\overline{FWFT}$ input to choose the desired timing mode must remain static throughout FIFO operation. Refer to Figure 3 (Master Reset) for a First Word Fall Through select timing diagram.

PROGRAMMING THE ALMOST-EMPTY AND ALMOST-FULL FLAGS

Four registers in the IDT72V3684/72V3694/72V36104 are used to hold the offset values for the Almost-Empty and Almost-Full flags. The Port B Almost-Empty flag ($\overline{AEB}$) Offset register is labeled X1 and the Port A Almost-Empty flag ($\overline{AEA}$) Offset register is labeled X2. The Port A Almost-Full flag ($\overline{AFA}$) Offset register is labeled Y1 and the Port B Almost-Full flag ($\overline{AFB}$) Offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO, programmed in parallel using the FIFO's Port A data inputs, or programmed in serial using the Serial Data (SD) input (see Table 1).

FS0/SD, FS1/$\overline{SEN}$ and FS2 function the same way in both IDT Standard and FWFT modes.

— PRESET VALUES

To load a FIFO's Almost-Empty flag and Almost-Full flag Offset registers with one of the five preset values listed in Table 1, the flag select inputs must be HIGH or LOW during a master reset. For example, to load the preset value of 64 into X1 and Y1, FS0, FS1 and FS2 must be HIGH when FIFO1 reset ($\overline{MRS1}$) returns HIGH. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 Master Reset ($\overline{MRS2}$), toggled simultaneously with FIFO1 Master Reset ($\overline{MRS1}$). For relevant preset value loading timing diagram, see Figure 3.

— PARALLEL LOAD FROM PORT A

To program the X1, X2, Y1, and Y2 registers from Port A, perform a Master Reset on both FIFOs simultaneously with FS2 HIGH or LOW, FS0 and FS1 LOW during the LOW-to-HIGH transition of MRS1 and MRS2. The state of FS2 at this point of reset will determine whether the parallel programming method has Interspersed Parity or Non-Interspersed Parity. Refer to Table 1 for Flag Programming Flag Offset setup . It is important to note that once parallel programming has been selected during a Master Reset by holding both FS0 & FS1 LOW, these inputs must remain LOW during all subsequent FIFO operation. They can only be toggled HIGH when future Master Resets are performed and other programming methods are desired.

After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the Offset registers in the order Y1, X1, Y2, X2. For Non-Interspersed Parity mode the Port A data inputs used by the Offset registers are (A13-A0), (A14-A0), or (A15-A0) for the IDT72V3684, IDT72V3694, or IDT72V36104, respectively. For Interspersed Parity mode the Port A data inputs used by the Offset registers are (A14-A9, A7-A0), (A15-A9, A7-A0), or (A16-A9, A7-A0) for the IDT72V3684, IDT72V3694, or IDT72V36104, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 1 to 16,380 for the IDT72V3684; 1 to 32,764 for the IDT72V3694; and 1 to 65,532 for the IDT72V36104. After all the offset registers are

TABLE 1 — FLAG PROGRAMMING

FS2	FS1/$\overline{SEN}$	FS0/SD	$\overline{MRS1}$	$\overline{MRS2}$	X1 AND Y1 REGISTERS[1]	X2 AND Y2 REGISTERS[2]
H	H	H	↑	X	64	X
H	H	H	X	↑	X	64
H	H	L	↑	X	16	X
H	H	L	X	↑	X	16
H	L	H	↑	X	8	X
H	L	H	X	↑	X	8
L	H	H	↑	X	256	X
L	H	H	X	↑	X	256
L	L	H	↑	X	1,024	X
L	L	H	X	↑	X	1,024
L	H	L	↑	↑	Serial programming via SD	Serial programming via SD
H	L	L	↑	↑	Parallel programming via Port A[3,5]	Parallel programming via Port A[3,5]
L	L	L	↑	↑	IP Mode[4,5]	IP Mode[4,5]

NOTES:
1. X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.
2. X2 register holds the offset for $\overline{AEA}$; Y2 register holds the offset for $\overline{AFB}$.
3. When this method of parallel programming is selected, Port A will assume Non-Interspersed Parity.
4. When IP Mode is selected, only parallel programming of the offset values via Port A, can be performed and Port A will assume Interspersed Parity.
5. IF parallel programming is selected during a Master Reset, then FS0 & FS1 must remain LOW during FIFO operation.

programmed from Port A, the Port B Full/Input Ready flag ($\overline{FFB}$/IRB) is set HIGH, and both FIFOs begin normal operation. Refer to Figure 5 for a timing diagram illustration of parallel programming of the flag offset values.

INTERSPERSED PARITY

Interspersed Parity is selected during a Master Reset of the FIFO. Refer to Table 1 for the setup configuration of Interspersed Parity. The Interspersed Parity function allows the user to select the location of the parity bits in the word loaded into the parallel port (A0-An) during programming of the flag offset values.

or IDT72V36104, respectively. The four registers are written in the order Y1, X1, Y2, and finally, X2. The first-bit write stores the most significant bit of the Y1 register and the last-bit write stores the least significant bit of the X2 register. Each register value can be programmed from 1 to 16,380 (IDT72V3684), 1 to 32,764 (IDT72V3694), or 1 to 65,532 (IDT72V36104).

When the option to program the offset registers serially is chosen, the Port A Full/Input Ready ($\overline{FFA}$/IRA) flag remains LOW until all register bits are written. $\overline{FFA}$/IRA is set HIGH by the LOW-to-HIGH transition of CLKA after the last bit is loaded to allow normal FIFO1 operation. The Port B Full/Input Ready ($\overline{FFB}$/

TABLE 2 — PORT A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	Data A (A0-A35) I/O	Port Function
H	X	X	X	X	High-Impedance	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO1 write
L	H	H	H	↑	Input	Mail1 write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	FIFO2 read
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail2 read (set $\overline{MBF2}$ HIGH)

TABLE 3 — PORT B ENABLE FUNCTION TABLE

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	Data B (B0-B35) I/O	Port Function
H	X	X	X	X	High-Impedance	None
L	L	L	X	X	Input	None
L	L	H	L	↑	Input	FIFO2 write
L	L	H	H	↑	Input	Mail2 write
L	H	L	L	X	Output	None
L	H	H	L	↑	Output	FIFO1 read
L	H	L	H	X	Output	None
L	H	H	H	↑	Output	Mail1 read (set $\overline{MBF1}$ HIGH)

If Interspersed Parity is selected then during parallel programming of the flag offset values, the device will ignore data line A8. If Non-Interspersed Parity is selected then data line A8 will become a valid bit. If Interspersed Parity is selected serial programming of the offset values is not permitted, only parallel programming can be done.

— SERIAL LOAD

To program the X1, X2, Y1, and Y2 registers serially, initiate a Master Reset with FS2 LOW, FS0/SD LOW and FS1/$\overline{SEN}$ HIGH during the LOW-to-HIGH transition of $\overline{MRS1}$ and $\overline{MRS2}$. After this reset is complete, the X and Y register values are loaded bit-wise through the FS0/SD input on each LOW-to-HIGH transition of CLKA that the FS1/$\overline{SEN}$ input is LOW. There are 56-, 60-, or 64-bit writes needed to complete the programming for the IDT72V3684, IDT72V3694, IRB) flag also remains LOW throughout the serial programming process, until all register bits are written. $\overline{FFB}$/IRB is set HIGH by the LOW-to-HIGH transition of CLKB after the last bit is loaded to allow normal FIFO2 operation. See Figure 6 for *Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values (IDT Standard and FWFT Modes)* timing diagram.

FIFO WRITE/READ OPERATION

The state of the Port A data (A0-A35) lines is controlled by Port A Chip Select ($\overline{CSA}$) and Port A Write/Read select (W/$\overline{RA}$). The A0-A35 lines are in the High-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 lines are active outputs when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is

TABLE 4 — FIFO1 FLAG OPERATION (IDT Standard and FWFT modes)

Number of Words in FIFO Memory[1,2]			Synchronized to CLKB		Synchronized to CLKA	
IDT72V3684[3]	IDT72V3694[3]	IDT72V36104[3]	$\overline{EFB}$/ORB	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$/IRA
0	0	0	L	L	H	H
1 to X1	1 to X1	1 to X1	H	L	H	H
(X1+1) to [16,384-(Y1+1)]	(X1+1) to [32,768-(Y1+1)]	(X1+1) to [65,536-(Y1+1)]	H	H	H	H
(16,384-Y1) to 16,383	(32,768-Y1) to 32,767	(65,536-Y1) to 65,535	H	H	L	H
16,384	32,768	65,536	H	H	L	L

NOTES:
1. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
2. Data in the output register does not count as a "word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. X1 is the Almost-Empty offset for FIFO1 used by $\overline{AEB}$. Y1 is the Almost-Full offset for FIFO1 used by $\overline{AFA}$. Both X1 and Y1 are selected during a FIFO1 reset or port A programming.
4. The ORB and IRA functions are active during FWFT mode; the $\overline{EFB}$ and $\overline{FFA}$ functions are active in IDT Standard mode.

TABLE 5 — FIFO2 FLAG OPERATION (IDT Standard and FWFT modes)

Number of Words in FIFO Memory[1,2]			Synchronized to CLKA		Synchronized to CLKB	
IDT72V3684[3]	IDT72V3694[3]	IDT72V36104[3]	$\overline{EFA}$/ORA	$\overline{AEA}$	$\overline{AFB}$	$\overline{FFB}$/IRB
0	0	0	L	L	H	H
1 to X2	1 to X2	1 to X2	H	L	H	H
(X2+1) to [16,384-(Y2+1)]	(X2+1) to [32,768-(Y2+1)]	(X2+1) to [65,536-(Y2+1)]	H	H	H	H
(16,384-Y2) to 16,383	(32,768-Y2) to 32,767	(65,536-Y2) to 65,535	H	H	L	H
16,384	32,768	65,536	H	H	L	L

NOTES:
1. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
2. Data in the output register does not count as a "word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. X2 is the Almost-Empty offset for FIFO2 used by $\overline{AEA}$. Y2 is the Almost-Full offset for FIFO2 used by $\overline{AFB}$. Both X2 and Y2 are selected during a FIFO2 reset or port A programming.
4. The ORA and IRB functions are active during FWFT mode; the $\overline{EFA}$ and $\overline{FFB}$ functions are active in IDT Standard mode.

LOW, and $\overline{FFA}$/IRA is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and $\overline{EFA}$/ORA is HIGH (see Table 2). FIFO reads and writes on Port A are independent of any concurrent Port B operation.

The Port B control signals are identical to those of Port A with the exception that the Port B Write/Read select ($\overline{W}$/RB) is the inverse of the Port A Write/Read select (W/$\overline{RA}$). The state of the Port B data (B0-B35) lines is controlled by the Port B Chip Select ($\overline{CSB}$) and Port B Write/Read select ($\overline{W}$/RB). The B0-B35 lines are in the high-impedance state when either $\overline{CSB}$ is HIGH or $\overline{W}$/RB is LOW. The B0-B35 lines are active outputs when $\overline{CSB}$ is LOW and $\overline{W}$/RB is HIGH.

Data is loaded into FIFO2 from the B0-B35 inputs on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is LOW, ENB is HIGH, MBB is LOW, and $\overline{FFB}$/IRB is HIGH. Data is read from FIFO1 to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is HIGH, ENB is HIGH, MBB is LOW, and $\overline{EFB}$/ORB is HIGH (see Table 3). FIFO reads and writes on Port B are independent of any concurrent Port A operation.

The setup and hold time constraints to the port clocks for the port Chip Selects and Write/Read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read select may change states during the setup and hold time window of the cycle.

When operating the FIFO in FWFT mode and the Output Ready flag is LOW, the next word written is automatically sent to the FIFO's output register by the LOW-to-HIGH transition of the port clock that sets the Output Ready flag HIGH. When the Output Ready flag is HIGH, subsequent data is clocked to the output registers only when a read is selected using the port's Chip Select, Write/Read select, Enable, and Mailbox select.

When operating the FIFO in IDT Standard mode, the first word will cause the Empty Flag to change state on the second LOW-to-HIGH transition of the Read Clock. The data word will not be automatically sent to the output register. Instead, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, Write/Read select, Enable, and Mailbox select. Write and read timing diagrams for Port A can be found in Figure 7 and 14. Relevant Port B write and read cycle timing

diagrams together with Bus-Matching and Endian select operations can be found in Figures 8 through 13.

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another. $\overline{EFA}$/ORA, $\overline{AEA}$, $\overline{FFA}$/IRA, and $\overline{AFA}$ are synchronized to CLKA. $\overline{EFB}$/ORB, $\overline{AEB}$, $\overline{FFB}$/IRB, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

EMPTY/OUTPUT READY FLAGS ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB)

These are dual purpose flags. In the FWFT mode, the Output Ready (ORA, ORB) function is selected. When the Output-Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

In the IDT Standard mode, the Empty Flag ($\overline{EFA}$, $\overline{EFB}$) function is selected. When the Empty Flag is HIGH, data is available in the FIFO's RAM memory for reading to the output register. When the Empty Flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

The Empty/Output Ready flag of a FIFO is synchronized to the port clock that reads data from its array. For both the FWFT and IDT Standard modes, the FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2.

In FWFT mode, from the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the Output Ready flag synchronizing clock. Therefore, an Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

In IDT Standard mode, from the time a word is written to a FIFO, the Empty Flag will indicate the presence of data available for reading in a minimum of two cycles of the Empty Flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The Empty Flag of the FIFO remains LOW until the second LOW-to-HIGH transition of the synchronizing clock occurs, forcing the Empty Flag HIGH; only then can data be read.

A LOW-to-HIGH transition on an Empty/Output Ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 15, 16, 17, and 18).

FULL/INPUT READY FLAGS ($\overline{FFA}$/IRA, $\overline{FFB}$/IRB)

This is a dual purpose flag. In FWFT mode, the Input Ready (IRA and IRB) function is selected. In IDT Standard mode, the Full Flag ($\overline{FFA}$ and $\overline{FFB}$) function is selected. For both timing modes, when the Full/Input Ready flag is HIGH, a memory location is free in the FIFO to receive new data. No memory locations are free when the Full/Input Ready flag is LOW and attempted writes to the FIFO are ignored.

The Full/Input Ready flag of a FIFO is synchronized to the port clock that writes data to its array. For both FWFT and IDT Standard modes, each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls a Full/Input Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from a FIFO, its previous memory location is ready to be written to in a minimum of two cycles of the Full/Input Ready flag synchronizing clock. Therefore, an Full/Input Ready flag is LOW if less than two cycles of the Full/Input Ready flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Full/Input Ready flag synchronizing clock after the read sets the Full/Input Ready flag HIGH.

A LOW-to-HIGH transition on a Full/Input Ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 19, 20, 21, and 22).

ALMOST-EMPTY FLAGS ($\overline{AEA}$, $\overline{AEB}$)

The Almost-Empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an Almost-Empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see *Almost-Empty flag and Almost-Full flag offset programming* section). An Almost-Empty flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X+1) or more words. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Empty flag synchronizing clock are required after a FIFO write for its Almost-Empty flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing (X+1) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle. (See Figure 23 and 24).

ALMOST-FULL FLAGS ($\overline{AFA}$, $\overline{AFB}$)

The Almost-Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost-Full flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see *Almost-Empty flag and Almost-Full flag offset programming* section). An Almost-Full flag is LOW when the number of words in its FIFO is greater than or equal to (16,384-Y), (32,768-Y), or (65,536-Y) for the IDT72V3684, IDT72V3694, or IDT72V36104 respectively. An Almost-Full flag is HIGH when the number of words in its FIFO is less than or equal to [16,384-(Y+1)], [32,768-(Y+1)], or [65,536-(Y+1)] for the IDT72V3684, IDT72V3694, or IDT72V36104 respectively. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for its Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing [16,384/32,768/65,536-(Y+1)] or less words remains LOW if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [16,384/32,768/65,536-(Y+1)]. An Almost-Full flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [16,384/32,768/65,536-(Y+1)]. A LOW-to-HIGH transition of an Almost-Full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [16,384/32,768/65,536-(Y+1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle (see Figure 25 and 26).

MAILBOX REGISTERS

Each FIFO has a 36-bit bypass register to pass command and control information between Port A and Port B without putting it in queue. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. The usable width of both the Mail1 and Mail2 registers matches the selected bus size for Port B.

A LOW-to-HIGH transition on CLKA writes data to the Mail 1 Register when a Port A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. If the selected Port B bus size is also 36 bits, then the usable width of the Mail1 register employs data lines A0-A35. If the selected Port B bus size is 18 bits, then the usable width of the Mail1 Register employs data lines A0-A17. (In this case, A18-A35 are don't care inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail1 Register employs data lines A0-A8. (In this case, A9-A35 are don't care inputs.)

A LOW-to-HIGH transition on CLKB writes B0-B35 data to the Mail2 Register when a Port B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. If the selected Port B bus size is also 36 bits, then the usable width of the Mail2 employs data lines B0-B35. If the selected Port B bus size is 18 bits, then the usable width of the Mail2 Register employs data lines B0-B17. (In this case, B18-B35 are don't care inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail2 Register employs data lines B0-B8. (In this case, B9-B35 are don't care inputs.)

Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port Mailbox select input is LOW and from the mail register when the port Mailbox select input is HIGH.

The Mail1 Register Flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a Port B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. For a 36-bit bus size, 36 bits of mailbox data are placed on B0-B35. For an 18-bit bus size, 18 bits of mailbox data are placed on B0-B17. (In this case, B18-B35 are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on B0-B8. (In this case, B9-B35 are indeterminate.)

The Mail2 Register Flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a Port A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH.

For a 36-bit bus size, 36 bits of mailbox data are placed on A0-A35. For an 18-bit bus size, 18 bits of mailbox data are placed on A0-A17. (In this case, A18-A35 are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on A0-A8. (In this case, A9-A35 are indeterminate.)

The data in a mail register remains intact after it is read and changes only when new data is written to the register. The Endian select feature has no effect on mailbox data. For mail register and Mail Register Flag timing diagrams, see Figure 27 and 28.

BUS SIZING

The Port B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from FIFO1 or written to FIFO2. The levels applied to the Port B Bus Size select (SIZE) and the Bus-Match select (BM) determine the Port B bus size. These levels should be static throughout FIFO operation. Both bus size selections are implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH, as shown in Figure 2.

Two different methods for sequencing data transfer are available for Port B when the bus size selection is either byte- or word-size. They are referred to as Big-Endian (most significant byte first) and Little-Endian (least significant byte first). The level applied to the Big-Endian select (BE) input during the LOW-to-HIGH transition of $\overline{MRS1}$ and $\overline{MRS2}$ selects the endian method that will be active during FIFO operation. BE is a don't care input when the bus size selected for Port B is long word. The endian method is implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH, as shown in Figure 2.

Only 36-bit long word data is written to or read from the two FIFO memories on the IDT72V3684/72V3694/72V36104. Bus-matching operations are done after data is read from the FIFO1 RAM and before data is written to the FIFO2 RAM. These bus-matching operations are not available when transferring data via mailbox registers. Furthermore, both the word- and byte-size bus selections limit the width of the data bus that can be used for mail register operations. In this case, only those byte lanes belonging to the selected word- or byte-size bus can carry mailbox data. The remaining data outputs will be indeterminate. The remaining data inputs will be don't care inputs. For example, when a word-size bus is selected, then mailbox data can be transmitted only between A0-A17 and B0-B17. When a byte-size bus is selected, then mailbox data can be transmitted only between A0-A8 and B0-B8. (See Figures 27 and 28).

BUS-MATCHING FIFO1 READS

Data is read from the FIFO1 RAM in 36-bit long word increments. If a long word bus size is implemented, the entire long word immediately shifts to the FIFO1 output register. If byte or word size is implemented on Port B, only the first one or two bytes appear on the selected portion of the FIFO1 output register, with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO1 reads output the rest of the long word to the FIFO1 output register in the order shown by Figure 2.

When reading data from FIFO1 in byte or word format, the unused B0-B35 outputs are indeterminate.

BUS-MATCHING FIFO2 WRITES

Data is written to the FIFO2 RAM in 36-bit long word increments. Data written to FIFO2 with a byte or word bus size stores the initial bytes or words in auxiliary registers. The CLKB rising edge that writes the fourth byte or the second word of long word to FIFO2 also stores the entire long word in the FIFO2 memory. The bytes are arranged in the manner shown in Figure 2.

When writing data to FIFO2 in byte or word format, the unused B0-B35 inputs are don't care inputs.

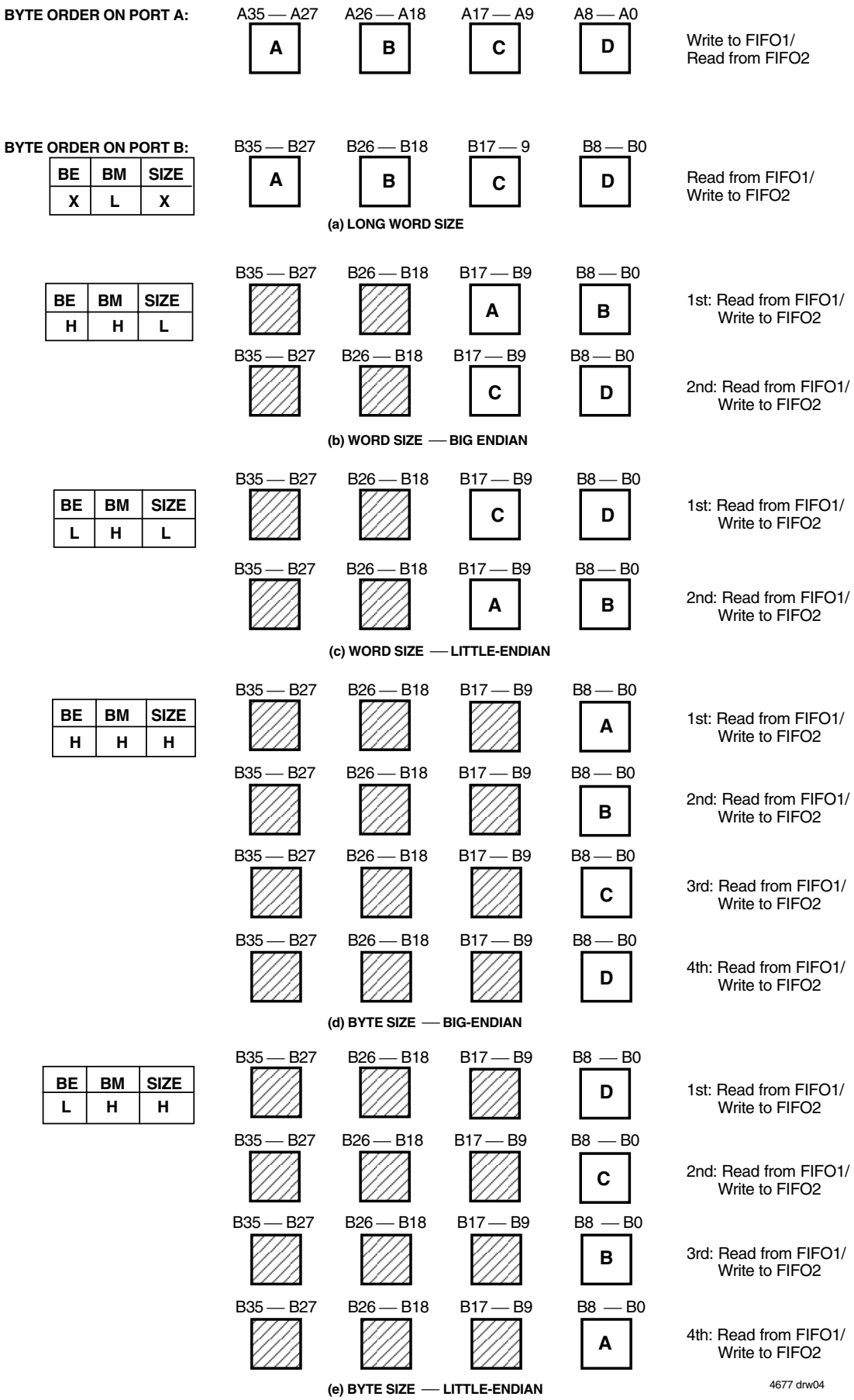
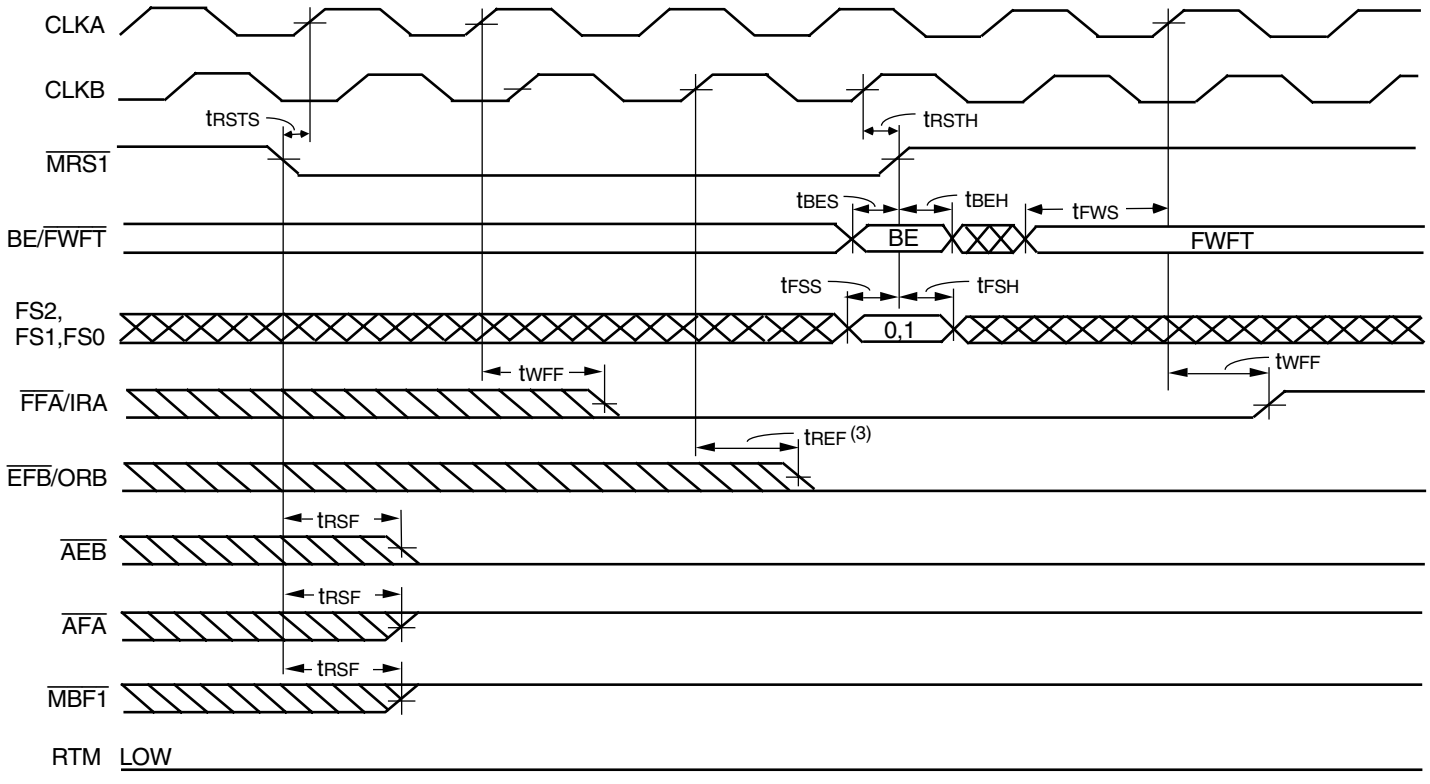
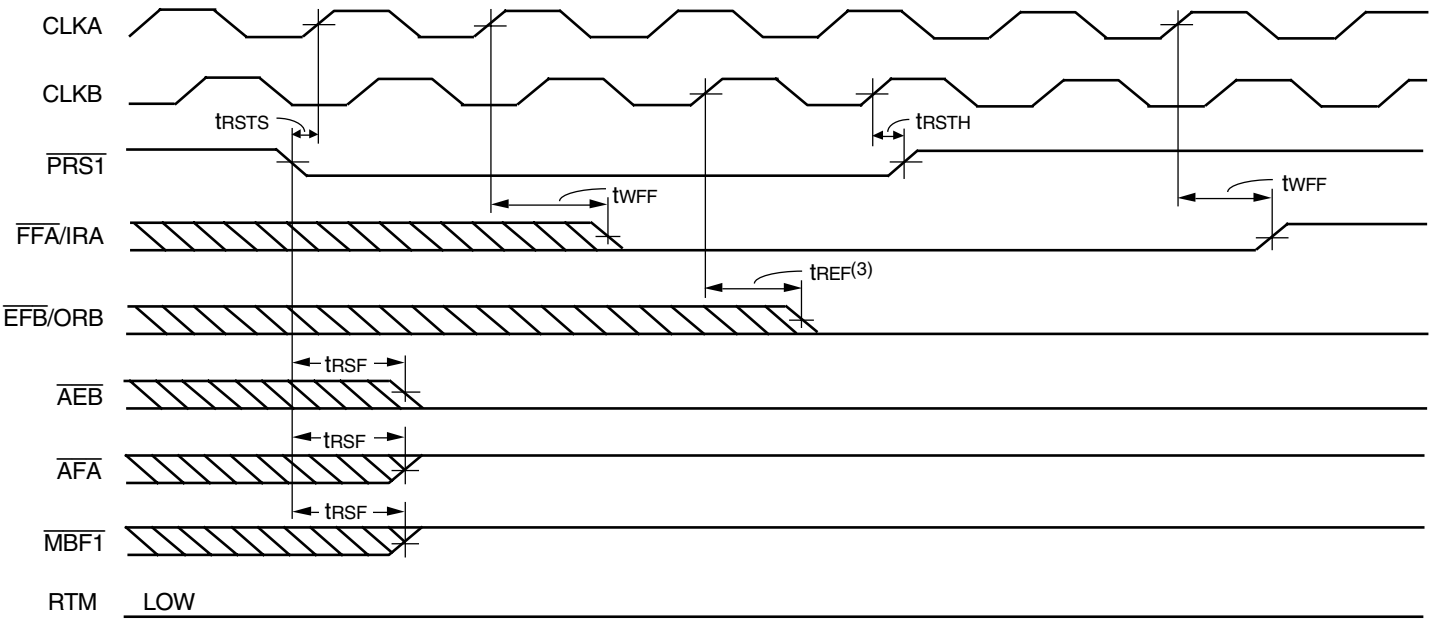


Figure 2. Bus Sizing



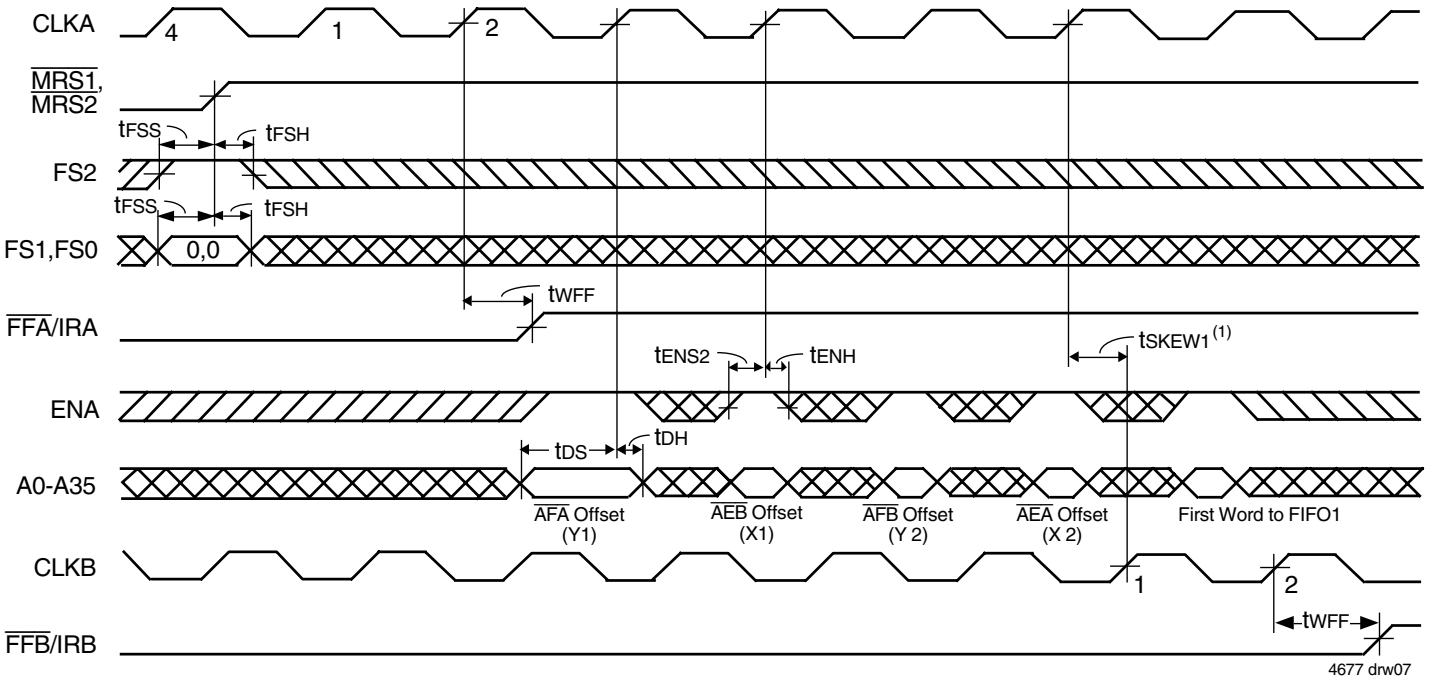
NOTES:
1. FIFO2 Master Reset ($\overline{MRS2}$) is performed in the same manner to load X2 and Y2 with a preset value. For FIFO2 Master Reset, $\overline{MRS1}$ must toggle simultaneously with $\overline{MRS2}$.
2. $\overline{PRS1}$ must be HIGH during Master Reset.
3. If BE/$\overline{FWFT}$ is HIGH, then $\overline{EFB}$/ORB will go LOW one CLKB cycle earlier than in this case where BE/$\overline{FWFT}$ is LOW.

Figure 3. FIFO1 Master Reset and Loading X1 and Y1 with a Preset Value of Eight(1) (IDT Standard and FWFT Modes)



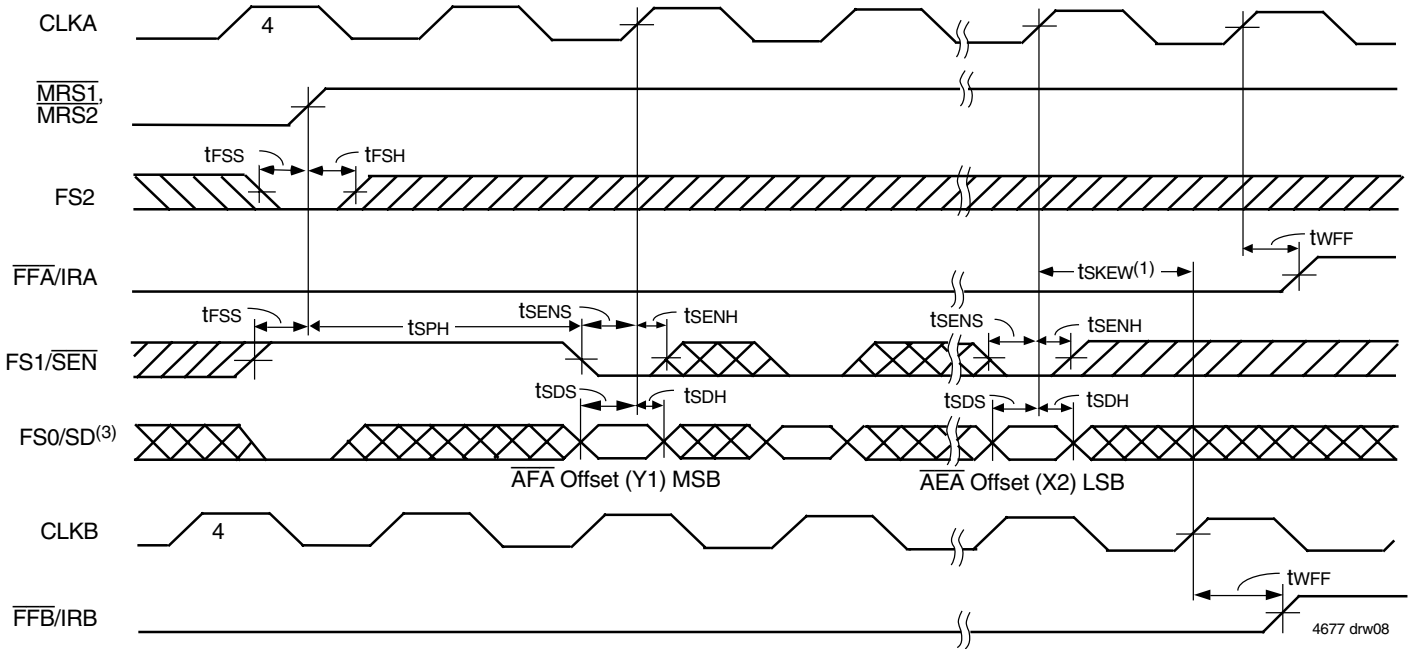
NOTES:
1. Partial Reset is performed in the same manner for FIFO2.
2. $\overline{MRS1}$ must be HIGH during Partial Reset.
3. If BE/$\overline{FWFT}$ is HIGH, then $\overline{EFB}$/ORB will go LOW one CLKB cycle earlier than in this case where BE/$\overline{FWFT}$ is LOW.

Figure 4. FIFO1 Partial Reset(1) (IDT Standard and FWFT Modes)



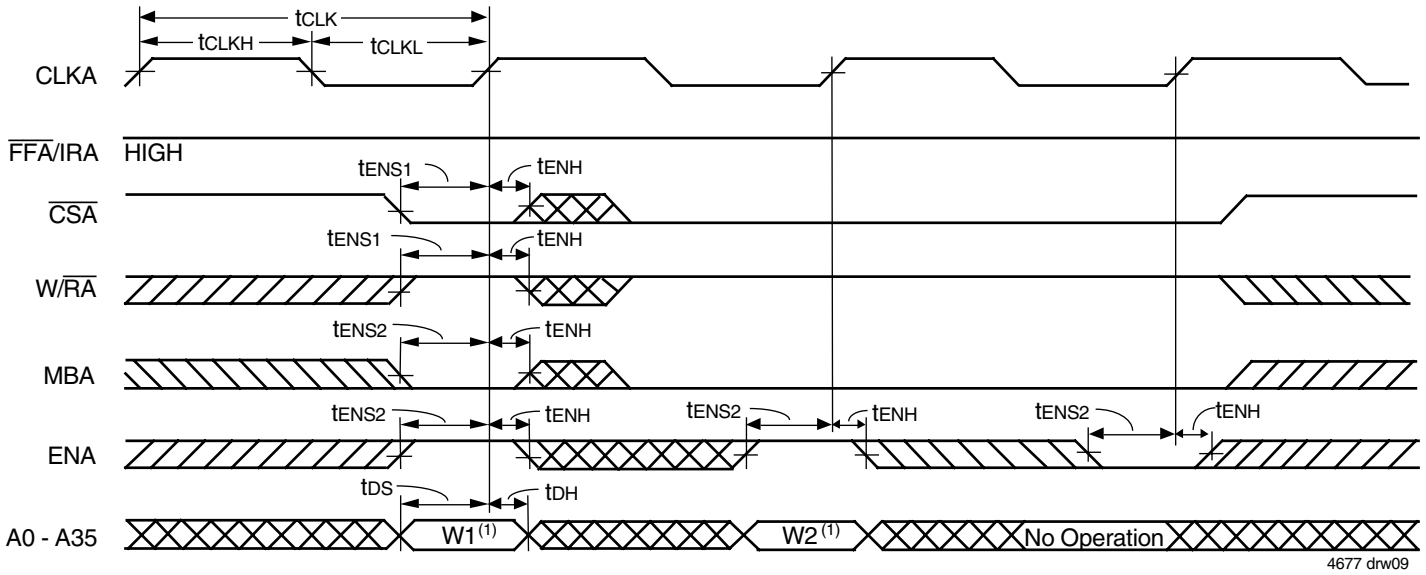
NOTES:
1. t_{SKEW1} is the minimum time between the rising CLKA edge and a rising CLKB edge for $\overline{FFB}$/IRB to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{SKEW1}, then $\overline{FFB}$/IRB may transition HIGH one CLKB cycle later than shown.
2. $\overline{CSA}$=LOW, W/$\overline{RA}$=HIGH,MBA=LOW. It is not necessary to program offset register on consecutive clock cycles.

Figure 5. Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes)



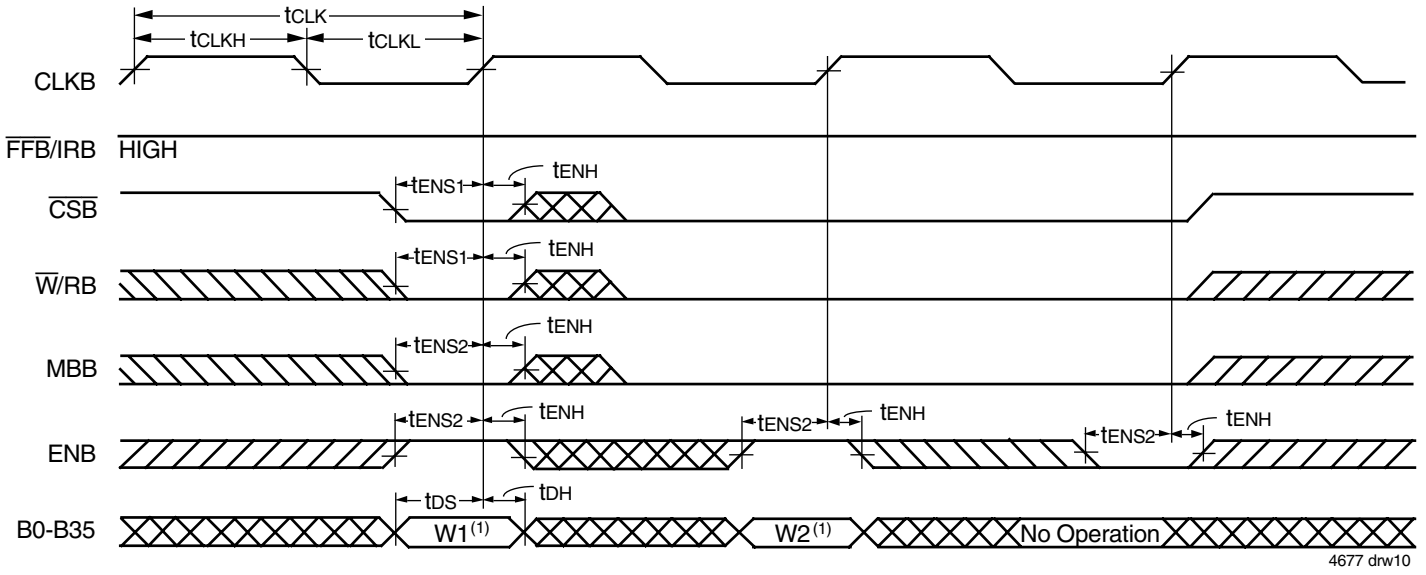
NOTES:
1. t_{SKEW1} is the minimum time between the rising CLKA edge and a rising CLKB edge for $\overline{FFB}$/IRB to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{SKEW1}, then $\overline{FFB}$/IRB may transition HIGH one CLKB cycle later than shown.
2. It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until $\overline{FFA}$/IRA and $\overline{FFB}$/IRB is set HIGH.
3. Programmable offsets are written serially to the SD input in the order $\overline{AFA}$ offset (Y1), $\overline{AEB}$ offset (X1), $\overline{AFB}$ offset (Y2), and $\overline{AEA}$ offset (X2).

Figure 6. Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values (IDT Standard and FWFT Modes)



NOTE:
1. Written to FIFO1.

Figure 7. Port A Write Cycle Timing for FIFO1 (IDT Standard and FWFT Modes)



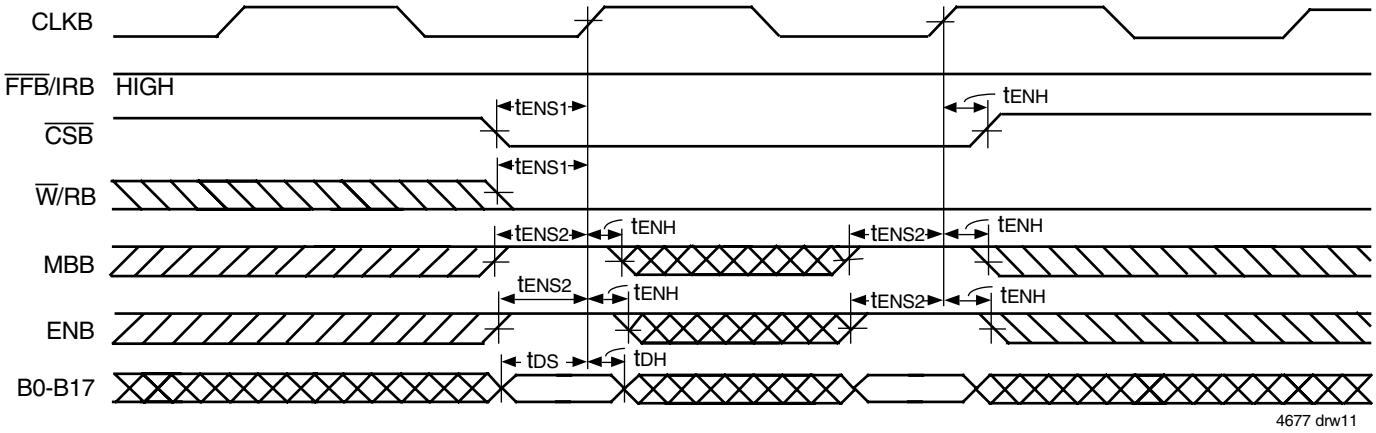
NOTE:
1. Written to FIFO2.

DATA SIZE TABLE FOR LONG-WORD WRITES TO FIFO2

SIZE MODE(1)			DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
BM	SIZE	BE	B35-B27	B26-B18	B17-B9	B8-B0	A35-A27	A26-A18	A17-A9	A8-A0
L	X	X	A	B	C	D	A	B	C	D

NOTE:
1. BE is selected at Master Reset: BM and SIZE must be static throughout device operation.

Figure 8. Port B Long-Word Write Cycle Timing for FIFO2 (IDT Standard and FWFT Modes)

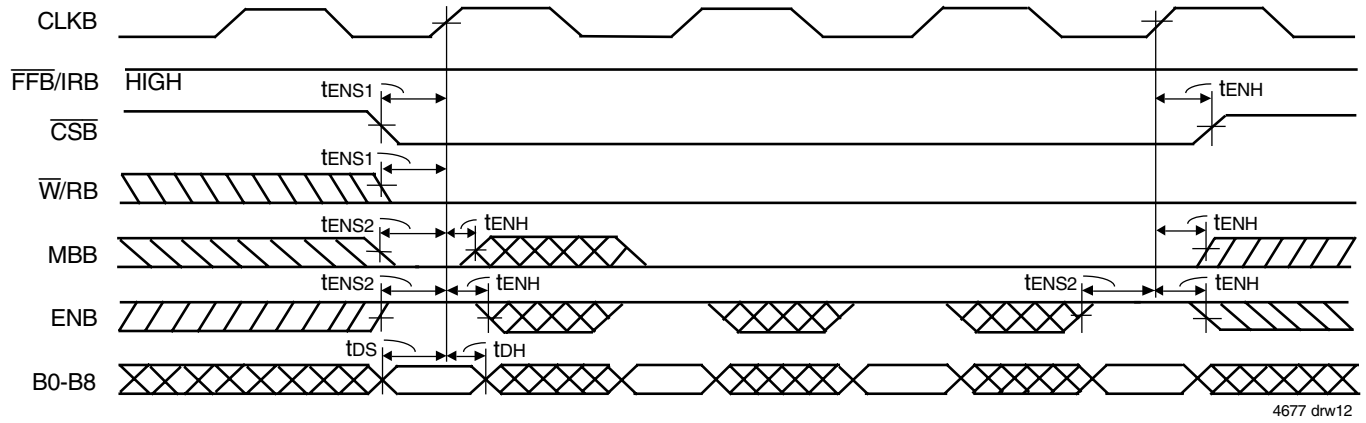


DATA SIZE TABLE FOR WORD WRITES TO FIFO2

SIZE MODE(1)			WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2			
BM	SIZE	BE		B17-B9	B8-B0	A35-A27	A26-A18	A17-A9	A8-A0
H	L	H	1	A	B	A	B	C	D
			2	C	D				
H	L	L	1	C	D	A	B	C	D
			2	A	B				

NOTE:
1. BE is selected at Master Reset; BM and SIZE must be static throughout device operation.

Figure 9. Port B Word Write Cycle Timing for FIFO2 (IDT Standard and FWFT Modes)

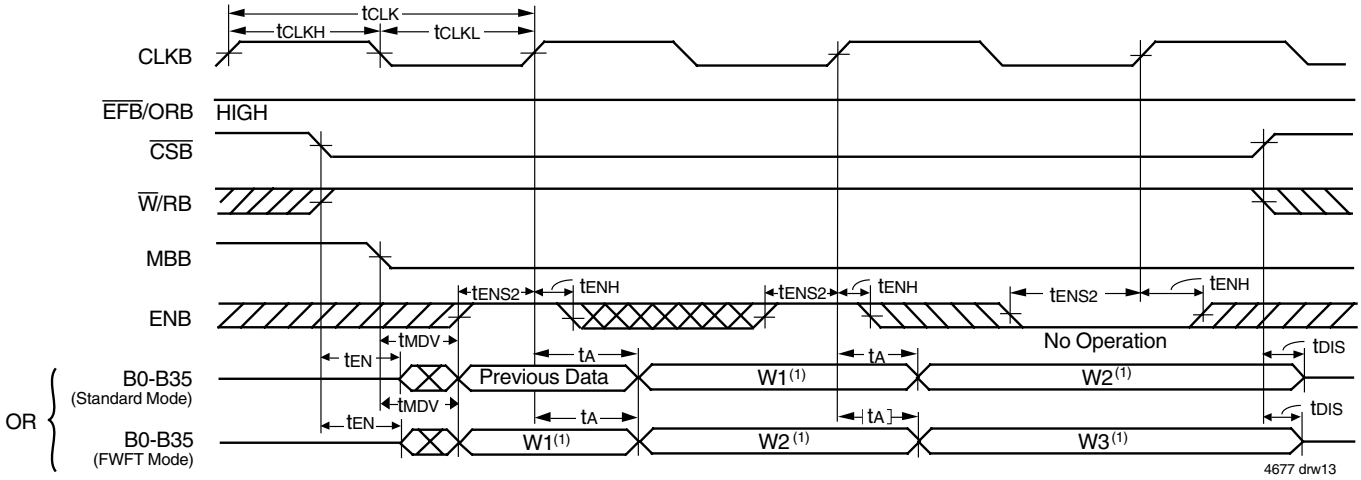


DATA SIZE TABLE FOR BYTE WRITES TO FIFO2

SIZE MODE(1)			WRITE NO.	DATA WRITTEN TO FIFO2	DATA READ FROM FIFO2			
BM	SIZE	BE		B8-B0	A35-A27	A26-A18	A17-A9	A8-A0
H	H	H	1	A	A	B	C	D
			2	B				
			3	C				
			4	D				
H	H	L	1	D	A	B	C	D
			2	C				
			3	B				
			4	A				

NOTE:
1. BE is selected at Master Reset; BM and SIZE must be static throughout device operation.

Figure 10. Port B Byte Write Cycle Timing for FIFO2 (IDT Standard and FWFT Modes)



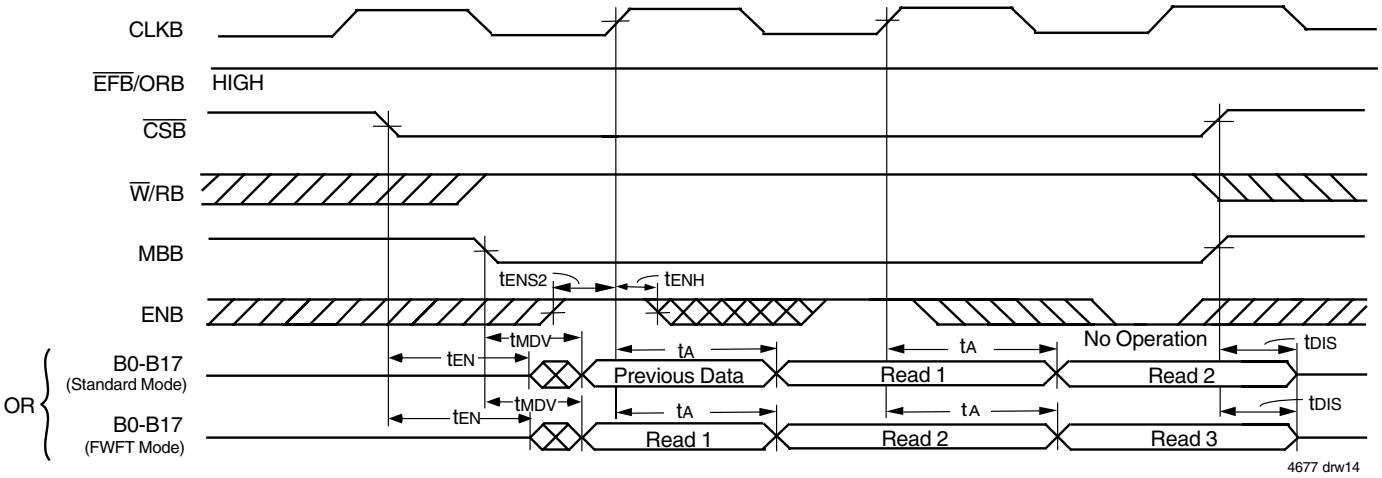
NOTE:
1. Read From FIFO1.

DATA SIZE TABLE FOR FIFO LONG-WORD READS FROM FIFO1

SIZE MODE(1)			DATA WRITTEN TO FIFO1				DATA READ FROM FIFO1			
BM	SIZE	BE	A35-A27	A26-A18	A17-A9	A8-A0	B35-B27	B26-B18	B17-B9	B8-B0
L	X	X	A	B	C	D	A	B	C	D

NOTE:
1. BE is selected at Master Reset; BM and SIZE must be static throughout device operation .

Figure 11. Port B Long-Word Read Cycle Timing for FIFO1 (IDT Standard and FWFT Modes)



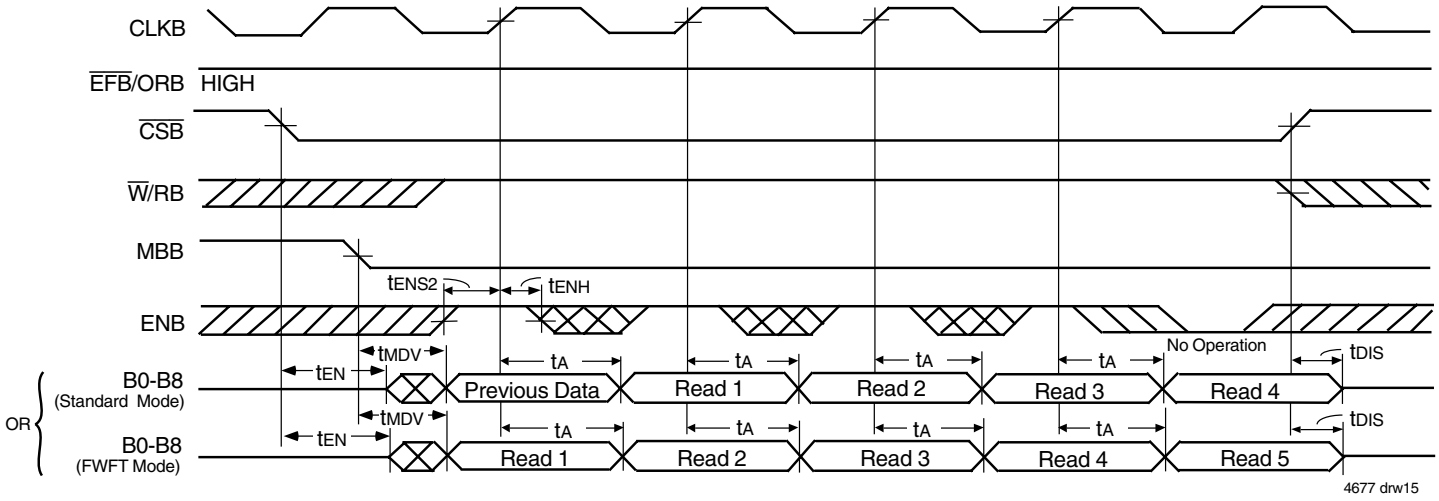
NOTE:
1. Unused word B18-B35 are indeterminate for word-size reads.

DATA SIZE TABLE FOR WORD READS FROM FIFO1

SIZE MODE(1)			DATA WRITTEN TO FIFO1				READ NO.	DATA READ FROM FIFO1	
BM	SIZE	BE	A35-A27	A26-A18	A17-A9	A8-A0		B17-B9	B8-B0
H	L	H	A	B	C	D	1	A	B
							2	C	D
H	L	L	A	B	C	D	1	C	D
							2	A	B

NOTE:
1. BE is selected at Master Reset; BM and SIZE must be static throughout device operation .

Figure 12. Port-B Word Read Cycle Timing for FIFO1 (IDT Standard and FWFT Modes)



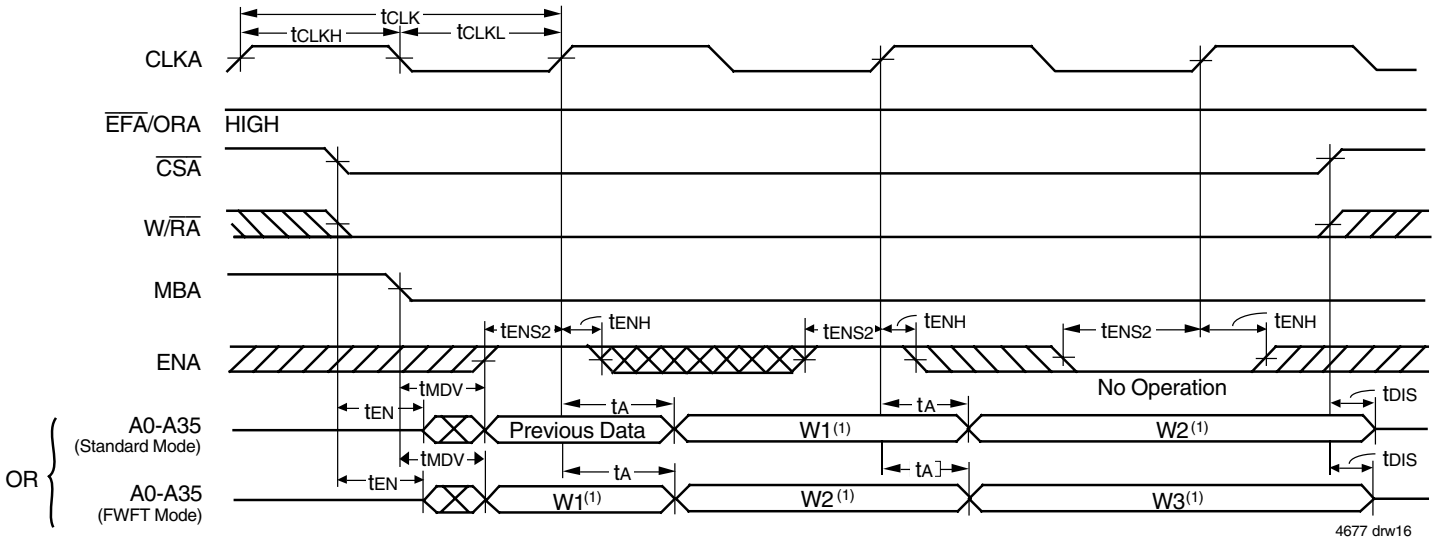
NOTE:
1. Unused bytes B9-B17, B18-B26, and B27-B35 are indeterminate for byte-size reads.

DATA SIZE TABLE FOR BYTE READS FROM FIFO1

SIZE MODE(1)			DATA WRITTEN TO FIFO1				READ NO.	DATA READ FROM FIFO1
BM	SIZE	BE	A35-A27	A26-A18	A17-A9	A8-A0		B8-B0
H	H	H	A	B	C	D	1 2 3 4	A B C D
H	H	L	A	B	C	D	1 2 3 4	D C B A

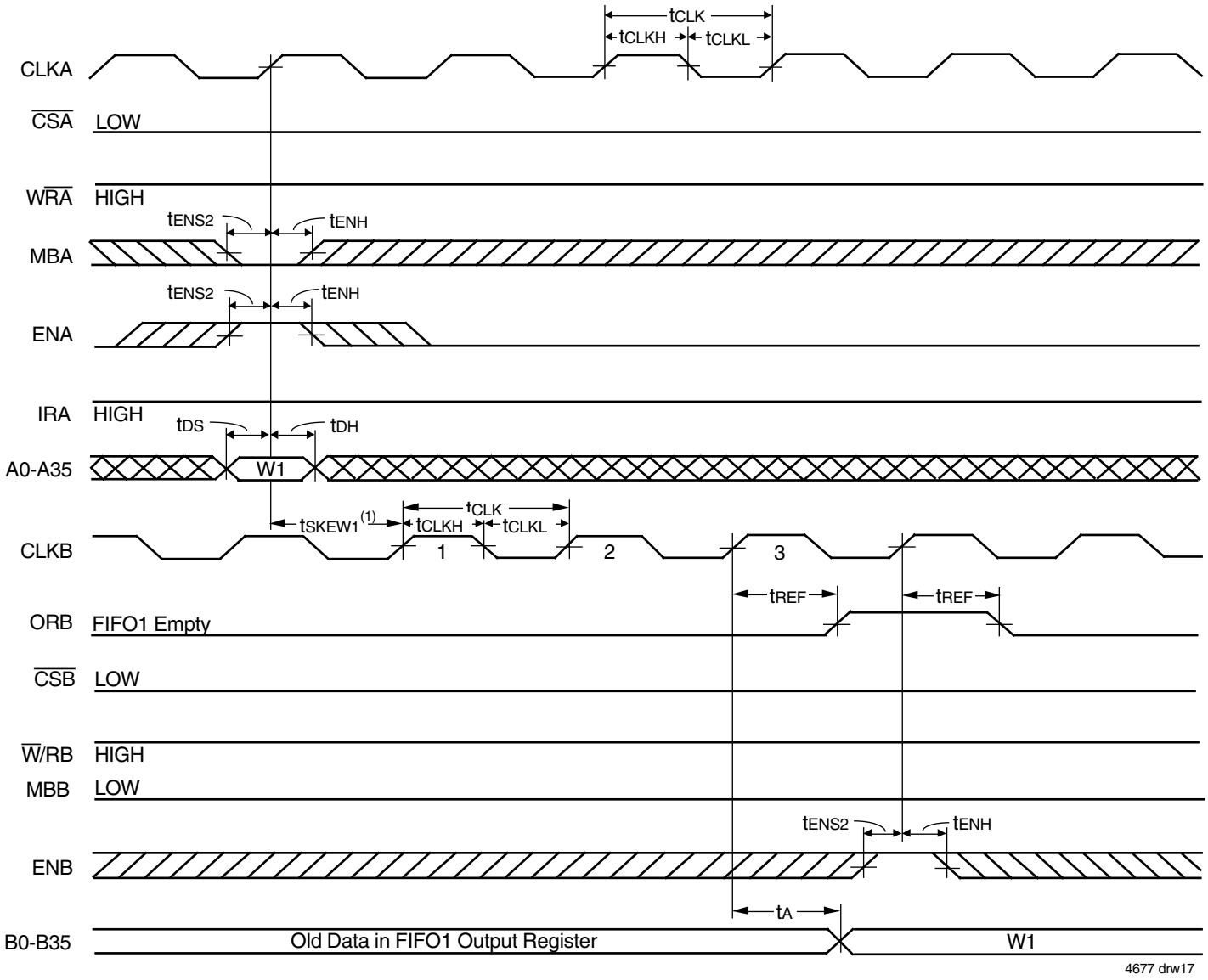
NOTE:
1. BE is selected at Master Reset; BM and SIZE must be static throughout device operation.

Figure 13. Port-B Byte Read Cycle Timing for FIFO1 (IDT Standard and FWFT Modes)



NOTE:
1. Read From FIFO2.

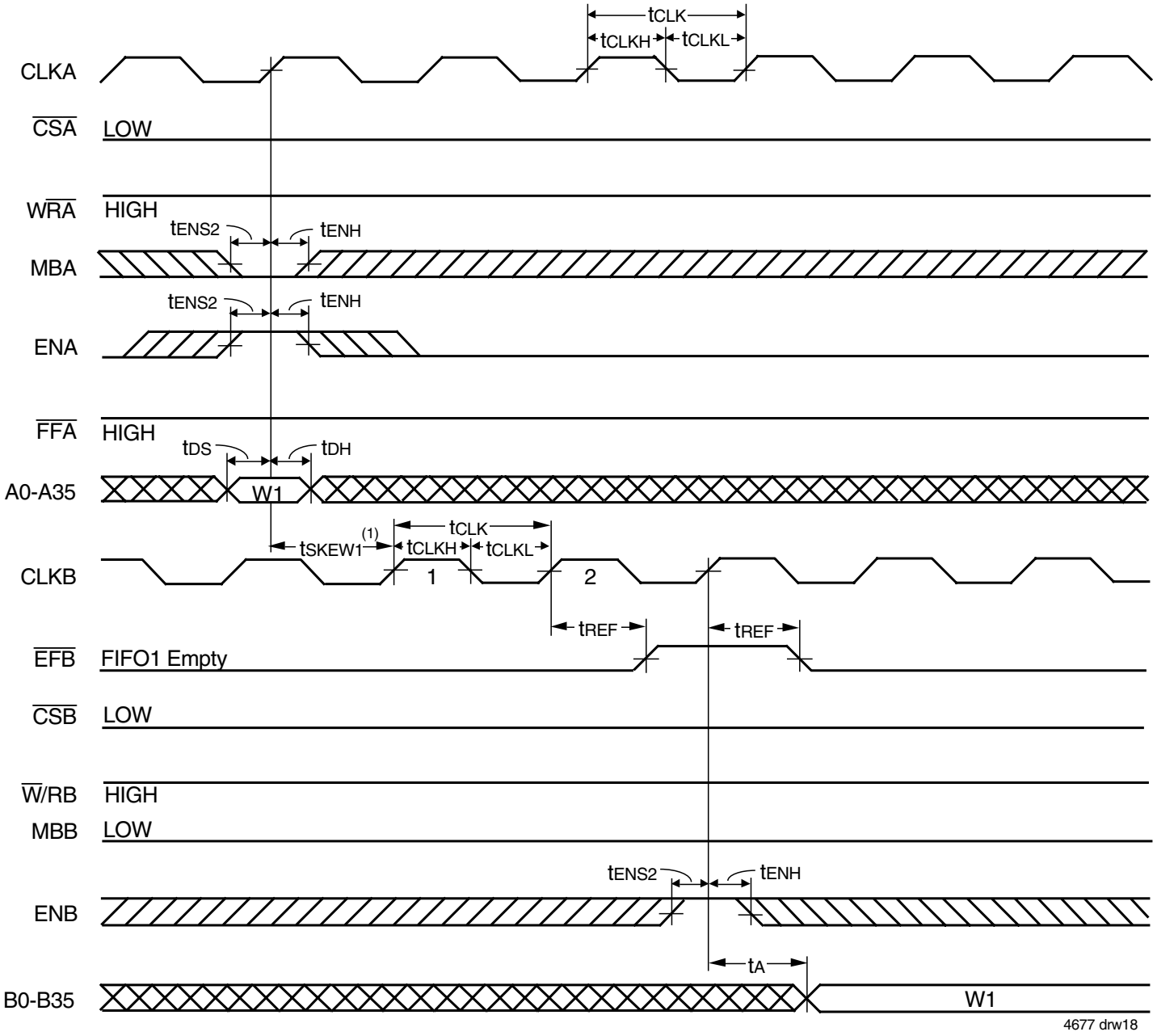
Figure 14. Port-A Read Cycle Timing for FIFO2 (IDT Standard and FWFT Modes)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition HIGH and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of ORB HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.
2. If Port B size is word or byte, ORB is set LOW by the last word or byte read from FIFO1, respectively.

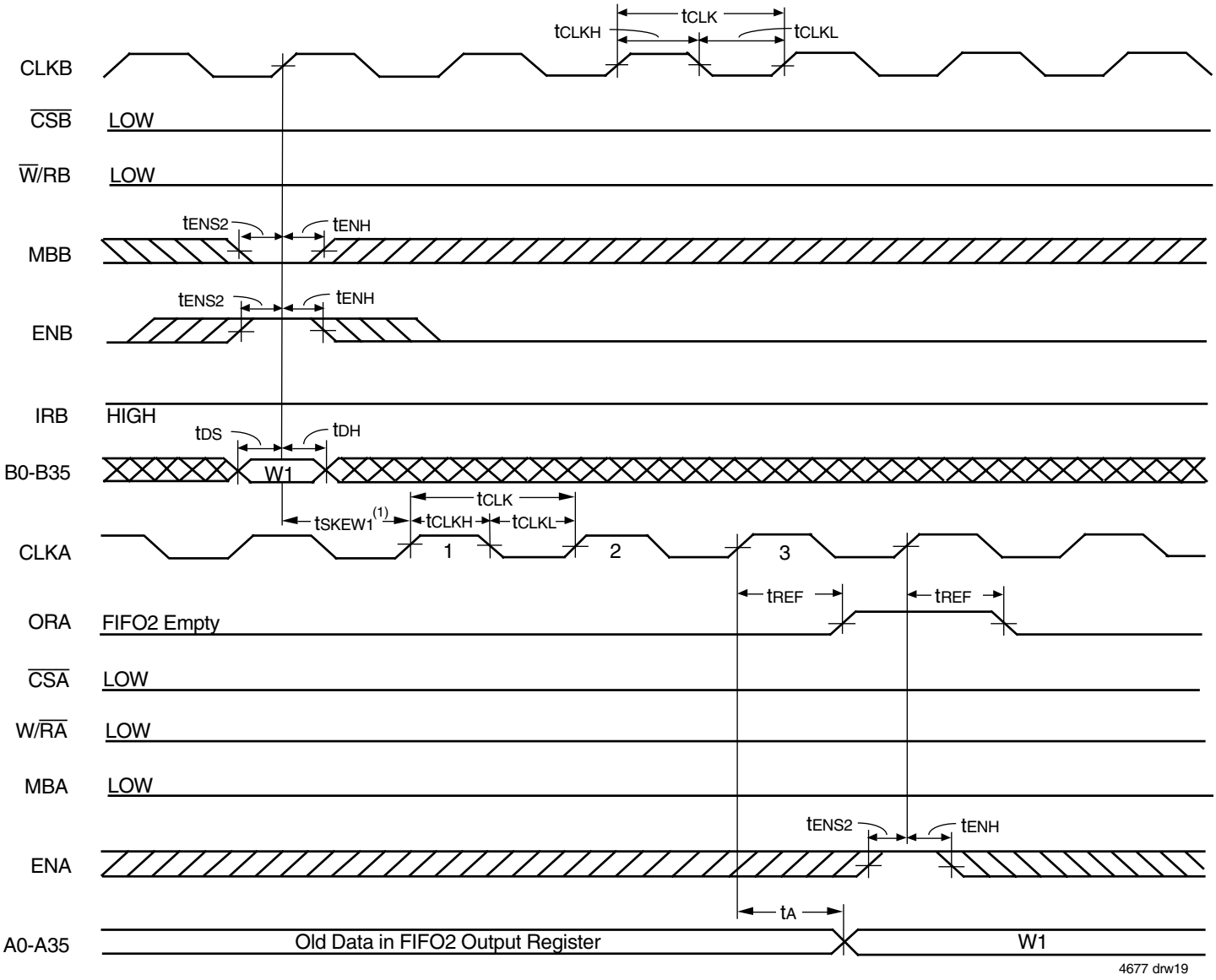
Figure 15. ORB Flag Timing and First Data Word Fall Through when FIFO1 is Empty (FWFT Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EFB}$ HIGH may occur one CLKB cycle later than shown.
2. If Port B size is word or byte, $\overline{EFB}$ is set LOW by the last word or byte read from FIFO1, respectively.

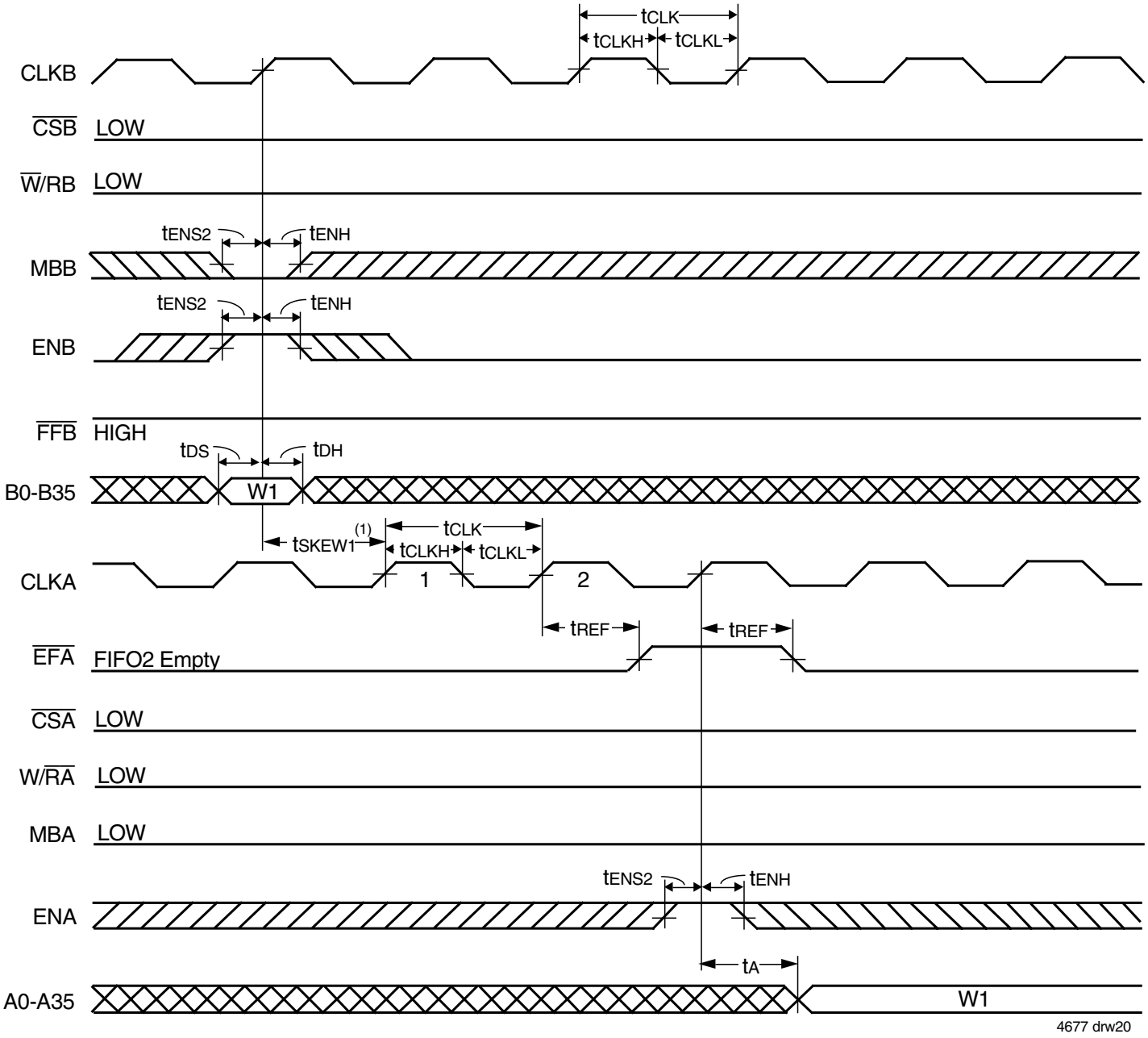
Figure 16. $\overline{EFB}$ Flag Timing and First Data Read Fall Through when FIFO1 is Empty (IDT Standard Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition HIGH and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the CLKB edge and the rising CLKA edge is less than t_{SKEW1}, then the transition of ORA HIGH and load of the first word to the output register may occur one CLKA cycle later than shown.
2. If Port B size is word or byte, t_{SKEW1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.

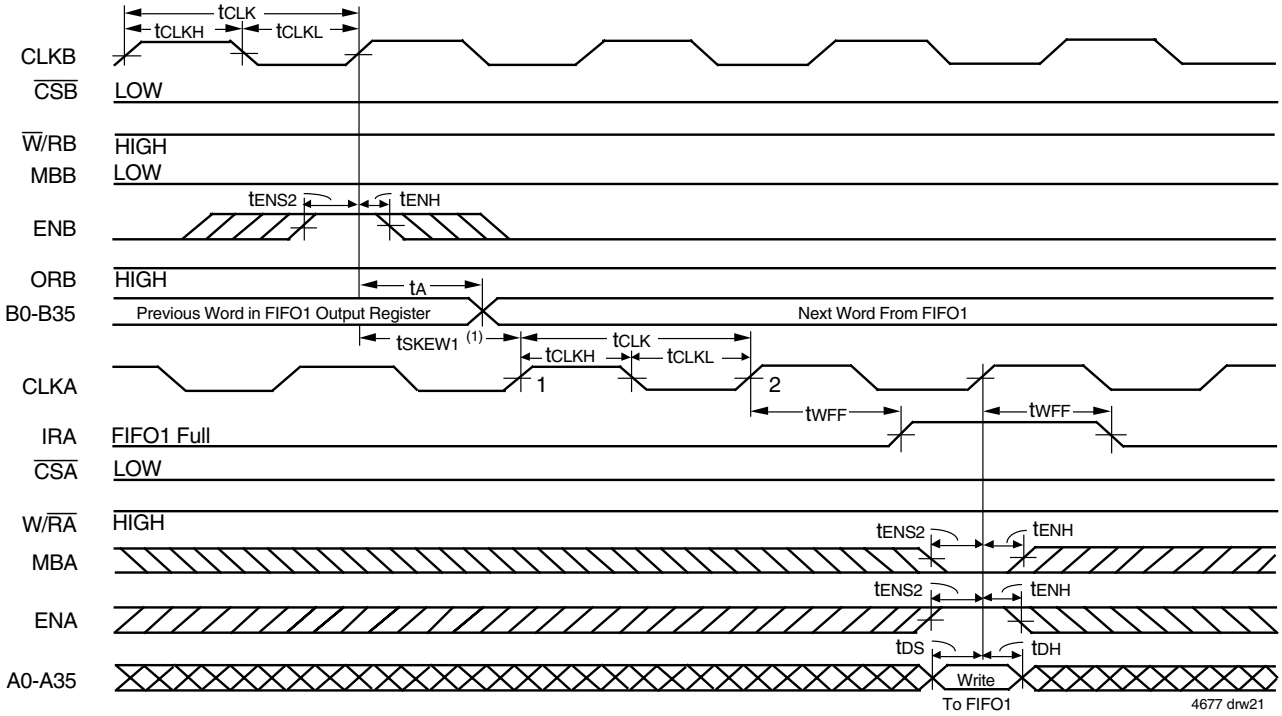
Figure 17. ORA Flag Timing and First Data Word Fall through when FIFO2 is Empty (FWFT Mode)



NOTES:

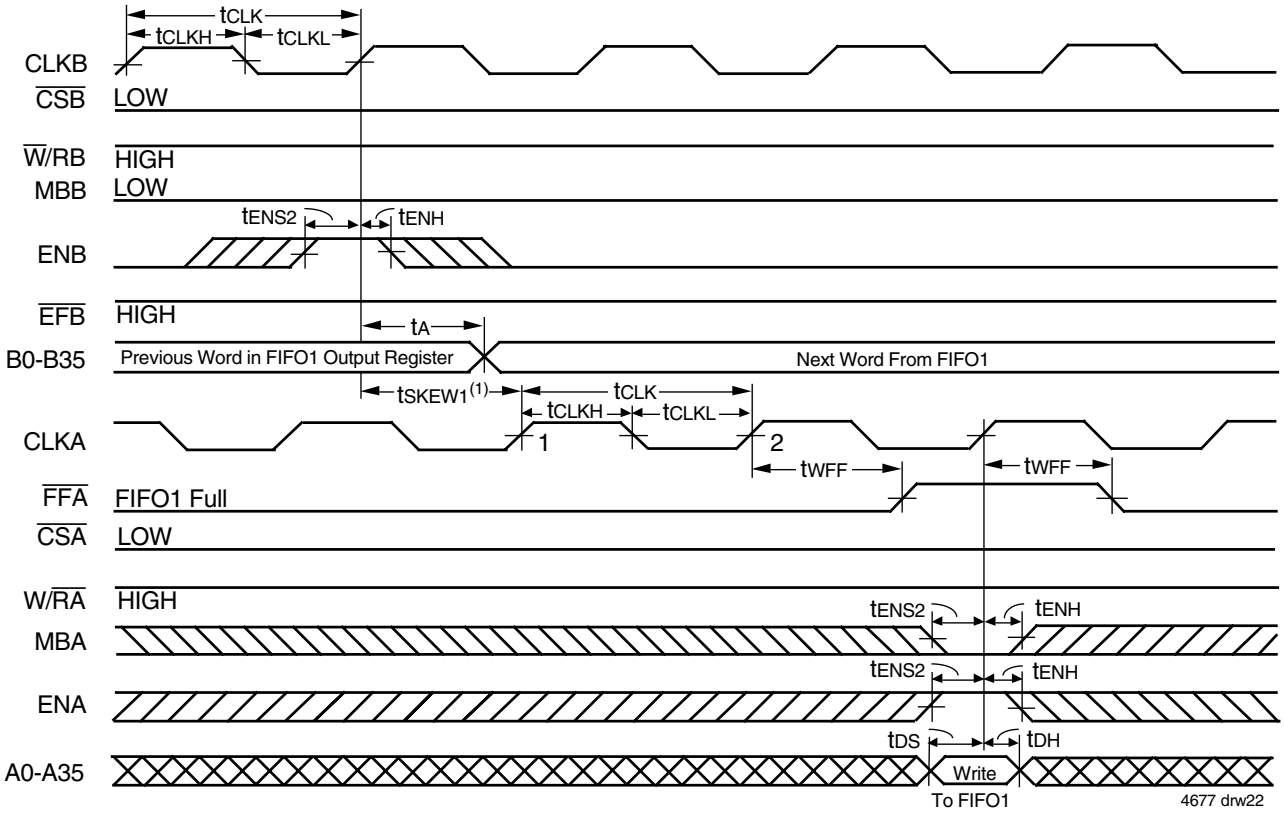
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{EFA}$ HIGH may occur one CLKA cycle later than shown.
2. If Port B size is word or byte, t_{SKEW1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.

Figure 18. $\overline{EFA}$ Flag Timing and First Data Read when FIFO2 is Empty (IDT Standard Mode)



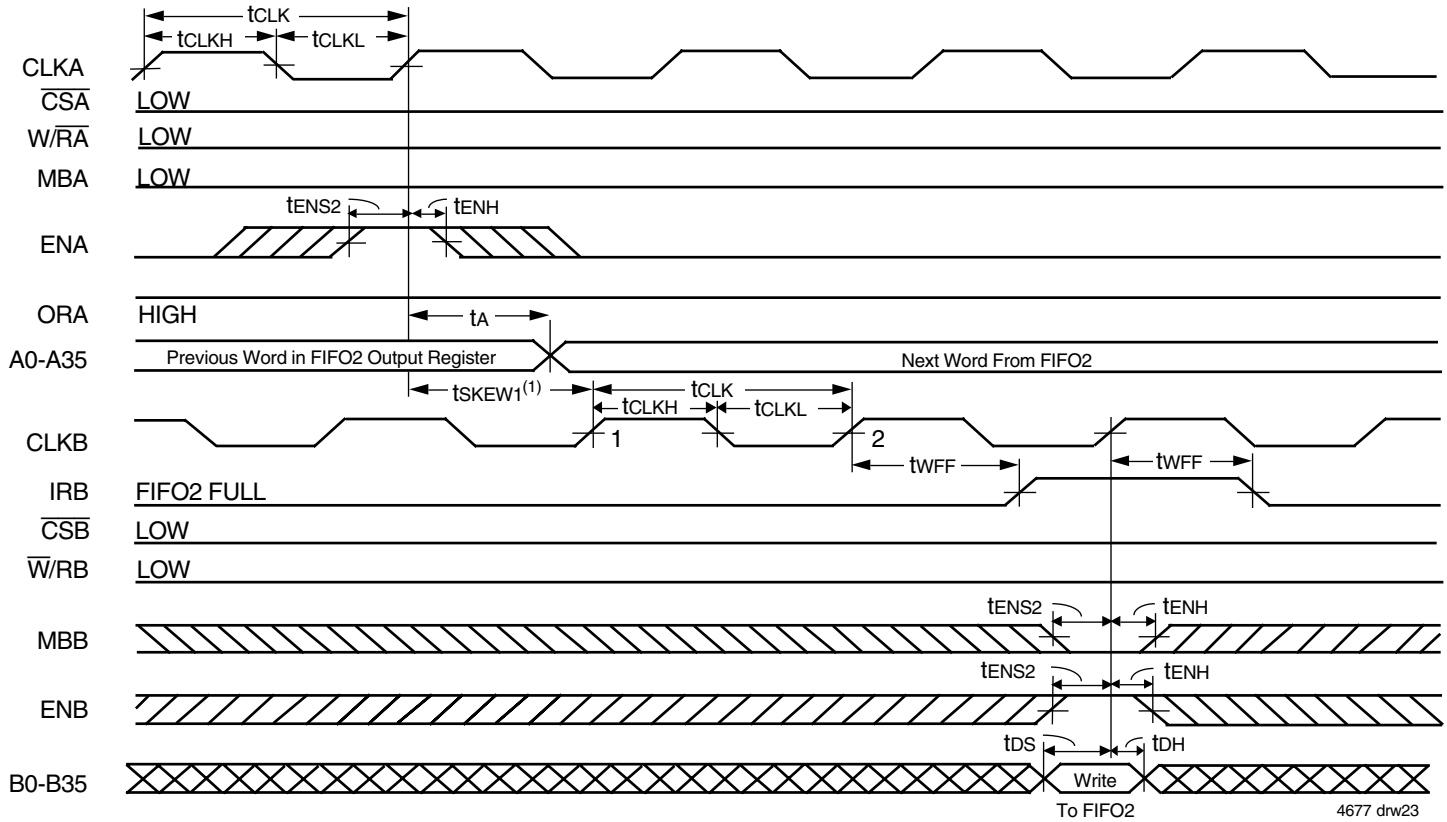
NOTES:
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then IRA may transition HIGH one CLKA cycle later than shown.
2. If Port B size is word or byte, t_{SKEW1} is referenced to the rising CLKB edge that reads the last word or byte write of the long word, respectively.

Figure 19. IRA Flag Timing and First Available Write when FIFO1 is Full (FWFT Mode)



NOTES:
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then $\overline{FFA}$ may transition HIGH one CLKA cycle later than shown.
2. If Port B size is word or byte, t_{SKEW1} is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.

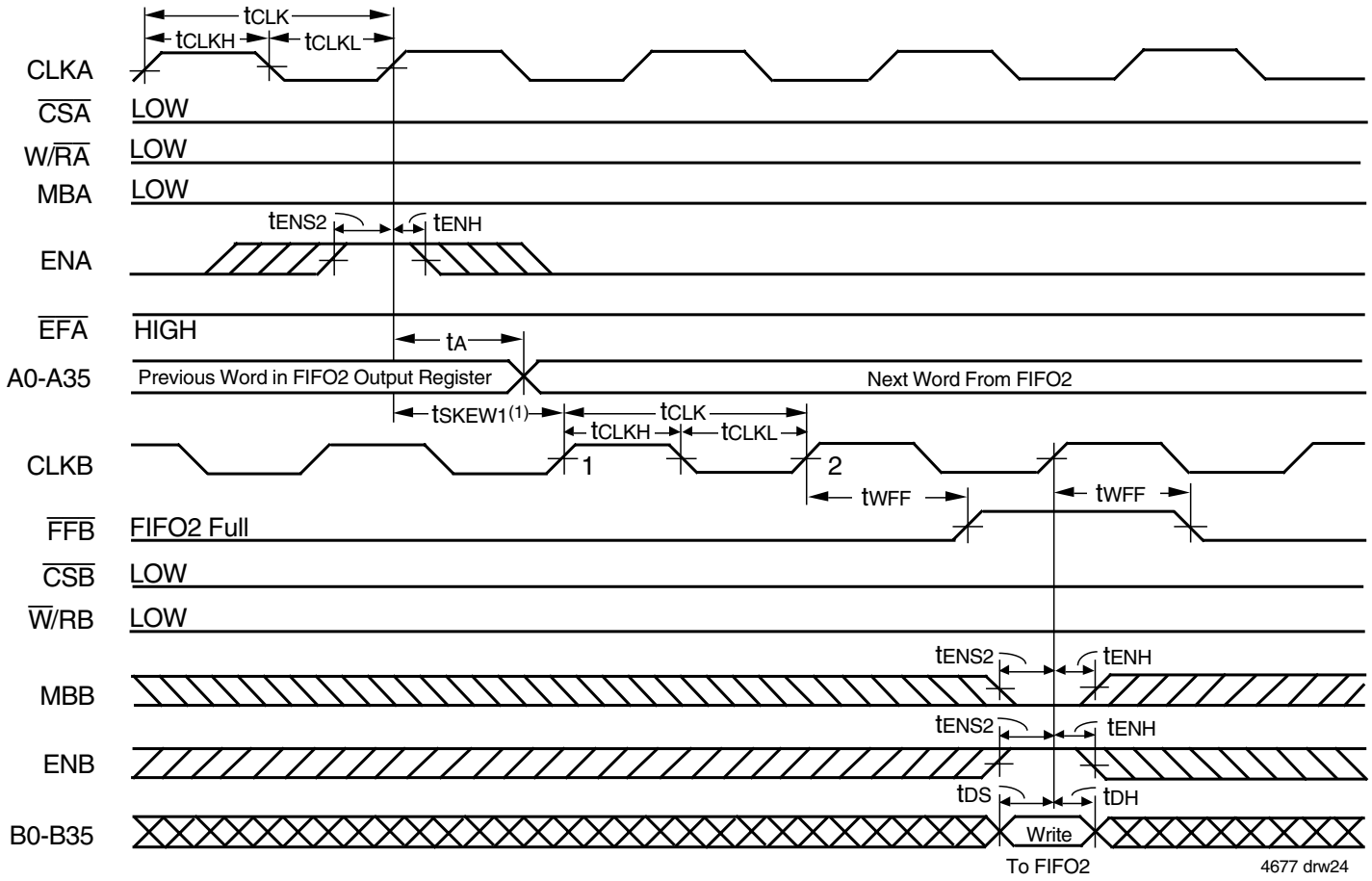
Figure 20. $\overline{FFA}$ Flag Timing and First Available Write when FIFO1 is Full (IDT Standard Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then IRB may transition HIGH one CLKB cycle later than shown.
2. If Port B size is word or byte, IRB is set LOW by the last word or byte write of the long word, respectively.

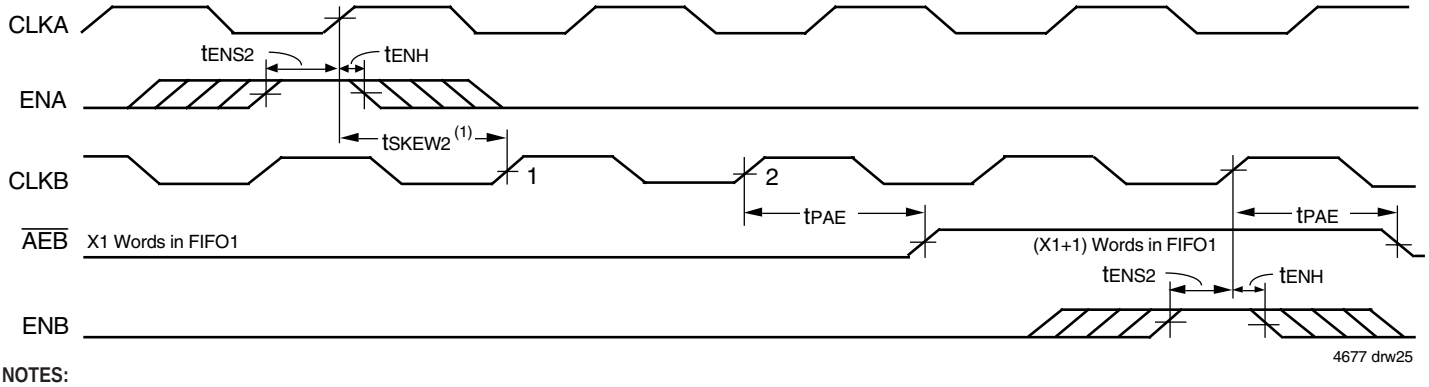
Figure 21. IRB Flag Timing and First Available Write when FIFO2 is Full (FWFT Mode)



NOTES:

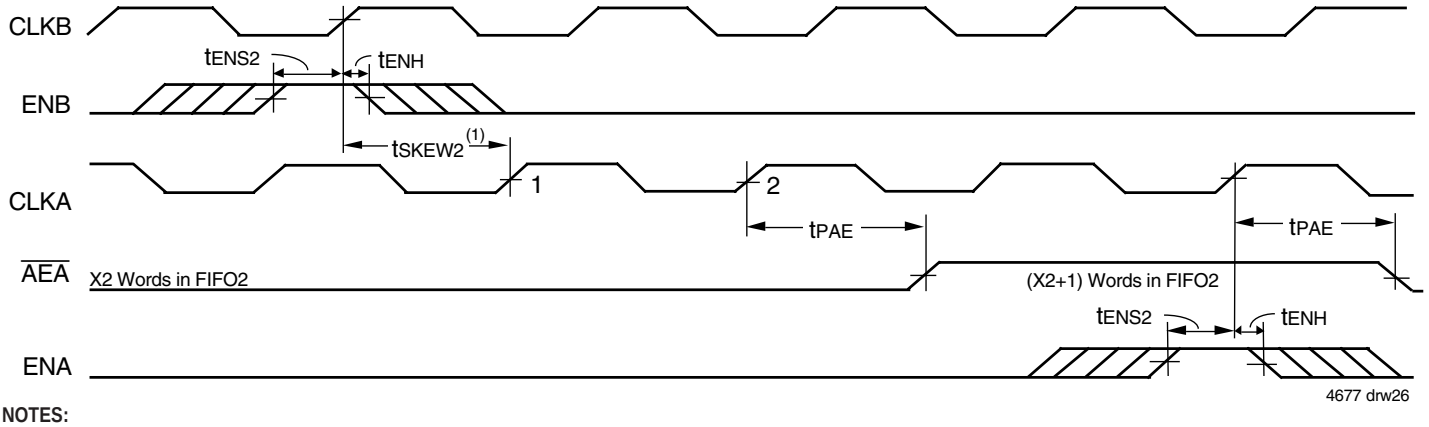
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then $\overline{FFB}$ may transition HIGH one CLKB cycle later than shown.
2. If Port B size is word or byte, $\overline{FFB}$ is set LOW by the last word or byte write of the long word, respectively.

Figure 22. $\overline{FFB}$ Flag Timing and First Available Write when FIFO2 is Full (IDT Standard Mode)



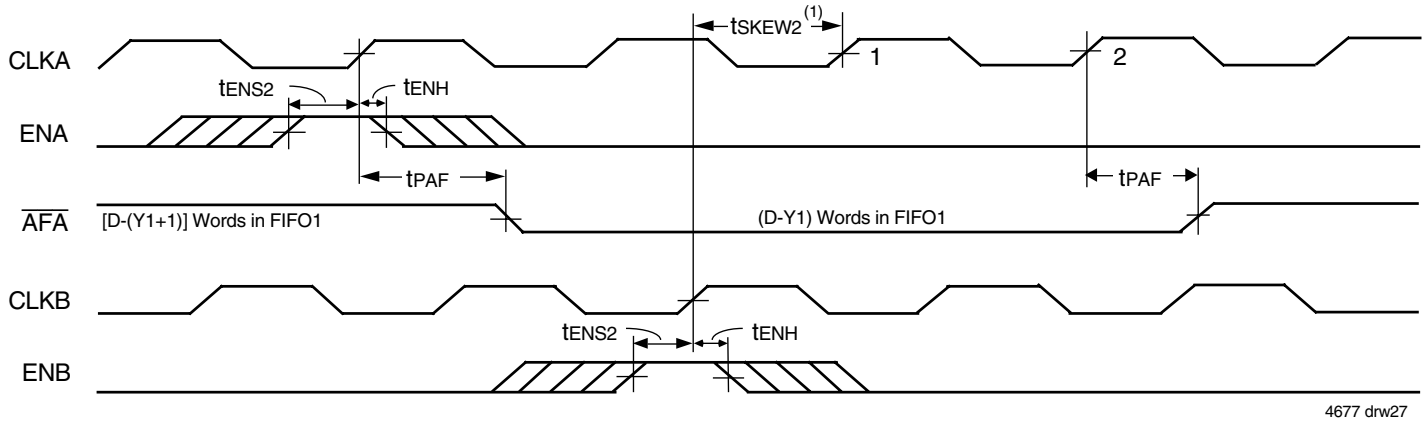
NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AEB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.
3. If Port B size is word or byte, $\overline{AEB}$ is set LOW by the last word or byte read from FIFO1, respectively.

Figure 23. Timing for $\overline{AEB}$ when FIFO1 is Almost-Empty (IDT Standard and FWFT Modes)



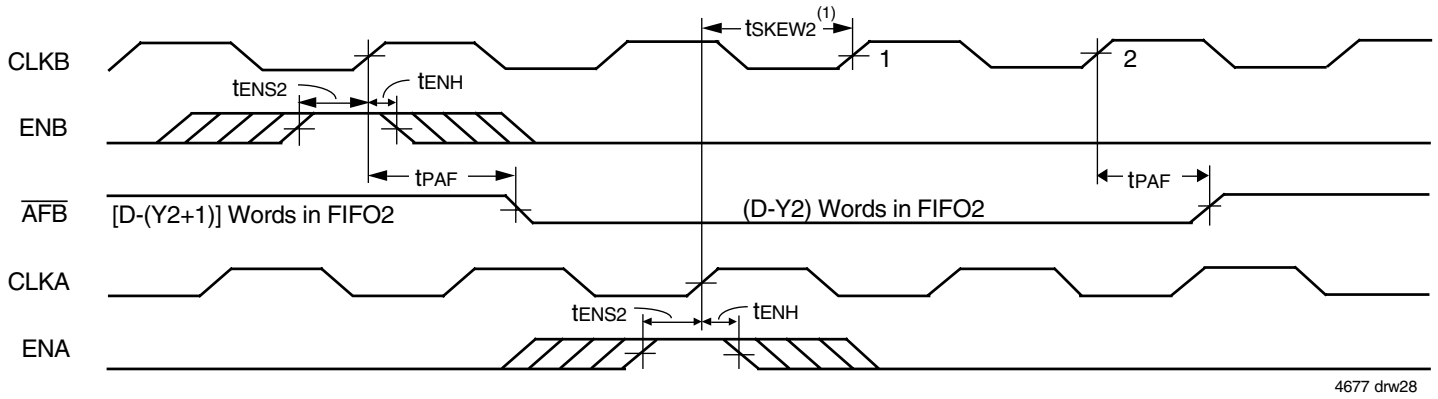
NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, $\overline{W}$/RB = LOW, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.
3. If Port B size is word or byte, tSKEW2 is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.

Figure 24. Timing for $\overline{AEA}$ when FIFO2 is Almost-Empty (IDT Standard and FWFT Modes)



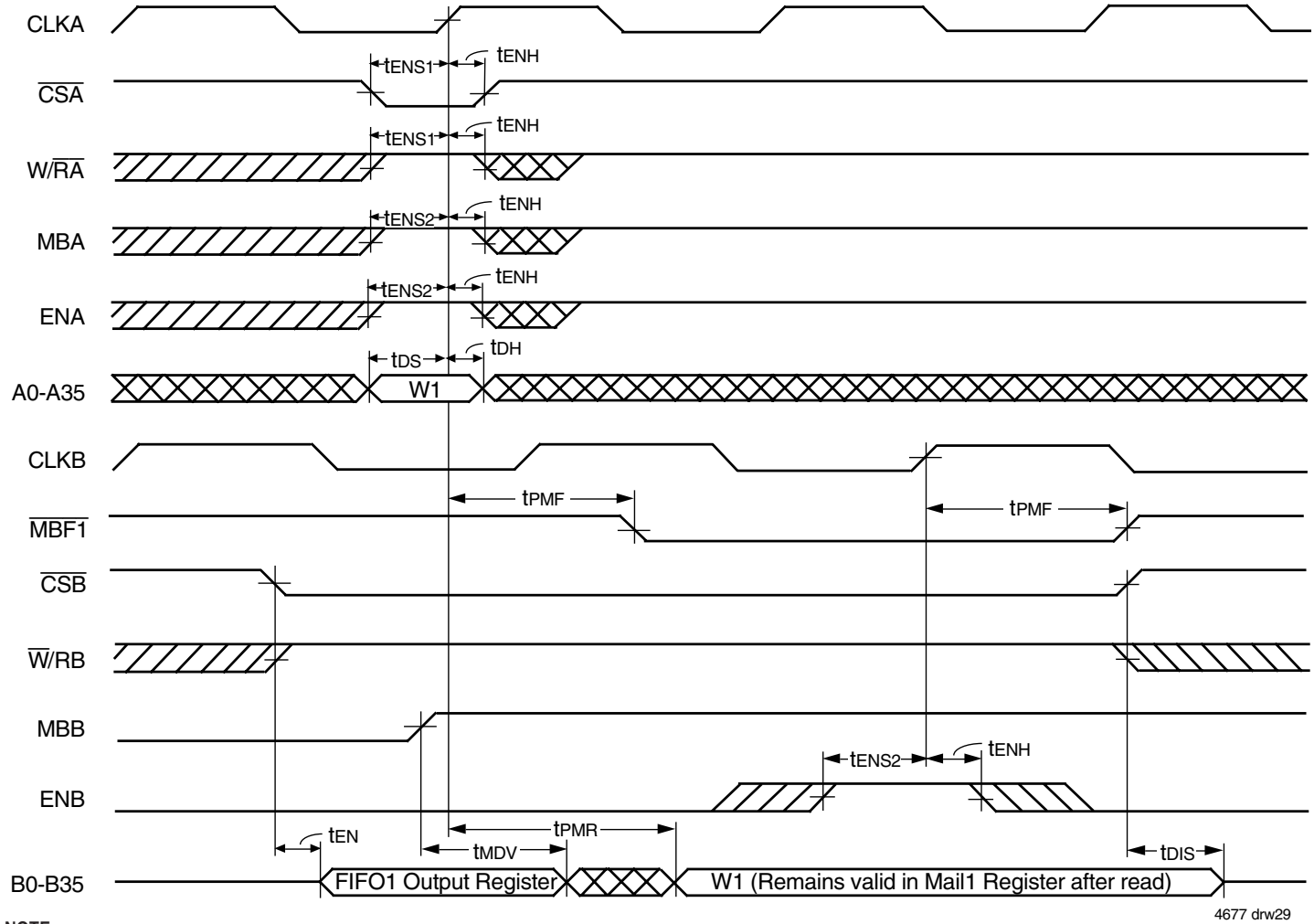
NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AFA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 16,384 for the IDT72V3684, 32,768 for the IDT72V3694, 65,536 for the IDT72V36104.
4. If Port B size is word or byte, tSKEW2 is referenced to the rising CLKB edge that reads the last word or byte of the long word, respectively.

Figure 25. Timing for $\overline{AFA}$ when FIFO1 is Almost-Full (IDT Standard and FWFT Modes)



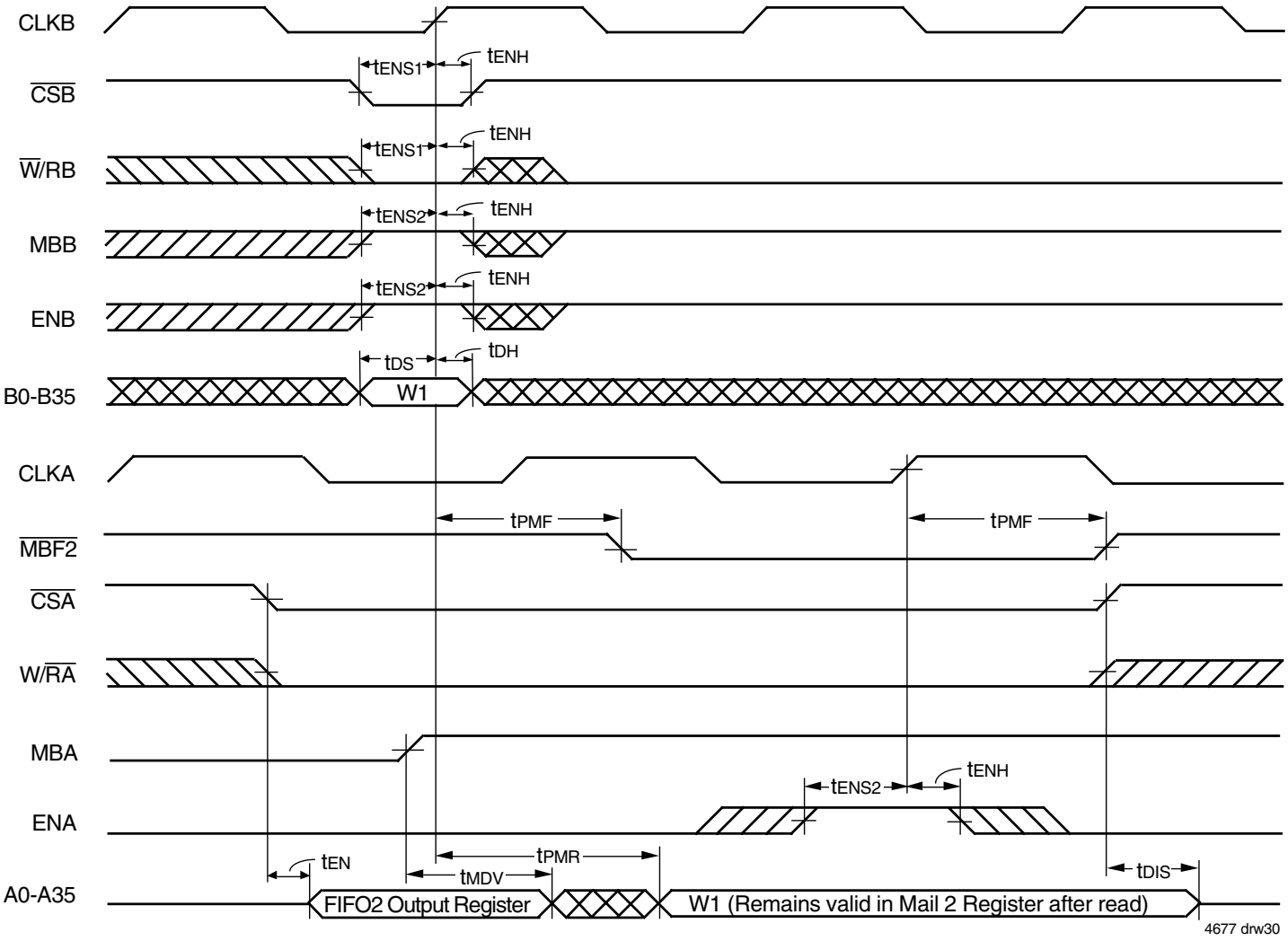
NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AFB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO2 write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 16,384 for the IDT72V3684, 32,768 for the IDT72V3694, 65,536 for the IDT72V36104.
4. If Port B size is word or byte, $\overline{AFB}$ is set LOW by the last word or byte write of the long word, respectively.

Figure 26. Timing for $\overline{AFB}$ when FIFO2 is Almost-Full (IDT Standard and FWFT Modes)



NOTE:
1. If Port B is configured for word size, data can be written to the Mail1 register using A0-A17 (A18-A35 are don't care inputs). In this first case B0-B17 will have valid data (B18-B35 will be indeterminate). If Port B is configured for byte size, data can be written to the Mail1 Register using A0-A8 (A9-A35 are don't care inputs). In this second case, B0-B8 will have valid data (B9-B35 will be indeterminate).

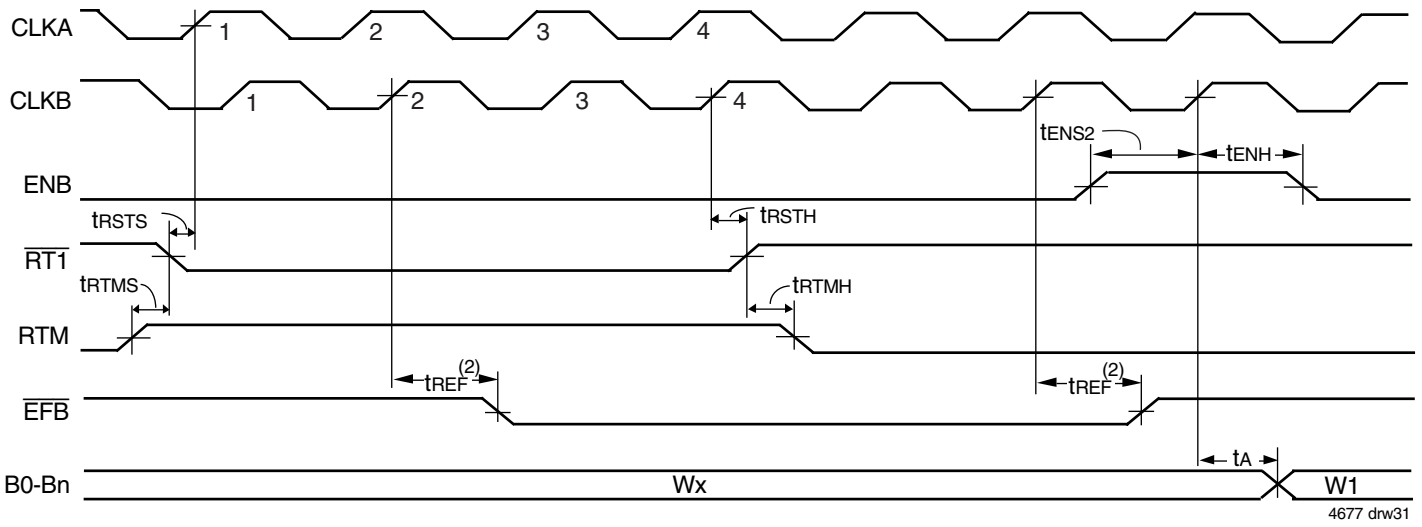
Figure 27. Timing for Mail1 Register and $\overline{MBF1}$ Flag (IDT Standard and FWFT Modes)



NOTE:

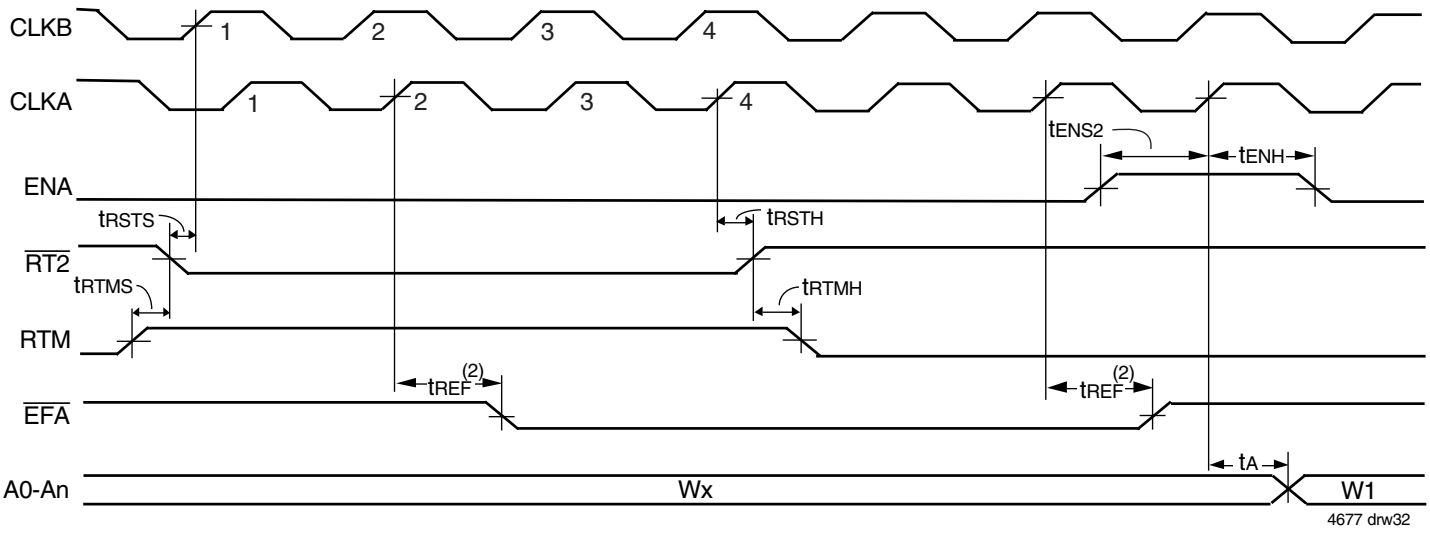
1. If Port B is configured for word size, data can be written to the Mail2 Register using B0-B17 (B18-B35 are don't care inputs). In this first case A0-A17 will have valid data (A18-A35 will be indeterminate). If Port B is configured for byte size, data can be written to the Mail2 Register using B0-B8 (B9-B35 are don't care inputs). In this second case, A0-A8 will have valid data (A9-A35 will be indeterminate).

Figure 28. Timing for Mail2 Register and $\overline{MBF2}$ Flag (IDT Standard and FWFT Modes)



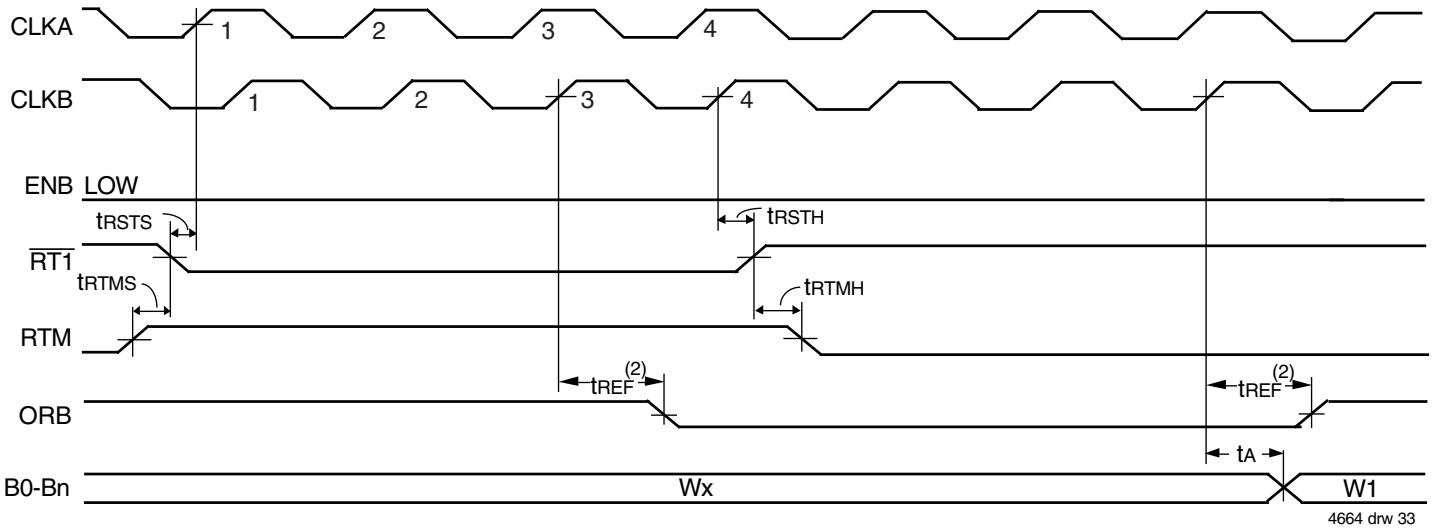
NOTES:
1. $\overline{CSB}$ = LOW
2. Retransmit setup is complete after $\overline{EFB}$ returns HIGH, only then can a read operation begin.
3. W1 = first word written to the FIFO1 after Master Reset on FIFO1.
4. No more than D-2 may be written to the FIFO1 between Reset of FIFO1 (Master or Partial) and Retransmit setup. Therefore, $\overline{FFA}$ will be LOW throughout the Retransmit setup procedure. D = 16,384, 32,768 and 65,536 for the IDT72V3684, IDT72V3694 and IDT72V36104 respectively.

Figure 29. Retransmit Timing for FIFO1 (IDT Standard Mode)



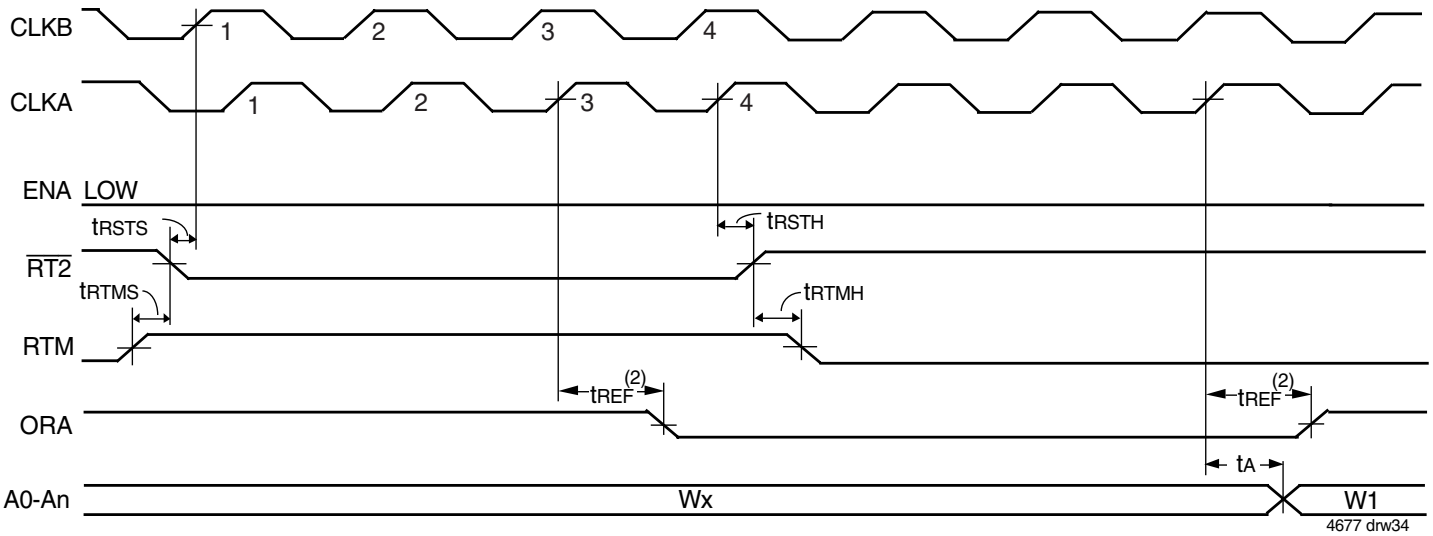
NOTES:
1. $\overline{CSA}$ = LOW
2. Retransmit setup is complete after $\overline{EFA}$ returns HIGH, only then can a read operation begin.
3. W1 = first word written to the FIFO1 after Master Reset on FIFO2.
4. No more than D-2 may be written to the FIFO1 between Reset of FIFO2 (Master or Partial) and Retransmit setup. Therefore, $\overline{FFB}$ will be LOW throughout the Retransmit setup procedure. D = 16,384, 32,768 and 65,536 for the IDT72V3684. IDT72V3694 and IDT72V36104 respectively.

Figure 30. Retransmit Timing for FIFO2 (IDT Standard Mode)



NOTES:
1. $\overline{CSB}$ = LOW
2. Retransmit setup is complete after $\overline{ORB}$ returns HIGH, only then can a read operation begin.
3. W1 = first word written to the FIFO1 after Master Reset on FIFO1.
4. No more than D-2 may be written to the FIFO1 between Reset of FIFO1 (Master or Partial) and Retransmit setup. Therefore, IRA will be LOW throughout the Retransmit setup procedure. D = 16,385, 32,769 and 65,537 for the IDT72V3684, IDT72V3694 and IDT72V36104 respectively.

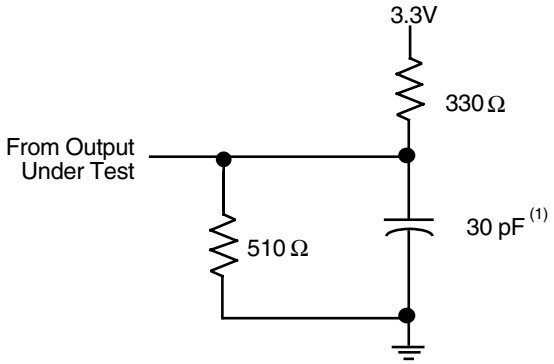
Figure 31. Retransmit Timing for FIFO1 (FWFT Mode)



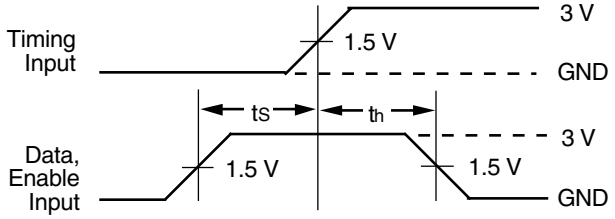
NOTES:
1. $\overline{CSA}$ = LOW
2. Retransmit setup is complete after $\overline{ORA}$ returns HIGH, only then can a read operation begin.
3. W1 = first word written to the FIFO2 after Master Reset on FIFO2.
4. No more than D-2 may be written to the FIFO2 between Reset of FIFO2 (Master or Partial) and Retransmit setup. Therefore, IRB will be LOW throughout the Retransmit setup procedure. D = 16,385, 32,769 and 65,537 for the IDT72V3684, IDT72V3694 and IDT72V36104 respectively.

Figure 32. Retransmit Timing for FIFO2 (FWFT Mode)

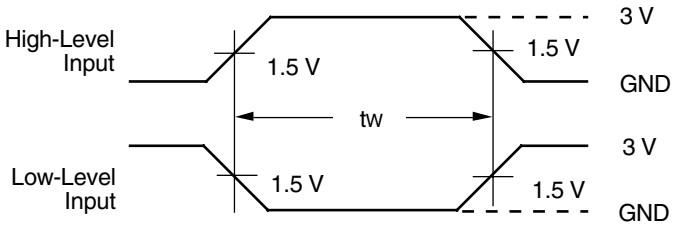
PARAMETER MEASUREMENT INFORMATION



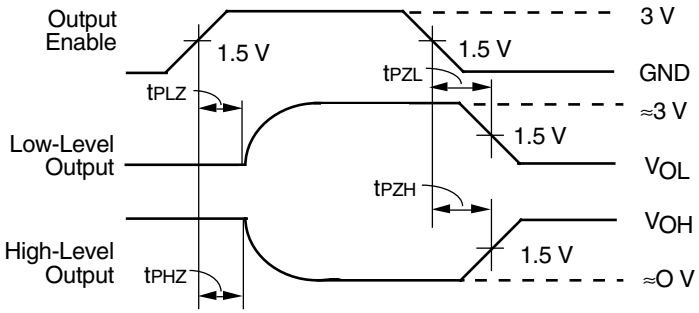
PROPAGATION DELAY LOAD CIRCUIT



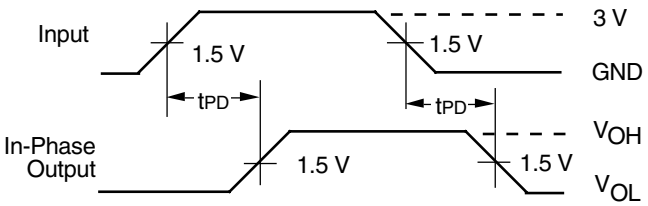
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



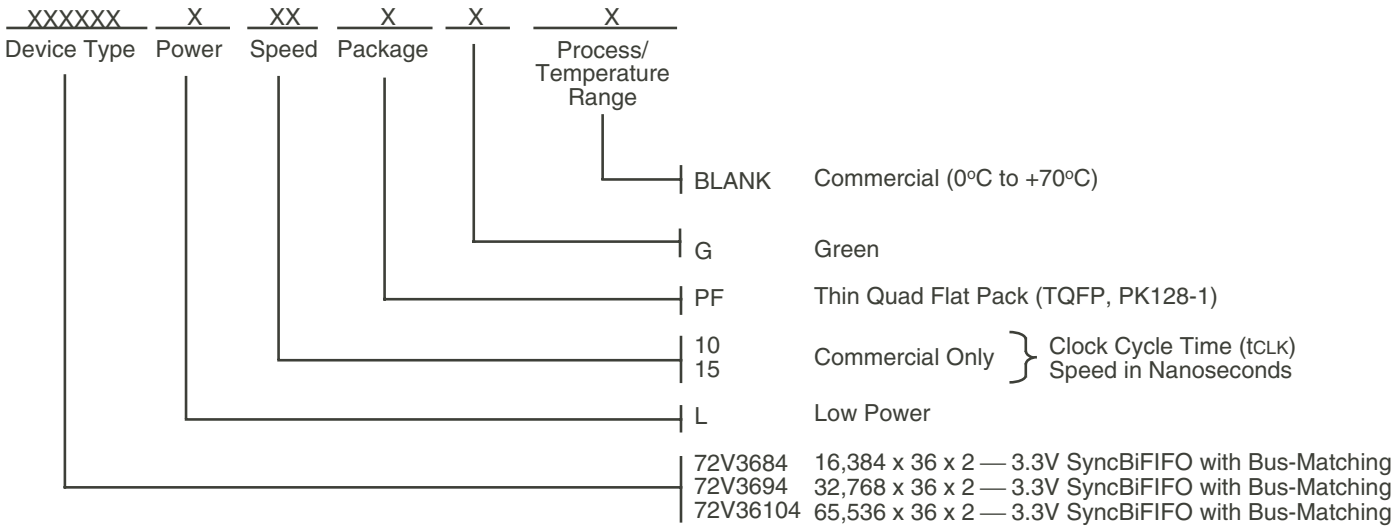
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

4677 drw35

NOTE:
1. Includes probe and jig capacitance.

Figure 33. Output Load and AC Test Conditions

ORDERING INFORMATION



4677 drw36

NOTES:
1. Industrial temperature range is available by special order.
2. Green parts available. For specific speeds and packages contact your sales office.

DATASHEET DOCUMENT HISTORY

10/31/2000	pgs. 1, 6, 8, 9, 12 and 36
12/14/2000	pgs. 4 and 5.
02/08/2001	pgs. 5 and 11.
03/27/2001	pgs. 6 and 7.
11/04/2003	pg. 1.
05/27/2008	pg. 1, 6, and 36.
02/05/2009	pg. 36.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
408-360-1753
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