

# Apacer Memory Product Specification

## 1024MB DDR2 SDRAM SO-DIMM

1024MB DDR2 SDRAM SO-DIMM based on 128Mx8 ,8Banks, 1.8V DDR2 SDRAM with SPD

### Features

- Performance range ( Bandwidth: 6.4 GB/sec )

| Part Number  | Max Freq. (Clock) | Speed Grade |
|--------------|-------------------|-------------|
| 78.02G86.XX2 | 400MHz(2.5ns@CL6) | 800Mbps     |

- JEDEC standard 1.8V  $\pm$  0.1V Power Supply
- VDDQ = 1.8V  $\pm$  0.1V
- Internal Bank: 8 Bank
- Posted CAS
- Programmable CAS Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4, 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Refresh and Self Refresh
  - Average Refresh Period 7.8us
- Serial presence detect with EEPROM
- Compliance with RoHS
- Compliance with CE
- Operating Temperature Rang:
  - Commercial 0°C  $\leq$  TC  $\leq$  85°C
  - Industrial -40°C  $\leq$  TA  $\leq$  85°C
- Refresh: auto-refresh, self-refresh
  - Average refresh period
    - 7.8us at 0°C  $\leq$  TC  $\leq$  85°C
    - 3.9us at 85°C  $\leq$  TC  $\leq$  95°C
- Industrial System Level -40°C  $\leq$  TA  $\leq$  70°C

### Description

This module is 128M bit x 64x1Rank Double Data Rate SDRAM high density memory modules based on first generation of 1024MB DDR2 SDRAM respectively.

It consists of eight CMOS 128M x 8 bit with 8banks Double Data Rate SDRAMs in 60Ball FBGA packages mounted on a 200pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR2 SDRAM.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory

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## Pin Configurations (Front side/Back side)

| Pin | Front                    | Pin | Back                    | Pin | Front           | Pin | Back                     | Pin | Front                    | Pin | Back                     | Pin | Front                    | Pin | Back                     |
|-----|--------------------------|-----|-------------------------|-----|-----------------|-----|--------------------------|-----|--------------------------|-----|--------------------------|-----|--------------------------|-----|--------------------------|
| 1   | V <sub>REF</sub>         | 2   | V <sub>SS</sub>         | 51  | DQS2            | 52  | DM2                      | 101 | A1                       | 102 | A0                       | 151 | DQ42                     | 152 | DQ46                     |
| 3   | V <sub>SS</sub>          | 4   | DQ4                     | 53  | V <sub>SS</sub> | 54  | V <sub>SS</sub>          | 103 | V <sub>DD</sub>          | 104 | V <sub>DD</sub>          | 153 | DQ43                     | 154 | DQ47                     |
| 5   | DQ0                      | 6   | DQ5                     | 55  | DQ18            | 56  | DQ22                     | 105 | A10/AP                   | 106 | BA1                      | 155 | V <sub>SS</sub>          | 156 | V <sub>SS</sub>          |
| 7   | DQ1                      | 8   | V <sub>SS</sub>         | 57  | DQ19            | 58  | DQ23                     | 107 | BA0                      | 108 | $\overline{\text{RAS}}$  | 157 | DQ48                     | 158 | DQ52                     |
| 9   | V <sub>SS</sub>          | 10  | DM0                     | 59  | V <sub>SS</sub> | 60  | V <sub>SS</sub>          | 109 | $\overline{\text{WE}}$   | 110 | S0                       | 159 | DQ49                     | 160 | DQ53                     |
| 11  | $\overline{\text{DQS0}}$ | 12  | V <sub>SS</sub>         | 61  | DQ24            | 62  | DQ28                     | 111 | V <sub>DD</sub>          | 112 | V <sub>DD</sub>          | 161 | V <sub>SS</sub>          | 162 | V <sub>SS</sub>          |
| 13  | DQS0                     | 14  | DQ6                     | 63  | DQ25            | 64  | DQ29                     | 113 | $\overline{\text{CAS}}$  | 114 | ODT0                     | 163 | NC, TEST                 | 164 | CK1                      |
| 15  | V <sub>SS</sub>          | 16  | DQ7                     | 65  | V <sub>SS</sub> | 66  | V <sub>SS</sub>          | 115 | NC/S1                    | 116 | A13                      | 165 | V <sub>SS</sub>          | 166 | $\overline{\text{CK1}}$  |
| 17  | DQ2                      | 18  | V <sub>SS</sub>         | 67  | DM3             | 68  | $\overline{\text{DQS3}}$ | 117 | V <sub>DD</sub>          | 118 | V <sub>DD</sub>          | 167 | $\overline{\text{DQS6}}$ | 168 | V <sub>SS</sub>          |
| 19  | DQ3                      | 20  | DQ12                    | 69  | NC              | 70  | DQS3                     | 119 | NC/ODT1                  | 120 | NC                       | 169 | DQS6                     | 170 | DM6                      |
| 21  | V <sub>SS</sub>          | 22  | DQ13                    | 71  | V <sub>SS</sub> | 72  | V <sub>SS</sub>          | 121 | V <sub>SS</sub>          | 122 | V <sub>SS</sub>          | 171 | V <sub>SS</sub>          | 172 | V <sub>SS</sub>          |
| 23  | DQ8                      | 24  | V <sub>SS</sub>         | 73  | DQ26            | 74  | DQ30                     | 123 | DQ32                     | 124 | DQ36                     | 173 | DQ50                     | 174 | DQ54                     |
| 25  | DQ9                      | 26  | DM1                     | 75  | DQ27            | 76  | DQ31                     | 125 | DQ33                     | 126 | DQ37                     | 175 | DQ51                     | 176 | DQ55                     |
| 27  | V <sub>SS</sub>          | 28  | V <sub>SS</sub>         | 77  | V <sub>SS</sub> | 78  | V <sub>SS</sub>          | 127 | V <sub>SS</sub>          | 128 | V <sub>SS</sub>          | 177 | V <sub>SS</sub>          | 178 | V <sub>SS</sub>          |
| 29  | $\overline{\text{DQS1}}$ | 30  | CK0                     | 79  | CKE0            | 80  | NC/CKE1                  | 129 | $\overline{\text{DQS4}}$ | 130 | DM4                      | 179 | DQ56                     | 180 | DQ60                     |
| 31  | DQS1                     | 32  | $\overline{\text{CK0}}$ | 81  | V <sub>DD</sub> | 82  | V <sub>DD</sub>          | 131 | DQS4                     | 132 | V <sub>SS</sub>          | 181 | DQ57                     | 182 | DQ61                     |
| 33  | V <sub>SS</sub>          | 34  | V <sub>SS</sub>         | 83  | NC              | 84  | NC                       | 133 | V <sub>SS</sub>          | 134 | DQ38                     | 183 | V <sub>SS</sub>          | 184 | V <sub>SS</sub>          |
| 35  | DQ10                     | 36  | DQ14                    | 85  | BA2             | 86  | NC                       | 135 | DQ34                     | 136 | DQ39                     | 185 | DM7                      | 186 | $\overline{\text{DQS7}}$ |
| 37  | DQ11                     | 38  | DQ15                    | 87  | V <sub>DD</sub> | 88  | V <sub>DD</sub>          | 137 | DQ35                     | 138 | V <sub>SS</sub>          | 187 | V <sub>SS</sub>          | 188 | DQ57                     |
| 39  | V <sub>SS</sub>          | 40  | V <sub>SS</sub>         | 89  | A12             | 90  | A11                      | 139 | V <sub>SS</sub>          | 140 | DQ44                     | 189 | DQ58                     | 190 | V <sub>SS</sub>          |
| 41  | V <sub>SS</sub>          | 42  | V <sub>SS</sub>         | 91  | A9              | 92  | A7                       | 141 | DQ40                     | 142 | DQ45                     | 191 | DQ59                     | 192 | DQ62                     |
| 43  | DQ16                     | 44  | DQ20                    | 93  | A8              | 94  | A6                       | 143 | DQ41                     | 144 | V <sub>SS</sub>          | 193 | V <sub>SS</sub>          | 194 | DQ63                     |
| 45  | DQ17                     | 46  | DQ21                    | 95  | V <sub>DD</sub> | 96  | V <sub>DD</sub>          | 145 | V <sub>SS</sub>          | 146 | $\overline{\text{DQS5}}$ | 195 | SDA                      | 196 | V <sub>SS</sub>          |
| 47  | V <sub>SS</sub>          | 48  | V <sub>SS</sub>         | 97  | A5              | 98  | A4                       | 147 | DM5                      | 148 | DQS5                     | 197 | SCL                      | 198 | SA0                      |
| 49  | $\overline{\text{DQS2}}$ | 50  | NC                      | 99  | A3              | 100 | A2                       | 149 | V <sub>SS</sub>          | 150 | V <sub>SS</sub>          | 199 | V <sub>DD</sub> SPD      | 200 | SA1                      |

## Pin Description

| Pin Name                                      | Function                                 | Pin Name   | Function   |
|---|--|--|--|
| CK0,CK1                                       | Clock Inputs, positive line              | SDA  | SPD Data Input/Output                                    |
| $\overline{\text{CK0}},\overline{\text{CK1}}$ | Clock Inputs, negative line              | SA1,SA0  | SPD address  |
| CKE0,CKE1                                     | Clock Enables                            | DQ0~DQ63   | Data Input/Output  |
| $\overline{\text{RAS}}$                       | Row Address Strobe                       | DM0~DM7  | Data Masks   |
| $\overline{\text{CAS}}$                       | Column Address Strobe                    | DQS0~DQS7  | Data strobes   |
| $\overline{\text{WE}}$                        | Write Enable                             | $\overline{\text{DQS0}}\text{~}\overline{\text{DQS7}}$ | Data strobes complement                                  |
| $\overline{\text{S0}},\overline{\text{S1}}$   | Chip Selects                             | TEST   | Logic Analyzer specific test pin (No connect on So-DIMM) |
| A0~A9, A11~A13                                | Address Inputs                           | V <sub>DD</sub>  | Core and I/O Power                                       |
| A10/AP  | Address Input/Autoprecharge              | V <sub>SS</sub>  | Ground   |
| BA0-BA2                                       | SDRAM Bank Address                       | V <sub>REF</sub>                                       | Input/Output Reference                                   |
| ODT0,ODT1                                     | On-die termination control               | V <sub>DD</sub> SPD                                    | SPD Power  |
| SCL   | Serial Presence Detect (SPD) Clock Input | NC   | Spare pins, No connect                                   |

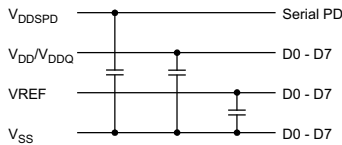
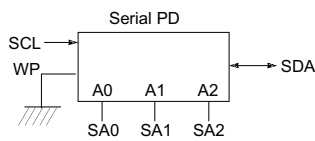
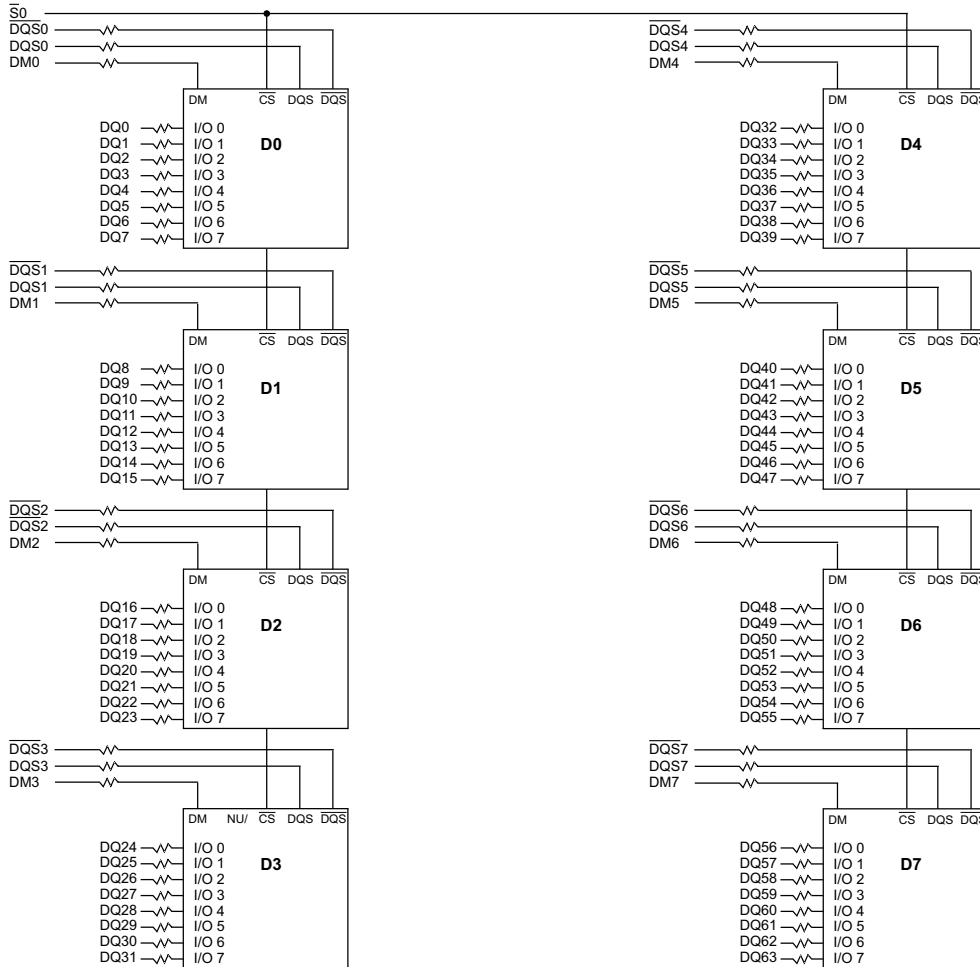
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## Input/Output Functional Description

| Symbol  | Type   | Function   |
|---|--------|--|
| CK0-CK1<br>CK0-CK1                                    | Input  | The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock input and output timing for read operations is synchronized to the input clock.  |
| CKE0-CKE1   | Input  | Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low, By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.   |
| $\overline{S0}$ - $\overline{S1}$                     | Input  | Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$ , Rank 1 is selected by $\overline{S1}$ . Ranks are also called "Physical banks".  |
| $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ | Input  | When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$ , $\overline{CAS}$ , $\overline{RAS}$ , and $\overline{WE}$ define the operation to be executed by the SDRAM.   |
| BA0~BA2   | Input  | Selects which DDR2 SDRAM internal bank is activated.   |
| ODT0~ODT1   | Input  | Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM Extended Mode Register Set (EMRS).  |
| A0~A9,<br>A10/AP,<br>A11~A13                          | Input  | During a Bank Activate command cycle, $\overline{A0}$ defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$ . During a Read or Write command cycle, $\overline{A0}$ defines the column address when sampled at the cross point of the rising edge of CK and falling edge of CK. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. |
| DQ0~DQ63  | In/Out | Data Input/Output pins.  |
| DM0~DM7   | Input  | The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.  |
| DQS0~DQS7<br>$\overline{DQS0}$ ~ $\overline{DQS7}$    | In/Out | The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$ If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.   |
| $V_{DD}$ , $V_{DD}$<br>SPD, $V_{SS}$                  | Supply | Power supplies for core, I/O, Serial Presence Detect, and ground for the module.   |
| SDA   | In/Out | This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to $V_{DD}$ to act as a pull up.   |
| SCL   | Input  | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to $V_{DD}$ to act as a pull up.  |
| SA0~SA1   | Input  | Address pins used to select the Serial Presence Detect base address.   |
| TEST  | In/Out | The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules(SO-DIMMs).   |

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## Functional Block Diagram



| * Clock Wiring |               |
|----------------|---------------|
| Clock Input    | DDR2 SDRAMs   |
| *CK0/CK0       | 2 DDR2 SDRAMs |
| *CK1/CK1       | 3 DDR2 SDRAMs |
| *CK2/CK2       | 3 DDR2 SDRAMs |

\*Wire per Clock Loading Table/Wiring Diagrams

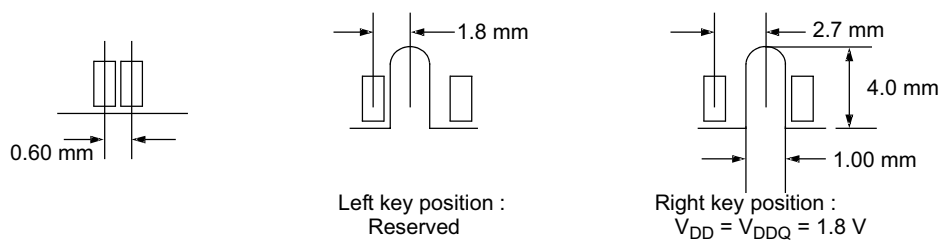
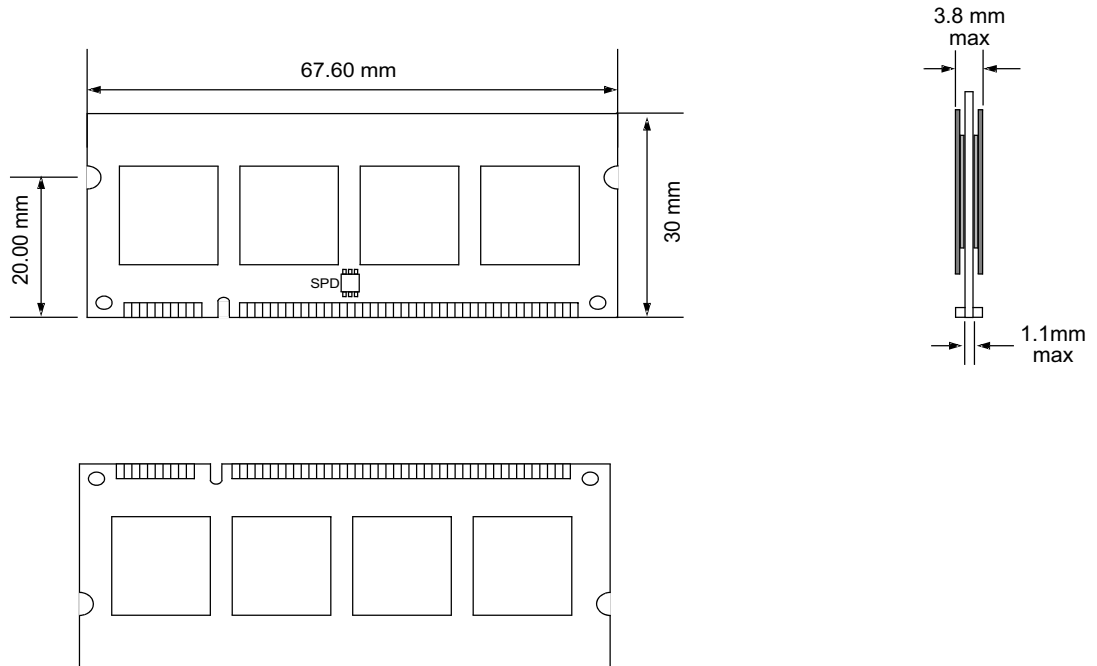
- BA0 - BA2 → BA0-BA2 : DDR2 SDRAMs D0 - D7
- A0 - A12 → A0-A12 : DDR2 SDRAMs D0 - D7
- RAS → RAS : DDR2 SDRAMs D0 - D7
- CAS → CAS : DDR2 SDRAMs D0 - D7
- CKE0 → CKE : DDR2 SDRAMs D0 - D7
- WE → WE : DDR2 SDRAMs D0 - D7
- ODT0 → ODT : DDR2 SDRAMs D0 - D7

### Notes :

1. DQ, DM, DQS/DQS resistors : 22 Ohms " 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 10 Ohms " 5%.

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## Physical Dimensions



Tolerances: +0.15mm unless otherwise specified