NBSG72A

2.5 V/3.3 V SiGe Differential 2 x 2 Crosspoint Switch with Output Level Select

The NBSG72A is a high-bandwidth fully differential 2×2 crosspoint switch with Output Level Select (OLS) capabilities. This is a part of the GigaComm™ family of high performance Silicon Germanium products. The device is housed in a low profile 3×3 mm 16-pin QFN package.

Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The OLS input is used to program the peak-to-peak output amplitude between 0 mV and 800 mV in five discrete steps. The SELECT inputs are single-ended and can be driven with either LVECL or LVCMOS/LVTTL input levels.

Features

- Maximum Input Clock Frequency > 7 GHz Typical
- Maximum Input Data Rate > 7 Gb/s Typical
- 200 ps Typical Propagation Delay (OLS = FLOAT)
- 55/45 ps Typical Rise/Fall Times (OLS = FLOAT)
- Selectable Swing PECL Output with Operating Range:
  V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- Selectable Output Levels (0 mV, 200 mV, 400 mV, 600 mV or 800 mV Peak-to-Peak Output)
- 50 Ω Internal Input Termination Resistors
- Single-Ended LVECL or LVCMOS/LVTTL Select Inputs (SELA, SELB)
- These are Pb-Free Devices

ON Semiconductor®

http://onsemi.com

QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*

```
SG
72A
ALYW■
■
```
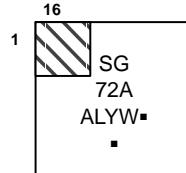
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
■	= Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

NBSG72A

Exposed Pad (EP)
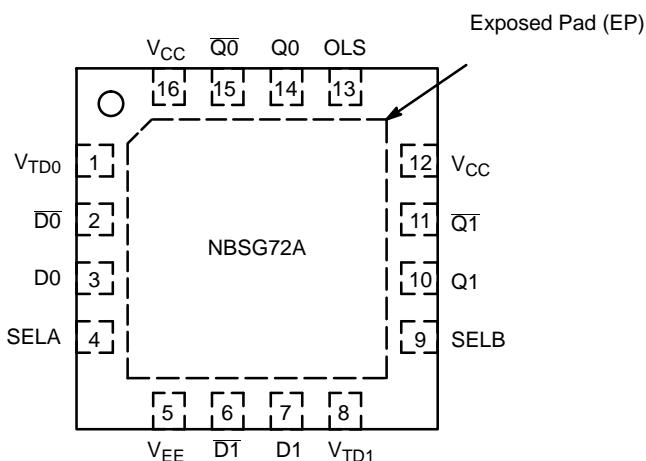
Figure 1. QFN–16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	VTD0	–	Common Internal 50 Ω Termination Pin for D0 and $\overline{D0}$ Input. See Table 4. (Note 1)
2	$\overline{D0}$	LVDS, CML, ECL, LVTTL, LVCMOS Input	Inverted Differential Input 0.
3	D0	LVDS, CML, ECL, LVTTL, LVCMOS Input	Noninverted Differential Input 0.
4	SELA	LVECL, LVCMOS Input	Select Logic Input A. Internal 75 kΩ Pulldown to V_{EE}.
5	V_{EE}	–	Negative Supply. All V_{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
6	$\overline{D1}$	LVDS, CML, ECL, LVTTL, LVCMOS Input	Inverted Differential Input 1.
7	D1	LVDS, CML, ECL, LVTTL, LVCMOS Input	Noninverted Differential Input 1.
8	VTD1	–	Common Internal 50 Ω Termination Pin for D1 and $\overline{D1}$ Input. See Table 4. (Note 1)
9	SELB	LVECL, LVCMOS Input	Select Logic Input B. Internal 75 kΩ Pulldown to V_{EE}.
10	Q1	RSECL Output	Noninverted Differential Output.
11	$\overline{Q1}$	RSECL Output	Inverted Differential Output.
12	V_{CC}	–	Positive Supply. All V_{CC} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
13	OLS (Note 2)	Input	Input Pin for Output Level Select (OLS) See Table 3.
14	Q0	RSECL Output	Noninverted Differential Output Typically Terminated with 50 Ω Resistor to $V_{TT} = V_{CC} - 2.0$ V.
15	$\overline{Q0}$	RSECL Output	Inverted Differential Output Typically Terminated with 50 Ω Resistor to $V_{TT} = V_{CC} - 2.0$ V.
16	V_{CC}	–	Positive Supply. All V_{CC} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
–	EP	–	The Exposed Pad (EP) on the QFN–16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to V_{EE} on the PC board.

1. In the differential configuration when the input termination pins (VTD0, VTD1) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.
2. When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, 2 kΩ resistor should be connected from OLS pin to V_{EE}.

NBSG72A
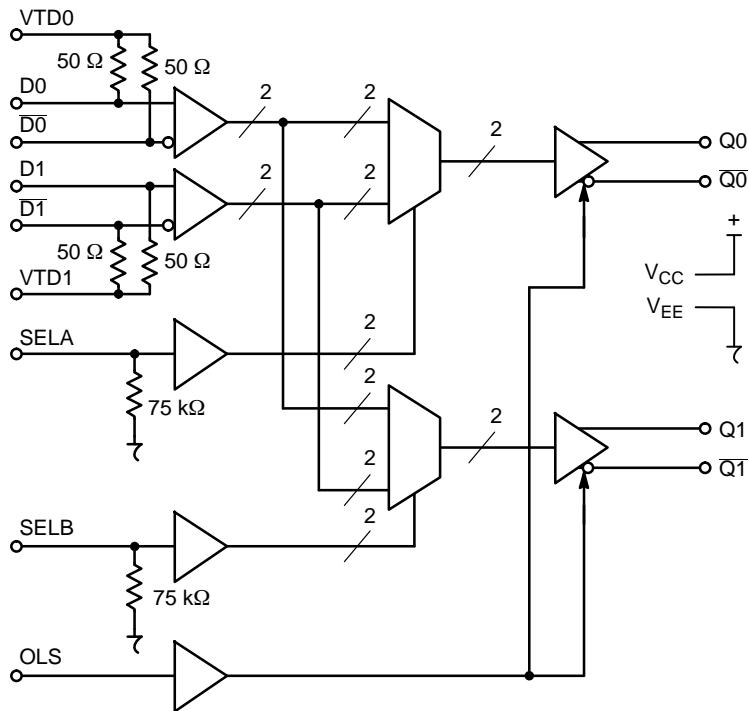
Figure 2. Logic/Block Diagram

Table 2. TRUTH TABLE

SELA	SELB	Q0	Q1
LOW	LOW	D0	D0
HIGH	LOW	D1	D0
LOW	HIGH	D0	D1
HIGH	HIGH	D1	D1

Table 3. OUTPUT LEVEL SELECT (OLS)

OLS	Output Amplitude (V_{OUTPP})	OLS Sensitivity
V_{CC}	800 mV	OLS − 75 mV
V_{CC} − 0.4 V	200 mV	OLS ± 150 mV
V_{CC} − 0.8 V	600 mV	OLS ± 100 mV
V_{CC} − 1.2 V	0	OLS ± 75 mV
V_{EE} (Note 3)	400 mV	OLS ± 100 mV
FLOAT	600 mV	N/A

3. When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

Table 4. INTERFACING OPTIONS

Interfacing Options	Connections
CML	Connect VTD0 and VTD1 to V_{CC}
LVDS	VTD0 and VTD1 Should Be Left Floating.
AC−COUPLED	Bias VTD0 and VTD1 Inputs within Common Mode Range (VIHCMR)
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVCMOS / LVTTL	The external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL and V_{CC}/2 for LVCMOS Inputs.

Table 5. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (SELA, SELB)		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 50 V > 1 kV
Moisture Sensitivity (Note 4)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count		436
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

4. For additional information, see Application Note AND8003/D.

Table 6. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	$V_{EE} = 0$ V		3.6	V
V_{EE}	Negative Power Supply	$V_{CC} = 0$ V		–3.6	V
V_I	Positive Input Negative Input	$V_{EE} = 0$ V $V_{CC} = 0$ V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 –3.6	V
V_{INPP}	Differential Input Voltage $|D_X - \overline{D_X}|$	$V_{EE} - V_{CC} \geq 2.8$ V $V_{EE} - V_{CC} < 2.8$ V		2.8 $|V_{CC} - V_{EE}|$	V
I_{out}	Output Current	Continuous Surge		25 50	mA
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
T_A	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 5)	0 lfpm 500 lfpm		42 35	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	(Note 5)		4	°C/W
T_{sol}	Wave Solder Pb-Free	< 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
5. JEDEC standard multilayer board – 1S2P (1 signal, 2 power).

Table 7. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT

(V_{CC} = 2.5 V; V_{EE} = 0 V) (Note 6)

Symbol	Characteristic	−40°C Min	−40°C Typ	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Typ	85°C Max	Unit
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	40	55	65	40	55	65	40	55	65	mA
PECL OUTPUTS (Note 7)											
V_{OH}	Output HIGH Voltage	1460	1510	1560	1490	1540	1590	1515	1565	1615	mV
V_{OL}	Output LOW Voltage										mV
	(OLS = V_{CC})	555	705	855	595	745	895	625	775	925	
	(OLS = V_{CC} − 0.4 V)	1235	1295	1385	1270	1330	1420	1295	1355	1445	
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)	775	895	1015	810	930	1050	840	960	1080	
	(OLS = V_{CC} − 1.2 V)	1455	1505	1585	1490	1540	1620	1510	1560	1640	
	(OLS = V_{EE})	1005	1095	1215	1040	1130	1250	1065	1155	1275	
V_{OUTPP}	Output Voltage Amplitude										mV
	(OLS = V_{CC})	670	800		660	795		655	790		
	(OLS = V_{CC} − 0.4 V)	125	215		120	210		120	210		
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)	510	615		505	610		500	605		
	(OLS = V_{CC} − 1.2 V)	0	5		0	0		0	0		
	(OLS = V_{EE})	325	415		320	410		320	410		
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 12 & 14) (Note 8)											
V_{IH}	Input HIGH Voltage D0, inv-D0, D1, inv-D1, SELA, SELB	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage D0, inv-D0, D1, inv-D1, SELA, SELB	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Reference Voltage Range (Note 9)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		260	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 13 & 15) (Note 10)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11) (Figure 16)	1200		2500	1200		2500	1200		2500	mV
I_{IH}	Input HIGH Current (@V_{IH})		35	100		35	100		35	100	µA
I_{IL}	Input LOW Current (@V_{IL})		20	100		20	100		20	100	µA
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with V_{CC}.
7. All outputs loaded with 50 Ω to V_{CC} − 2.0 V.
8. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
9. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
10. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
11. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT

(V_{CC} = 3.3 V; V_{EE} = 0 V) (Note 12)

Symbol	Characteristic	−40°C Min	−40°C Typ	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Typ	85°C Max	Unit
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	40	55	65	40	55	65	40	55	65	mA
PECL OUTPUTS (Note 13)											
V_{OH}	Output HIGH Voltage	2260	2310	2360	2290	2340	2390	2315	2365	2415	mV
V_{OL}	Output LOW Voltage										mV
	(OLS = V_{CC})	1320	1470	1620	1360	1510	1660	1390	1540	1690	
	(OLS = V_{CC} − 0.4 V)	2030	2090	2180	2065	2125	2215	2090	2150	2240	
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)	1550	1670	1790	1585	1705	1825	1615	1735	1855	
	(OLS = V_{CC} − 1.2 V)	2260	2310	2390	2290	2340	2420	2315	2365	2445	
	**(OLS = V_{EE})	1785	1875	1995	1820	2030	2030	1850	1940	2060	
V_{OUTPP}	Output Voltage Amplitude										mV
	(OLS = V_{CC})	705	815		695	805		590	800		
	(OLS = V_{CC} − 0.4 V)	130	220		125	215		125	215		
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)	535	640		530	635		525	630		
	(OLS = V_{CC} − 1.2 V)	0	0		0	0		0	0		
	**(OLS = V_{EE})	345	435		340	430		335	425		
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 12 & 14) (Note 14)											
V_{IH}	Input HIGH Voltage D0, inv-D0, D1, inv-D1, SELA, SELB	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage D0, inv-D0, D1, inv-D1, SELA, SELB	0		V_{IH} − 150	0		V_{IH} − 150	0		V_{IH} − 150	mV
V_{th}	Input Threshold Reference Voltage Range (Note 15)	950		V_{CC} − 75	950		V_{CC} − 75	950		V_{CC} − 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		2600	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 13 & 15) (Note 16)											
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	0		V_{IHD} − 75	0		V_{IHD} − 75	0		V_{IHD} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 17) (Figure 16)	1200		3300	1200		3300	1200		3300	mV
I_{IH}	Input HIGH Current (@V_{IH})		35	100		35	100		35	100	μA
I_{IL}	Input LOW Current (@V_{IL})		20	100		20	100		20	100	μA
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.
12. Input and output parameters vary 1:1 with V_{CC}.
13. All outputs loaded with 50 Ω to V_{CC} − 2.0 V.
14. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
15. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
16. V_{IHD}, V_{ILD}, V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
17. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

(V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V) (Note 18)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	40	55	65	40	55	65	40	55	65	mA
NECL OUTPUTS (Note 19)											
V_{OH}	Output HIGH Voltage	–1040	–990	–940	–1010	–960	–910	–985	–935	–885	mV
V_{OL}	Output LOW Voltage –3.465 V ≤ V_{EE} ≤ –3.0 V										mV
	(OLS = V_{CC})	–1980	–1830	–1680	–1940	–1790	–1640	–1910	–1760	–1610	
	(OLS = V_{CC} – 0.4 V)	–1270	–1210	–1120	–1235	–1175	–1085	–1210	–1150	–1060	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	–1750	–1630	–1510	–1715	–1595	–1475	–1685	–1565	–1445	
	(OLS = V_{CC} – 1.2 V)	–1040	–990	–910	–1010	–960	–880	–985	–935	–855	
	**(OLS = V_{EE})	–1515	–1425	–1305	–1480	–1390	–1270	–1450	–1360	–1240	
	–3.0 V < V_{EE} ≤ –2.375 V										
	(OLS = V_{CC})	–1945	–1795	–1645	–1905	–1755	–1605	–1875	–1725	–1575	
	(OLS = V_{CC} – 0.4 V)	–1265	–1205	–1115	–1230	–1170	–1080	–1205	–1145	–1055	
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	–1725	–1605	–1485	–1690	–1570	–1450	–1660	–1540	–1420	
	(OLS = V_{CC} – 1.2 V)	–1045	–995	–915	–1010	–960	–880	–900	–940	–860	
	(OLS = V_{EE})	–1495	–1405	–1285	–1460	–1370	–1250	–1435	–1345	–1225	
V_{OUTPP}	Output Voltage Amplitude –3.465 V ≤ V_{EE} ≤ –3.0 V										mV
	(OLS = V_{CC})	705	815		695	805		690	800		
	(OLS = V_{CC} – 0.4 V)	130	220		125	215		125	215		
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	535	640		530	635		525	630		
	(OLS = V_{CC} – 1.2 V)	0	0		0	0		0	0		
	**(OLS = V_{EE})	345	435		340	430		335	425		
	–3.0 V < V_{EE} ≤ –2.375 V										
	(OLS = V_{CC})	670	800		660	795		655	790		
	(OLS = V_{CC} – 0.4 V)	125	215		120	210		120	210		
	(OLS = V_{CC} – 0.8 V, OLS = FLOAT)	510	615		505	610		500	605		
	(OLS = V_{CC} – 1.2 V)	0	5		0	0		0	5		
	(OLS = V_{EE})	325	415		320	410		320	410		
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 12 & 14) (Note 20)											
V_{IH}	Input HIGH Voltage (Single-Ended) D0, inv-D0, D1, inv-D1, SELA, SELB	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{IL}	Input LOW Voltage (Single-Ended) D0, inv-D0, D1, inv-D1, SELA, SELB	V_{EE}		V_{IH} – 150	V_{EE}		V_{IH} – 150	V_{EE}		V_{IH} – 150	mV
V_{th}	Input Threshold Reference Voltage Range (Note 21)	V_{EE} + 950		V_{CC} – 75	V_{EE} + 950		V_{CC} – 75	V_{EE} + 950		V_{CC} – 75	mV
V_{ISE}	Single-Ended Input Voltage (V_{IH} – V_{IL})	150		2600	150		2600	150		260	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 13 & 15) (Note 22)											
V_{IHD}	Differential Input HIGH Voltage	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	V_{EE} + 1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		V_{IHD} – 75	V_{EE}		V_{IHD} – 75	V_{EE}		V_{IHD} – 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD})	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 23) (Figure 16)	V_{EE} + 1200		0.0	V_{EE} + 1200		0.0	V_{EE} + 1200		0.0	mV
I_{IH}	Input HIGH Current (@V_{IH})		35	1000		35	1000		35	100	μA
I_{IL}	Input LOW Current (@V_{IL})		20	100		20	100		20	1000	μA

Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT (continued)

(V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V) (Note 18)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 13 & 15) (Note 22)											
I_{OLS}	OLS Input Current (see Figure 10) (OLS = V_{CC})		300	900		300	900		300	900	µA
	(OLS = V_{CC} − 0.4 V)		100	300		100	300		100	300	
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)		5	100		5	100		5	100	
	(OLS = V_{CC} − 1.2 V)	−300	−100		−300	−100		−300	−100		
	−3.465 V ≤ V_{EE} ≤ −3.0 V *(OLS = V_{EE})	−1500	−600		−1500	−600		−1500	−600		
	−3.0 V < V_{EE} ≤ −2.375 V (OLS = V_{EE})	−1000	−400		−1000	−400		−1000	−400		
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

18. Input and output parameters vary 1:1 with V_{CC}.

19. All outputs loaded with 50 Ω to V_{CC} − 2.0 V.

20. V_{th}, V_{IH}, $V_{IL,}$ and V_{ISE} parameters must be complied with simultaneously.

21. V_{th} is applied to the complementary input when operating in single-ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.

22. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.

23. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 10. AC CHARACTERISTICS

(V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V) (Note 24)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude $\quad f_{in}$ < 5 GHz $\qquad\qquad\qquad\qquad\qquad\quad f_{in} \leq$ 7 GHz	400 200	590 250		450 180	590 250		440 130	590 250		mV
t_{PLH}	Propagation Delay to Output Differential $\qquad\qquad\qquad$ D0, D1 → Q0, Q1 $\qquad\qquad\qquad$ SELA, SELB → Q0, Q1	170 190	205 265	255 350	170 190	205 265	255 350	170 190	210 265	260 350	ps
t_{PHL}	Propagation Delay to Output Differential $\qquad\qquad\qquad$ D0, D1 → Q0, Q1 $\qquad\qquad\qquad$ SELA, SELB → Q0, Q1	170 150	205 215	255 270	170 150	205 215	255 270	170 150	210 215	260 270	ps
t_{SKEW}	Duty Cycle Skew (Note 25) Within-Device Skew Device-to-Device Skew	 	5.0 5.0 15	25 25 50	 	5.0 5.0 15	25 25 50	 	5.0 5.0 15	25 25 50	ps
t_{JITTER}	RMS Random Clock Jitter (Note 26) $\leq$ 1 GHz $\qquad\qquad$ OLS = V_{CC} $\leq$ 5 GHz $\qquad\qquad$ OLS = V_{CC} $\leq$ 6.5 GHz $\qquad\quad$ OLS = V_{CC} $\leq$ 1 GHz $\qquad$ OLS = V_{CC} – 400 mV $\leq$ 5 GHz $\qquad$ OLS = V_{CC} – 400 mV $\leq$ 6.5 GHz $\quad\;$ OLS = V_{CC} – 400 mV $\leq$ 1 GHz $\qquad$ OLS = V_{CC} – 800 mV $\leq$ 5 GHz $\qquad$ OLS = V_{CC} – 800 mV $\leq$ 6.5 GHz $\quad\;$ OLS = V_{CC} – 800 mV $\leq$ 1 GHz $\qquad\qquad$ OLS = V_{EE} $\leq$ 5 GHz $\qquad\qquad$ OLS = V_{EE} $\leq$ 6.5 GHz $\qquad\quad$ OLS = V_{EE} Peak-to-Peak Data Dependent Jitter (Note 27) $\qquad\qquad\qquad f_{in} \leq$ 7 Gb/s	 0.16 0.14 0.21 0.23 0.18 0.2 0.17 0.14 0.2 0.18 0.16 0.18 12	 0.3 0.4 0.5 0.4 0.5 0.5 0.3 0.4 0.5 0.3 0.6 0.5 18	 	 0.17 0.16 0.31 0.23 0.19 0.25 0.18 0.16 0.27 0.19 0.17 0.24 12	 0.3 0.4 0.7 0.4 0.5 0.6 0.3 0.3 0.7 0.3 0.4 0.6 18	 0.18 0.19 0.44 0.25 0.23 0.32 0.19 0.2 0.38 0.2 0.2 0.34 12	 0.4 0.4 0.9 0.4 0.5 0.7 0.3 0.3 0.9 0.3 0.4 0.8 18	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 28)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times $\qquad$ (Q0, Q1) (20% – 80%) $\qquad\qquad\qquad\qquad t_r$ @ 1 GHz $\qquad\qquad\qquad\qquad\quad t_f$	 40 30	 55 45	 70 55	 40 30	 55 45	 70 55	 40 30	 55 45	 70 55	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

24. Measured using a 75 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} – 2.0 V. OLS = FLOAT. Input edge rates 40 ps (20% – 80%).
25. t_{SKEW} = |t_{PLH} – t_{PHL}| for a nominal 50% differential clock input waveform.
26. Additive RMS jitter with 50% Duty Cycle clock signal.
27. Additive Peak-to-Peak data dependent jitter with NRZ PRBS 2^{31-1} data at 7 Gb/s.
28. Input Voltage Swing is a single-ended measurement operating in differential mode. V_{INPP} (max) cannot exceed V_{CC} – V_{EE}.
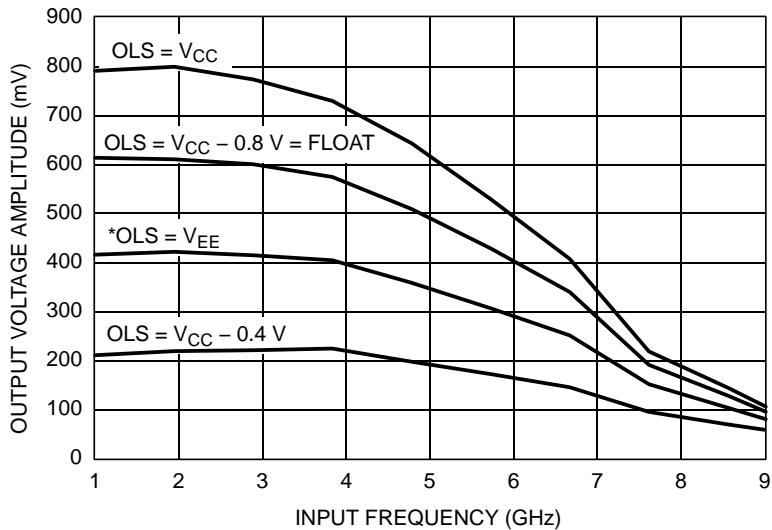
Figure 3. Output Voltage Amplitude (V$_{OUTPP}$) vs.
Input Clock Frequency (f$_{in}$) @ Ambient Temperature (Typical)

*When an output level of 400 mV is desired and V$_{CC}$ − V$_{EE}$ > 3.0 V, a 2 kΩ resistor should be connected from OLS to V$_{EE}$.
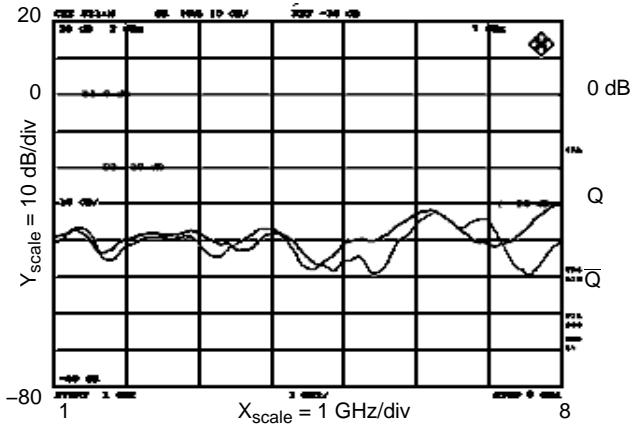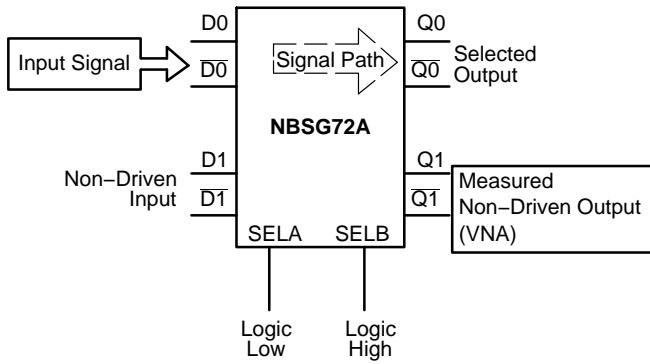

Figure 4. Channel-to-Channel Crosstalk Isolation at Ambient Temperature
**(D0 to Q0 Signal Path Selected; SelA = Low, SelB = High)**
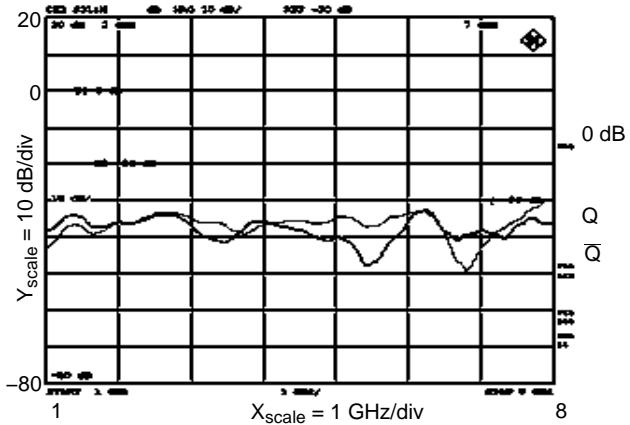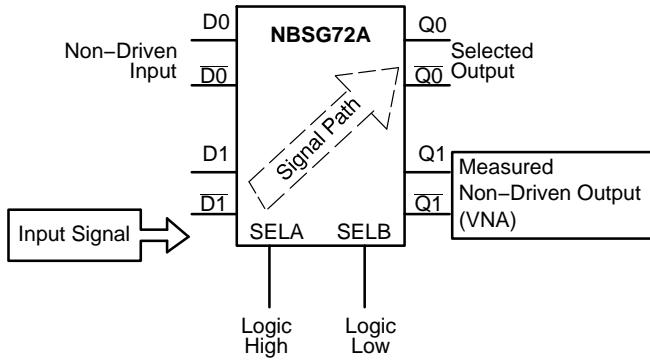
Figure 5. Channel-to-Channel Crosstalk Isolation at Ambient Temperature
(D1 to Q0 Signal Path Selected; SelA = High, SelB = Low)
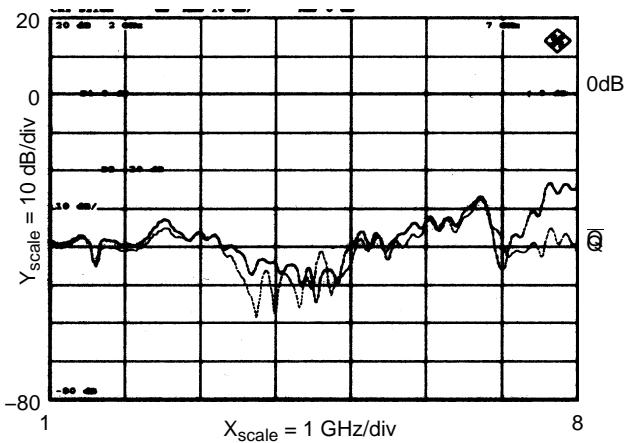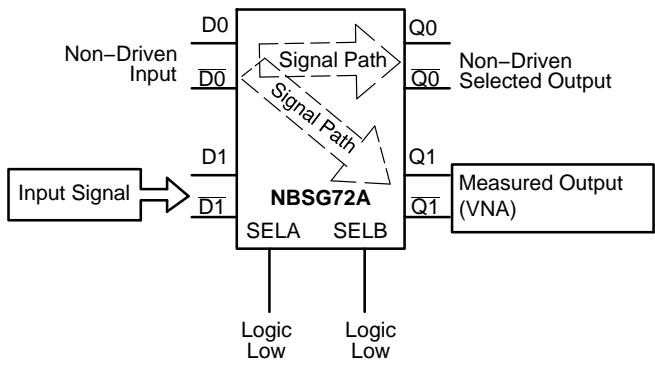
**Figure 6. Channel-to-Channel Crosstalk Isolation at Ambient Temperature
(D0 to Q0 and Q1 Signal Path Selected; SelA = Low, SelB = Low)**
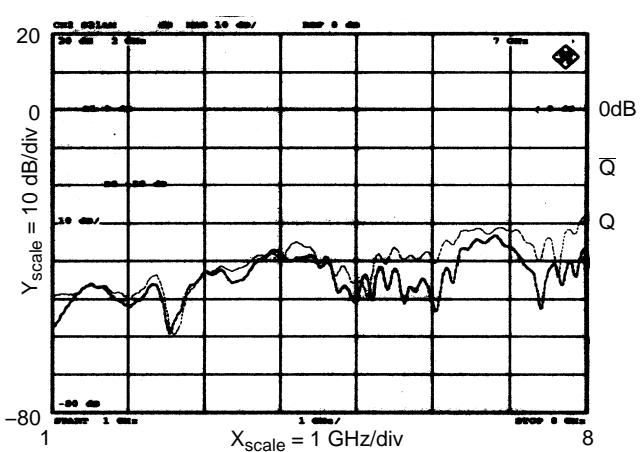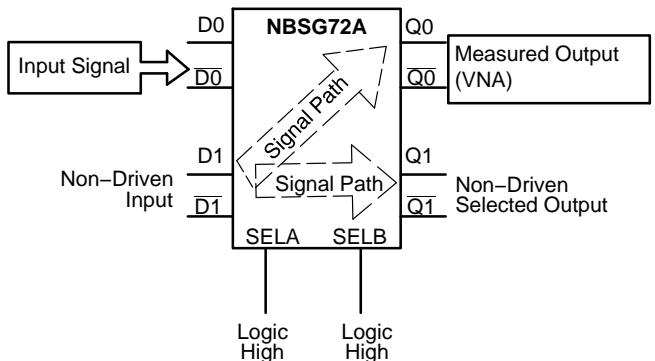
**Figure 7. Channel-to-Channel Crosstalk Isolation at Ambient Temperature
(D1 to Q0 and Q1 Signal Path Selected; SelA = High, SelB = High)**

Total System Jitter = 17.2 ps
Input Generator Jitter = 10 ps
Device Jitter = 6.8 ps

X = 60 ps/div
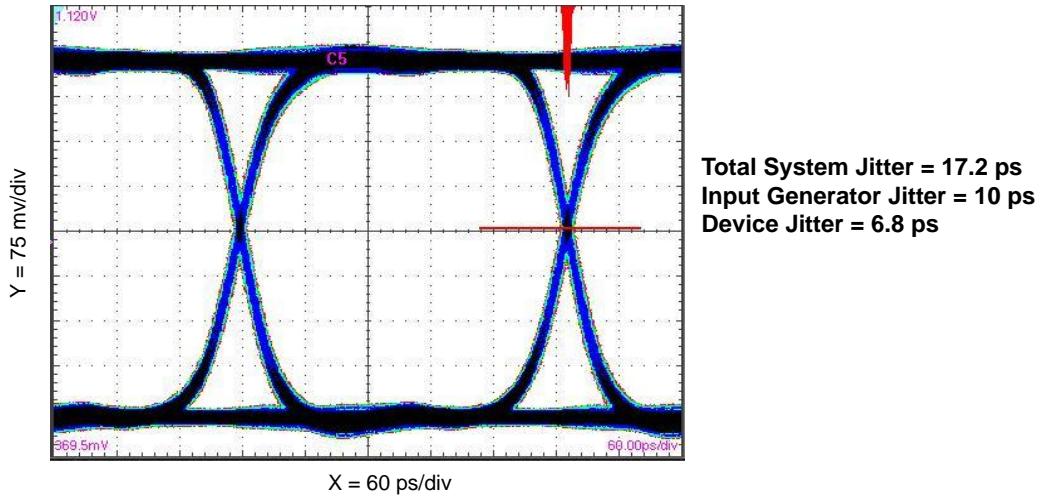
Figure 8. Eye Diagram at 3.2 Gb/s
(V_{CC} − V_{EE} = 3.3 V, OLS = FLOAT @ 25°C with input pattern of $2^{31}-1$ PRBS, 5000 Waveforms)

Total System Jitter = 17.2 ps
Input Generator Jitter = 10 ps
Device Jitter = 7.2 ps

X = 21 ps/div
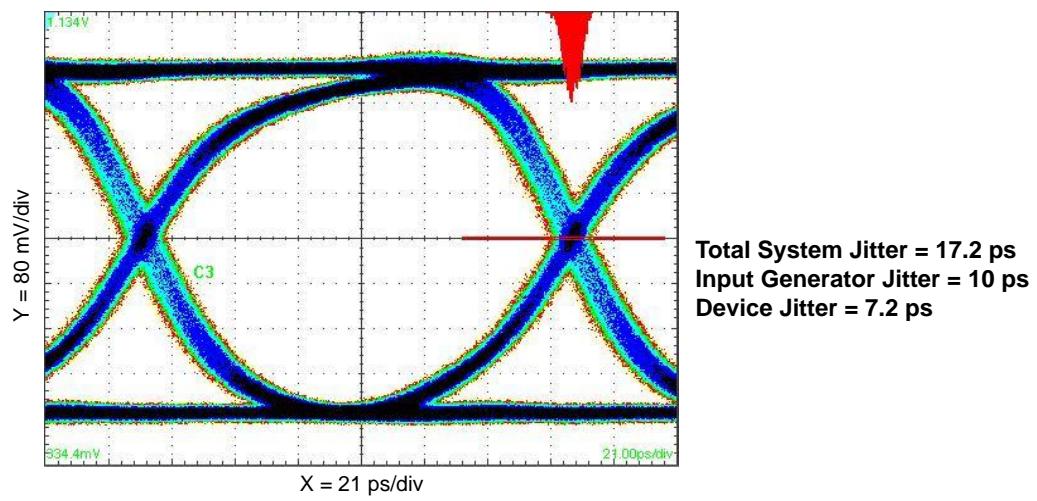
Figure 9. Eye Diagram at 7 Gb/s/s
(V_{CC} − V_{EE} = 3.3 V, OLS = FLOAT @ 25°C with input pattern of $2^{31}-1$ PRBS, 5000 Waveforms)
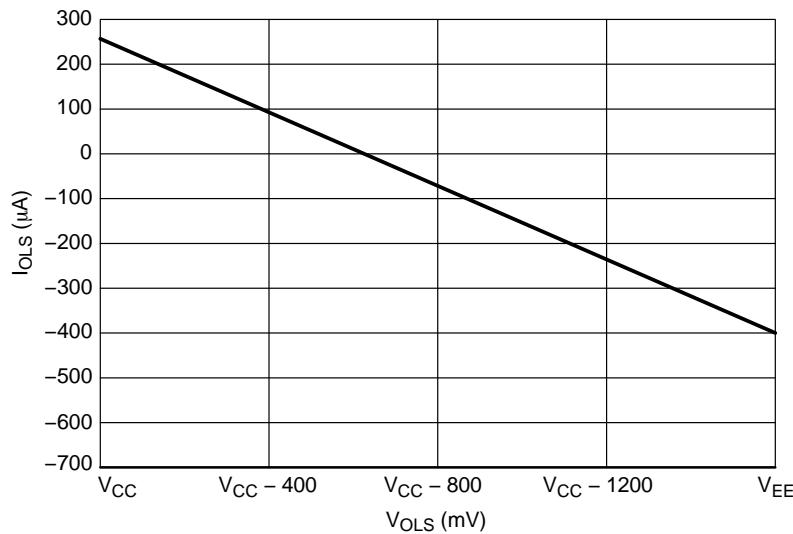
Figure 10. Typical OLS Input Current vs. OLS Input Voltage
(V$_{CC}$ − V$_{EE}$ = 3.3 V @ 25°C)
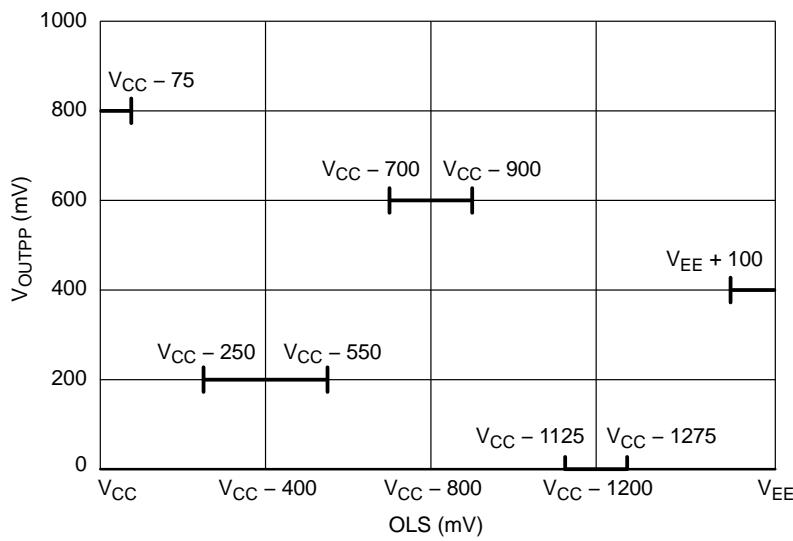
Figure 11. OLS Operating Area
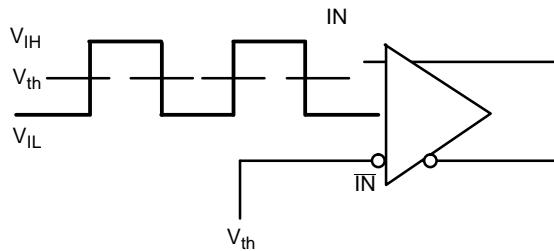
**Figure 12. Differential Input Driven
Single-Ended**
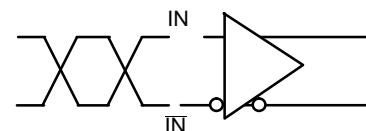
**Figure 13. Differential Inputs
Driven Differentially**
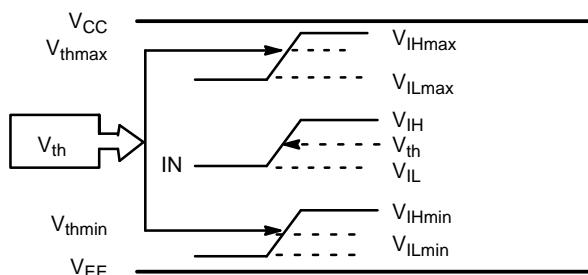
Figure 14. V_{th} Diagram
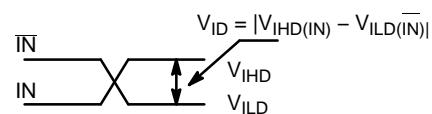
**Figure 15. Differential Inputs Driven
Differentially**
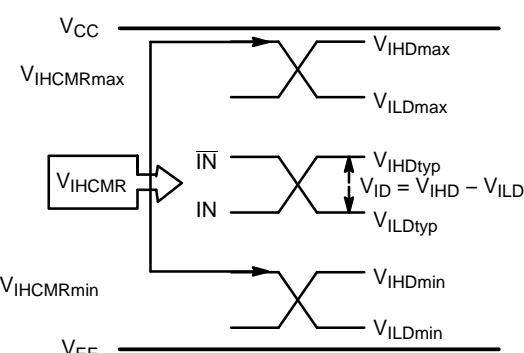
Figure 16. V_{IHCMR} Diagram
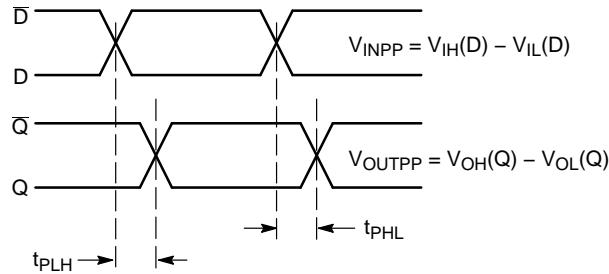
Figure 17. AC Reference Measurement

$V_{TT} = V_{CC} - 2.0\ V$
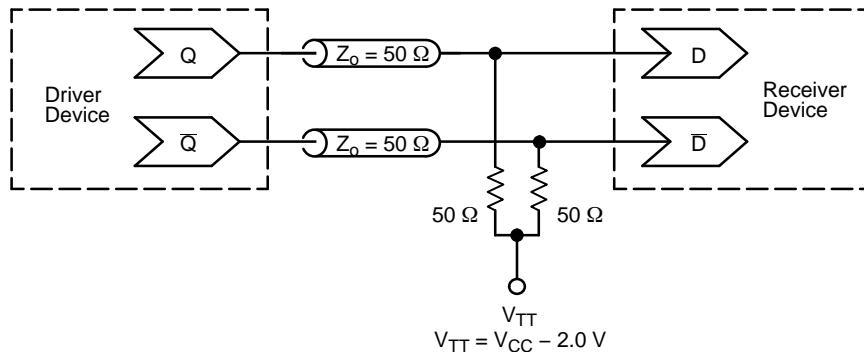
**Figure 18. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

ORDERING INFORMATION

Device	Package	Shipping[†]
NBSG72AMNG	QFN-16 (Pb-Free / Halide-Free)	123 Units / Tube
NBSG72AMNR2G	QFN-16 (Pb-Free / Halide-Free)	3000 / Tape & Reel

Board	Description
NBSG72AMNEVB	NBSG72AMN Evaluation Board

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPICE Modeling Kit

AN1504/D – Metastability and the ECLinPS™ Family

AN1568/D – Interfacing between LVDC and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

NBSG72A

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F
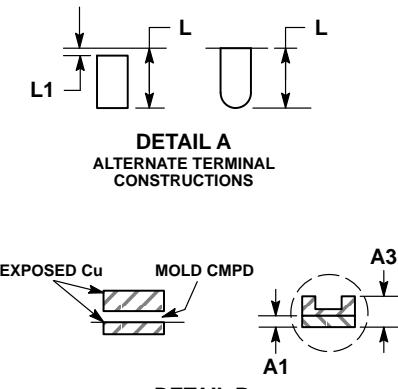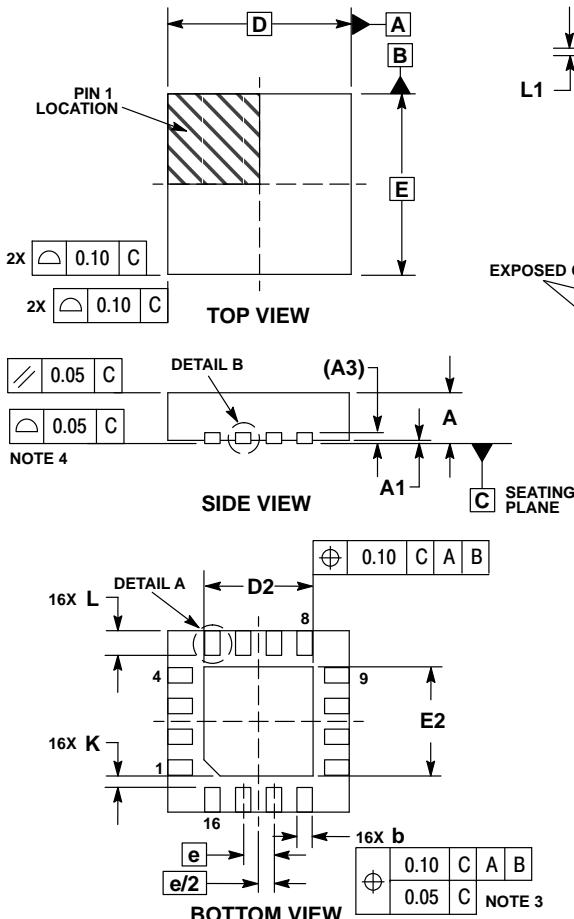
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

TOP VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DETAIL B
ALTERNATE CONSTRUCTIONS

SIDE VIEW

BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS
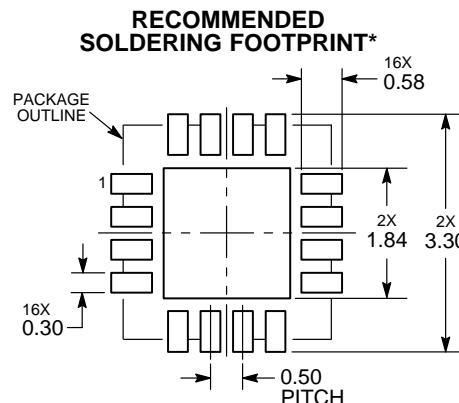
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GigaComm is a trademark of Semiconductor Components Industries, LLC.

NBSG72A/D