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FAIRCHILD SEMICONDUCTOR TM

September 1999

# Si4532DY*

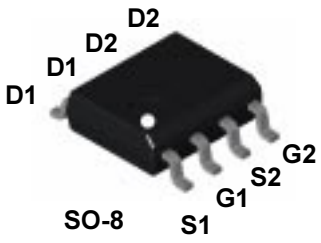
## Dual N- and P-Channel Enhancement Mode Field Effect Transistor

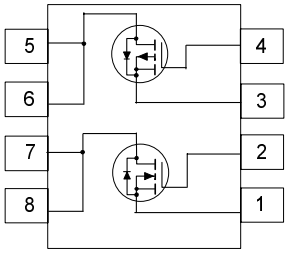
### General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild's propretary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- N-Channel 3.9A, 30V. $R_{DS(ON)}$ = 0.065Ω @$V_{GS}$ = 10V
  $R_{DS(ON)}$ = 0.095Ω @$V_{GS}$ = 4.5V.
- P-Channel -3.5A,-30V. $R_{DS(ON)}$= 0.085Ω @$V_{GS}$ = -10V
  $R_{DS(ON)}$= 0.190 Ω @$V_{GS}$ = -4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | N-Channel | P-Channel | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | -30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | 20 | -20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 3.9 | -3.5 | A |
| | - Pulsed | | 20 | -20 | |
| $P_D$ | Power Dissipation for Dual Operation | | 2 | | W |
| | Power Dissipation for Single Operation | (Note 1a) | 1.6 | | |
| | | (Note 1b) | 1 | | |
| | | (Note 1c) | 0.9 | | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | | 62.5 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 40 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|
| 4532 | Si4532DY | 13" | 12mm | 2500 units |

* Die and manufacturing source subject to change without prior notification.

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

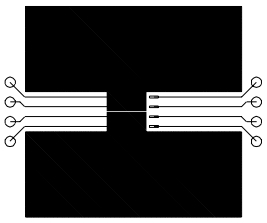
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | N-Ch | 30 | | | V |
| | | $V_{GS}$ = 0 V, $I_D$ = -250 μA | P-Ch | -30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | N-Ch | | | 1 | μA |
| | | $V_{DS}$ = -24 V, $V_{GS}$ = 0 V | P-Ch | | | -1 | μA |
| $I_{GSSF}$ | Gate-Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | All | | | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | All | | | -100 | nA |
| **On Characteristics** (Note 2) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | N-Ch | 1 | | 3 | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 μA | P-Ch | -1 | | -3 | V |
| $R_{DS(on)}$ | Static Drain-Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.9 A | N-Ch | | 0.053 | 0.065 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 3.1 A | | | 0.081 | 0.095 | |
| | | $V_{GS}$ = -10 V, $I_D$ = -2.5 A | P-Ch | | 0.06 | 0.085 | |
| | | $V_{GS}$ = -4.5 V, $I_D$ = -1.8 A | | | 0.095 | 0.19 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | N-Ch | 15 | | | A |
| | | $V_{GS}$ = -10 V, $V_{DS}$ = -5 V | P-Ch | -15 | | | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 15 V, $I_D$ = 3.9 A | N-Ch | | 7 | | S |
| | | $V_{DS}$ = -15 V, $I_D$ = -2.5 A | P-Ch | | 5 | | |
| **Dynamic Characteristics** | | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | N-Ch | | 235 | | pF |
| | | | P-Ch | | 420 | | |
| $C_{oss}$ | Input Capacitance | $V_{DS}$ = -10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | N-Ch | | 150 | | pF |
| | | | P-Ch | | 140 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | N-Ch | | 49 | | pF |
| | | | P-Ch | | 60 | | |

## Electrical Characteristics (continued)

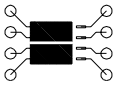
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Switching Characteristics** (Note 2) | | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | N-Ch | | 7 | 13 | ns |
| | | | P-Ch | | 9 | 18 | |
| $t_r$ | Turn-On Rise Time | | N-Ch | | 18 | 29 | ns |
| | | | P-Ch | | 8 | 16 | |
| $t_{d(off)}$ | Turn-Off Delay Time | $V_{DD}$ = -10 V, $I_D$ = -2.5 A, $V_{GS}$ = -10 V, $R_{GEN}$ = 6 Ω | N-Ch | | 15 | 27 | ns |
| | | | P-Ch | | 18 | 29 | |
| $t_f$ | Turn-Off Fall Time | | N-Ch | | 0.8 | 8 | ns |
| | | | P-Ch | | 6 | 12 | |
| $t_{rr}$ | Drain-Source Reverse Recovery Time | $I_F$ = 1.7 A, di/dt = 100A/μs | N-Ch | | | 80 | nS |
| | | $I_F$ = -1.7 A, di/dt = 100A/μs | P-Ch | | | 80 | |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 10 V, $I_D$ = 3.9 A, $V_{GS}$ = 10 V | N-Ch | | 3.7 | 15 | nC |
| | | | P-Ch | | 5 | 15 | |
| $Q_{gs}$ | Gate-Source Charge | $V_{DS}$ = -10 V, $I_D$ = -2.5 A, $V_{GS}$ = -10 V | N-Ch | | 0.9 | | nC |
| | | | P-Ch | | 1.7 | | |
| $Q_{gd}$ | Gate-Drain Charge | | N-Ch | | 1.9 | | nC |
| | | | P-Ch | | 1.8 | | |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | N-Ch | | | 1.7 | A |
| | | | P-Ch | | | -1.7 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.7 A (Note 2) | N-Ch | | 0.75 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = -1.7 A (Note 2) | P-Ch | | -0.75 | -1.2 | V |

**Notes:**

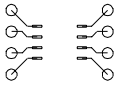
**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78° C/W when mounted on a 0.05 in² pad of 2 oz. copper.



b) 125° C/W when mounted on a 0.02 in² pad of 2 oz. copper.



c) 135° C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

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