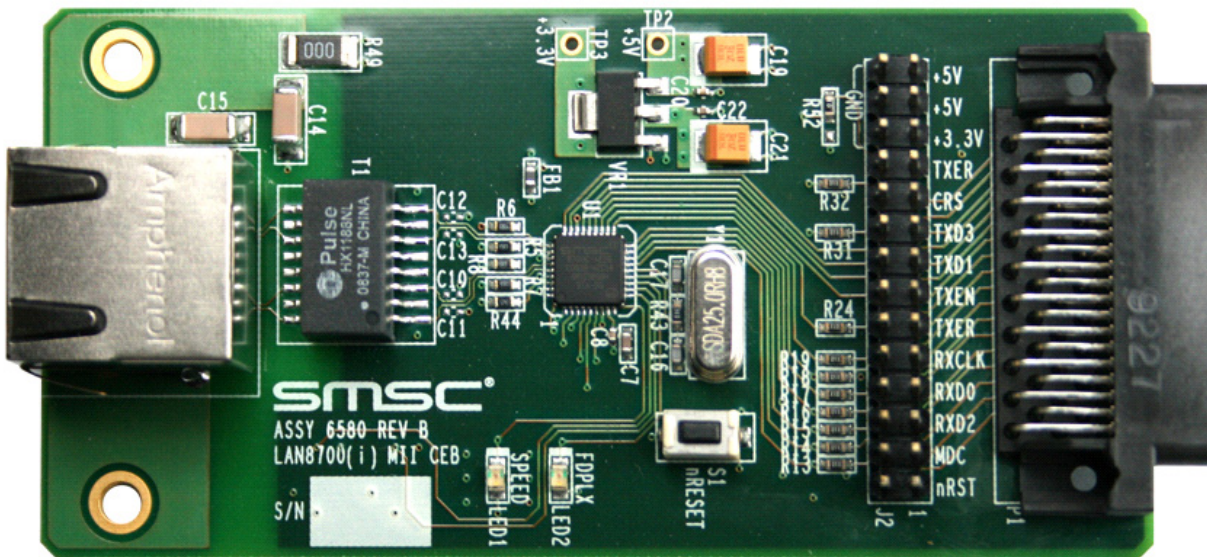


## EVB8700 Evaluation Board User Manual



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## 1 Introduction

The SMSC LAN8700 is a low-power, variable I/O voltage, analog interface IC with HP Auto-MDIX support for high-performance embedded Ethernet applications. The LAN8700 consists of an encoder/decoder, scrambler/descrambler, wave-shaping transmitter, output driver, twisted-pair receiver with adaptive equalizer and baseline wander (BLW) correction, and clock and data recovery functions.

The EVB8700 is an Evaluation Board (EVB) that interfaces a standard 40-pin female MII connector from an existing MAC controller to the SMSC LAN8700 Ethernet PHY, and out to an RJ45 Ethernet Jack for 10/100 connectivity.

A simplified block diagram of the EVB8700 can be seen in [Figure 1.1](#).

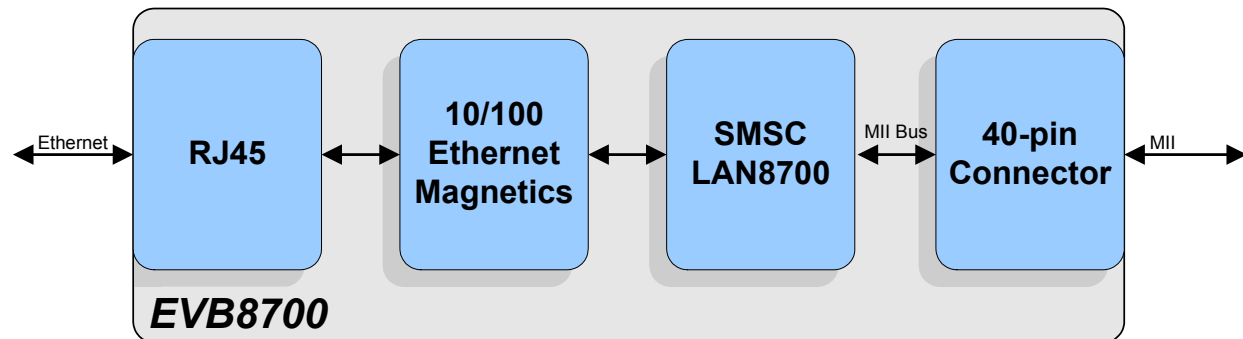


Figure 1.1 EVB8700 Block Diagram

### 1.1 References

Concepts and material available in the following documents may be helpful when using the EVB8700.

Table 1.1 References

DOCUMENT	LOCATION
SMSC LAN8700 Datasheet	<a href="http://www.smSC.com/lan8700">http://www.smSC.com/lan8700</a>
SMSC EVB8700 Evaluation Board Schematic	<a href="http://www.smSC.com/lan8700">http://www.smSC.com/lan8700</a>
AN16-12 LAN8700 User Application and Configuration Guide	<a href="http://www.smSC.com/lan8700">http://www.smSC.com/lan8700</a>
AN8-13 Suggested Magnetics	<a href="http://www.smSC.com/lan8700">http://www.smSC.com/lan8700</a>

## 2 Board Details

This section includes the following EVB8700 board details:

- Power
- Configuration
- Mechanicals

### 2.1 Power

Power is normally supplied to the EVB8700's +3.3V regulator externally via the +5V power pins of the MII connector. If desired, the EVB8700 can be powered without +5V present on the MII connector by supplying +5V to the TP2 test point with ground connected to pin 20 of header J2.

**Note:** Before connecting an external power supply to TP2, ensure power is not present on the MII connector's +5V pins. Connecting +5V simultaneously via the MII connector and TP2 may result in permanent damage to the board.

### 2.2 Configuration

The following sub-sections describe the various board features and configuration settings. A top view of the EVB8700 is shown in [Figure 2.1](#).

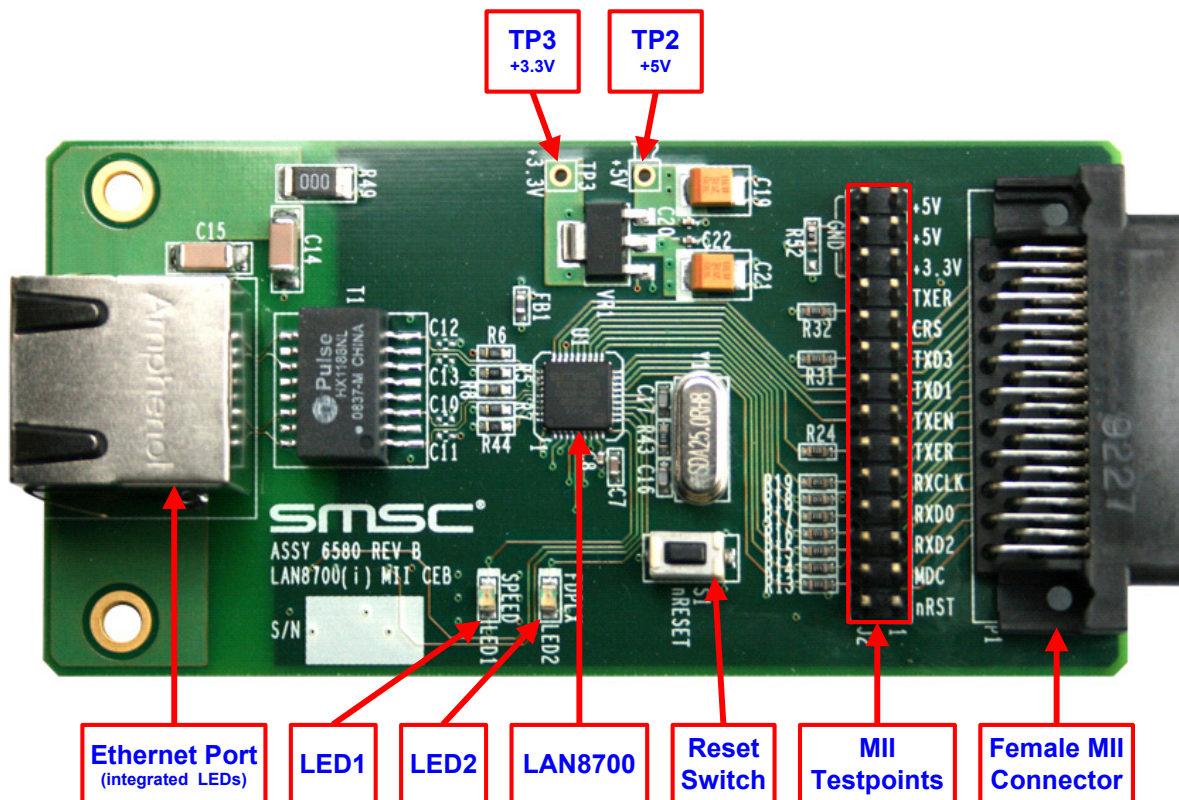


Figure 2.1 EVB8700 Top View

**Note:** Though the LAN8700 supports an RMI mode of operation and/or use of an external +1.8V regulator, the EVB8700 does not support these modes.

## 2.2.1 PHY Address and LED Configuration

The LAN8700 allows the user to configure the default PHY address at power-up via the PHYAD[4:0] configuration straps. Because these straps share functionality with device LEDs, care must be taken to properly configure these signals. [Table 2.1](#) details the proper configuration required for each PHY address value. By default, all EVB8700 PHY address straps are configured to a value of “1”.

**Note:** The PHYAD1 and PHYAD2 LEDs may function active-high or active-low depending on the boards PHY address configuration. Refer to [Table 2.1](#) and the LAN8700 Datasheet for additional information.

**Table 2.1 PHY Address Configuration Settings**

	“0”	“1” (DEFAULT)
<b>PHYAD4 (MSB)</b>	R11 populated	R11 unpopulated
<b>PHYAD3</b>	R46 unpopulated R48 populated R36 populated LED2 anode connected to FDUPLEX pin (flipped)	R46 populated R48 unpopulated R36 unpopulated LED2 cathode connected to FDUPLEX pin
<b>PHYAD2</b>	R2 populated in position 2-3 R1 populated in position 2-3 R35 populated <b>Note:</b> RJ45 Yellow LED will be active-high	R2 populated in position 1-2 R1 populated in position 1-2 R35 unpopulated <b>Note:</b> RJ45 Yellow LED will be active-low
<b>PHYAD1</b>	R3 populated in position 2-3 R4 populated in position 2-3 R34 populated <b>Note:</b> RJ45 Green LED will be active-high	R3 populated in position 1-2 R4 populated in position 1-2 R34 unpopulated <b>Note:</b> RJ45 Green LED will be active-low
<b>PHYAD0 (LSB)</b>	R45 unpopulated R47 populated R33 populated LED1 anode connected to SPEED100 pin (flipped)	R45 populated R47 unpopulated R33 unpopulated LED1 cathode connected to SPEED100 pin

LED reference designators and definitions are detailed in [Table 2.2](#).

**Table 2.2 LEDs**

REFERENCE	COLOR	INDICATION
J1	Green	Ethernet Link
	Yellow	Ethernet Activity
LED1	Green	Ethernet Speed
LED2	Green	Ethernet Full-Duplex

## 2.2.2 Boot Mode Configuration

The LAN8700 can be configured to boot into a specific mode of operation at power-up via the MODE[2:0] configuration straps. By default, the MODE[2:0] configuration straps are pulled-up internally to “1”. Unpopulated pull-down resistor pads are provided for each MODE[2:0] configuration strap. These pull-down resistors should only be populated when the corresponding MODE[2:0] configuration strap is desired to default to “0”. A list of the LAN8700 modes and their corresponding pull-down resistor configurations are shown in [Table 2.3](#).

**Table 2.3 MODE[2:0] Resistor Configuration**

MODE[2:0]	MODE DEFINITIONS	MODE[2:0] PULL-DOWN RESISTORS		
		R40 (MODE2)	R41 (MODE1)	R42 (MODE0)
000	10BASE-T Half Duplex Auto-negotiation disabled	Populated	Populated	Populated
001	10BASE-T Full Duplex Auto-negotiation disabled.	Populated	Populated	Unpopulated
010	100BASE-TX Half Duplex Auto-negotiation disabled CRS is active during Transmit & Receive	Populated	Unpopulated	Populated
011	100BASE-TX Full Duplex Auto-negotiation disabled CRS is active during Receive	Populated	Unpopulated	Unpopulated
100	100BASE-TX Half Duplex is advertised Auto-negotiation enabled. CRS is active during Transmit & Receive.	Unpopulated	Populated	Populated
101	Repeater mode ( <a href="#">Note 2.1</a> ) Auto-negotiation enabled 100BASE-TX Half Duplex is advertised CRS is active during receive	Unpopulated	Populated	Unpopulated
110	Power Down mode ( <a href="#">Note 2.2</a> )	Unpopulated	Unpopulated	Populated
111	All capable. Auto-negotiation enabled (Default)	Unpopulated	Unpopulated	Unpopulated

**Note 2.1** Refer to the LAN8700 Datasheet for additional information on Repeater mode.

**Note 2.2** Refer to the LAN8700 Datasheet for additional information on Power-Down mode.

### 2.2.3 nINT/TX\_ER/TXD4 Pin Configuration

The nINT, TX\_ER, and TXD4 functions share a common LAN8700 pin. This pin can operate in two functional modes: nINT (Interrupt) Mode and TX\_ER/TXD4 Mode. The RXD3/nINTSEL pin is used to select one of these two modes. The EVB8700 must be properly configured for each mode as follows:

#### nINT Mode (Default EVB8700 Mode)

- The nINTSEL configuration strap is pulled-up internally (by default) to select nINT mode. (R39 unpopulated)
- R52 must be in the 1-2 position, which routes nINT to pin 21 of the J2 MII header

#### TX\_ER/TXD4 Mode

- The nINTSEL configuration strap is pulled-down to select TX\_ER/TXD4 mode. (R39 populated)
- R52 must be in the 2-3 position, which routes TX\_ER/TXD4 to pin 11 of the J2 MII header

For additional information on the functionality of the nINT/TX\_ER/TXD4 pin, refer to the LAN8700 Datasheet and EVB8700 schematics.

### 2.2.4 Test Points

**Table 2.4 Test Points**

TEST POINT	DESCRIPTION	CONNECTION
TP2	+5V Test Point (Unpopulated) ( <a href="#">Note 2.3</a> )	+5V
TP3	+3.3V Test Point (Unpopulated)	+3.3V

**Note 2.3** Test point TP2 can be used as an alternative source of +5V to the EVB8700. Refer to [Section 2.1, "Power," on page 3](#) for additional information.

### 2.2.5 System Connections

**Table 2.5 System Connections**

PLUG/HEADER	DESCRIPTION	PART
J1	RJ45 with Integrated LEDs	Amphenol RJSBE5381C1
J2	2x14 MII Header <b>Note:</b> Refer <a href="#">Table 2.6</a> to for a full pin list	Adam Tech PH2-28-U-A
P1	40-pin Female MII Connector <b>Note:</b> This connector follows the standardized MII pinout. Refer to the EVB8700 schematic for additional information. ( <a href="#">Note 2.4</a> )	Tyco 5173278-2

Table 2.6 J2 - 2x14 MII Header Pinout

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	Ground	15	TXD1
2	MDIO ( <a href="#">Note 2.4</a> )	16	TXD2
3	MDC	17	TXD3
4	RXD3/nINTSEL	18	COL/MII/CRS_DV
5	RXD2/MODE2	19	CRS/PHYAD4
6	RXD1/MODE1	20	Ground
7	RXD0/MODE0	21	nINT ( <a href="#">Note 2.5</a> )
8	RX_DV	22	+3.3V
9	RX_CLK/REGOFF	23	+3.3V
10	RX_ER/RXD4	24	Ground
11	TX_ER/TXD4 ( <a href="#">Note 2.5</a> )	25	+5V
12	TX_CLK	26	Ground
13	TX_EN	27	+5V
14	TXD0	28	Ground

**Note 2.4** Resistor R12 acts as a pull-up on the MDIO pin. In most situations, the MAC circuitry provides this pull-up and R12 is not required.

**Note 2.5** Pins 11 and 21 of the J2 header both connect to resistor R52. This resistor must be positioned correctly in order to divert the nINT/TX\_ER/TXD4 pin of the LAN8700 to the correct J2 location, as determined by the nINTSEL configuration strap value. Refer to [Section 2.2.3, "nINT/TX\\_ER/TXD4 Pin Configuration,"](#) on page 6 for additional information.

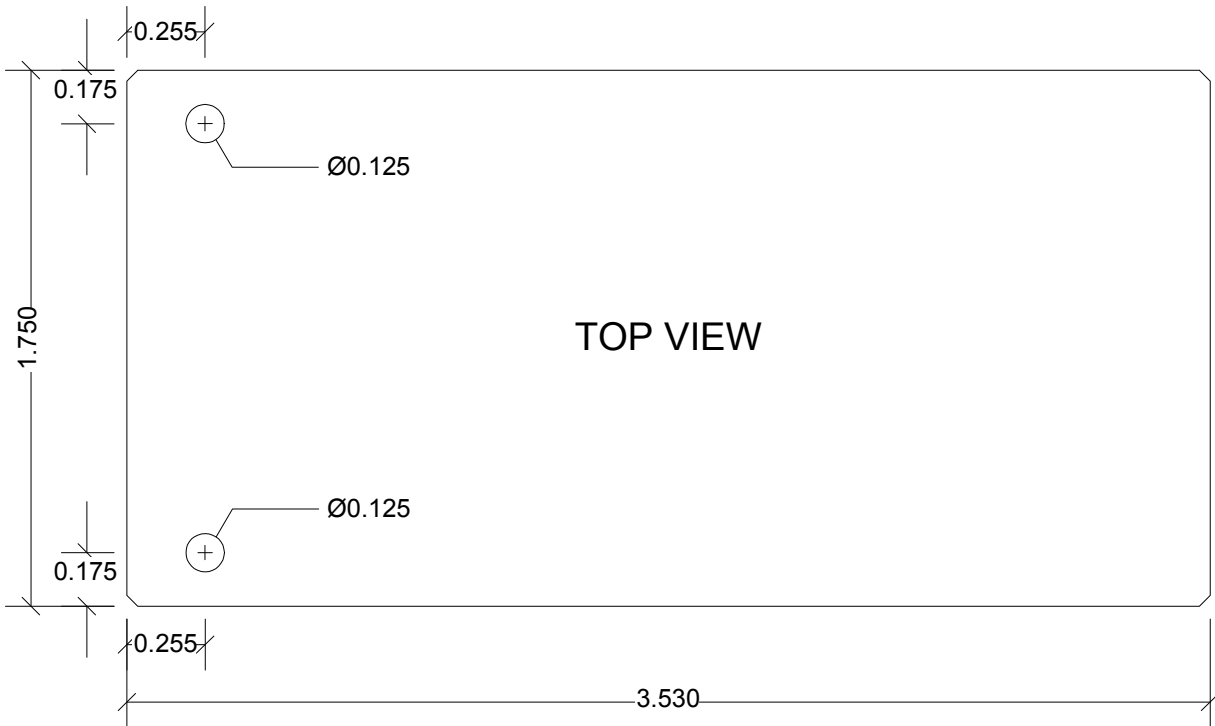
## 2.2.6 Switches

Table 2.7 Switches

SWITCH	DESCRIPTION	FUNCTION
S1	Reset switch	When pressed, triggers a board reset

## 2.3 Mechanicals

Figure 2.2 details the EVB8700 mechanical dimensions.



**Figure 2.2 EVB8700 Mechanicals**



### 3 User Manual Revision History

Table 3.1 Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 (02-23-10)	Initial Release	