

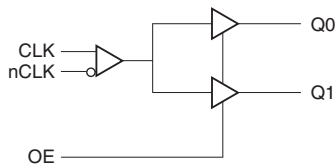
GENERAL DESCRIPTION

The 83026I-01 is a low skew, 1-to-2 Differential-to-LVCMOS/LVTTL Fanout Buffer. The differential input can accept most differential signal types (LVPECL, LVDS, LVHSTL, HCSL and SSTL) and translate to two single-ended LVCMOS/LVTTL outputs. The small 8-lead SOIC footprint makes this device ideal for use in applications with limited board space.

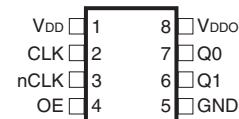
FEATURES

- Two LVCMOS / LVTTL outputs
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 350MHz
- Output skew: 15ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Additive phase jitter, RMS: 0.03ps (typical)
- Small 8 lead SOIC package saves board space
- 3.3V core, 3.3V, 2.5V or 1.8V output operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS (6) package

BLOCK DIAGRAM

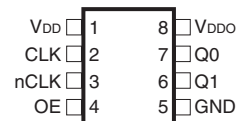


PIN ASSIGNMENT



83026I-01 8-Lead SOIC

3.8mm x 4.8mm, x 1.47mm package body
M Package
Top View



83026I-01 8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|------------------|--------|---------------------|---|
| 1 | V _{DD} | Power | | Positive supply pin. |
| 2 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 3 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. V _{DD} /2 default when left floating. |
| 4 | OE | Input | Pullup | Output enable. When HIGH, outputs are enabled. When LOW, outputs are in High Impedance State. LVCMOS / LVTTTL interface levels. |
| 5 | GND | Power | | Power supply ground. |
| 6 | Q1 | Output | | Clock output. LVCMOS / LVTTTL interface levels. |
| 7 | Q0 | Output | | Clock output. LVCMOS / LVTTTL interface levels. |
| 8 | V _{DDO} | Power | | Output supply pin. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--|---|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| C _{PD} | Power Dissipation Capacitance (per output) | V _{DD} , V _{DDO} = 3.465V | | | 17 | pF |
| | | V _{DD} = 3.465V, V _{DDO} = 2.625V | | | 16 | pF |
| | | V _{DD} = 3.465V, V _{DDO} = 1.95V | | | 15 | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{OUT} | Output Impedance | V _{DD} , V _{DDO} = 3.3V | | 7 | | Ω |
| | | V _{DD} = 3.3V, V _{DDO} = 2.5V | | 8 | | Ω |
| | | V _{DD} = 3.3V, V _{DDO} = 1.8V | | 10 | | Ω |

TABLE 3. CONTROL FUNCTION TABLE

| Input | Outputs |
|-------|---------|
| OE | Q0, Q1 |
| 0 | HiZ |
| 1 | Active |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | |
| 8 Lead SOIC | 112.7°C/W (0 lfpm) |
| 8 Lead TSSOP | 101.7°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.71V$ TO $3.465V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| | | | 2.375 | 2.5 | 2.625 | V |
| | | | 1.71 | 1.8 | 1.89 | V |
| I_{DD} | Power Supply Current | | | 10 | mA | |
| I_{DDO} | Output Supply Current | | | 3 | mA | |

TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.375V$ TO $3.465V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------------------|-----------------|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | OE | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | OE | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | OE | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| I_{IL} | Input Low Current | OE | $V_{DD} = 3.465V, V_{IN} = 0V$ | | | μA |
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{DDO} = 3.135V$ | | 2.6 | V |
| | | | $V_{DDO} = 2.375V$ | | 1.8 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | | | 0.5 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information section, "Output Load Test Circuit" diagrams.

TABLE 3C. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|-----------------|--------------------------------|---------|------------------|---------|
| V_{IH} | Input High Voltage | OE | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | OE | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | OE | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| I_{IL} | Input Low Current | OE | $V_{DD} = 3.465V, V_{IN} = 0V$ | | -150 | μA |
| V_{OH} | Output High Voltage | | $I_{OH} = -100\mu A$ | | $V_{DDO} - 0.2$ | V |
| | | | $I_{OH} = -2mA$ | | $V_{DDO} - 0.45$ | V |
| V_{OL} | Output Low Voltage | | $I_{OL} = 100\mu A$ | | 0.2 | V |
| | | | $I_{OL} = 2mA$ | | 0.45 | V |

TABLE 3D. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.71V$ TO $3.465V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|-----------------|--------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | nCLK | $V_{IN} = V_{DD} = 3.465V$ | | 150 | μA |
| | | CLK | $V_{IN} = V_{DD} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | nCLK | $V_{IN} = 0V, V_{DD} = 3.465V$ | -150 | | μA |
| | | CLK | $V_{IN} = 0V, V_{DD} = 3.465V$ | -5 | | μA |
| V_{PP} | Peak-to-Peak Input Voltage; NOTE 1 | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 2, 3 | | GND + 0.5 | | $V_{DD} - 0.85$ | V |

NOTE 1: V_{PP} can exceed 1.3V provided that there is sufficient offset level to keep $V_{IL} > 0V$.

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{DD} + 0.3V$.

NOTE 3: Common mode voltage is defined as V_{IH} .

TABLE 4A. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---|-----------------------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 350 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | $f \leq 350MHz$ | 1.3 | 1.9 | 2.5 | ns |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | | 15 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | | 900 | ps |
| t_{jit} | Buffer Additive Phase Jitter, RMS, refer to Additive Phase Jitter Section | | | 0.03 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 150 | | 800 | ps |
| odc | Output Duty Cycle | $f \leq 66MHz$ | 48 | | 52 | % |
| | | $67MHz \leq f \leq 166MHz$ | 45 | | 55 | % |
| | | $167MHz \leq f \leq 350MHz$ | 40 | | 60 | % |

NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 6.

TABLE 4B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|---|-----------------------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 350 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | $f \leq 350MHz$ | 1.5 | 2.0 | 2.6 | ns |
| $tsk(o)$ | Output Skew; NOTE 2, 4 | | | | 15 | ps |
| $tsk(pp)$ | Part-to-Part Skew; NOTE 3, 4 | | | | 750 | ps |
| t_{jit} | Buffer Additive Phase Jitter, RMS, refer to Additive Phase Jitter Section | | | 0.03 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 150 | | 800 | ps |
| odc | Output Duty Cycle | $f \leq 66MHz$ | 48 | | 52 | % |
| | | $67MHz \leq f \leq 166MHz$ | 46 | | 54 | % |
| | | $167MHz \leq f \leq 350MHz$ | 40 | | 60 | % |

NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4C. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 5\%$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|---|-----------------------------|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 350 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | $f \leq 350MHz$ | 1.9 | 2.5 | 3.1 | ns |
| $tsk(o)$ | Output Skew; NOTE 2, 4 | | | | 15 | ps |
| $tsk(pp)$ | Part-to-Part Skew; NOTE 3, 4 | | | | 600 | ps |
| t_{jit} | Buffer Additive Phase Jitter, RMS, refer to Additive Phase Jitter Section | | | 0.03 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 900 | ps |
| odc | Output Duty Cycle | $f \leq 66MHz$ | 48 | | 52 | % |
| | | $67MHz \leq f \leq 166MHz$ | 43 | | 57 | % |
| | | $167MHz \leq f \leq 350MHz$ | 40 | | 60 | % |

NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at $V_{DDO}/2$.

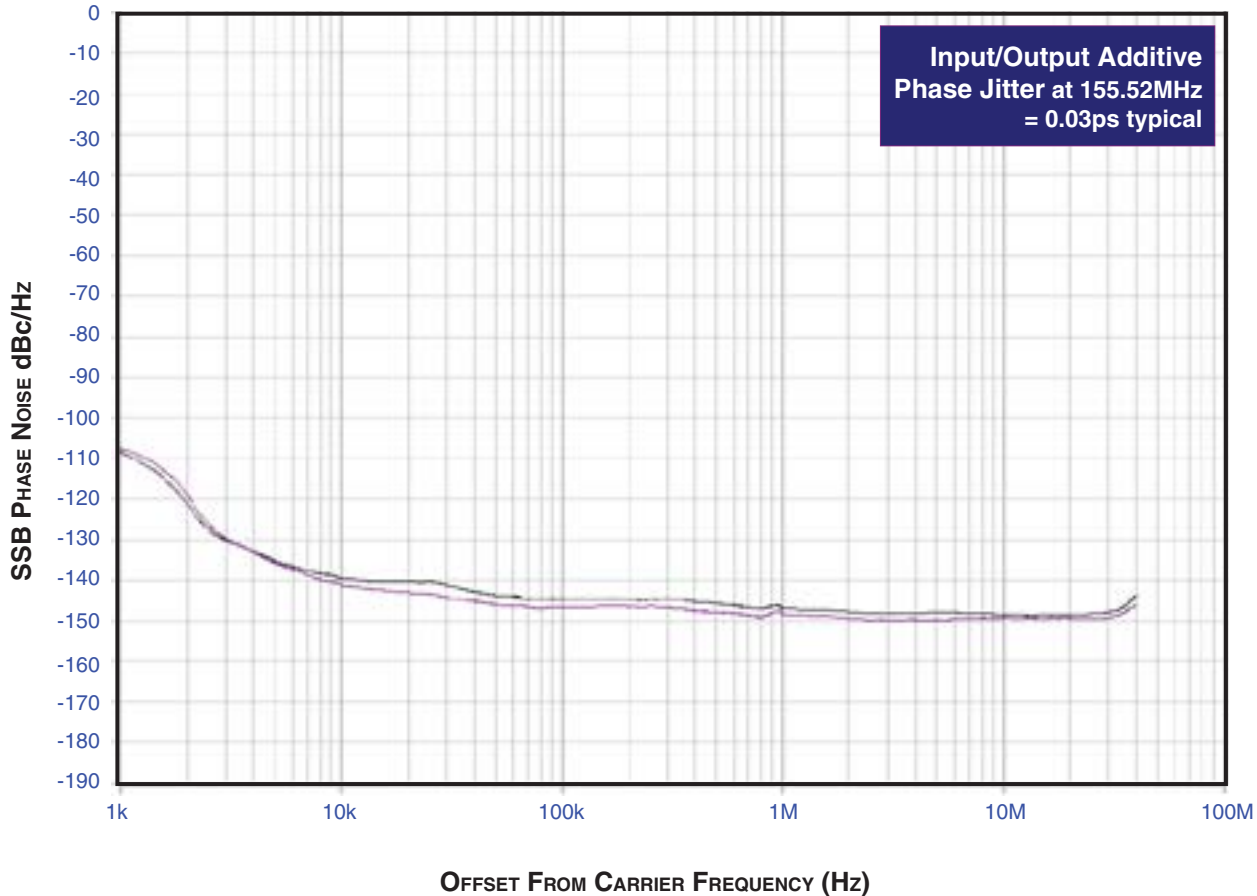
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the

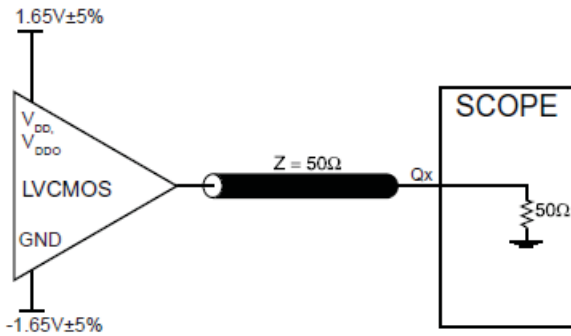
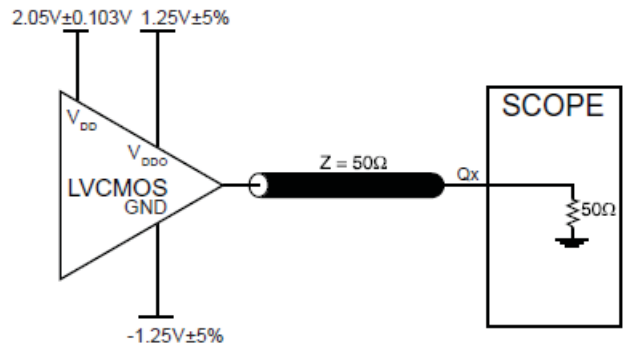
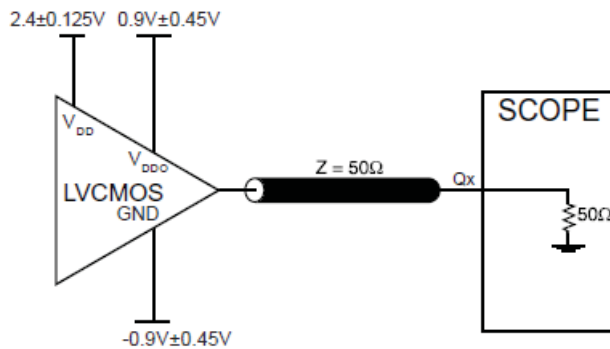
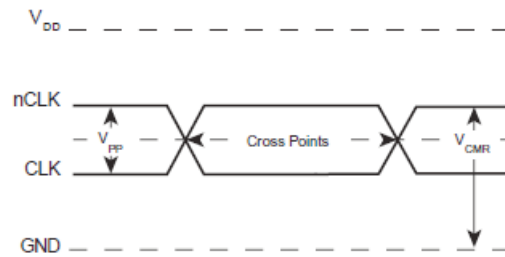
1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The

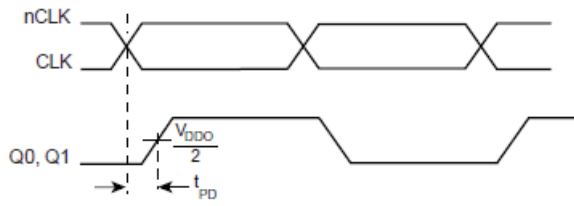
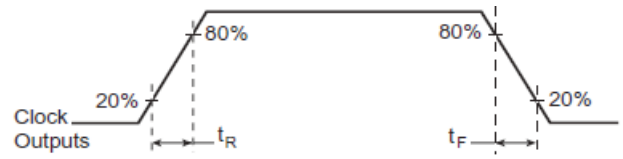
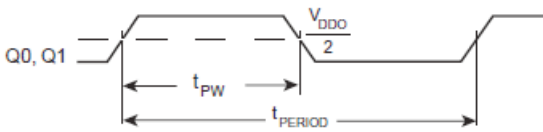
device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

PARAMETER MEASUREMENT INFORMATION


3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT

DIFFERENTIAL INPUT LEVEL

OUTPUT SKEW

PART-TO-PART SKEW


PROPAGATION DELAY

OUTPUT RISE/FALL TIME


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

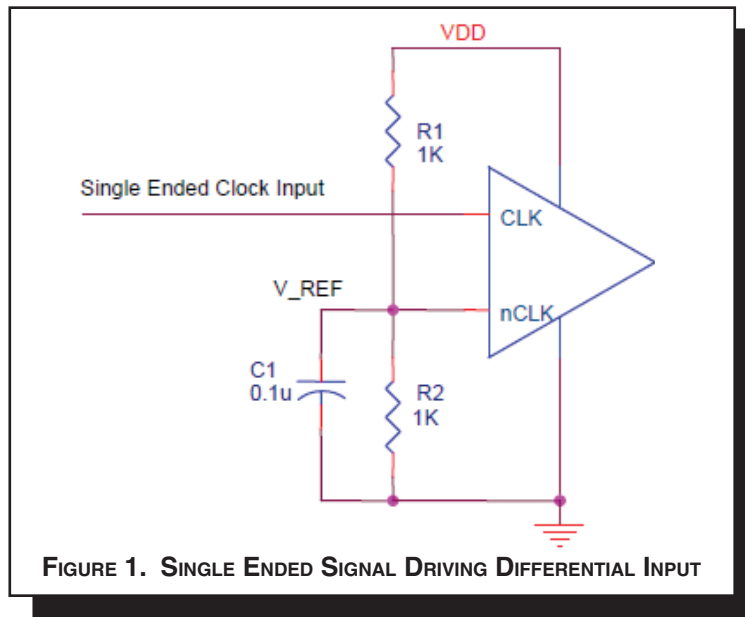
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.



RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVC MOS OUTPUTS

All unused LVC MOS output can be left floating. We recommend that there is no trace attached.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are

examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A*, the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

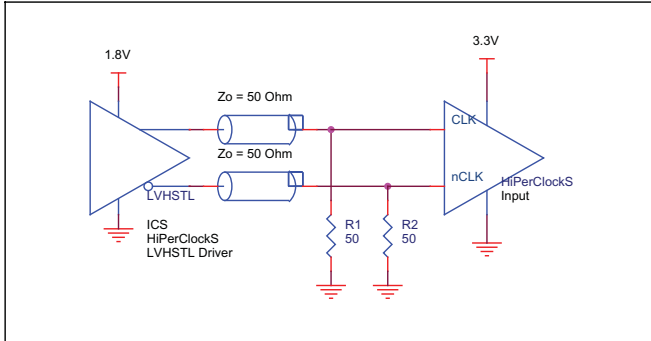


FIGURE 2A. CLK/nCLK INPUT DRIVEN BY LVHSTL DRIVER

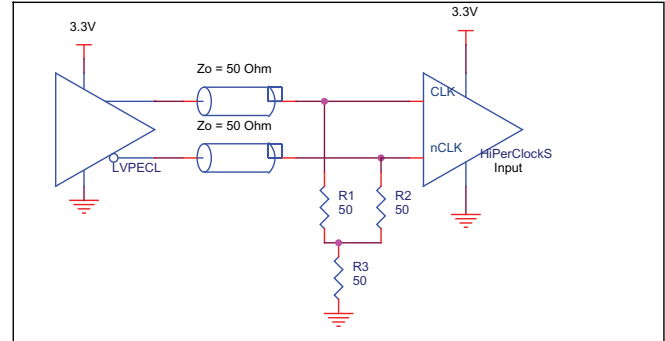


FIGURE 2B. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

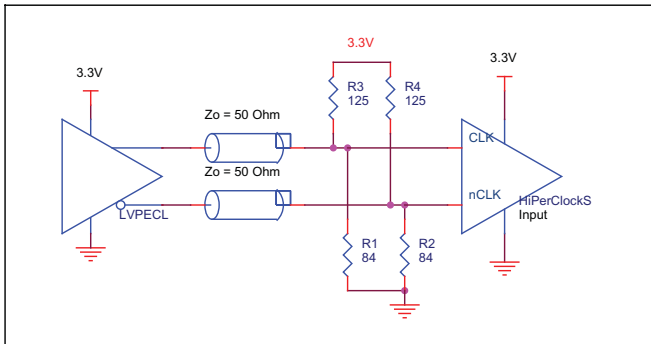


FIGURE 2C. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

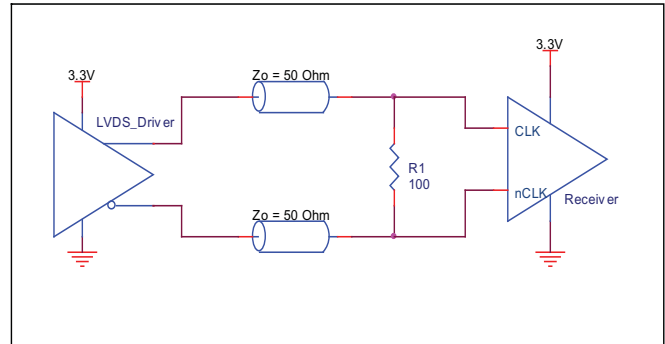


FIGURE 2D. CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

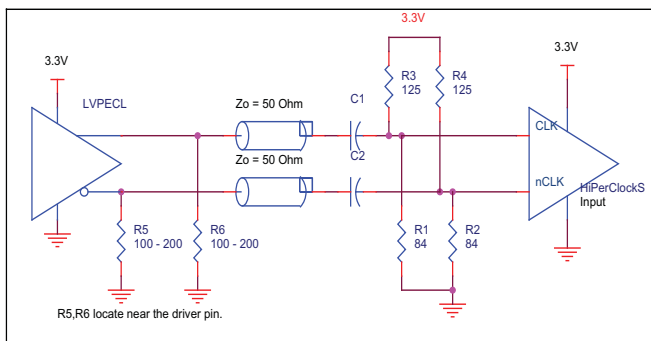


FIGURE 2E. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

SCHEMATIC EXAMPLE

Figure 3 shows an application schematic example of 830261-01. The 830261-01 CLK/nCLK input can directly accept various types of differential signal. In this example, the input is driven by an LVDS driver. The 830261-01 outputs are LVC MOS drivers. In

this example, series termination approach is shown. Additional termination approaches are shown in the LVC MOS Termination Application Note.

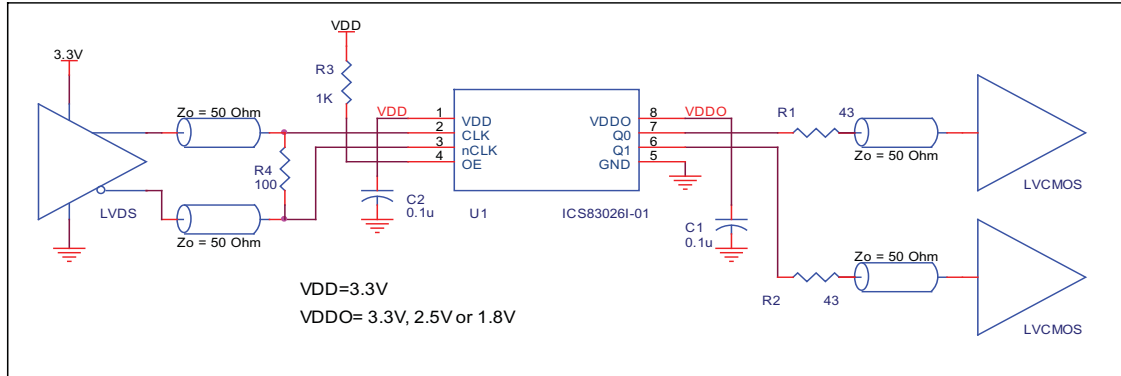


FIGURE 3. 830261-01 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 5A. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|-----------|-----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

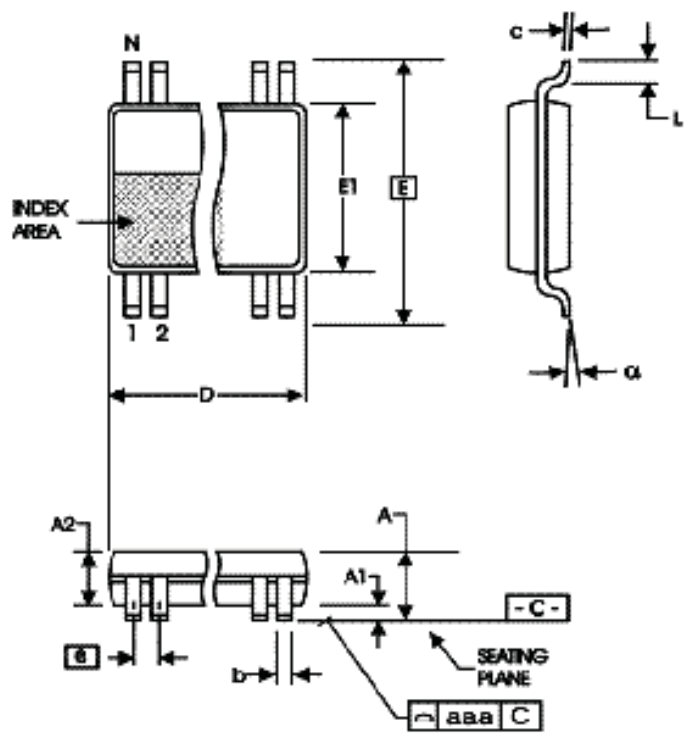
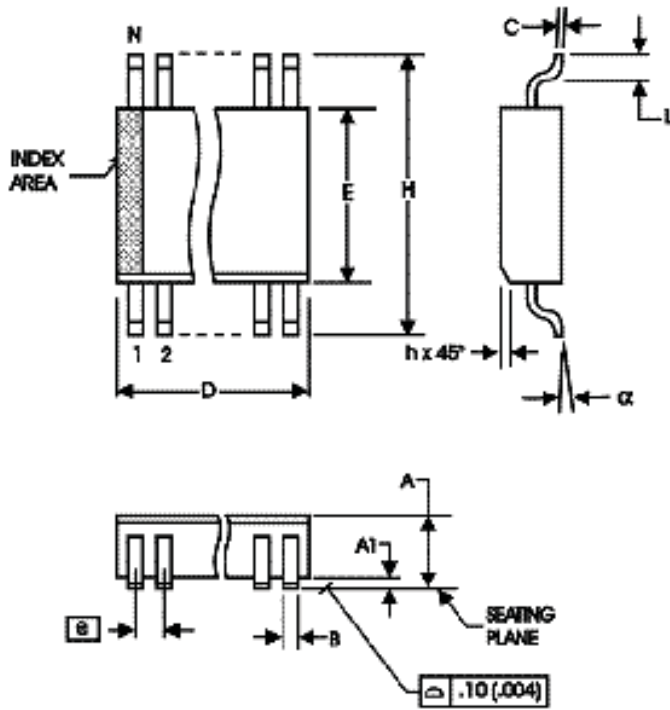
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 5B. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|----------|----------|
| | 0 | 200 | 500 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

TRANSISTOR COUNT

The transistor count for ICS830261-01 is: 260

PACKAGE OUTLINE - SUFFIX M FOR 8 LEAD SOIC
PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

TABLE 6A. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | MINIMUM | MAXIMUM |
| N | 8 | |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BASIC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-012

TABLE 6B. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 8 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------|--------------------------|--------------------|----------------|
| 83026BMI-01LF | 026BI01L | 8 lead "Lead Free" SOIC | Tube | -40°C to +85°C |
| 83026BMI-01LFT | 026BI01L | 8 lead "Lead Free" SOIC | Tape and Reel | -40°C to +85°C |
| 83026BGI-01LF | BI01L | 8 lead "Lead Free" TSSOP | Tube | -40°C to +85°C |
| 83026BGI-01LFT | BI01L | 8 lead "Lead Free" TSSOP | Tape and Reel | -40°C to +85°C |

| REVISION HISTORY SHEET | | | | |
|------------------------|-------|------|---|----------|
| Rev | Table | Page | Description of Change | Date |
| A | T7 | 1 | Added 8 Lead TSSOP package to Pin Assignment. | 6/25/04 |
| | | 3 | Absolute Maximum Ratings - added 8 Lead TSSOP to Package Thermal Impedance. | |
| | | 11 | Added 8 Lead TSSOP Reliability Information table. | |
| | | 12 | Added 8 Lead TSSOP Package Outline and Package Dimensions. | |
| | | 13 | Ordering Information Table - added 8 Lead TSSOP ordering information. | |
| A | | 6 | Additive Phase Jitter - corrected X axis on plot. | 8/2/05 |
| A | T3C | 3 | LVC MOS DC Characteristics - corrected Test Conditions for IIH and IIL. | 8/12/05 |
| A | T7 | 1 | Features Section - added lead-free bullet | 1/16/06 |
| | | 9 | Added Recommendations for Unused Output Pins. | |
| | | 13 | Ordering Information Table - added lead-free part number, marking, and note. | |
| A | T7 | 13 | Ordering Information Table - added lead-free marking | 10/22/07 |
| A | T7 | 13 | Updated datasheet's header/footer with IDT from ICS. | 8/4/10 |
| | | 15 | Removed ICS prefix from Part/Order Number column. Added Contact Page. | |
| A | T7 | 1 | Removed the ICS prefix on part numbers. | 12/15/15 |
| | | 13 | Features Section - removed reference to leaded packages. Ordering Information - removed 2500 from Tape and Reel. Removed LF note below the table. Updated datasheet header and footer | |



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