# ML628
# Virtex-6 FPGA
# GTX and GTH Transceiver
# Characterization Board
## *User Guide*

**UG771 (v1.0.1) July 6, 2011**

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# Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 03/23/11 | 1.0 | Initial Xilinx release. |
| 07/06/11 | 1.0.1 | Revised link in Appendix D, on page 71 to point to the version of UG806 supporting ISE software version 13.2. |

# *Table of Contents*

# About This Guide

This document describes the basic setup, features, and operation of the ML628 Virtex®-6 FPGA GTX and GTH transceiver characterization board. The ML628 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex-6 XC6VHX380T-2C FFG1923 FPGA. The latest revision of this document is available online at:

http://www.xilinx.com/products/boards/ml628/reference_designs.htm

## Guide Contents

This user guide contains the following chapters and appendices:

- Chapter 1, ML628 Board Features and Operation, describes the components, features, and operation of the ML628 Virtex-6 FPGA GTX and GTH transceiver characterization board.
- Appendix A, Default Jumper Positions, lists the jumpers that must be installed on the board for proper operation.
- Appendix B, VITA 57.1 FMC HPC Connector Pinout, provides a pinout reference for the FPGA mezzanine card (FMC) connector.
- Appendix C, ML628 Master UCF Listing, provides a listing of the ML628 master user constraints file (UCF).
- Appendix D, References, provides a list of references and links to related documentation.

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

## Conventions

This document uses the following conventions. An example illustrates each convention.

### Typographical

The following typographical conventions are used in this document:

| Convention | Meaning or Use | Example |
|---|---|---|
| `Courier font` | Messages, prompts, and program files that the system displays | `speed grade: - 100` |
| **`Courier bold`** | Literal commands that you enter in a syntactical statement | **`ngdbuild`** *design_name* |
| **Helvetica bold** | Commands that you select from a menu | **File → Open** |
| | Keyboard shortcuts | **Ctrl+C** |
| *Italic font* | Variables in a syntax statement for which you must supply values | **`ngdbuild`** *design_name* |
| | References to other manuals | See the *Command Line Tools User Guide* for more information. |
| | Emphasis in text | If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected. |

## Online Document

The following conventions are used in this document:

| Convention | Meaning or Use | Example |
|---|---|---|
| Blue text | Cross-reference link to a location in the current document | See the section "Additional Resources" for details.<br>Refer to "Title Formats" in Chapter 1 for details. |
| Blue, underlined text | Hyperlink to a website (URL) | Go to http://www.xilinx.com for the latest speed files. |

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Chapter 1

# ML628 Board Features and Operation

This chapter describes the components, features, and operation of the ML628 Virtex®-6 FPGA GTX and GTH transceiver characterization board. The ML628 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex-6 XC6VHX380T-2C FFG1923 FPGA. ML628 schematics, bill-of-material (BOM), layout files and reference designs are available online at:

http://www.xilinx.com/products/boards/ml628/reference_designs.htm

## ML628 Board Features

- Virtex-6 XC6VHX380T-2C FFG1923 FPGA
- On-board power supplies for all necessary voltages
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Platform Cable USB or Parallel Cable III/IV cables
- System ACE™ controller
- Separate power modules supporting all Virtex-6 FPGA GTX and GTH transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to global clock inputs
- Two single-ended global clock inputs with SMA connectors
- Two pairs of differential global clock inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Six Samtec BullsEye connector pads for the GTH transceivers and reference clocks
- Ten Samtec BullsEye connector pads for the GTX transceivers and reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Two VITA 57.1 FMC HPC connectors
- USB to UART bridge
- $I^2C$ bus
- PMBus connectivity to on-board digital power supplies
- Active cooling for the FPGA

The ML628 board block diagram is shown in Figure 1-1.

***Caution!*** The ML628 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

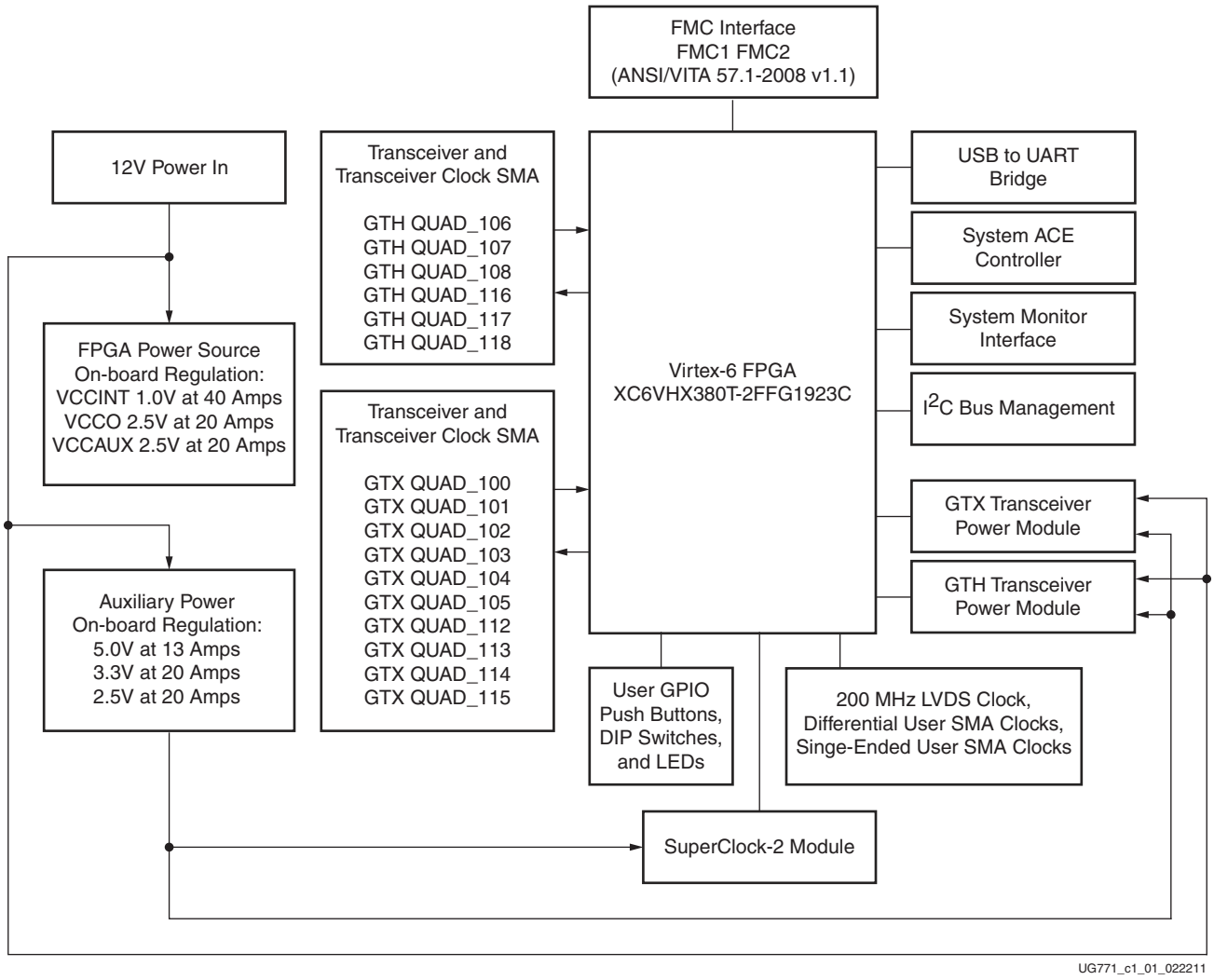
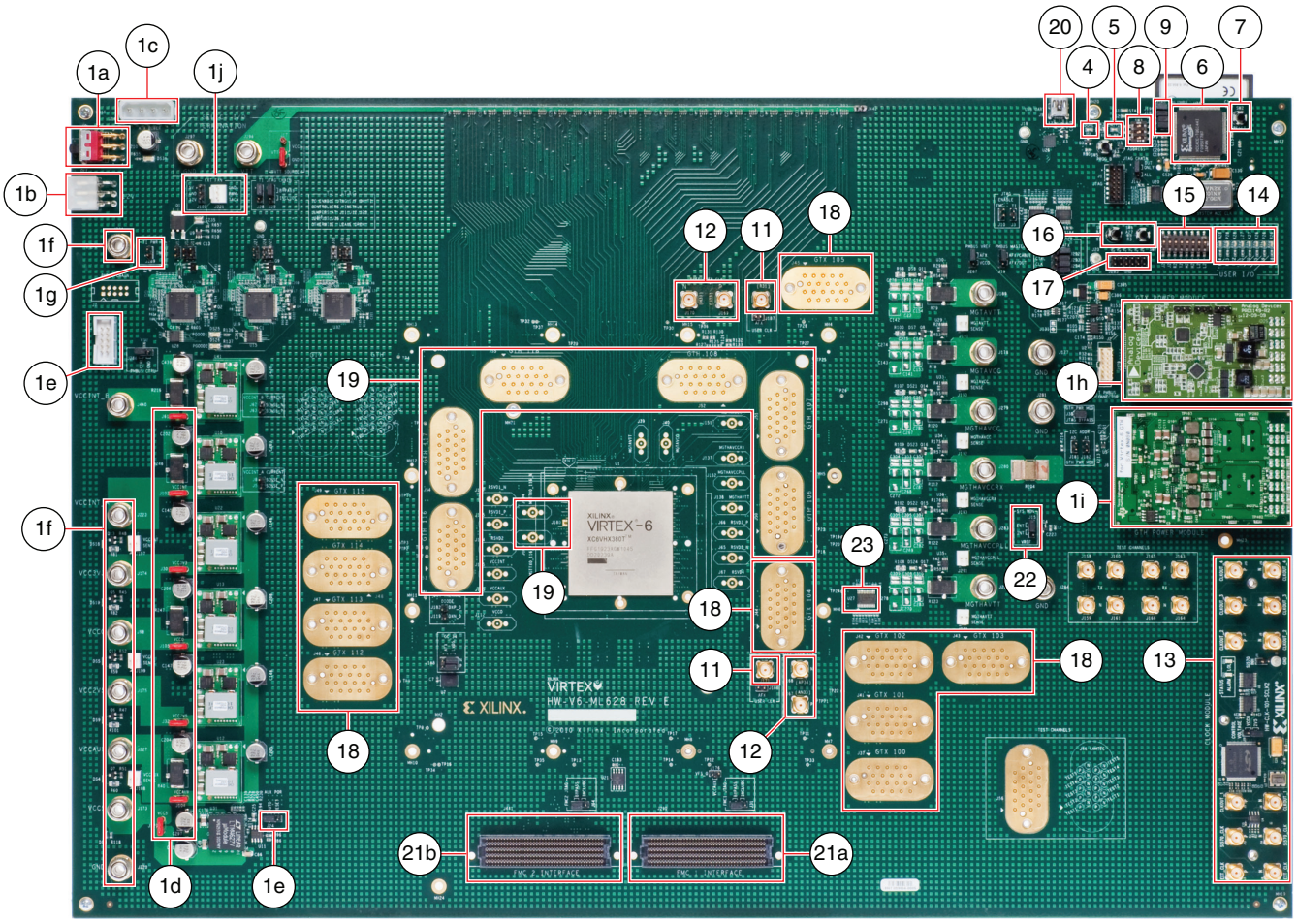



*Figure 1-1:* **ML628 Board Block Diagram**

# Detailed Description

Figure 1-2 shows the ML628 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

***Note:*** Figure 1-2 is for reference only and might not reflect the current revision of the board.




1a Main power switch (SW1)
1b 12V Mini-Fit connector (J122)
1c 12V ATX connector (J141)
1d Power regulation jumpers (J30, J32, J61, J102, J104, J105, J129)
1e Regulation inhibit (J289)
1f External power supply jacks
1g TI PMBus connector (J14)
1h GTX transceiver power supply module
1i GTH transceiver power supply module
1j Active cooling power connector (J221)
2 FPGA configuration connector (J1)
3 PROG_B push button, active Low (SW5)
4 DONE LED (DS6)
5 INIT LED (DS20)
6 System ACE controller (U25)
7 System ACE reset, active Low (SW2)
8 Configuration address DIP switch (SW3)
9 JTAG isolation jumpers (J22, J23, J195, J196)
10 200 MHz 2.5V LVDS oscillator (U7)
11 Single-ended SMA global clock input (J171, J172)
12 Differential SMA global clock inputs (J167 - J170)
13 SuperClock-2 module
14 User LEDs, active High (DS10 - DS17)
15 User DIP switches, active High (SW7)
16 User push buttons, active High (SW4, SW6)
17 User test I/O (J285)
18 GTX transceiver Connector Pad
19 GTH transceiver Connector Pad
20 USB to UART bridge (J9 and U26)
21a FMC1 connector (J290)
21b FMC2 connector (J441)
22 System Monitor
23 $I^2C$ bus management (U27)

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*Figure 1-2:* **ML628 Board Features**

## Power Management

Numbers 1a through 1j refer to the callouts in Figure 1-2:

1a: Main power switch (SW1)

1b: 12V Mini-Fit connector (J122)

1c: 12V ATX connector (J141)

1d: Power regulation jumpers (J30, J32, J61, J102, J104, J105, J129)

1e: Regulation inhibit (J289)

1f: External power supply jacks (J234, J440, J223, J174, J98, J175, J227, J173, J220)

1g: TI PMBus cable connector (J14)

1h: GTX transceiver power supply module

1i: GTH transceiver power supply module

1j: Active heatsink power connector

### Board Power and Switch

The ML628 board is powered through J122 using the 12V AC adapter included with the board. J122 is a 6-pin (2 x 3) right angle Mini-Fit type connector.

***Caution!*** Do ***NOT*** plug a PC ATX power supply 6-pin connector into J122 on the ML628 board. The ATX 6-pin connector has a different pinout than J122. Connecting an ATX 6-pin connector into J122 will damage the ML628 board and void the board warranty.

Power can also be provided through:

- Connector J141 which accepts an ATX hard disk 4-pin power plug
- Jack J234 which can be used to connect to a bench-top power supply

  ***Caution!*** Do ***NOT*** apply power to J122 and connectors J141 and/or J234 at the same time. Doing so will damage the ML628 board.

The ML628 board power is turned on or off by switch SW1. When the switch is in the ON position, power is applied to the board and a green LED (DS36) illuminates.

## Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

***Note:*** Power regulation jumpers are not shown in Figure 1-3.

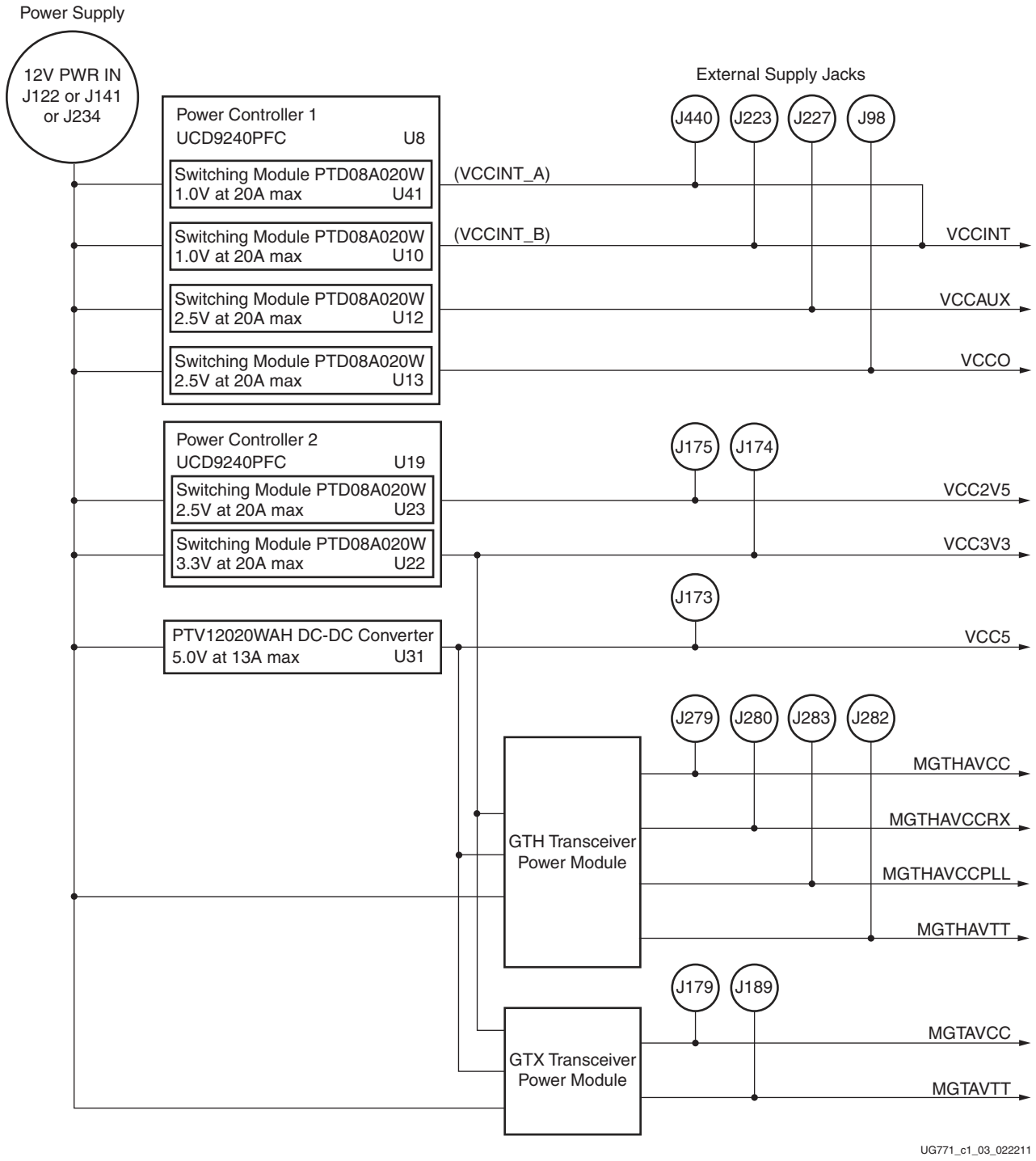


*Figure 1-3:* **ML628 Board Power Supply Block Diagram**

The ML628 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and auxiliary voltages listed in Table 1-1. The board can also be configured to use external bench power supply for each voltage. See Using External Power Sources.

*Table 1-1:* **Onboard Power System Devices**

| Device | Reference Designator | Description | Power Rail Net Name | Typical Voltage | Power Regulation Jumper | External Supply Jack |
|---|---|---|---|---|---|---|
| **Core voltage controller and regulators** | | | | | | |
| UCD9240PFC | U8 | PMBus compliant digital PWM system controller (address = 52) | | | | |
| PTD08A020W | U10 | Adjustable switching regulator 20A, 0.6V to 3.6V | VCCINT[1] | 1.0V | J102 | J223 |
| PTD08A020W | U41 | Adjustable switching regulator 20A, 0.6V to 3.6V | VCCINT (VCCINT_B) | 1.0V | J61 | J440 |
| PTD08A020W | U12 | Adjustable switching regulator 20A, 0.6Vto 3.6V | VCCAUX | 2.5V | J104 | J227 |
| PTD08A020W | U13 | Adjustable switching regulator 20A, 0.6V to 3.6V | VCCO | 2.5V | J105 | J98 |
| **Auxiliary voltage controller and regulators** | | | | | | |
| UCD9240PFC | U19 | PMBus compliant digital PWM system controller (address = 53) | | | | |
| PTD08A020W | U23 | Adjustable switching regulator 20A, 0.6V to 3.6V | VCC2V5 | 2.5V | J31 | J175 |
| PTD08A020W | U22 | Adjustable switching regulator 20A, 0.6V to 3.6V | VCC3V3 | 3.3V | J30 | J174 |
| **5V auxiliary power** | | | | | | |
| PTV12020WAH | U31 | Switching regulator 13A, 5.0V | VCC5 | 5.0V | J129 | J173 |

**Notes:**

1. The UCD9240PCF (U8) synchronizes the PTD power stages (U10 and U41) so that a maximum of 40A can be supplied to the VCCINT rail

## Using External Power Sources

The maximum output current rating for each power regulator is listed in Table 1-1. If a design exceeds this value on any power rail, power for that rail must be supplied through the external power jack using a supply capable of providing the required current.

Each power rail has a corresponding jack and jumper that is used to supply voltage to the rail using an external power supply. The jack, jumper, and regulator for each power rail is listed in Table 1-1.

> ***Caution!*** The power regulation jumper (see Power Regulation Jumper column inTable 1-1) must be removed before applying external power to the power rail through its corresponding supply jack.
>
> ***Caution!*** The external power supply jacks have a maximum current rating of 15A.

### Disabling Onboard Power

Voltage regulators U10, U12, U13, U22, U23, and U41 are disabled by installing a jumper at J289 (TI PWR INHIBIT). Voltage regulator U31 is disabled by installing a jumper across pins 2–3 of header J24 (AUX POR - RESET).

### Default Jumper Positions

A list of shunts and shorting plugs and their required positions for normal board operation is provided in Appendix A, Default Jumper Positions.

### Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The three onboard TI power controllers (U8 at PMBUS address 52, U19 at PMBUS address 53, and U32 at PMBUS address 54) are wired to the same PMBus. The PMBus connector, J14, is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

### References

More information about the power system components used by the ML628 board are available from the Texas Instruments digital power website at:

http://www.ti.com/ww/en/analog/digital-power/index.html

## GTH Transceiver Power Module

The GTH transceiver power module supplies MGTHAVCC, MGTHAVCCRX, MGTHAVTT and MGTHAVCCPLL voltages to the FPGA GTH transceivers. Two GTH power modules are provided with the ML628 board for evaluation. Either of the modules can be plugged into the connectors J6 and J197 in the outlined and labeled power module location shown in Figure 1-4.

***Note:*** The GTH and GTX power modules have different connectors and form factors to prevent GTH modules from being connected to the GTX headers and vice versa.

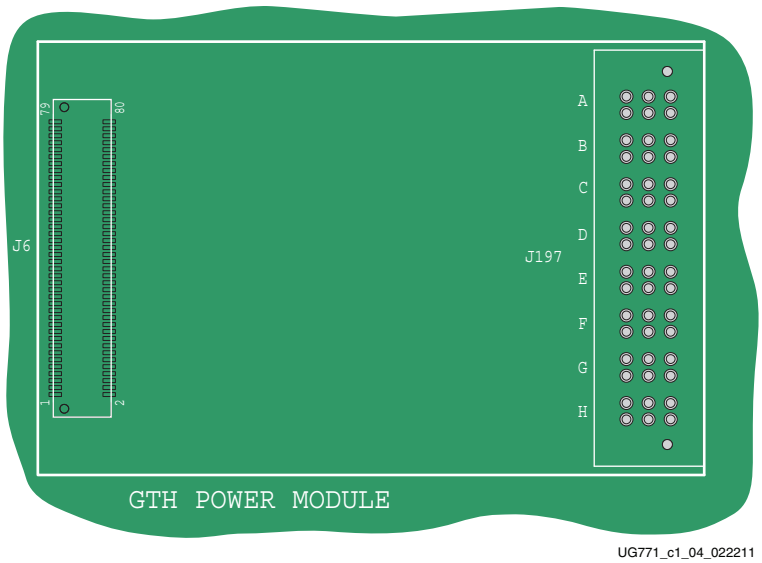


*Figure 1-4:* **Mounting Location, GTH Transceiver Power Module**

Table 1-2 describes the nominal voltage values for the MGTHAVCC, MGTHAVCCRX, MGTHAVTT and MGTHAVCCPLL power rails. The table also lists the maximum current ratings for each rail supplied by either module.

*Table 1-2:* **GTH Transceiver Power Module**

| Power Supply Rail Net Name | Nominal Voltage | Maximum Current Rating |
|---|---|---|
| MGTHAVCC | 1.1V | 5.10A |
| MGTHAVCCRX | 1.1V | 3.45A |
| MGTHAVTT | 1.2V | 1.50A |
| MGTHAVCCPLL | 1.8V | 2.60A |

The GTH transceiver power rails also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply. The external jacks are indicated in Table 1-3.

***Caution!*** The GTH module ***MUST*** be removed when providing external power to the GTH transceiver rails.

*Table 1-3:* **GTH External Supply Jacks**

| Power Supply Rail Net Name | External Supply Jack |
|---|---|
| MGTHAVCC | J279 |
| MGTHAVCCRX | J280 |
| MGTHAVTT | J282 |
| MGTHAVCCPLL | J283 |

## GTX Transceiver Power Module

The GTX transceiver power module supplies MGTAVCC and MGTAVTT voltages to the FPGA GTX transceivers. Three GTX power modules are provided with the ML628 board for evaluation. Any one of the three modules can be plugged into connectors J34 and J179 in the outlined and labeled power module location shown in Figure 1-5.

***Note:*** The GTX and GTH power modules have different connectors and form factors to prevent GTX modules from being connected to the GTH headers and vice versa.

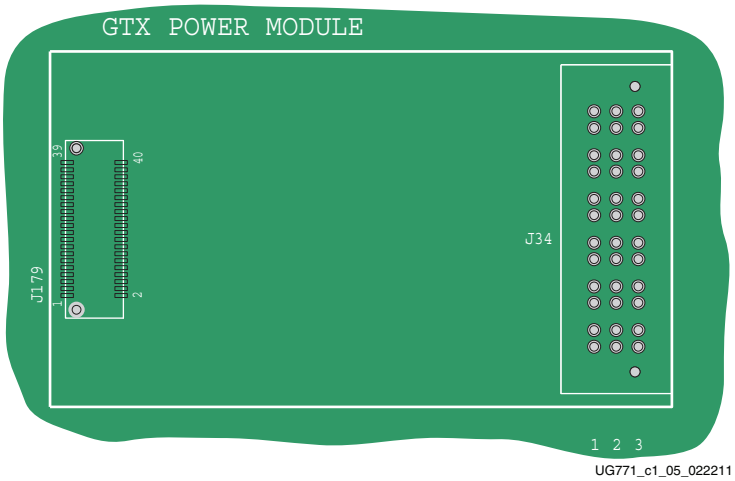


*Figure 1-5:* **Mounting Location, GTX Transceiver Power Module**

Table 1-4 describes the nominal voltage values for the MGTAVCC and MGTAVTT power rails. It also lists the maximum current ratings for each rail supplied by GTX modules included with the ML628 board.

***Caution!*** The Intersil module features an MGTAVCC voltage adjust header, J1. Make sure to ***REMOVE*** any jumper across J1 before powering the board with the Intersil module installed. Failure to do so may damage the FPGA.

*Table 1-4:* **GTX Transceiver Power Module**

| Power Supply Rail Net Name | Nominal Voltage | Maximum Current Rating |
|---|---|---|
| MGTAVCC | 1.025V | 10A |
| MGTAVTT | 1.2V | 6A |

The GTX transceiver power rails also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply (The external jacks are shown in Table 1-4).

***Caution!*** The GTX module ***MUST*** be removed when providing external power to the GTX transceiver rails.

*Table 1-5:* **GTX External Supply Jacks**

| Power Supply Rail Net Name | External Supply Jack |
|---|---|
| MGTHAVCC | J279 |
| MGTHAVCCRX | J280 |
| MGTHAVTT | J282 |
| MGTHAVCCPLL | J283 |

## Active Heatsink Power Connector

An active heatsink is provided for the FPGA (Figure 1-6). A 12V fan is affixed to the heatsink and is powered from the 3-pin header J101.

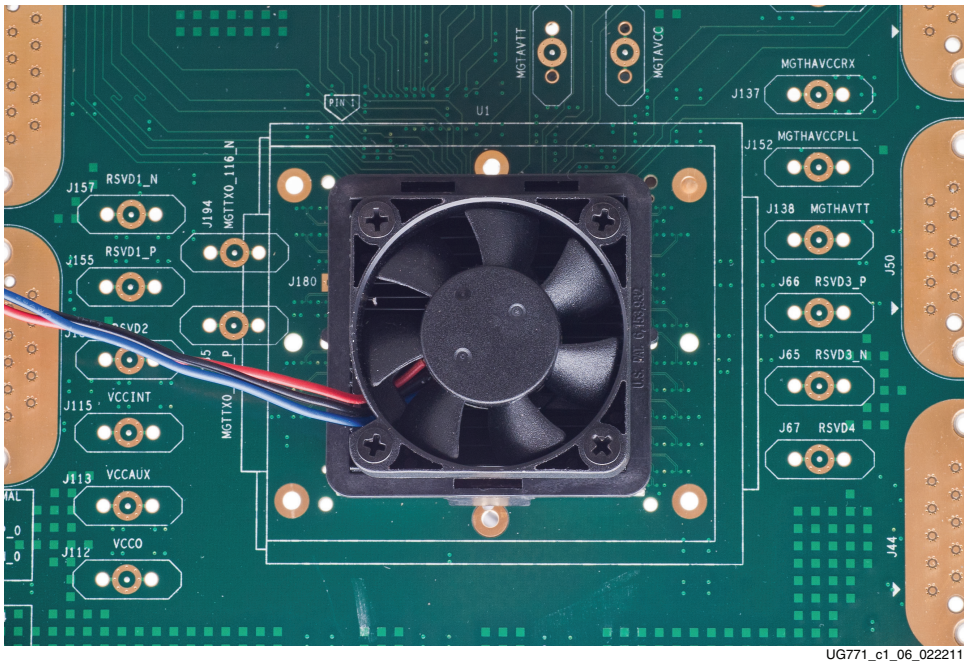


*Figure 1-6:* **Active Heatsink**

The fan power connections are detailed in Table 1-6 and shown in Figure 1-7.

*Table 1-6:* Fan Power Connections

| Fan Wire | Header |
|---|---|
| Black | J101 - GND |
| Red | J101 - 12V |
| Blue | Not Connected |

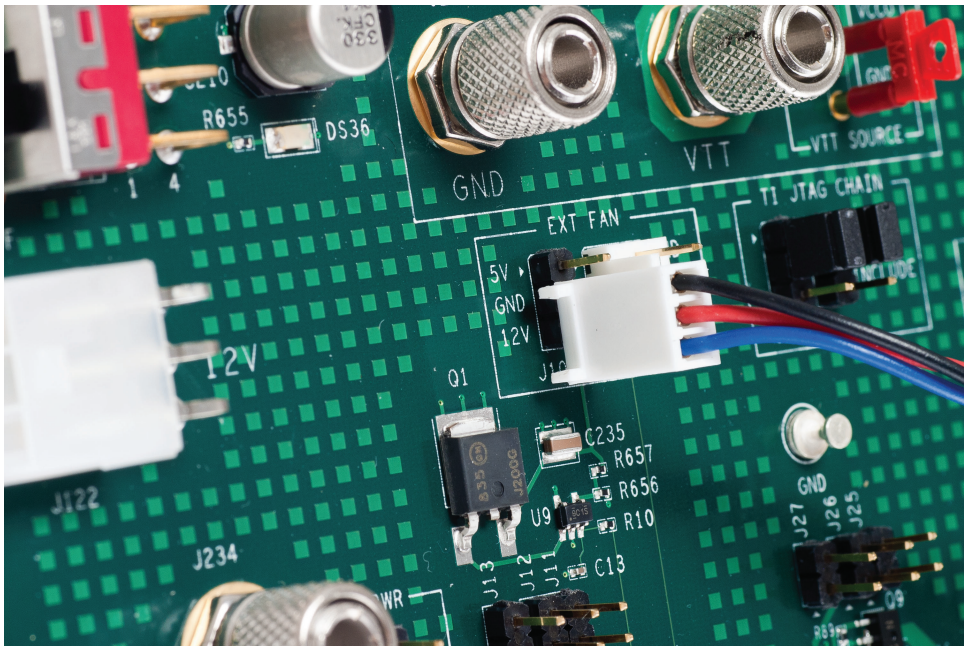


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*Figure 1-7:* **Fan Power Connector (J101)**

## FPGA Configuration

[Figure 1-2, callout 2]

The FPGA is configured in JTAG mode only using one of the following options:

- Platform Cable USB
- Parallel Cable IV
- Parallel Cable III
- System ACE controller

Detailed information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution*.

The FPGA is configured through one of the aforementioned cables by connecting the cable to the JTAG cable connector, J1.

The FPGA is configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card (see Configuration Address DIP Switches, page 19).

The JTAG chain of the board is illustrated in Figure 1-8 (the four System ACE interface isolation jumpers described in JTAG Isolation Jumpers are not shown). Shorting pins 1–2 on header J162 automatically bypasses the FMC modules, GTH transceiver power supply module and GTX transceiver power supply module in the chain.

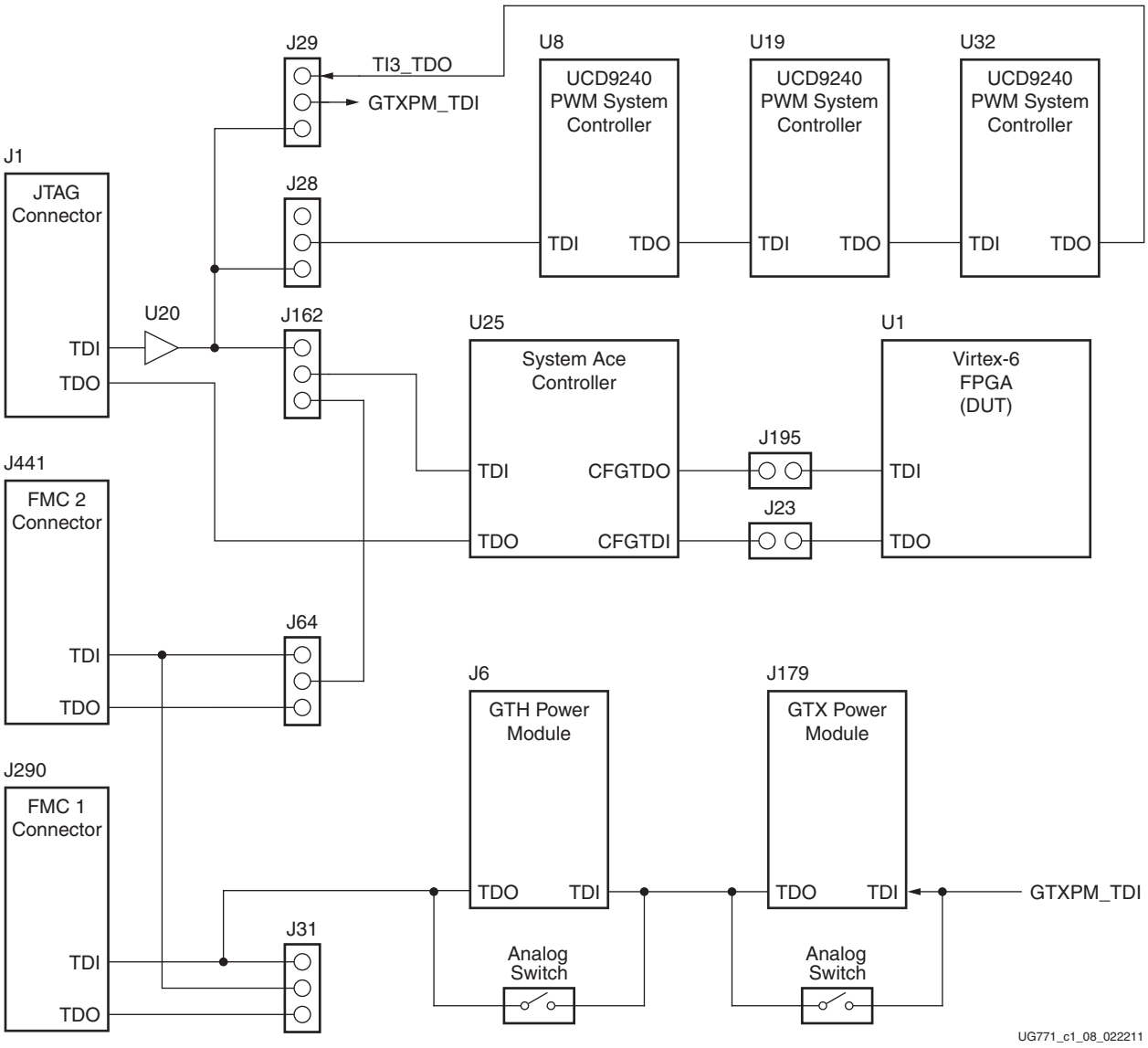


*Figure 1-8:* **JTAG Chain**

## PROG_B Push Button

[Figure 1-2, callout 3]

Pressing the PROG push button (SW5) grounds the active-Low program pin of the FPGA.

## DONE LED

[Figure 1-2, callout 4]

The DONE LED (DS6) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS6 lights indicating the FPGA is successfully configured.

## INIT LED

[Figure 1-2, callout 5]

The INIT LED (DS20) lights during FPGA initialization.

## System ACE Controller

[Figure 1-2, callout 6]

The onboard System ACE controller (U25) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGA. The CompactFlash card connects to the CompactFlash card connector (U24) located directly below the System ACE controller on the back side of the board.

## System ACE Controller Reset

[Figure 1-2, callout 7]

Pressing push button SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

## Configuration Address DIP Switches

[Figure 1-2, callout 8]

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are shown in Table 1-7.

*Table 1-7:* **SW3 DIP Switch Configuration**

| Address | ADR2 | ADR1 | ADR0 |
|---|---|---|---|
| 0 | O(1) | O | O |
| 1 | O | O | C(2) |
| 2 | O | C | O |
| 3 | O | C | C |
| 4 | C | O | O |
| 5 | C | O | C |
| 6 | C | C | O |
| 7 | C | C | C |

**Notes:**

1. O indicates the open switch position (logic 0).
2. C indicates the closed switch position (logic 1).

## JTAG Isolation Jumpers

[Figure 1-2, callout 9]

The group of four 2-pin headers shown in Figure 1-9 provide the option to isolate the FPGA JTAG interface from the System ACE controller by removing the shunts from all

four headers. The FPGA JTAG interface can also be driven directly from these headers by attaching the flying wire JTAG cable to pin 2 of each header. Figure 1-9 shows a more detailed representation of the isolation jumpers as part of the broader JTAG chain in Figure 1-8.

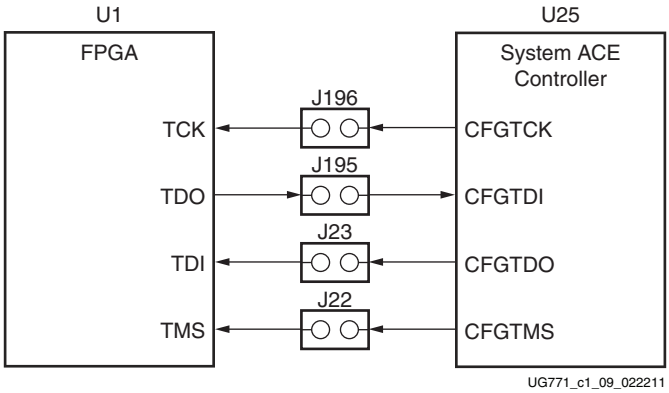


*Figure 1-9:* **JTAG Isolation Jumpers**

Table 1-8 indicates the FPGA pin name associated with each jumper.

*Table 1-8:* **JTAG Isolation Jumpers**

| Reference Designator | FPGA Pin Name |
|---|---|
| J22 | TMS |
| J23 | TDI |
| J195 | TDO |
| J196 | TCK |

## 200 MHz 2.5V LVDS Oscillator

[Figure 1-2, callout 10]

The ML628 board has one 2.5V LVDS differential 200 MHz oscillator (U7) connected to the FPGA global clock inputs. Table 1-9 lists the FPGA pin connections to the LVDS oscillator. The 200 MHz differential clock is enabled by placing two shunts (P, N) across J188 header pins 1–3 and 2–4 (LVDS).

*Table 1-9:* **LVDS Oscillator Global Clock Connections**

| FPGA Pin | Net Name | U7 Pin |
|---|---|---|
| AK13 | IIO_LVDS_GC_34_P | 4 |
| AK12 | IO_LVDS_GC_34_N | 5 |

## Single-Ended SMA Global Clock Inputs

[Figure 1-2, callout 11]

The ML628 board provides two single-ended clock input SMA connectors that can be used for connecting to an external function generator. The FPGA clock pins are connected to the SMA connectors as shown in Table 1-10.

To use these clock inputs, remove jumpers across AFX SEL headers J186 and J187.

*Table 1-10:* **Single-Ended SMA Clock Connections**

| FPGA Pin | Net Name | SMA Connector |
|---|---|---|
| AP33 | CLK_1 | J171 |
| R31 | CLK_2 | J172 |

## Differential SMA Global Clock Inputs

[Figure 1-2, callout 12]

The ML628 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA clock pins are connected to the SMA connectors as shown in Table 1-11.

*Table 1-11:* **Differential SMA Clock Connections**

| FPGA Pin | Net Name | SMA Connector |
|---|---|---|
| AN33 | CLK_DIFF_1_P | J167 |
| AP33 | CLK_DIFF_1_N | J168 |
| J33 | CLK_DIFF_2_P | J169 |
| H33 | CLK_DIFF_2_N | J170 |

## SuperClock-2 Module

[Figure 1-2, callout 13]

The SuperClock-2 module connects to the clock module interface connector (J32) and provides a programmable, low-noise and low-jitter clock source for the ML628 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-12 shows the FPGA I/O mapping for the SuperClock-2 module interface. The ML628 board also supplies 5V, 3.3V, and 2.5V input power to the clock module interface.

*Table 1-12:* **SuperClock-2 FPGA I/O Mapping**

| FPGA Pin | Net Name | J32 Pin |
|---|---|---|
| B35 | CM_LVDS1_P | 1 |
| B36 | CM_LVDS1_N | 3 |
| C12 | CM_LVDS2_P | 9 |
| C11 | CM_LVDS2_N | 11 |
| BC33 | CM_LVDS3_P | 17 |
| BD33 | CM_LVDS3_N | 19 |
| A23 | CM_GCLK_P | 25 |
| A24 | CM_GCLK_N | 27 |
| G26 | CM_CTRL_0 | 61 |

*Table 1-12:* **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

| FPGA Pin | Net Name | J32 Pin |
|---|---|---|
| G25 | CM_CTRL_1 | 63 |
| H23 | CM_CTRL_2 | 65 |
| J23 | CM_CTRL_3 | 67 |
| J25 | CM_CTRL_4 | 69 |
| K25 | CM_CTRL_5 | 71 |
| D26 | CM_CTRL_6 | 73 |
| E26 | CM_CTRL_7 | 75 |
| D25 | CM_CTRL_8 | 77 |
| E25 | CM_CTRL_9 | 79 |
| M25 | CM_CTRL_10 | 81 |
| M24 | CM_CTRL_11 | 83 |
| A25 | CM_CTRL_12 | 85 |
| B25 | CM_CTRL_13 | 87 |
| L25 | CM_CTRL_14 | 89 |
| L24 | CM_CTRL_15 | 91 |
| B24 | CM_CTRL_16 | 93 |
| C23 | CM_CTRL_17 | 95 |
| C24 | CM_CTRL_18 | 97 |
| D23 | CM_CTRL_19 | 99 |
| K23 | CM_CTRL_20 | 101 |
| L23 | CM_CTRL_21 | 103 |
| B26 | CM_CTRL_22 | 105 |
| C26 | CM_CTRL_23 | 107 |
| D24 | CM_RST | 66 |

## User LEDs (Active High)

[Figure 1-2, callout 14]

DS10 through DS17 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-13. These LEDs can be used to indicate status or any other purpose determined by the user.

*Table 1-13:* **User LEDs**

| FPGA Pin | Net Name | Reference Designator |
|---|---|---|
| N28 | APP_LED1 | DS17 |
| P28 | APP_LED2 | DS16 |
| K28 | APP_LED3 | DS15 |
| L27 | APP_LED4 | DS14 |
| K27 | APP_LED5 | DS13 |
| K26 | APP_LED6 | DS12 |
| P26 | APP_LED7 | DS11 |
| R26 | APP_LED8 | DS10 |

## User DIP Switches (Active High)

[Figure 1-2, callout 15]

The DIP switch SW7 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-14. These pins can be used to set control pins or any other purpose determined by the user.

*Table 1-14:* **User DIP Switches**

| FPGA Pin | Net Name | Reference Designator |
|---|---|---|
| J29 | USER_SW1 | SW7 |
| J28 | USER_SW2 | |
| R27 | USER_SW3 | |
| T27 | USER_SW4 | |
| H29 | USER_SW5 | |
| H28 | USER_SW6 | |
| L29 | USER_SW7 | |
| L28 | USER_SW8 | |

## User Push Buttons (Active High)

[Figure 1-2, callout 16]

SW5 and SW6 are active-High user push buttons that are connected to user I/O pins on the FPGA as shown in Table 1-15. These switches can be used for any purpose determined by the user.

*Table 1-15:* **User Push Buttons**

| FPGA Pin | Net Name | Reference Designator |
|---|---|---|
| A27 | USER_PB1 | SW6 |
| B27 | USER_PB2 | SW4 |

## User Test I/O

[Figure 1-2, callout 17]

A standard 2 x 6, 100-mil pitch header (J285) brings out 6 FPGA I/O for test purposes. Table 1-16 lists these pins.

*Table 1-16:* **User Test I/O**

| FPGA Pin | Net Name | J285 Pin |
|---|---|---|
| M26 | USER_I0_1 | 2 |
| N26 | USER_I0_2 | 4 |
| C28 | USER_I0_3 | 6 |
| C27 | USER_I0_4 | 8 |
| A29 | USER_I0_5 | 10 |
| A28 | USER_I0_6 | 12 |

## GTH Transceivers and Reference Clocks

[Figure 1-2, callout 19]

The ML628 board provides access to all GTH transceiver and reference clock pins on the FPGA as shown in Figure 1-10. The GTH transceivers are grouped into six sets of four RX-TX "lanes." Four lanes are referred to as a "Quad."

***Note:*** Figure 1-10 is for reference only and might not reflect the current revision of the board.

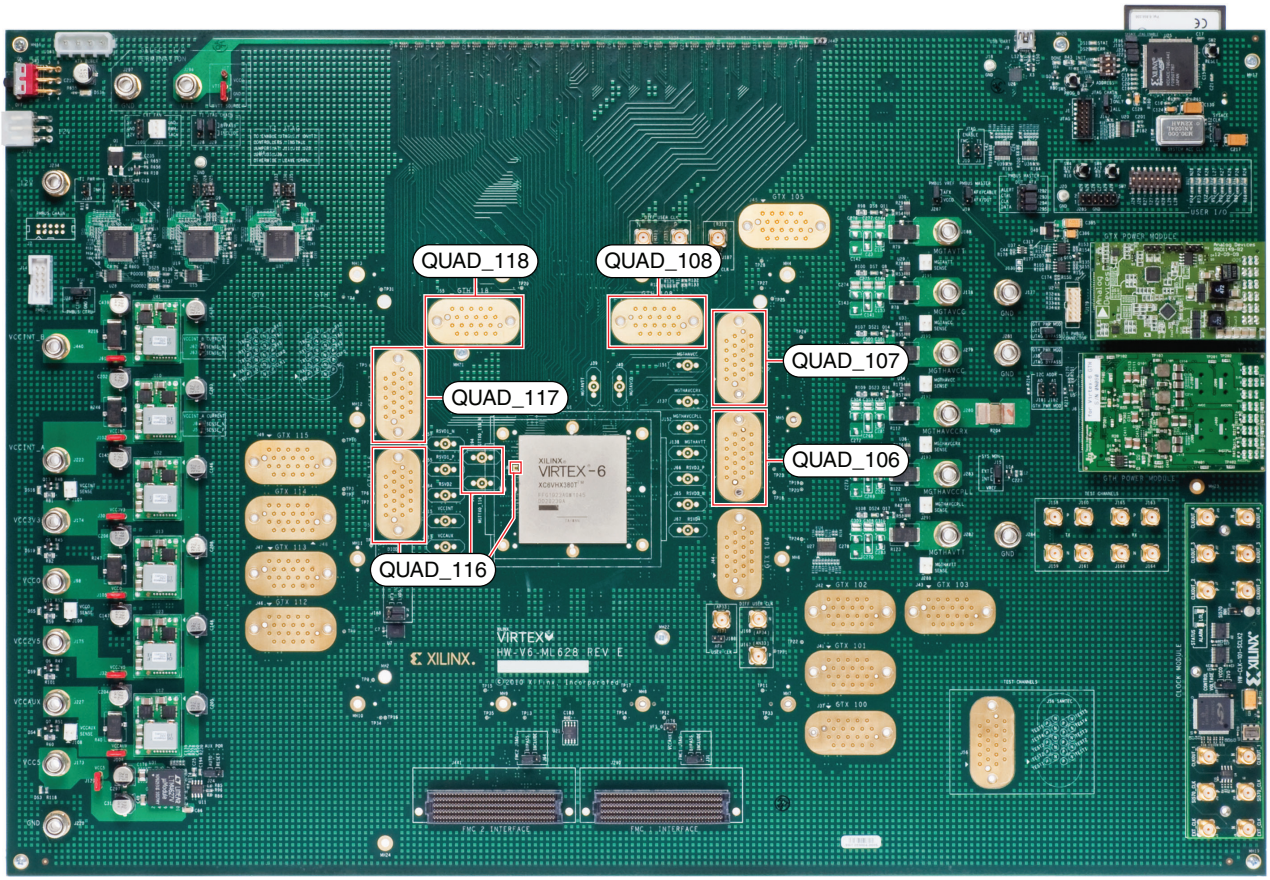


*Figure 1-10:* **GTH Quad Locations**

Each GTH Quad and its associated reference clock (CLK0) are routed from the FPGA to a connector pad which is designed to interface with Samtec BullsEye connectors such as the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for other cable assemblies . Figure 1-11 "A" shows the connector pad. Figure 1-11 "B" shows the connector pinout.

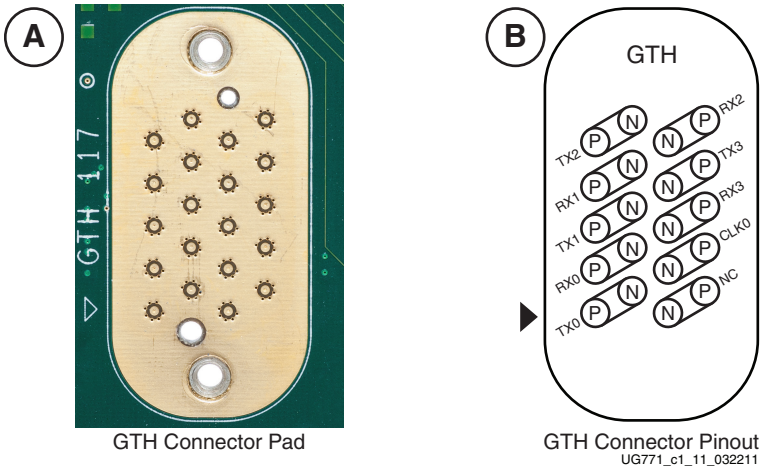


*Figure 1-11:* **A – GTH BullsEye Connector Pad. B – GTH BullsEye Connector Pad**

Two GTH transmitters are *not* connected to a BullsEye connector pad. These are transmitter pairs MGTTX0_116_P / MGTTX0_116_N and MGTTX1_116_P / MGTTX1_116_N. To provide optimum test conditions for these transmitters, both pairs are routed on very short traces (less than 1-inch) to separate connectors located near the perimeter of the FPGA.

MGTTX0_116_P and MGTTX0_116_N are terminated to removable SMA connectors (Molex part number 73251-1851) J185 and J194, respectively. MGTTX1_116_P and MGTTX1_116_N are terminated to probe pad J180 (Figure 1-12).

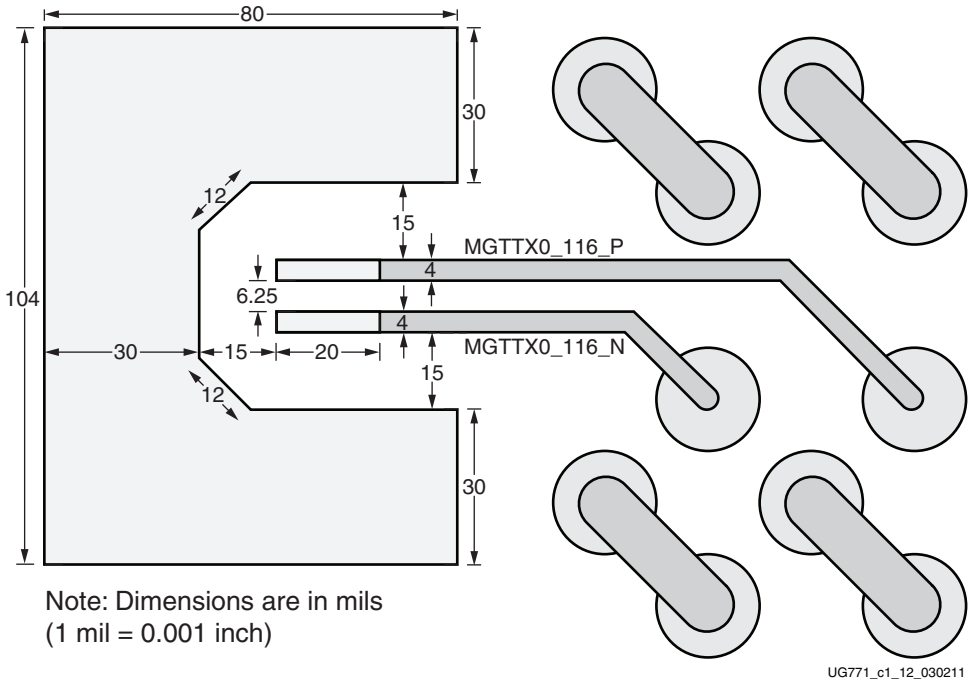


*Figure 1-12:* **Microprobe Test Pad Dimensions (J180)**

Information for each GTH transceiver pin is shown in Table 1-17.

*Table 1-17:* **GTH Transceiver Pins**

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| T43 | MGTTX0_106_P | 106 | J50 | 3,025 |
| T44 | MGTTX0_106_N | 106 | J50 | 3,025 |
| U41 | MGTRX0_106_P | 106 | J50 | 2,135 |
| U42 | MGTRX0_106_N | 106 | J50 | 2,135 |
| P43 | MGTTX1_106_P | 106 | J50 | 3,337 |
| P44 | MGTTX1_106_N | 106 | J50 | 3,337 |
| T39 | MGTRX1_106_P | 106 | J50 | 2,250 |
| T40 | MGTRX1_106_N | 106 | J50 | 2,250 |
| M43 | MGTTX2_106_P | 106 | J50 | 2,793 |

*Table 1-17:* **GTH Transceiver Pins *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| M44 | MGTTX2_106_N | 106 | J50 | 2,793 |
| N37 | MGTRX2_106_P | 106 | J50 | 2,192 |
| N38 | MGTRX2_106_N | 106 | J50 | 2,192 |
| N41 | MGTTX3_106_P | 106 | J50 | 2,800 |
| N42 | MGTTX3_106_N | 106 | J50 | 2,799 |
| M39 | MGTRX3_106_P | 106 | J50 | 2,711 |
| M40 | MGTRX3_106_N | 106 | J50 | 2,710 |
| L41 | MGTTX0_107_P | 107 | J51 | 3,050 |
| L42 | MGTTX0_107_N | 107 | J51 | 3,049 |
| K39 | MGTRX0_107_P | 107 | J51 | 2,919 |
| K40 | MGTRX0_107_N | 107 | J51 | 2,920 |
| K43 | MGTTX1_107_P | 107 | J51 | 3,890 |
| K44 | MGTTX1_107_N | 107 | J51 | 3,890 |
| L37 | MGTRX1_107_P | 107 | J51 | 3,184 |
| L38 | MGTRX1_107_N | 107 | J51 | 3,184 |
| G41 | MGTTX2_107_P | 107 | J51 | 3,905 |
| G42 | MGTTX2_107_N | 107 | J51 | 3,906 |
| H39 | MGTRX2_107_P | 107 | J51 | 3,407 |
| H40 | MGTRX2_107_N | 107 | J51 | 3,406 |
| H43 | MGTTX3_107_P | 107 | J51 | 3,865 |
| H44 | MGTTX3_107_N | 107 | J51 | 3,864 |
| J37 | MGTRX3_107_P | 107 | J51 | 3,525 |
| J38 | MGTRX3_107_N | 107 | J51 | 3,525 |
| F43 | MGTTX0_108_P | 108 | J52 | 3,644 |
| F44 | MGTTX0_108_N | 108 | J52 | 3,645 |
| G37 | MGTRX0_108_P | 108 | J52 | 2,791 |
| G38 | MGTRX0_108_N | 108 | J52 | 2,791 |
| D43 | MGTTX1_108_P | 108 | J52 | 2,677 |
| D44 | MGTTX1_108_N | 108 | J52 | 2,678 |
| F39 | MGTRX1_108_P | 108 | J52 | 2,528 |
| F40 | MGTRX1_108_N | 108 | J52 | 2,528 |
| A41 | MGTTX2_108_P | 108 | J52 | 2,349 |

*Table 1-17:* **GTH Transceiver Pins *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| A42 | MGTTX2_108_N | 108 | J52 | 2,349 |
| B39 | MGTRX2_108_P | 108 | J52 | 2,207 |
| B40 | MGTRX2_108_N | 108 | J52 | 2,207 |
| C41 | MGTTX3_108_P | 108 | J52 | 2,874 |
| C42 | MGTTX3_108_N | 108 | J52 | 2,874 |
| D39 | MGTRX3_108_P | 108 | J52 | 2,564 |
| D40 | MGTRX3_108_N | 108 | J52 | 2,563 |
| T2 | MGTTX0_116_P | 116 | J185 | 3,565 |
| T1 | MGTTX0_116_N | 116 | J194 | 3,565 |
| U4 | MGTRX0_116_P | 116 | J53 | 967 |
| U3 | MGTRX0_116_N | 116 | J53 | 967 |
| P2 | MGTTX1_116_P | 116 | J180 | 3,704 |
| P1 | MGTTX1_116_N | 116 | J180 | 3,704 |
| T6 | MGTRX1_116_P | 116 | J53 | 132 |
| T5 | MGTRX1_116_N | 116 | J53 | 89 |
| M2 | MGTTX2_116_P | 116 | J53 | 2,766 |
| M1 | MGTTX2_116_N | 116 | J53 | 2,767 |
| N8 | MGTRX2_116_P | 116 | J53 | 3,214 |
| N7 | MGTRX2_116_N | 116 | J53 | 3,214 |
| N4 | MGTTX3_116_P | 116 | J53 | 2,911 |
| N3 | MGTTX3_116_N | 116 | J53 | 2,912 |
| M6 | MGTRX3_116_P | 116 | J53 | 3,052 |
| M5 | MGTRX3_116_N | 116 | J53 | 3,051 |
| L4 | MGTTX0_117_P | 117 | J54 | 2,898 |
| L3 | MGTTX0_117_N | 117 | J54 | 2,899 |
| K6 | MGTRX0_117_P | 117 | J54 | 3,144 |
| K5 | MGTRX0_117_N | 117 | J54 | 3,145 |
| K2 | MGTTX1_117_P | 117 | J54 | 3,926 |
| K1 | MGTTX1_117_N | 117 | J54 | 3,927 |
| L8 | MGTRX1_117_P | 117 | J54 | 3,156 |
| L7 | MGTRX1_117_N | 117 | J54 | 3,156 |
| G4 | MGTTX2_117_P | 117 | J54 | 3,269 |

*Table 1-17:* **GTH Transceiver Pins *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| G3 | MGTTX2_117_N | 117 | J54 | 3,268 |
| H6 | MGTRX2_117_P | 117 | J54 | 3,475 |
| H5 | MGTRX2_117_N | 117 | J54 | 3,474 |
| H2 | MGTTX3_117_P | 117 | J54 | 2,717 |
| H1 | MGTTX3_117_N | 117 | J54 | 2,717 |
| J8 | MGTRX3_117_P | 117 | J54 | 2,902 |
| J7 | MGTRX3_117_N | 117 | J54 | 2,901 |
| F2 | MGTTX0_118_P | 118 | J55 | 3,492 |
| F1 | MGTTX0_118_N | 118 | J55 | 3,492 |
| G8 | MGTRX0_118_P | 118 | J55 | 3,433 |
| G7 | MGTRX0_118_N | 118 | J55 | 3,434 |
| D2 | MGTTX1_118_P | 118 | J55 | 2,864 |
| D1 | MGTTX1_118_N | 118 | J55 | 2,865 |
| F6 | MGTRX1_118_P | 118 | J55 | 3,151 |
| F5 | MGTRX1_118_N | 118 | J55 | 3,152 |
| A4 | MGTTX2_118_P | 118 | J55 | 2,271 |
| A3 | MGTTX2_118_N | 118 | J55 | 2,271 |
| B6 | MGTRX2_118_P | 118 | J55 | 2,518 |
| B5 | MGTRX2_118_N | 118 | J55 | 2,518 |
| C4 | MGTTX3_118_P | 118 | J55 | 2560 |
| C3 | MGTTX3_118_N | 118 | J55 | 2,561 |
| D6 | MGTRX3_118_P | 118 | J55 | 2,426 |
| D5 | MGTRX3_118_N | 118 | J55 | 2426 |

Information for each GTH transceiver clock input is shown in Table 1-18.

*Table 1-18:* **GTH Transceiver Clock Inputs to the FPGA**

| FPGA Pin | Net Name | Quad | Connector |
|---|---|---|---|
| R41 | MGTREFCLK_106_P | 106 | J50 |
| R42 | MGTREFCLK_106_N | 106 | J50 |
| J41 | MGTREFCLK_107_P | 107 | J51 |
| J42 | MGTREFCLK_107_N | 107 | J51 |
| E41 | MGTREFCLK_108_P | 108 | J52 |
| E42 | MGTREFCLK_108_N | 108 | J52 |

*Table 1-18:* **GTH Transceiver Clock Inputs to the FPGA *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector |
|---|---|---|---|
| R4 | MGTREFCLK_116_P | 116 | J53 |
| R3 | MGTREFCLK_116_N | 116 | J53 |
| J4 | MGTREFCLK_117_P | 117 | J54 |
| J3 | MGTREFCLK_117_N | 117 | J54 |
| E4 | MGTREFCLK_118_P | 118 | J55 |
| E3 | MGTREFCLK_118_N | 118 | J55 |

## GTX Transceivers and Reference Clocks

[Figure 1-2, callout 18]

The ML628 board provides access to all GTX transceiver and reference clock pins on the FPGA as shown in Figure 1-13. The GTX transceivers are grouped into six sets of four RX-TX "lanes." Four lanes are referred to as a "Quad."

***Note:*** Figure 1-13 is for reference only and might not reflect the current revision of the board.

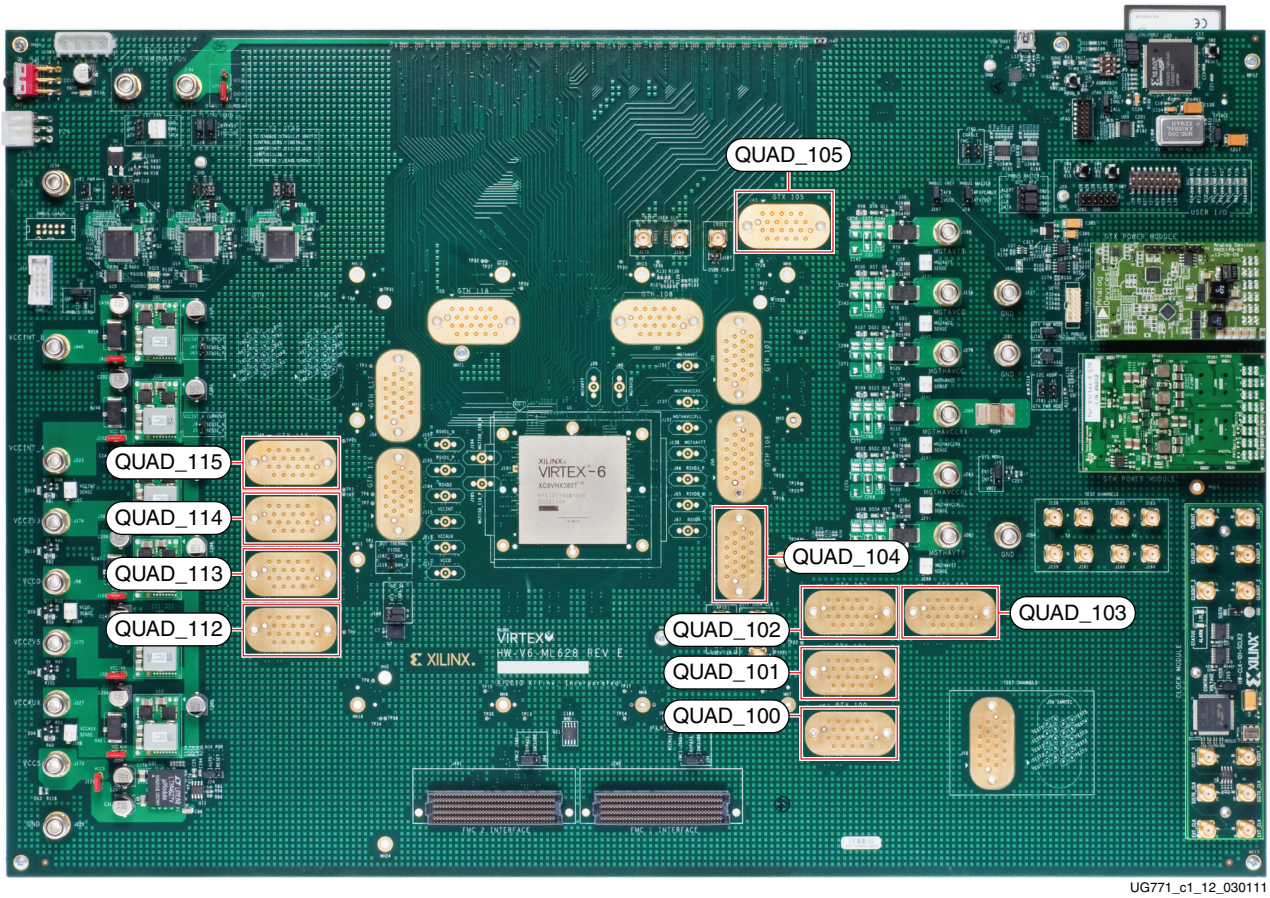


*Figure 1-13:* **GTX Transceiver and Reference Clock SMA Locations**

Each GTX Quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad which is designed to interface with Samtec BullsEye connectors such as the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for information about other cable assemblies. Figure 1-14 "A" shows the connector pad. Figure 1-14 "B" shows the connector pinout.

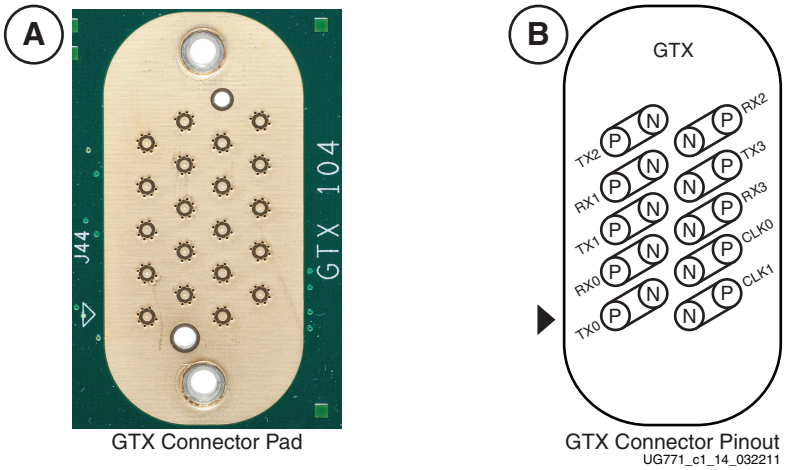


*Figure 1-14:* **A – GTX BullsEye Connector Pad. B – GTX BullsEye Connector Pad**

Information for each GTX transceiver pin is shown in Table 1-19.

*Table 1-19:* **GTX Transceiver Pins**

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| BB44 | MGTTX0_100_P | 100 | J37 | 5,825 |
| BB43 | MGTTX0_100_N | 100 | J37 | 5,825 |
| BD40 | MGTRX0_100_P | 100 | J37 | 5,316 |
| BD39 | MGTRX0_100_N | 100 | J37 | 5,316 |
| AY44 | MGTTX1_100_P | 100 | J37 | 6,178 |
| AY43 | MGTTX1_100_N | 100 | J37 | 6,178 |
| BC42 | MGTRX1_100_P | 100 | J37 | 5,702 |
| BC41 | MGTRX1_100_N | 100 | J37 | 5,701 |
| AW42 | MGTTX2_100_P | 100 | J37 | 7,107 |
| AW41 | MGTTX2_100_N | 100 | J37 | 7,107 |
| BB40 | MGTRX2_100_P | 100 | J37 | 6,653 |
| BB39 | MGTRX2_100_N | 100 | J37 | 6,652 |
| AV44 | MGTTX3_100_P | 100 | J37 | 6,662 |
| AV43 | MGTTX3_100_N | 100 | J37 | 6,662 |
| BA42 | MGTRX3_100_P | 100 | J37 | 6,158 |
| BA41 | MGTRX3_100_N | 100 | J37 | 6,157 |

*Table 1-19:* **GTX Transceiver Pins *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| AU42 | MGTTX0_101_P | 101 | J41 | 5,335 |
| AU41 | MGTTX0_101_N | 101 | J41 | 5,335 |
| AY40 | MGTRX0_101_P | 101 | J41 | 4,955 |
| AY39 | MGTRX0_101_N | 101 | J41 | 4,955 |
| AT44 | MGTTX1_101_P | 101 | J41 | 5,647 |
| AT43 | MGTTX1_101_N | 101 | J41 | 5,647 |
| AV40 | MGTRX1_101_P | 101 | J41 | 5,347 |
| AV39 | MGTRX1_101_N | 101 | J41 | 5,347 |
| AR42 | MGTTX2_101_P | 101 | J41 | 5,990 |
| AR41 | MGTTX2_101_N | 101 | J41 | 5,990 |
| AT40 | MGTRX2_101_P | 101 | J41 | 5,586 |
| AT39 | MGTRX2_101_N | 101 | J41 | 5,586 |
| AP44 | MGTTX3_101_P | 101 | J41 | 6,987 |
| AP43 | MGTTX3_101_N | 101 | J41 | 6,988 |
| AP40 | MGTRX3_101_P | 101 | J41 | 5,677 |
| AP39 | MGTRX3_101_N | 101 | J41 | 5,678 |
| AN42 | MGTTX0_102_P | 102 | J42 | 5,056 |
| AN41 | MGTTX0_102_N | 102 | J42 | 5,055 |
| AL38 | MGTRX0_102_P | 102 | J42 | 4,603 |
| AL37 | MGTRX0_102_N | 102 | J42 | 4,603 |
| AM44 | MGTTX1_102_P | 102 | J42 | 5,241 |
| AM43 | MGTTX1_102_N | 102 | J42 | 5,241 |
| AM40 | MGTRX1_102_P | 102 | J42 | 5,029 |
| AM39 | MGTRX1_102_N | 102 | J42 | 5,028 |
| AL42 | MGTTX2_102_P | 102 | J42 | 5,883 |
| AL41 | MGTTX2_102_N | 102 | J42 | 5,883 |
| AJ38 | MGTRX2_102_P | 102 | J42 | 5,468 |
| AJ37 | MGTRX2_102_N | 102 | J42 | 5,469 |
| AK44 | MGTTX3_102_P | 102 | J42 | 5,806 |
| AK43 | MGTTX3_102_N | 102 | J42 | 5,806 |
| AK40 | MGTRX3_102_P | 102 | J42 | 5,383 |
| AK39 | MGTRX3_102_N | 102 | J42 | 5,382 |

*Table 1-19:* **GTX Transceiver Pins *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| AJ42 | MGTTX0_103_P | 103 | J43 | 6,626 |
| AJ41 | MGTTX0_103_N | 103 | J43 | 6,627 |
| AH40 | MGTRX0_103_P | 103 | J43 | 6,500 |
| AH39 | MGTRX0_103_N | 103 | J43 | 6,500 |
| AH44 | MGTTX1_103_P | 103 | J43 | 7,261 |
| AH43 | MGTTX1_103_N | 103 | J43 | 7,261 |
| AG38 | MGTRX1_103_P | 103 | J43 | 7,179 |
| AG37 | MGTRX1_103_N | 103 | J43 | 7,180 |
| AG42 | MGTTX2_103_P | 103 | J43 | 7,333 |
| AG41 | MGTTX2_103_N | 103 | J43 | 7,333 |
| AF40 | MGTRX2_103_P | 103 | J43 | 7,092 |
| AF39 | MGTRX2_103_N | 103 | J43 | 7,091 |
| AF44 | MGTTX3_103_P | 103 | J43 | 8,388 |
| AF43 | MGTTX3_103_N | 103 | J43 | 8,388 |
| AE38 | MGTRX3_103_P | 103 | J43 | 7,453 |
| AE37 | MGTRX3_103_N | 103 | J43 | 7,454 |
| AE42 | MGTTX0_104_P | 104 | J44 | 2,665 |
| AE41 | MGTTX0_104_N | 104 | J44 | 2,666 |
| AD40 | MGTRX0_104_P | 104 | J44 | 2,994 |
| AD39 | MGTRX0_104_N | 104 | J44 | 2,994 |
| AD44 | MGTTX1_104_P | 104 | J44 | 2,696 |
| AD43 | MGTTX1_104_N | 104 | J44 | 2,696 |
| AC38 | MGTRX1_104_P | 104 | J44 | 2,786 |
| AC37 | MGTRX1_104_N | 104 | J44 | 2,786 |
| AC42 | MGTTX2_104_P | 104 | J44 | 3,091 |
| AC41 | MGTTX2_104_N | 104 | J44 | 3,092 |
| AB40 | MGTRX2_104_P | 104 | J44 | 2,435 |
| AB39 | MGTRX2_104_N | 104 | J44 | 2,436 |
| AB44 | MGTTX3_104_P | 104 | J44 | 3,846 |
| AB43 | MGTTX3_104_N | 104 | J44 | 3,847 |
| AA38 | MGTRX3_104_P | 104 | J44 | 3,139 |
| AA37 | MGTRX3_104_N | 104 | J44 | 3,140 |

*Table 1-19:* **GTX Transceiver Pins *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| AA42 | MGTTX0_105_P | 105 | J45 | 8,305 |
| AA41 | MGTTX0_105_N | 105 | J45 | 8,305 |
| Y40 | MGTRX0_105_P | 105 | J45 | 7,237 |
| Y39 | MGTRX0_105_N | 105 | J45 | 7,236 |
| Y44 | MGTTX1_105_P | 105 | J45 | 7,068 |
| Y43 | MGTTX1_105_N | 105 | J45 | 7,068 |
| W38 | MGTRX1_105_P | 105 | J45 | 7,455 |
| W37 | MGTRX1_105_N | 105 | J45 | 7,456 |
| W42 | MGTTX2_105_P | 105 | J45 | 6,717 |
| W41 | MGTTX2_105_N | 105 | J45 | 6,717 |
| V40 | MGTRX2_105_P | 105 | J45 | 8,331 |
| V39 | MGTRX2_105_N | 105 | J45 | 8,331 |
| V44 | MGTTX3_105_P | 105 | J45 | 6,213 |
| V43 | MGTTX3_105_N | 105 | J45 | 6,212 |
| U38 | MGTRX3_105_P | 105 | J45 | 7,386 |
| U37 | MGTRX3_105_N | 105 | J45 | 7,385 |
| AN3 | MGTTX0_112_P | 112 | J46 | 6,021 |
| AN4 | MGTTX0_112_N | 112 | J46 | 6,020 |
| AL7 | MGTRX0_112_P | 112 | J46 | 5,915 |
| AL8 | MGTRX0_112_N | 112 | J46 | 5,914 |
| AM1 | MGTTX1_112_P | 112 | J46 | 5,559 |
| AM2 | MGTTX1_112_N | 112 | J46 | 5,560 |
| AM5 | MGTRX1_112_P | 112 | J46 | 5,708 |
| AM6 | MGTRX1_112_N | 112 | J46 | 5,707 |
| AL3 | MGTTX2_112_P | 112 | J46 | 5,395 |
| AL4 | MGTTX2_112_N | 112 | J46 | 5,396 |
| AJ7 | MGTRX2_112_P | 112 | J46 | 4,506 |
| AJ8 | MGTRX2_112_N | 112 | J46 | 4,506 |
| AK1 | MGTTX3_112_P | 112 | J46 | 5,986 |
| AK2 | MGTTX3_112_N | 112 | J46 | 5,985 |
| AK5 | MGTRX3_112_P | 112 | J46 | 5,094 |
| AK6 | MGTRX3_112_N | 112 | J46 | 5,094 |

*Table 1-19:* **GTX Transceiver Pins *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| AJ3 | MGTTX0_113_P | 113 | J47 | 5,669 |
| AJ4 | MGTTX0_113_N | 113 | J47 | 5,668 |
| AH5 | MGTRX0_113_P | 113 | J47 | 5,878 |
| AH6 | MGTRX0_113_N | 113 | J47 | 5,878 |
| AH1 | MGTTX1_113_P | 113 | J47 | 5,020 |
| AH2 | MGTTX1_113_N | 113 | J47 | 5,020 |
| AG7 | MGTRX1_113_P | 113 | J47 | 5,715 |
| AG8 | MGTRX1_113_N | 113 | J47 | 5,715 |
| AG3 | MGTTX2_113_P | 113 | J47 | 5,026 |
| AG4 | MGTTX2_113_N | 113 | J47 | 5,025 |
| AF5 | MGTRX2_113_P | 113 | J47 | 4,225 |
| AF6 | MGTRX2_113_N | 113 | J47 | 4,224 |
| AF1 | MGTTX3_113_P | 113 | J47 | 5,457 |
| AF2 | MGTTX3_113_N | 113 | J47 | 5,456 |
| AE7 | MGTRX3_113_P | 113 | J47 | 5,135 |
| AE8 | MGTRX3_113_N | 113 | J47 | 5,135 |
| AE3 | MGTTX0_114_P | 114 | J48 | 4,623 |
| AE4 | MGTTX0_114_N | 114 | J48 | 4,623 |
| AD5 | MGTRX0_114_P | 114 | J48 | 4,150 |
| AD6 | MGTRX0_114_N | 114 | J48 | 4,150 |
| AD1 | MGTTX1_114_P | 114 | J48 | 5,211 |
| AD2 | MGTTX1_114_N | 114 | J48 | 5,211 |
| AC7 | MGTRX1_114_P | 114 | J48 | 4,693 |
| AC8 | MGTRX1_114_N | 114 | J48 | 4,693 |
| AC3 | MGTTX2_114_P | 114 | J48 | 5,330 |
| AC4 | MGTTX2_114_N | 114 | J48 | 5,330 |
| AB5 | MGTRX2_114_P | 114 | J48 | 5,465 |
| AB6 | MGTRX2_114_N | 114 | J48 | 5,465 |
| AB1 | MGTTX3_114_P | 114 | J48 | 5,542 |
| AB2 | MGTTX3_114_N | 114 | J48 | 5,541 |
| AA7 | MGTRX3_114_P | 114 | J48 | 4,896 |
| AA8 | MGTRX3_114_N | 114 | J48 | 4,897 |

*Table 1-19:* **GTX Transceiver Pins *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector | Trace Length (Mils) |
|---|---|---|---|---|
| AA3 | MGTTX0_115_P | 115 | J49 | 5,020 |
| AA4 | MGTTX0_115_N | 115 | J49 | 5,020 |
| Y5 | MGTRX0_115_P | 115 | J49 | 5,269 |
| Y6 | MGTRX0_115_N | 115 | J49 | 5,269 |
| Y1 | MGTTX1_115_P | 115 | J49 | 4,563 |
| Y2 | MGTTX1_115_N | 115 | J49 | 4,562 |
| W7 | MGTRX1_115_P | 115 | J49 | 5,134 |
| W8 | MGTRX1_115_N | 115 | J49 | 5,134 |
| W3 | MGTTX2_115_P | 115 | J49 | 4,238 |
| W4 | MGTTX2_115_N | 115 | J49 | 4,238 |
| V5 | MGTRX2_115_P | 115 | J49 | 4,534 |
| V6 | MGTRX2_115_N | 115 | J49 | 4,533 |
| V1 | MGTTX3_115_P | 115 | J49 | 4,941 |
| V2 | MGTTX3_115_N | 115 | J49 | 4,941 |
| U7 | MGTRX3_115_P | 115 | J49 | 4,698 |
| U8 | MGTRX3_115_N | 115 | J49 | 4,698 |

Information for each GTX transceiver clock input is shown in Table 1-20.

*Table 1-20:* **GTX Transceiver Clock Inputs to the FPGA**

| FPGA Pin | Net Name | Quad | Connector |
|---|---|---|---|
| BA37 | MGTREFCLK0_100_P | 100 | J37 |
| BA38 | MGTREFCLK0_100_N | 100 | J37 |
| AW37 | MGTREFCLK1_100_P | 100 | J37 |
| AW38 | MGTREFCLK1_100_N | 100 | J37 |
| AU37 | MGTREFCLK0_101_P | 101 | J41 |
| AU38 | MGTREFCLK0_101_N | 101 | J41 |
| AR37 | MGTREFCLK1_101_P | 101 | J41 |
| AR38 | MGTREFCLK1_101_N | 101 | J41 |
| AN37 | MGTREFCLK0_102_P | 102 | J42 |
| AN38 | MGTREFCLK0_102_N | 102 | J42 |
| AH35 | MGTREFCLK1_102_P | 102 | J42 |
| AH36 | MGTREFCLK1_102_N | 102 | J42 |
| AF35 | MGTREFCLK0_103_P | 103 | J43 |

*Table 1-20:* **GTX Transceiver Clock Inputs to the FPGA *(Cont'd)***

| FPGA Pin | Net Name | Quad | Connector |
|---|---|---|---|
| AF36 | MGTREFCLK0_103_N | 103 | J43 |
| AD35 | MGTREFCLK1_103_P | 103 | J43 |
| AD36 | MGTREFCLK1_103_N | 103 | J43 |
| AB35 | MGTREFCLK0_104_P | 104 | J44 |
| AB36 | MGTREFCLK0_104_N | 104 | J44 |
| Y35 | MGTREFCLK1_104_P | 104 | J44 |
| Y36 | MGTREFCLK1_104_N | 104 | J44 |
| V35 | MGTREFCLK0_105_P | 105 | J45 |
| V36 | MGTREFCLK0_105_N | 105 | J45 |
| T35 | MGTREFCLK1_105_P | 105 | J45 |
| T36 | MGTREFCLK1_105_N | 105 | J45 |
| AN8 | MGTREFCLK0_112_P | 112 | J46 |
| AN7 | MGTREFCLK0_112_N | 112 | J46 |
| AH10 | MGTREFCLK1_112_P | 112 | J46 |
| AH9 | MGTREFCLK1_112_N | 112 | J46 |
| AF10 | MGTREFCLK0_113_P | 113 | J47 |
| AF9 | MGTREFCLK0_113_N | 113 | J47 |
| AD10 | MGTREFCLK1_113_P | 113 | J47 |
| AD9 | MGTREFCLK1_113_N | 113 | J47 |
| AB10 | MGTREFCLK0_114_P | 114 | J48 |
| AB9 | MGTREFCLK0_114_N | 114 | J48 |
| Y10 | MGTREFCLK1_114_P | 114 | J48 |
| Y9 | MGTREFCLK1_114_N | 114 | J48 |
| V10 | MGTREFCLK0_115_P | 115 | J49 |
| V9 | MGTREFCLK0_115_N | 115 | J49 |
| T10 | MGTREFCLK1_115_P | 115 | J49 |
| T9 | MGTREFCLK1_115_N | 115 | J49 |

## USB to UART Bridge

[Figure 1-2, callout 20]

Communications between the ML628 board and a host computer are through a USB cable connected to J9. Control is provided by U26, a USB to UART bridge (Silicon Laboratories CP2103). Table 1-21 lists the pin assignments and signals for the USB connector J9.

*Table 1-21:* **USB Type B Connector Pin Assignments and Signals**

| J9 Pin | Signal Name | Description |
|---|---|---|
| 1 | VBUS | +5V into the CP2103 USB to UART bridge at U26. Used to sense USB network connection. |
| 2 | USB_DATA_N | Bidirectional differential serial data (N-side) |
| 3 | USB_DATA_P | Bidirectional differential serial data (P-side) |
| 4 | GROUND | Signal ground |

The CP2103 supports an IO voltage range of 1.8V to 2.5V on the ML628 board. The connections between the FPGA and CP2103 should use the LVCMOS25 IO standard. UART IP (for example, Xilinx® XPS UART Lite) must be implemented in the FPGA fabric. The FPGA supports the USB to UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 at U26 are listed in Table 1-22.

*Table 1-22:* **FPGA to U26 (CP2103 USB to UART Bridge) Connections**

| FPGA Pin | FPGA Function | Net Name | U26 Pin | U26 Function |
|---|---|---|---|---|
| E27 | RTS, output | USB_CTS | 22 | CTS, input |
| F27 | CTS, input | USB_RTS | 23 | RTS, output |
| B29 | TX, data out | USB_RX | 24 | RXD, data in |
| C29 | RX, data in | USB_TX | 25 | TXD, data out |

The bridge device also provides as many as 4 GPIO signals that can be defined by the user for status and control information (Table 1-23).

*Table 1-23:* **CP2103 USB to UART Bridge User GPIO**

| FPGA Pin | Net Name | U26 Pin |
|---|---|---|
| E28 | USB_GPIO0 | 19 |
| F28 | USB_GPIO1 | 18 |
| M27 | USB_GPIO2 | 17 |
| N27 | USB_GPIO3 | 16 |

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB to UART bridge to appear as a COM

port to the host computer communications application software (for example, HyperTermimal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the ML628 board.

## FMC HPC Connectors

[Figure 1-2, callouts 21a and 21b]

The ML628 board features two high pin count (HPC) connectors as defined by the VITA 57.1.1 FMC specification. The FMC HPC connector is a 10 x 40 position socket. See Appendix B, VITA 57.1 FMC HPC Connector Pinout, for a cross-reference of signal names to pin coordinates.

FMC1 HPC connector (J290) provides connectivity for:

- 80 differential user defined pairs:
  - 34 LA pairs
  - 24 HA pairs
  - 22 HB pairs
- 4 differential clocks

FMC2 HPC connector (J441) provides connectivity for:

- 76 differential user defined pairs:
  - 34 LA pairs
  - 24 HA pairs
  - 18 HB pairs
- 4 differential clocks

***Note:*** The $V_{ADJ}$ voltage for the FMC HPC connectors on the ML628 board is fixed at 2.5V (non-adjustable). The 2.5V rail cannot be turned off. The VITA 57.1 FMC interfaces on the ML628 board are compatible with 2.5V mezzanine cards capable of supporting 2.5V $V_{ADJ}$.

The FMC HPC connectors on the ML628 board are identified as: FMC1 at J290 and FMC2 at J441. The connections for each of these connectors are listed in Table 1-24 and Table 1-25 respectively.

*Table 1-24:* **VITA 57.1 FMC1 HPC Connections at J290**

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| AL22 | FMC1_CLK0_M2C_P | H4 |
| AM22 | FMC1_CLK0_M2C_N | H5 |
| N12 | FMC1_CLK1_M2C_P | G2 |
| M12 | FMC1_CLK1_M2C_N | G3 |
| AJ26 | FMC1_CLK2_M2C_P | K4 |
| AK27 | FMC1_CLK2_M2C_N | K5 |
| BB22 | FMC1_CLK3_M2C_P | J2 |
| BC22 | FMC1_CLK3_M2C_N | J3 |
| AY22 | FMC1_HA00_CC_P | F4 |
| BA22 | FMC1_HA00_CC_N | F5 |

*Table 1-24:* **VITA 57.1 FMC1 HPC Connections at J290 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| BA20 | FMC1_HA01_CC_P | E2 |
| BB20 | FMC1_HA01_CC_N | E3 |
| AU21 | FMC1_HA02_P | K7 |
| AV21 | FMC1_HA02_N | K8 |
| AN23 | FMC1_HA03_P | J6 |
| AN22 | FMC1_HA03_N | J7 |
| AW21 | FMC1_HA04_P | F7 |
| AY21 | FMC1_HA04_N | F8 |
| AV23 | FMC1_HA05_P | E6 |
| AW23 | FMC1_HA05_N | E7 |
| AP23 | FMC1_HA06_P | K10 |
| AR23 | FMC1_HA06_N | K11 |
| AY23 | FMC1_HA07_P | J9 |
| BA23 | FMC1_HA07_N | J10 |
| AW20 | FMC1_HA08_P | F10 |
| AY20 | FMC1_HA08_N | F11 |
| AT20 | FMC1_HA09_P | E9 |
| AU20 | FMC1_HA09_N | E10 |
| AV19 | FMC1_HA10_P | K13 |
| AW19 | FMC1_HA10_N | K14 |
| AU22 | FMC1_HA11_P | J12 |
| AV22 | FMC1_HA11_N | J13 |
| BA19 | FMC1_HA12_P | F13 |
| BB19 | FMC1_HA12_N | F14 |
| BC23 | FMC1_HA13_P | E12 |
| BD23 | FMC1_HA13_N | E13 |
| AT23 | FMC1_HA14_P | J15 |
| AT22 | FMC1_HA14_N | J16 |
| BB21 | FMC1_HA15_P | F16 |
| BC21 | FMC1_HA15_N | F17 |
| BC19 | FMC1_HA16_P | E15 |
| BD19 | FMC1_HA16_N | E16 |
| AR22 | FMC1_HA17_CC_P | K16 |

*Table 1-24:* **VITA 57.1 FMC1 HPC Connections at J290 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| AR21 | FMC1_HA17_CC_N | K17 |
| BD21 | FMC1_HA18_P | J18 |
| BD20 | FMC1_HA18_N | J19 |
| BA24 | FMC1_HA19_P | F19 |
| BB24 | FMC1_HA19_N | F20 |
| AN24 | FMC1_HA20_P | E18 |
| AP24 | FMC1_HA20_N | E19 |
| AT24 | FMC1_HA21_P | K19 |
| AU24 | FMC1_HA21_N | K20 |
| BC24 | FMC1_HA22_P | J21 |
| BD24 | FMC1_HA22_N | J22 |
| AL24 | FMC1_HA23_P | K22 |
| AM24 | FMC1_HA23_N | K23 |
| BA30 | FMC1_HB00_CC_P | K25 |
| BB30 | FMC1_HB00_CC_N | K26 |
| AW30 | FMC1_HB01_P | J24 |
| AY30 | FMC1_HB01_N | J25 |
| BD30 | FMC1_HB02_P | F22 |
| BD31 | FMC1_HB02_N | F23 |
| AL30 | FMC1_HB03_P | E21 |
| AM30 | FMC1_HB03_N | E22 |
| BB32 | FMC1_HB04_P | F25 |
| BC32 | FMC1_HB04_N | F26 |
| AY32 | FMC1_HB05_P | E24 |
| BA32 | FMC1_HB05_N | E25 |
| AU31 | FMC1_HB06_CC_P | K28 |
| AV31 | FMC1_HB06_CC_N | K29 |
| AM31 | FMC1_HB07_P | J27 |
| AM32 | FMC1_HB07_N | J28 |
| AW31 | FMC1_HB08_P | F28 |
| AY31 | FMC1_HB08_N | F29 |
| AR31 | FMC1_HB09_P | E27 |
| AT32 | FMC1_HB09_N | E28 |

*Table 1-24:* **VITA 57.1 FMC1 HPC Connections at J290 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| AK31 | FMC1_HB10_P | K31 |
| AL32 | FMC1_HB10_N | K32 |
| AP30 | FMC1_HB11_P | J30 |
| AR30 | FMC1_HB11_N | J31 |
| AT30 | FMC1_HB12_P | F31 |
| AU30 | FMC1_HB12_N | F32 |
| AJ30 | FMC1_HB13_P | E30 |
| AJ31 | FMC1_HB13_N | E31 |
| AU32 | FMC1_HB14_P | K34 |
| AV32 | FMC1_HB14_N | K35 |
| AP31 | FMC1_HB15_P | J33 |
| AR32 | FMC1_HB15_N | J34 |
| AN31 | FMC1_HB16_P | F34 |
| AN32 | FMC1_HB16_N | F35 |
| AJ29 | FMC1_HB17_CC_P | K37 |
| AK30 | FMC1_HB17_CC_N | K38 |
| AK32 | FMC1_HB18_P | J36 |
| AL33 | FMC1_HB18_N | J37 |
| BA33 | FMC1_HB19_P | E33 |
| BA34 | FMC1_HB19_N | E34 |
| AW35 | FMC1_HB20_P | F37 |
| AY35 | FMC1_HB20_N | F38 |
| AW33 | FMC1_HB21_P | E36 |
| AY33 | FMC1_HB21_N | E37 |
| C31 | FMC1_I2C_SDA | U27.10 |
| C30 | FMC1_I2C_SCL | U27.11 |
| AV24 | FMC1_LA00_CC_P | G6 |
| AW24 | FMC1_LA00_CC_N | G7 |
| BB26 | FMC1_LA01_CC_P | D8 |
| BC26 | FMC1_LA01_CC_N | D9 |
| AL25 | FMC1_LA02_P | H7 |
| AM25 | FMC1_LA02_N | H8 |
| AP25 | FMC1_LA03_P | G9 |

*Table 1-24:* **VITA 57.1 FMC1 HPC Connections at J290 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| AR25 | FMC1_LA03_N | G10 |
| AP26 | FMC1_LA04_P | H10 |
| AR26 | FMC1_LA04_N | H11 |
| AW25 | FMC1_LA05_P | D11 |
| AY25 | FMC1_LA05_N | D12 |
| AK22 | FMC1_LA06_P | C10 |
| AL23 | FMC1_LA06_N | C11 |
| AU26 | FMC1_LA07_P | H13 |
| AV26 | FMC1_LA07_N | H14 |
| BA25 | FMC1_LA08_P | G12 |
| BB25 | FMC1_LA08_N | G13 |
| AJ23 | FMC1_LA09_P | D14 |
| AK23 | FMC1_LA09_N | D15 |
| AW26 | FMC1_LA10_P | C14 |
| AY26 | FMC1_LA10_N | C15 |
| AM26 | FMC1_LA11_P | H16 |
| AN26 | FMC1_LA11_N | H17 |
| AT25 | FMC1_LA12_P | G15 |
| AU25 | FMC1_LA12_N | G16 |
| BC28 | FMC1_LA13_P | D17 |
| BD28 | FMC1_LA13_N | D18 |
| AJ24 | FMC1_LA14_P | C18 |
| AK25 | FMC1_LA14_N | C19 |
| AY27 | FMC1_LA15_P | H19 |
| BA27 | FMC1_LA15_N | H20 |
| BB27 | FMC1_LA16_P | G18 |
| BC27 | FMC1_LA16_N | G19 |
| AU27 | FMC1_LA17_CC_P | D20 |
| AV27 | FMC1_LA17_CC_N | D21 |
| AV28 | FMC1_LA18_CC_P | C22 |
| AW28 | FMC1_LA18_CC_N | C23 |
| AM27 | FMC1_LA19_P | H22 |
| AN27 | FMC1_LA19_N | H23 |

*Table 1-24:* **VITA 57.1 FMC1 HPC Connections at J290 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| BC29 | FMC1_LA20_P | G21 |
| BD29 | FMC1_LA20_N | G22 |
| BA29 | FMC1_LA21_P | H25 |
| BB29 | FMC1_LA21_N | H26 |
| AJ25 | FMC1_LA22_P | G24 |
| AK26 | FMC1_LA22_N | G25 |
| AY28 | FMC1_LA23_P | D23 |
| BA28 | FMC1_LA23_N | D24 |
| AR27 | FMC1_LA24_P | H28 |
| AT27 | FMC1_LA24_N | H29 |
| AL27 | FMC1_LA25_P | G27 |
| AL28 | FMC1_LA25_N | G28 |
| AT29 | FMC1_LA26_P | D26 |
| AU29 | FMC1_LA26_N | D27 |
| AR28 | FMC1_LA27_P | C26 |
| AT28 | FMC1_LA27_N | C27 |
| AJ28 | FMC1_LA28_P | H31 |
| AK28 | FMC1_LA28_N | H32 |
| AV29 | FMC1_LA29_P | G30 |
| AW29 | FMC1_LA29_N | G31 |
| AN28 | FMC1_LA30_P | H34 |
| AP28 | FMC1_LA30_N | H35 |
| AN29 | FMC1_LA31_P | G33 |
| AP29 | FMC1_LA31_N | G34 |
| BB31 | FMC1_LA32_P | H37 |
| BC31 | FMC1_LA32_N | H38 |
| AL29 | FMC1_LA33_P | G36 |
| AM29 | FMC1_LA33_N | G37 |
| BD25 | FMC1_PRSNT_M2C_L | H2 |
| U38.16 | FMC1_TCK | D29 |
| J31.1 / U5.2 / J6.61 | FMC1_TDI | D30 |

*Table 1-24:* **VITA 57.1 FMC1 HPC Connections at J290 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| U38.18 | FMC1_TMS | D33 |

**Notes:**

1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example, U27.9 = U27 pin 9.

*Table 1-25:* **VITA 57.1 FMC2 HPC Connections at J441**

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| BC6 | FMC2_CLK0_M2C_P | H4 |
| BD6 | FMC2_CLK0_M2C_N | H5 |
| AL13 | FMC2_CLK1_M2C_P | G2 |
| AL12 | FMC2_CLK1_M2C_N | G3 |
| AJ20 | FMC2_CLK2_M2C_P | K4 |
| AJ19 | FMC2_CLK2_M2C_N | K5 |
| BB5 | FMC2_CLK3_M2C_P | J2 |
| BB4 | FMC2_CLK3_M2C_N | J3 |
| AU11 | FMC2_HA00_CC_P | F4 |
| AU10 | FMC2_HA00_CC_N | F5 |
| AV9 | FMC2_HA01_CC_P | E2 |
| AW8 | FMC2_HA01_CC_N | E3 |
| AT12 | FMC2_HA02_P | K7 |
| AU12 | FMC2_HA02_N | K8 |
| AV12 | FMC2_HA03_P | J6 |
| AW11 | FMC2_HA03_N | J7 |
| AY7 | FMC2_HA04_P | F7 |
| AY6 | FMC2_HA04_N | F8 |
| AL17 | FMC2_HA05_P | E6 |
| AM16 | FMC2_HA05_N | E7 |
| AU7 | FMC2_HA06_P | K10 |
| AV6 | FMC2_HA06_N | K11 |
| AV11 | FMC2_HA07_P | J9 |
| AW10 | FMC2_HA07_N | J10 |
| AW9 | FMC2_HA08_P | F10 |
| AY8 | FMC2_HA08_N | F11 |
| AP14 | FMC2_HA09_P | E9 |

*Table 1-25:* **VITA 57.1 FMC2 HPC Connections at J441 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| AR13 | FMC2_HA09_N | E10 |
| AV7 | FMC2_HA10_P | K13 |
| AW6 | FMC2_HA10_N | K14 |
| AP11 | FMC2_HA11_P | J12 |
| AR11 | FMC2_HA11_N | J13 |
| AM15 | FMC2_HA12_P | F13 |
| AN14 | FMC2_HA12_N | F14 |
| AN13 | FMC2_HA13_P | E12 |
| AN12 | FMC2_HA13_N | E13 |
| AU9 | FMC2_HA14_P | J15 |
| AV8 | FMC2_HA14_N | J16 |
| AJ16 | FMC2_HA15_P | F16 |
| AJ15 | FMC2_HA15_N | F17 |
| AK17 | FMC2_HA16_P | E15 |
| AK16 | FMC2_HA16_N | E16 |
| AP13 | FMC2_HA17_CC_P | K16 |
| AR12 | FMC2_HA17_CC_N | K17 |
| AK15 | FMC2_HA18_P | J18 |
| AL15 | FMC2_HA18_N | J19 |
| AL14 | FMC2_HA19_P | F19 |
| AM14 | FMC2_HA19_N | F20 |
| AW1 | FMC2_HA20_P | E18 |
| AY1 | FMC2_HA20_N | E19 |
| BD5 | FMC2_HA21_P | K19 |
| BD4 | FMC2_HA21_N | K20 |
| AY2 | FMC2_HA22_P | J21 |
| BA2 | FMC2_HA22_N | J22 |
| BB2 | FMC2_HA23_P | K22 |
| BB1 | FMC2_HA23_N | K23 |
| BC13 | FMC2_HB00_CC_P | K25 |
| BC12 | FMC2_HB00_CC_N | K26 |
| BC16 | FMC2_HB01_P | J24 |
| BD15 | FMC2_HB01_N | J25 |

*Table 1-25:* **VITA 57.1 FMC2 HPC Connections at J441 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| BC17 | FMC2_HB02_P | F22 |
| BD16 | FMC2_HB02_N | F23 |
| AY17 | FMC2_HB03_P | E21 |
| AY16 | FMC2_HB03_N | E22 |
| BD14 | FMC2_HB04_P | F25 |
| BD13 | FMC2_HB04_N | F26 |
| BD11 | FMC2_HB05_P | E24 |
| BD10 | FMC2_HB05_N | E25 |
| BB16 | FMC2_HB06_CC_P | K28 |
| BB15 | FMC2_HB06_CC_N | K29 |
| AV16 | FMC2_HB07_P | J27 |
| AW16 | FMC2_HB07_N | J28 |
| BB12 | FMC2_HB08_P | F28 |
| BC11 | FMC2_HB08_N | F29 |
| AY18 | FMC2_HB09_P | E27 |
| BA18 | FMC2_HB09_N | E28 |
| AP21 | FMC2_HB10_P | K31 |
| AR20 | FMC2_HB10_N | K32 |
| AV18 | FMC2_HB11_P | J30 |
| AW18 | FMC2_HB11_N | J31 |
| BA17 | FMC2_HB12_P | F31 |
| BB17 | FMC2_HB12_N | F32 |
| AP20 | FMC2_HB13_P | E30 |
| AP19 | FMC2_HB13_N | E31 |
| AU17 | FMC2_HB14_P | K34 |
| AV17 | FMC2_HB14_N | K35 |
| AT19 | FMC2_HB15_P | J33 |
| AU19 | FMC2_HB15_N | J34 |
| AR18 | FMC2_HB16_P | F34 |
| AT18 | FMC2_HB16_N | F35 |
| AT17 | FMC2_HB17_CC_P | K37 |
| AU16 | FMC2_HB17_CC_N | K38 |
| U27.13 | FMC2_I2C_SDA(1) | C31 |

*Table 1-25:* **VITA 57.1 FMC2 HPC Connections at J441 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| U27.14 | FMC2_I2C_SCL(1) | C30 |
| BC8 | FMC2_LA00_CC_P | G6 |
| BC7 | FMC2_LA00_CC_N | G7 |
| BA5 | FMC2_LA01_CC_P | D8 |
| BA4 | FMC2_LA01_CC_N | D9 |
| BC3 | FMC2_LA02_P | H7 |
| BC2 | FMC2_LA02_N | H8 |
| AY3 | FMC2_LA03_P | G9 |
| BA3 | FMC2_LA03_N | G10 |
| BD9 | FMC2_LA04_P | H10 |
| BD8 | FMC2_LA04_N | H11 |
| AW5 | FMC2_LA05_P | D11 |
| AY5 | FMC2_LA05_N | D12 |
| BA12 | FMC2_LA06_P | C10 |
| BB11 | FMC2_LA06_N | C11 |
| BA8 | FMC2_LA07_P | H13 |
| BA7 | FMC2_LA07_N | H14 |
| AY12 | FMC2_LA08_P | G12 |
| AY11 | FMC2_LA08_N | G13 |
| BB10 | FMC2_LA09_P | D14 |
| BC9 | FMC2_LA09_N | D15 |
| BB7 | FMC2_LA10_P | C14 |
| BB6 | FMC2_LA10_N | C15 |
| AY10 | FMC2_LA11_P | H16 |
| BA9 | FMC2_LA11_N | H17 |
| BA10 | FMC2_LA12_P | G15 |
| BB9 | FMC2_LA12_N | G16 |
| AY15 | FMC2_LA13_P | D17 |
| BA15 | FMC2_LA13_N | D18 |
| AM21 | FMC2_LA14_P | C18 |
| AN21 | FMC2_LA14_N | C19 |
| BA14 | FMC2_LA15_P | H19 |
| BA13 | FMC2_LA15_N | H20 |

*Table 1-25:* **VITA 57.1 FMC2 HPC Connections at J441 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| AW13 | FMC2_LA16_P | G18 |
| AY13 | FMC2_LA16_N | G19 |
| AT14 | FMC2_LA17_CC_P | D20 |
| AT13 | FMC2_LA17_CC_N | D21 |
| AU15 | FMC2_LA18_CC_P | C22 |
| AV14 | FMC2_LA18_CC_N | C23 |
| AL20 | FMC2_LA19_P | H22 |
| AM20 | FMC2_LA19_N | H23 |
| AU14 | FMC2_LA20_P | G21 |
| AV13 | FMC2_LA20_N | G22 |
| AW15 | FMC2_LA21_P | H25 |
| AW14 | FMC2_LA21_N | H26 |
| AK20 | FMC2_LA22_P | G24 |
| AL19 | FMC2_LA22_N | G25 |
| AR15 | FMC2_LA23_P | D23 |
| AT15 | FMC2_LA23_N | D24 |
| AP18 | FMC2_LA24_P | H28 |
| AR17 | FMC2_LA24_N | H29 |
| AJ18 | FMC2_LA25_P | G27 |
| AK18 | FMC2_LA25_N | G28 |
| AM19 | FMC2_LA26_P | D26 |
| AN19 | FMC2_LA26_N | D27 |
| AN18 | FMC2_LA27_P | C26 |
| AN17 | FMC2_LA27_N | C27 |
| AJ21 | FMC2_LA28_P | H31 |
| AK21 | FMC2_LA28_N | H32 |
| AP16 | FMC2_LA29_P | G30 |
| AR16 | FMC2_LA29_N | G31 |
| AL18 | FMC2_LA30_P | H34 |
| AM17 | FMC2_LA30_N | H35 |
| AN16 | FMC2_LA31_P | G33 |
| AP15 | FMC2_LA31_N | G34 |
| BC18 | FMC2_LA32_P | H37 |

*Table 1-25:* **VITA 57.1 FMC2 HPC Connections at J441 *(Cont'd)***

| FPGA Pin | Net Name | FMC Pin |
|---|---|---|
| BD18 | FMC2_LA32_N | H38 |
| BB14 | FMC2_LA33_P | G36 |
| BC14 | FMC2_LA33_N | G37 |
| BC4 | FMC2_PRSNT_M2C_L | H2 |
| U38.15 | FMC2_TCK(1) | D29 |
| J31.2 / J64.1 | FMC2_TDI(1) | D30 |
| J162.3 / J64.2 | FMC2_TDO(1) | D31 |
| U38.17 | FMC2_TMS(1) | D33 |

**Notes:**

1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example, U27.9 = U27 pin 9.

*Table 1-26:* **Power Supply Voltages for the HPC Connector**

| Voltage Supply | Allowable Voltage Range | Number of Pins | Maximum Amps | Tolerance | Maximum Capacitive Load |
|---|---|---|---|---|---|
| $V_{ADJ}$ | Fixed 2.5V | 4 | 4 | ±5% | 1,000 µF |
| $3P3V_{AUX}$ | 3.3V | 1 | 0.020 | ±5% | 150 µF |
| 3P3V | 3.3V | 4 | 3 | ±5% | 1,000 µF |
| 12P0V | 12V | 2 | 1 | ±5% | 1,000 µF |

## System Monitor

[Figure 1-2, callout 22]

System Monitor measurements can be monitored using the ChipScope™ Pro tool. The ML628 board provides two ways of setting the System Monitor reference voltage:

- **Jumper pins 1-2 (EXT) on J15:** In this configuration, an on-board, low temperature coefficient, 1.25V reference (U14, Texas Instruments part number REF3012AIDBZT) is connected to System Monitor VREFP.
- **Jumper pins 2-3 (INT) on J15:** In this configuration, the FPGA's System Monitor uses an internal reference circuit.

***Note:*** A jumper should be installed in one of the two positions during normal operation.

## I²C Bus Management

[Figure 1-2, callout 23]

The I²C bus is controlled through U27, an 8-channel I²C-bus multiplexer (NXP Semiconductor PCA9547). The FPGA communicates with the multiplexer through I²C data and clock signals mapped to FPGA pins H34 and H33, respectively. The I²C idcode for the PCA9547 device is 0x70. The bus hosts five components:

- SuperClock-2 module
- GTH transceiver power supply module
- GTX transceiver power supply module
- FMC1
- FMC2

An $I^2C$ component can be accessed by selecting the appropriate channel through the control register of the MUX as shown in Table 1-27.

*Table 1-27:* **$I^2C$ Channel Assignments**

| U27 Channel | $I^2C$ Component |
|---|---|
| 0 | SuperClock-2 module |
| 1 | GTX transceiver power supply module |
| 2 | GTH transceiver power supply module |
| 3 | FMC1 |
| 4 | FMC2 |

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# Appendix A

# Default Jumper Positions

Table A-1 shows the standard (black) shunts that must be installed on the board for proper operation. Table A-2 shows the high current (red) shunts that must be installed to enable the on-board power supplies. These jumpers must always be installed except where specifically noted in this user guide. Refer to PCB Assembly Drawing 0431587 for the default placement of all on-board jumpers and their respective connectors as they are located on the board.

***Note:*** Any connector not shown in Table A-1 should be left open for normal operation.

*Table A-1:* **Standard Shunts**

| Connector | Name | Shunt Position | Quantity | Pins (Jumper Label) |
|---|---|---|---|---|
| J286 | PMBUS CTRL | Installed | 1 | 1-2 (GND) |
| J24 | AUX POR | Installed | 1 | 1–2 (AUTO) |
| J176 | VFS_0 | Installed | 1 | 1–2 (VCCAUX) |
| J188 | *SYSTEM CLOCK*(1) | Installed Horizontally | 2 | 1–3, 2–4 (LVDS) |
| J292 | PMBUS ALERT | Installed | 1 | 2–3 (AFX) |
| J293 | PMBUS CTRL | Installed | 1 | 2–3 (AFX) |
| J294 | PMBUS CLK | Installed | 1 | 2–3 (AFX) |
| J295 | PMBUS DATA | Installed | 1 | 2–3 (AFX) |
| J19 | *PMBUS LEVEL TRANSLATION*(1) | Installed | 1 | 1–2 (AFX/CABLE) |
| J287 | *PMBUS LEVEL TRANSLATION*(1) | Installed | 1 | 1–2 (AFX) |
| J162 | JTAG CHAIN | Installed | 1 | 1–2 (DUT ONLY) |
| J4 | SYSTEM ACE CLK | Installed | 1 | 1–2 (ON) |
| J22 | SYSACE JTAG ENABLE | Installed | 1 | 1–2 |
| J23 | SYSACE JTAG ENABLE | Installed | 1 | 1–2 |
| J195 | SYSACE JTAG ENABLE | Installed | 1 | 1–2 |
| J196 | SYSACE JTAG ENABLE | Installed | 1 | 1–2 |
| J15 | SYS MON | Installed | 1 | 1–2 (EXT) |
| J31 | FMC1 JTAG | Installed | 1 | 1-2 (BYPASS) |
| J64 | FMC2 JTAG | Installed | 1 | 1-2 (BYPASS) |

**Notes:**

1. Italicized entries in the Name column are not visible in the PCB silkscreen labels.

*Table A-2:* **Digital Power Shorting Plugs**

| Connector | Name | Shorting Plug Position |
|---|---|---|
| J30 | VCC3V3 | Installed |
| J32 | VCC2V5 | Installed |
| J102 | VCCINT_A | Installed |
| J61 | VCCINT_B | Installed |
| J104 | VCCAUX | Installed |
| J105 | VCCO | Installed |
| J129 | VCC5 | Installed |

# *VITA 57.1 FMC HPC Connector Pinout*

Table B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

| | K | J | H | G | F | E | D | C | B | A |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREF_B_M2C | GND | VREF_A_M2C | GND | PG_M2C | GND | PG_C2M | GND | RES1 | GND |
| 2 | GND | CLK3_M2C_P | PRSNT_M2C_L | CLK1_M2C_P | GND | HA01_P_CC | GND | DP0_C2M_P | GND | DP1_M2C_P |
| 3 | GND | CLK3_M2C_N | GND | CLK1_M2C_N | GND | HA01_N_CC | GND | DP0_C2M_N | GND | DP1_M2C_N |
| 4 | CLK2_M2C_P | GND | CLK0_M2C_P | GND | HA00_P_CC | GND | GBTCLK0_M2C_P | GND | DP9_M2C_P | GND |
| 5 | CLK2_M2C_N | GND | CLK0_M2C_N | GND | HA00_N_CC | GND | GBTCLK0_M2C_N | GND | DP9_M2C_N | GND |
| 6 | GND | HA03_P | GND | LA00_P_CC | GND | HA05_P | GND | DP0_M2C_P | GND | DP2_M2C_P |
| 7 | HA02_P | HA03_N | LA02_P | LA00_N_CC | HA04_P | HA05_N | GND | DP0_M2C_N | GND | DP2_M2C_N |
| 8 | HA02_N | GND | LA02_N | GND | HA04_N | GND | LA01_P_CC | GND | DP8_M2C_P | GND |
| 9 | GND | HA07_P | GND | LA03_P | GND | HA09_P | LA01_N_CC | GND | DP8_M2C_N | GND |
| 10 | HA06_P | HA07_N | LA04_P | LA03_N | HA08_P | HA09_N | GND | LA06_P | GND | DP3_M2C_P |
| 11 | HA06_N | GND | LA04_N | GND | HA08_N | GND | LA05_P | LA06_N | GND | DP3_M2C_N |
| 12 | GND | HA11_P | GND | LA08_P | GND | HA13_P | LA05_N | GND | DP7_M2C_P | GND |
| 13 | HA10_P | HA11_N | LA07_P | LA08_N | HA12_P | HA13_N | GND | GND | DP7_M2C_N | GND |
| 14 | HA10_N | GND | LA07_N | GND | HA12_N | GND | LA09_P | LA10_P | GND | DP4_M2C_P |
| 15 | GND | HA14_P | GND | LA12_P | GND | HA16_P | LA09_N | LA10_N | GND | DP4_M2C_N |
| 16 | HA17_P_CC | HA14_N | LA11_P | LA12_N | HA15_P | HA16_N | GND | GND | DP6_M2C_P | GND |
| 17 | HA17_N_CC | GND | LA11_N | GND | HA15_N | GND | LA13_P | GND | DP6_M2C_N | GND |
| 18 | GND | HA18_P | GND | LA16_P | GND | HA20_P | LA13_N | LA14_P | GND | DP5_M2C_P |
| 19 | HA21_P | HA18_N | LA15_P | LA16_N | HA19_P | HA20_N | GND | LA14_N | GND | DP5_M2C_N |
| 20 | HA21_N | GND | LA15_N | GND | HA19_N | GND | LA17_P_CC | GND | GBTCLK1_M2C_P | GND |
| 21 | GND | HA22_P | GND | LA20_P | GND | HB03_P | LA17_N_CC | GND | GBTCLK1_M2C_N | GND |
| 22 | HA23_P | HA22_N | LA19_P | LA20_N | HB02_P | HB03_N | GND | LA18_P_CC | GND | DP1_C2M_P |
| 23 | HA23_N | GND | LA19_N | GND | HB02_N | GND | LA23_P | LA18_N_CC | GND | DP1_C2M_N |
| 24 | GND | HB01_P | GND | LA22_P | GND | HB05_P | LA23_N | GND | DP9_C2M_P | GND |
| 25 | HB00_P_CC | HB01_N | LA21_P | LA22_N | HB04_P | HB05_N | GND | GND | DP9_C2M_N | GND |
| 26 | HB00_N_CC | GND | LA21_N | GND | HB04_N | GND | LA26_P | LA27_P | GND | DP2_C2M_P |
| 27 | GND | HB07_P | GND | LA25_P | GND | HB09_P | LA26_N | LA27_N | GND | DP2_C2M_N |
| 28 | HB06_P_CC | HB07_N | LA24_P | LA25_N | HB08_P | HB09_N | GND | GND | DP8_C2M_P | GND |
| 29 | HB06_N_CC | GND | LA24_N | GND | HB08_N | GND | TCK | GND | DP8_C2M_N | GND |
| 30 | GND | HB11_P | GND | LA29_P | GND | HB13_P | TDI | SCL | GND | DP3_C2M_P |
| 31 | HB10_P | HB11_N | LA28_P | LA29_N | HB12_P | HB13_N | TDO | SDA | GND | DP3_C2M_N |
| 32 | HB10_N | GND | LA28_N | GND | HB12_N | GND | 3P3VAUX | GND | DP7_C2M_P | GND |
| 33 | GND | HB15_P | GND | LA31_P | GND | HB19_P | TMS | GND | DP7_C2M_N | GND |
| 34 | HB14_P | HB15_N | LA30_P | LA31_N | HB16_P | HB19_N | TRST_L | GA0 | GND | DP4_C2M_P |
| 35 | HB14_N | GND | LA30_N | GND | HB16_N | GND | GA1 | 12P0V | GND | DP4_C2M_N |
| 36 | GND | HB18_P | GND | LA33_P | GND | HB21_P | 3P3V | GND | DP6_C2M_P | GND |
| 37 | HB17_P_CC | HB18_N | LA32_P | LA33_N | HB20_P | HB21_N | GND | 12P0V | DP6_C2M_N | GND |
| 38 | HB17_N_CC | GND | LA32_N | GND | HB20_N | GND | 3P3V | GND | GND | DP5_C2M_P |
| 39 | GND | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | DP5_C2M_N |
| 40 | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | RES0 | GND |

UG771_aB_01_100710

*Figure B-1:* **FMC HPC Connector Pinout**

Appendix C

# ML628 Master UCF Listing

The ML628 master user constraints file (UCF) template provides for designs targeting the ML628 Virtex-6 FPGA GTX and GTH transceiver characterization board. Net names in the constraints listed below correlate with net names on the ML628 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL. See the Constraints Guide for more information.

Users can refer to the UCF files generated by tools such as Memory Interface Generator (MIG) for memory interfaces and Base System Builder (BSB) for more detailed I/O standards information required for each particular interface. The FMC connectors J290 and J441 are connected to 2.5V $V_{cco}$ banks. Because each user's FMC card implements customer-specific circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

ML628 Master UCF Listing:

```
NET "APP_LED1"            LOC = "U1.N28";
NET "APP_LED2"            LOC = "U1.P28";
NET "APP_LED3"            LOC = "U1.K28";
NET "APP_LED4"            LOC = "U1.L27";
NET "APP_LED5"            LOC = "U1.K27";
NET "APP_LED6"            LOC = "U1.K26";
NET "APP_LED7"            LOC = "U1.P26";
NET "APP_LED8"            LOC = "U1.R26";
NET "CCLK_0"              LOC = "U1.AC33";
NET "CLK_1"               LOC = "U1.AP33";
NET "CLK_2"               LOC = "U1.R31";
NET "CLK_DIFF_1_N"        LOC = "U1.AP34";
NET "CLK_DIFF_1_P"        LOC = "U1.AN33";
NET "CLK_DIFF_2_N"        LOC = "U1.H33";
NET "CLK_DIFF_2_P"        LOC = "U1.J33";
NET "CM_CTRL_0"           LOC = "U1.G26";
NET "CM_CTRL_1"           LOC = "U1.G25";
NET "CM_CTRL_2"           LOC = "U1.H23";
NET "CM_CTRL_3"           LOC = "U1.J23";
NET "CM_CTRL_4"           LOC = "U1.J25";
NET "CM_CTRL_5"           LOC = "U1.K25";
NET "CM_CTRL_6"           LOC = "U1.D26";
NET "CM_CTRL_7"           LOC = "U1.E26";
NET "CM_CTRL_8"           LOC = "U1.D25";
NET "CM_CTRL_9"           LOC = "U1.E25";
NET "CM_CTRL_10"          LOC = "U1.M25";
NET "CM_CTRL_11"          LOC = "U1.M24";
NET "CM_CTRL_12"          LOC = "U1.A25";
NET "CM_CTRL_13"          LOC = "U1.B25";
NET "CM_CTRL_14"          LOC = "U1.L25";
```

```
NET "CM_CTRL_15"          LOC = "U1.L24";
NET "CM_CTRL_16"          LOC = "U1.B24";
NET "CM_CTRL_17"          LOC = "U1.C23";
NET "CM_CTRL_18"          LOC = "U1.C24";
NET "CM_CTRL_19"          LOC = "U1.D23";
NET "CM_CTRL_20"          LOC = "U1.K23";
NET "CM_CTRL_21"          LOC = "U1.L23";
NET "CM_CTRL_22"          LOC = "U1.B26";
NET "CM_CTRL_23"          LOC = "U1.C26";
NET "CM_GCLK_N"           LOC = "U1.A24";
NET "CM_GCLK_P"           LOC = "U1.A23";
NET "CM_LVDS1_N"          LOC = "U1.B36";
NET "CM_LVDS1_P"          LOC = "U1.B35";
NET "CM_LVDS2_N"          LOC = "U1.C11";
NET "CM_LVDS2_P"          LOC = "U1.C12";
NET "CM_LVDS3_N"          LOC = "U1.BD33";
NET "CM_LVDS3_P"          LOC = "U1.BC33";
NET "CM_RST"              LOC = "U1.D24";
NET "DUT_I2C_SCL"         LOC = "U1.R25";
NET "DUT_I2C_SDA"         LOC = "U1.P25";
NET "DUT_PMB_ALERT"       LOC = "U1.G27";
NET "DUT_PMB_CLK"         LOC = "U1.F29";
NET "DUT_PMB_CTRL"        LOC = "U1.H27";
NET "DUT_PMB_DATA"        LOC = "U1.G29";
NET "FMC1_CLK0_M2C_N"     LOC = "U1.AM22";
NET "FMC1_CLK0_M2C_P"     LOC = "U1.AL22";
NET "FMC1_CLK1_M2C_N"     LOC = "U1.M12";
NET "FMC1_CLK1_M2C_P"     LOC = "U1.N12";
NET "FMC1_CLK2_M2C_N"     LOC = "U1.AK27";
NET "FMC1_CLK2_M2C_P"     LOC = "U1.AJ26";
NET "FMC1_CLK3_M2C_N"     LOC = "U1.BC22";
NET "FMC1_CLK3_M2C_P"     LOC = "U1.BB22";
NET "FMC1_HA00_CC_N"      LOC = "U1.BA22";
NET "FMC1_HA00_CC_P"      LOC = "U1.AY22";
NET "FMC1_HA01_CC_N"      LOC = "U1.BB20";
NET "FMC1_HA01_CC_P"      LOC = "U1.BA20";
NET "FMC1_HA02_N"         LOC = "U1.AV21";
NET "FMC1_HA02_P"         LOC = "U1.AU21";
NET "FMC1_HA03_N"         LOC = "U1.AN22";
NET "FMC1_HA03_P"         LOC = "U1.AN23";
NET "FMC1_HA04_N"         LOC = "U1.AY21";
NET "FMC1_HA04_P"         LOC = "U1.AW21";
NET "FMC1_HA05_N"         LOC = "U1.AW23";
NET "FMC1_HA05_P"         LOC = "U1.AV23";
NET "FMC1_HA06_N"         LOC = "U1.AR23";
NET "FMC1_HA06_P"         LOC = "U1.AP23";
NET "FMC1_HA07_N"         LOC = "U1.BA23";
NET "FMC1_HA07_P"         LOC = "U1.AY23";
NET "FMC1_HA08_N"         LOC = "U1.AY20";
NET "FMC1_HA08_P"         LOC = "U1.AW20";
NET "FMC1_HA09_N"         LOC = "U1.AU20";
NET "FMC1_HA09_P"         LOC = "U1.AT20";
NET "FMC1_HA10_N"         LOC = "U1.AW19";
NET "FMC1_HA10_P"         LOC = "U1.AV19";
NET "FMC1_HA11_N"         LOC = "U1.AV22";
NET "FMC1_HA11_P"         LOC = "U1.AU22";
NET "FMC1_HA12_N"         LOC = "U1.BB19";
NET "FMC1_HA12_P"         LOC = "U1.BA19";
NET "FMC1_HA13_N"         LOC = "U1.BD23";
```

```
NET "FMC1_HA13_P"          LOC = "U1.BC23";
NET "FMC1_HA14_N"          LOC = "U1.AT22";
NET "FMC1_HA14_P"          LOC = "U1.AT23";
NET "FMC1_HA15_N"          LOC = "U1.BC21";
NET "FMC1_HA15_P"          LOC = "U1.BB21";
NET "FMC1_HA16_N"          LOC = "U1.BD19";
NET "FMC1_HA16_P"          LOC = "U1.BC19";
NET "FMC1_HA17_CC_N"       LOC = "U1.AR21";
NET "FMC1_HA17_CC_P"       LOC = "U1.AR22";
NET "FMC1_HA18_N"          LOC = "U1.BD20";
NET "FMC1_HA18_P"          LOC = "U1.BD21";
NET "FMC1_HA19_N"          LOC = "U1.BB24";
NET "FMC1_HA19_P"          LOC = "U1.BA24";
NET "FMC1_HA20_N"          LOC = "U1.AP24";
NET "FMC1_HA20_P"          LOC = "U1.AN24";
NET "FMC1_HA21_N"          LOC = "U1.AU24";
NET "FMC1_HA21_P"          LOC = "U1.AT24";
NET "FMC1_HA22_N"          LOC = "U1.BD24";
NET "FMC1_HA22_P"          LOC = "U1.BC24";
NET "FMC1_HA23_N"          LOC = "U1.AM24";
NET "FMC1_HA23_P"          LOC = "U1.AL24";
NET "FMC1_HB00_CC_N"       LOC = "U1.BB30";
NET "FMC1_HB00_CC_P"       LOC = "U1.BA30";
NET "FMC1_HB01_N"          LOC = "U1.AY30";
NET "FMC1_HB01_P"          LOC = "U1.AW30";
NET "FMC1_HB02_N"          LOC = "U1.BD31";
NET "FMC1_HB02_P"          LOC = "U1.BD30";
NET "FMC1_HB03_N"          LOC = "U1.AM30";
NET "FMC1_HB03_P"          LOC = "U1.AL30";
NET "FMC1_HB04_N"          LOC = "U1.BC32";
NET "FMC1_HB04_P"          LOC = "U1.BB32";
NET "FMC1_HB05_N"          LOC = "U1.BA32";
NET "FMC1_HB05_P"          LOC = "U1.AY32";
NET "FMC1_HB06_CC_N"       LOC = "U1.AV31";
NET "FMC1_HB06_CC_P"       LOC = "U1.AU31";
NET "FMC1_HB07_N"          LOC = "U1.AM32";
NET "FMC1_HB07_P"          LOC = "U1.AM31";
NET "FMC1_HB08_N"          LOC = "U1.AY31";
NET "FMC1_HB08_P"          LOC = "U1.AW31";
NET "FMC1_HB09_N"          LOC = "U1.AT32";
NET "FMC1_HB09_P"          LOC = "U1.AR31";
NET "FMC1_HB10_N"          LOC = "U1.AL32";
NET "FMC1_HB10_P"          LOC = "U1.AK31";
NET "FMC1_HB11_N"          LOC = "U1.AR30";
NET "FMC1_HB11_P"          LOC = "U1.AP30";
NET "FMC1_HB12_N"          LOC = "U1.AU30";
NET "FMC1_HB12_P"          LOC = "U1.AT30";
NET "FMC1_HB13_N"          LOC = "U1.AJ31";
NET "FMC1_HB13_P"          LOC = "U1.AJ30";
NET "FMC1_HB14_N"          LOC = "U1.AV32";
NET "FMC1_HB14_P"          LOC = "U1.AU32";
NET "FMC1_HB15_N"          LOC = "U1.AR32";
NET "FMC1_HB15_P"          LOC = "U1.AP31";
NET "FMC1_HB16_N"          LOC = "U1.AN32";
NET "FMC1_HB16_P"          LOC = "U1.AN31";
NET "FMC1_HB17_CC_N"       LOC = "U1.AK30";
NET "FMC1_HB17_CC_P"       LOC = "U1.AJ29";
NET "FMC1_HB18_N"          LOC = "U1.AL33";
NET "FMC1_HB18_P"          LOC = "U1.AK32";
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NET "FMC1_HB19_N"          LOC = "U1.BA34";
NET "FMC1_HB19_P"          LOC = "U1.BA33";
NET "FMC1_HB20_N"          LOC = "U1.AY35";
NET "FMC1_HB20_P"          LOC = "U1.AW35";
NET "FMC1_HB21_N"          LOC = "U1.AY33";
NET "FMC1_HB21_P"          LOC = "U1.AW33";
NET "FMC1_LA00_CC_N"       LOC = "U1.AW24";
NET "FMC1_LA00_CC_P"       LOC = "U1.AV24";
NET "FMC1_LA01_CC_N"       LOC = "U1.BC26";
NET "FMC1_LA01_CC_P"       LOC = "U1.BB26";
NET "FMC1_LA02_N"          LOC = "U1.AM25";
NET "FMC1_LA02_P"          LOC = "U1.AL25";
NET "FMC1_LA03_N"          LOC = "U1.AR25";
NET "FMC1_LA03_P"          LOC = "U1.AP25";
NET "FMC1_LA04_N"          LOC = "U1.AR26";
NET "FMC1_LA04_P"          LOC = "U1.AP26";
NET "FMC1_LA05_N"          LOC = "U1.AY25";
NET "FMC1_LA05_P"          LOC = "U1.AW25";
NET "FMC1_LA06_N"          LOC = "U1.AL23";
NET "FMC1_LA06_P"          LOC = "U1.AK22";
NET "FMC1_LA07_N"          LOC = "U1.AV26";
NET "FMC1_LA07_P"          LOC = "U1.AU26";
NET "FMC1_LA08_N"          LOC = "U1.BB25";
NET "FMC1_LA08_P"          LOC = "U1.BA25";
NET "FMC1_LA09_N"          LOC = "U1.AK23";
NET "FMC1_LA09_P"          LOC = "U1.AJ23";
NET "FMC1_LA10_N"          LOC = "U1.AY26";
NET "FMC1_LA10_P"          LOC = "U1.AW26";
NET "FMC1_LA11_N"          LOC = "U1.AN26";
NET "FMC1_LA11_P"          LOC = "U1.AM26";
NET "FMC1_LA12_N"          LOC = "U1.AU25";
NET "FMC1_LA12_P"          LOC = "U1.AT25";
NET "FMC1_LA13_N"          LOC = "U1.BD28";
NET "FMC1_LA13_P"          LOC = "U1.BC28";
NET "FMC1_LA14_N"          LOC = "U1.AK25";
NET "FMC1_LA14_P"          LOC = "U1.AJ24";
NET "FMC1_LA15_N"          LOC = "U1.BA27";
NET "FMC1_LA15_P"          LOC = "U1.AY27";
NET "FMC1_LA16_N"          LOC = "U1.BC27";
NET "FMC1_LA16_P"          LOC = "U1.BB27";
NET "FMC1_LA17_CC_N"       LOC = "U1.AV27";
NET "FMC1_LA17_CC_P"       LOC = "U1.AU27";
NET "FMC1_LA18_CC_N"       LOC = "U1.AW28";
NET "FMC1_LA18_CC_P"       LOC = "U1.AV28";
NET "FMC1_LA19_N"          LOC = "U1.AN27";
NET "FMC1_LA19_P"          LOC = "U1.AM27";
NET "FMC1_LA20_N"          LOC = "U1.BD29";
NET "FMC1_LA20_P"          LOC = "U1.BC29";
NET "FMC1_LA21_N"          LOC = "U1.BB29";
NET "FMC1_LA21_P"          LOC = "U1.BA29";
NET "FMC1_LA22_N"          LOC = "U1.AK26";
NET "FMC1_LA22_P"          LOC = "U1.AJ25";
NET "FMC1_LA23_N"          LOC = "U1.BA28";
NET "FMC1_LA23_P"          LOC = "U1.AY28";
NET "FMC1_LA24_N"          LOC = "U1.AT27";
NET "FMC1_LA24_P"          LOC = "U1.AR27";
NET "FMC1_LA25_N"          LOC = "U1.AL28";
NET "FMC1_LA25_P"          LOC = "U1.AL27";
NET "FMC1_LA26_N"          LOC = "U1.AU29";
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NET "FMC1_LA26_P”          LOC = "U1.AT29";
NET "FMC1_LA27_N”          LOC = "U1.AT28";
NET "FMC1_LA27_P”          LOC = "U1.AR28";
NET "FMC1_LA28_N”          LOC = "U1.AK28";
NET "FMC1_LA28_P”          LOC = "U1.AJ28";
NET "FMC1_LA29_N”          LOC = "U1.AW29";
NET "FMC1_LA29_P”          LOC = "U1.AV29";
NET "FMC1_LA30_N”          LOC = "U1.AP28";
NET "FMC1_LA30_P”          LOC = "U1.AN28";
NET "FMC1_LA31_N”          LOC = "U1.AP29";
NET "FMC1_LA31_P”          LOC = "U1.AN29";
NET "FMC1_LA32_N”          LOC = "U1.BC31";
NET "FMC1_LA32_P”          LOC = "U1.BB31";
NET "FMC1_LA33_N”          LOC = "U1.AM29";
NET "FMC1_LA33_P”          LOC = "U1.AL29";
NET "FMC1_PRSNT_M2C_L”     LOC = "U1.BD25";
NET "FMC2_CLK0_M2C_N”      LOC = "U1.BD6";
NET "FMC2_CLK0_M2C_P”      LOC = "U1.BC6";
NET "FMC2_CLK1_M2C_N”      LOC = "U1.AL12";
NET "FMC2_CLK1_M2C_P”      LOC = "U1.AL13";
NET "FMC2_CLK2_M2C_N”      LOC = "U1.AJ19";
NET "FMC2_CLK2_M2C_P”      LOC = "U1.AJ20";
NET "FMC2_CLK3_M2C_N”      LOC = "U1.BB4";
NET "FMC2_CLK3_M2C_P”      LOC = "U1.BB5";
NET "FMC2_HA00_CC_N”       LOC = "U1.AU10";
NET "FMC2_HA00_CC_P”       LOC = "U1.AU11";
NET "FMC2_HA01_CC_N”       LOC = "U1.AW8";
NET "FMC2_HA01_CC_P”       LOC = "U1.AV9";
NET "FMC2_HA02_N”          LOC = "U1.AU12";
NET "FMC2_HA02_P”          LOC = "U1.AT12";
NET "FMC2_HA03_N”          LOC = "U1.AW11";
NET "FMC2_HA03_P”          LOC = "U1.AV12";
NET "FMC2_HA04_N”          LOC = "U1.AY6";
NET "FMC2_HA04_P”          LOC = "U1.AY7";
NET "FMC2_HA05_N”          LOC = "U1.AM16";
NET "FMC2_HA05_P”          LOC = "U1.AL17";
NET "FMC2_HA06_N”          LOC = "U1.AV6";
NET "FMC2_HA06_P”          LOC = "U1.AU7";
NET "FMC2_HA07_N”          LOC = "U1.AW10";
NET "FMC2_HA07_P”          LOC = "U1.AV11";
NET "FMC2_HA08_N”          LOC = "U1.AY8";
NET "FMC2_HA08_P”          LOC = "U1.AW9";
NET "FMC2_HA09_N”          LOC = "U1.AR13";
NET "FMC2_HA09_P”          LOC = "U1.AP14";
NET "FMC2_HA10_N”          LOC = "U1.AW6";
NET "FMC2_HA10_P”          LOC = "U1.AV7";
NET "FMC2_HA11_N”          LOC = "U1.AR11";
NET "FMC2_HA11_P”          LOC = "U1.AP11";
NET "FMC2_HA12_N”          LOC = "U1.AN14";
NET "FMC2_HA12_P”          LOC = "U1.AM15";
NET "FMC2_HA13_N”          LOC = "U1.AN12";
NET "FMC2_HA13_P”          LOC = "U1.AN13";
NET "FMC2_HA14_N”          LOC = "U1.AV8";
NET "FMC2_HA14_P”          LOC = "U1.AU9";
NET "FMC2_HA15_N”          LOC = "U1.AJ15";
NET "FMC2_HA15_P”          LOC = "U1.AJ16";
NET "FMC2_HA16_N”          LOC = "U1.AK16";
NET "FMC2_HA16_P”          LOC = "U1.AK17";
NET "FMC2_HA17_CC_N”       LOC = "U1.AR12";
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NET "FMC2_HA17_CC_P"       LOC = "U1.AP13";
NET "FMC2_HA18_N"          LOC = "U1.AL15";
NET "FMC2_HA18_P"          LOC = "U1.AK15";
NET "FMC2_HA19_N"          LOC = "U1.AM14";
NET "FMC2_HA19_P"          LOC = "U1.AL14";
NET "FMC2_HA20_N"          LOC = "U1.AY1";
NET "FMC2_HA20_P"          LOC = "U1.AW1";
NET "FMC2_HA21_N"          LOC = "U1.BD4";
NET "FMC2_HA21_P"          LOC = "U1.BD5";
NET "FMC2_HA22_N"          LOC = "U1.BA2";
NET "FMC2_HA22_P"          LOC = "U1.AY2";
NET "FMC2_HA23_N"          LOC = "U1.BB1";
NET "FMC2_HA23_P"          LOC = "U1.BB2";
NET "FMC2_HB00_CC_N"       LOC = "U1.BC12";
NET "FMC2_HB00_CC_P"       LOC = "U1.BC13";
NET "FMC2_HB01_N"          LOC = "U1.BD15";
NET "FMC2_HB01_P"          LOC = "U1.BC16";
NET "FMC2_HB02_N"          LOC = "U1.BD16";
NET "FMC2_HB02_P"          LOC = "U1.BC17";
NET "FMC2_HB03_N"          LOC = "U1.AY16";
NET "FMC2_HB03_P"          LOC = "U1.AY17";
NET "FMC2_HB04_N"          LOC = "U1.BD13";
NET "FMC2_HB04_P"          LOC = "U1.BD14";
NET "FMC2_HB05_N"          LOC = "U1.BD10";
NET "FMC2_HB05_P"          LOC = "U1.BD11";
NET "FMC2_HB06_CC_N"       LOC = "U1.BB15";
NET "FMC2_HB06_CC_P"       LOC = "U1.BB16";
NET "FMC2_HB07_N"          LOC = "U1.AW16";
NET "FMC2_HB07_P"          LOC = "U1.AV16";
NET "FMC2_HB08_N"          LOC = "U1.BC11";
NET "FMC2_HB08_P"          LOC = "U1.BB12";
NET "FMC2_HB09_N"          LOC = "U1.BA18";
NET "FMC2_HB09_P"          LOC = "U1.AY18";
NET "FMC2_HB10_N"          LOC = "U1.AR20";
NET "FMC2_HB10_P"          LOC = "U1.AP21";
NET "FMC2_HB11_N"          LOC = "U1.AW18";
NET "FMC2_HB11_P"          LOC = "U1.AV18";
NET "FMC2_HB12_N"          LOC = "U1.BB17";
NET "FMC2_HB12_P"          LOC = "U1.BA17";
NET "FMC2_HB13_N"          LOC = "U1.AP19";
NET "FMC2_HB13_P"          LOC = "U1.AP20";
NET "FMC2_HB14_N"          LOC = "U1.AV17";
NET "FMC2_HB14_P"          LOC = "U1.AU17";
NET "FMC2_HB15_N"          LOC = "U1.AU19";
NET "FMC2_HB15_P"          LOC = "U1.AT19";
NET "FMC2_HB16_N"          LOC = "U1.AT18";
NET "FMC2_HB16_P"          LOC = "U1.AR18";
NET "FMC2_HB17_CC_N"       LOC = "U1.AU16";
NET "FMC2_HB17_CC_P"       LOC = "U1.AT17";
NET "FMC2_LA00_CC_N"       LOC = "U1.BC7";
NET "FMC2_LA00_CC_P"       LOC = "U1.BC8";
NET "FMC2_LA01_CC_N"       LOC = "U1.BA4";
NET "FMC2_LA01_CC_P"       LOC = "U1.BA5";
NET "FMC2_LA02_N"          LOC = "U1.BC2";
NET "FMC2_LA02_P"          LOC = "U1.BC3";
NET "FMC2_LA03_N"          LOC = "U1.BA3";
NET "FMC2_LA03_P"          LOC = "U1.AY3";
NET "FMC2_LA04_N"          LOC = "U1.BD8";
NET "FMC2_LA04_P"          LOC = "U1.BD9";
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NET "FMC2_LA05_N"          LOC = "U1.AY5";
NET "FMC2_LA05_P"          LOC = "U1.AW5";
NET "FMC2_LA06_N"          LOC = "U1.BB11";
NET "FMC2_LA06_P"          LOC = "U1.BA12";
NET "FMC2_LA07_N"          LOC = "U1.BA7";
NET "FMC2_LA07_P"          LOC = "U1.BA8";
NET "FMC2_LA08_N"          LOC = "U1.AY11";
NET "FMC2_LA08_P"          LOC = "U1.AY12";
NET "FMC2_LA09_N"          LOC = "U1.BC9";
NET "FMC2_LA09_P"          LOC = "U1.BB10";
NET "FMC2_LA10_N"          LOC = "U1.BB6";
NET "FMC2_LA10_P"          LOC = "U1.BB7";
NET "FMC2_LA11_N"          LOC = "U1.BA9";
NET "FMC2_LA11_P"          LOC = "U1.AY10";
NET "FMC2_LA12_N"          LOC = "U1.BB9";
NET "FMC2_LA12_P"          LOC = "U1.BA10";
NET "FMC2_LA13_N"          LOC = "U1.BA15";
NET "FMC2_LA13_P"          LOC = "U1.AY15";
NET "FMC2_LA14_N"          LOC = "U1.AN21";
NET "FMC2_LA14_P"          LOC = "U1.AM21";
NET "FMC2_LA15_N"          LOC = "U1.BA13";
NET "FMC2_LA15_P"          LOC = "U1.BA14";
NET "FMC2_LA16_N"          LOC = "U1.AY13";
NET "FMC2_LA16_P"          LOC = "U1.AW13";
NET "FMC2_LA17_CC_N"       LOC = "U1.AT13";
NET "FMC2_LA17_CC_P"       LOC = "U1.AT14";
NET "FMC2_LA18_CC_N"       LOC = "U1.AV14";
NET "FMC2_LA18_CC_P"       LOC = "U1.AU15";
NET "FMC2_LA19_N"          LOC = "U1.AM20";
NET "FMC2_LA19_P"          LOC = "U1.AL20";
NET "FMC2_LA20_N"          LOC = "U1.AV13";
NET "FMC2_LA20_P"          LOC = "U1.AU14";
NET "FMC2_LA21_N"          LOC = "U1.AW14";
NET "FMC2_LA21_P"          LOC = "U1.AW15";
NET "FMC2_LA22_N"          LOC = "U1.AL19";
NET "FMC2_LA22_P"          LOC = "U1.AK20";
NET "FMC2_LA23_N"          LOC = "U1.AT15";
NET "FMC2_LA23_P"          LOC = "U1.AR15";
NET "FMC2_LA24_N"          LOC = "U1.AR17";
NET "FMC2_LA24_P"          LOC = "U1.AP18";
NET "FMC2_LA25_N"          LOC = "U1.AK18";
NET "FMC2_LA25_P"          LOC = "U1.AJ18";
NET "FMC2_LA26_N"          LOC = "U1.AN19";
NET "FMC2_LA26_P"          LOC = "U1.AM19";
NET "FMC2_LA27_N"          LOC = "U1.AN17";
NET "FMC2_LA27_P"          LOC = "U1.AN18";
NET "FMC2_LA28_N"          LOC = "U1.AK21";
NET "FMC2_LA28_P"          LOC = "U1.AJ21";
NET "FMC2_LA29_N"          LOC = "U1.AR16";
NET "FMC2_LA29_P"          LOC = "U1.AP16";
NET "FMC2_LA30_N"          LOC = "U1.AM17";
NET "FMC2_LA30_P"          LOC = "U1.AL18";
NET "FMC2_LA31_N"          LOC = "U1.AP15";
NET "FMC2_LA31_P"          LOC = "U1.AN16";
NET "FMC2_LA32_N"          LOC = "U1.BD18";
NET "FMC2_LA32_P"          LOC = "U1.BC18";
NET "FMC2_LA33_N"          LOC = "U1.BC14";
NET "FMC2_LA33_P"          LOC = "U1.BB14";
NET "FMC2_PRSNT_M2C_L"     LOC = "U1.BC4";
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NET "GTH_MOD_SPI_CS"       LOC = "U1.F25";
NET "GTX_MOD_SPI_CS"       LOC = "U1.N23";
NET "MGTREFCLK0_100_N"     LOC = "U1.BA38";
NET "MGTREFCLK0_100_P"     LOC = "U1.BA37";
NET "MGTREFCLK0_101_N"     LOC = "U1.AU38";
NET "MGTREFCLK0_101_P"     LOC = "U1.AU37";
NET "MGTREFCLK0_102_N"     LOC = "U1.AN38";
NET "MGTREFCLK0_102_P"     LOC = "U1.AN37";
NET "MGTREFCLK0_103_N"     LOC = "U1.AF36";
NET "MGTREFCLK0_103_P"     LOC = "U1.AF35";
NET "MGTREFCLK0_104_N"     LOC = "U1.AB36";
NET "MGTREFCLK0_104_P"     LOC = "U1.AB35";
NET "MGTREFCLK0_105_N"     LOC = "U1.V36";
NET "MGTREFCLK0_105_P"     LOC = "U1.V35";
NET "MGTREFCLK0_112_N"     LOC = "U1.AN7";
NET "MGTREFCLK0_112_P"     LOC = "U1.AN8";
NET "MGTREFCLK0_113_N"     LOC = "U1.AF9";
NET "MGTREFCLK0_113_P"     LOC = "U1.AF10";
NET "MGTREFCLK0_114_N"     LOC = "U1.AB9";
NET "MGTREFCLK0_114_P"     LOC = "U1.AB10";
NET "MGTREFCLK0_115_N"     LOC = "U1.V9";
NET "MGTREFCLK0_115_P"     LOC = "U1.V10";
NET "MGTREFCLK1_100_N"     LOC = "U1.AW38";
NET "MGTREFCLK1_100_P"     LOC = "U1.AW37";
NET "MGTREFCLK1_101_N"     LOC = "U1.AR38";
NET "MGTREFCLK1_101_P"     LOC = "U1.AR37";
NET "MGTREFCLK1_102_N"     LOC = "U1.AH36";
NET "MGTREFCLK1_102_P"     LOC = "U1.AH35";
NET "MGTREFCLK1_103_N"     LOC = "U1.AD36";
NET "MGTREFCLK1_103_P"     LOC = "U1.AD35";
NET "MGTREFCLK1_104_N"     LOC = "U1.Y36";
NET "MGTREFCLK1_104_P"     LOC = "U1.Y35";
NET "MGTREFCLK1_105_N"     LOC = "U1.T36";
NET "MGTREFCLK1_105_P"     LOC = "U1.T35";
NET "MGTREFCLK1_112_N"     LOC = "U1.AH9";
NET "MGTREFCLK1_112_P"     LOC = "U1.AH10";
NET "MGTREFCLK1_113_N"     LOC = "U1.AD9";
NET "MGTREFCLK1_113_P"     LOC = "U1.AD10";
NET "MGTREFCLK1_114_N"     LOC = "U1.Y9";
NET "MGTREFCLK1_114_P"     LOC = "U1.Y10";
NET "MGTREFCLK1_115_N"     LOC = "U1.T9";
NET "MGTREFCLK1_115_P"     LOC = "U1.T10";
NET "MGTREFCLK_106_N"      LOC = "U1.R42";
NET "MGTREFCLK_106_P"      LOC = "U1.R41";
NET "MGTREFCLK_107_N"      LOC = "U1.J42";
NET "MGTREFCLK_107_P"      LOC = "U1.J41";
NET "MGTREFCLK_108_N"      LOC = "U1.E42";
NET "MGTREFCLK_108_P"      LOC = "U1.E41";
NET "MGTREFCLK_116_N"      LOC = "U1.R3";
NET "MGTREFCLK_116_P"      LOC = "U1.R4";
NET "MGTREFCLK_117_N"      LOC = "U1.J3";
NET "MGTREFCLK_117_P"      LOC = "U1.J4";
NET "MGTREFCLK_118_N"      LOC = "U1.E3";
NET "MGTREFCLK_118_P"      LOC = "U1.E4";
NET "MGTRX0_100_N"         LOC = "U1.BD39";
NET "MGTRX0_100_P"         LOC = "U1.BD40";
NET "MGTRX0_101_N"         LOC = "U1.AY39";
NET "MGTRX0_101_P"         LOC = "U1.AY40";
NET "MGTRX0_102_N"         LOC = "U1.AL37";
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NET "MGTRX0_102_P"          LOC = "U1.AL38";
NET "MGTRX0_103_N"          LOC = "U1.AH39";
NET "MGTRX0_103_P"          LOC = "U1.AH40";
NET "MGTRX0_104_N"          LOC = "U1.AD39";
NET "MGTRX0_104_P"          LOC = "U1.AD40";
NET "MGTRX0_105_N"          LOC = "U1.Y39";
NET "MGTRX0_105_P"          LOC = "U1.Y40";
NET "MGTRX0_106_N"          LOC = "U1.U42";
NET "MGTRX0_106_P"          LOC = "U1.U41";
NET "MGTRX0_107_N"          LOC = "U1.K40";
NET "MGTRX0_107_P"          LOC = "U1.K39";
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*Appendix D*

# *References*

Additional information relevant to Virtex®-6 devices, the ML628 Virtex-6 FPGA GTX and GTH transceiver characterization board, and intellectual property is available in the documents listed here:

- UG806, *ML628 IBERT Getting Started Guide*
- DS150, *Virtex-6 Family Overview*
- DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*
- UG360, *Virtex-6 FPGA Configuration User Guide*
- UG361, *Virtex-6 FPGA SelectIO Resources User Guide*
- UG362, *Virtex-6 FPGA User Guide: Clocking Resources*
- UG364, *Virtex-6 FPGA Configurable Logic Block User Guide*
- UG365, *Virtex-6 FPGA Packaging and Pinout Specifications*
- UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
- UG370, *Virtex-6 FPGA System Monitor User Guide*
- UG371, *Virtex-6 FPGA GTH Transceivers User Guide*
- DS581, *XPS External Peripheral Controller (EPC) Data Sheet*
- DS606, *XPS IIC Bus Interface (v2.00a) Data Sheet*
- UG770, *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide*

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.