Si721x Field Output Hall Effect Magnetic Position Sensors Data Sheet

The Si7211/2/3/4/5/6 family of Hall-effect sensors from Silicon Labs combines a chopper-stabilized Hall element with a low-noise analog amplifier, 13-bit analog to digital converter. After A/D conversion the magnetic field data is available in analog. PWM or SENT format (depending on the part number). Leveraging Silicon Labs' proven CMOS design techniques, the Si721x family incorporates digital signal processing to provide precise compensation for temperature and offset drift.

Compared with existing Hall-effect sensors, the Si721x family offers industry-leading sensitivity and low noise, which enables use with larger air gaps and smaller magnets. For automotive applications, the Si720x family is AEC-Q100 qualified.

In the simplest case, the Si721x devices are offered in a 3 pin package with power, ground, and a single output pin that is signal corresponding to the magnetic field in analog, PWM, or SENT format.

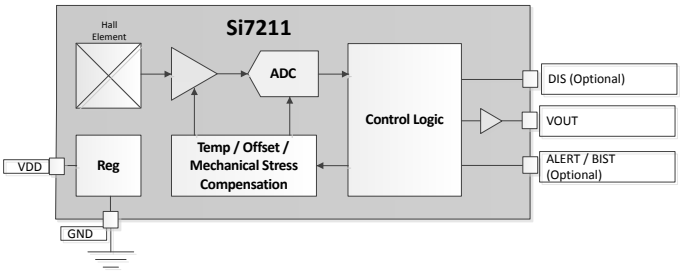
The Si721x devices are also offered in a 5 pin SOT23 and 8 pin DFN packages where the additional pins can be used for sleep mode (DIS) or to activate an on-chip coil for built in self-test (BISTb).

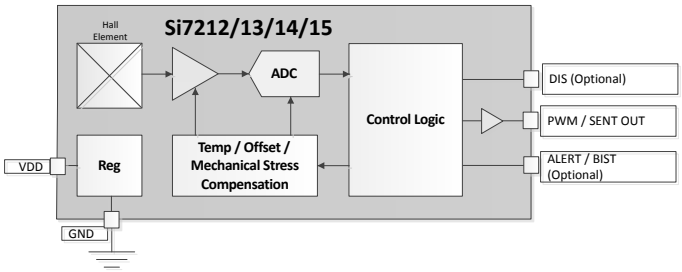
Applications

- Mechanical position sensing in consumer, industrial and automotive applications
- Camera image stabilization, zoom, and autofocus
- Fluid level sensing
- Control knobs and selector switches

FEATURES

- High-sensitivity Hall-Effect Sensor
  - Low noise output corresponding to magnetic field
  - Integrated digital signal processing for temperature and offset drift compensation
- Low 400 nA Typical Standby Current Consumption
- Configurable Sensitivity, Output Polarity and Sample Rate
- Sensitivity Drift < ±3% Over Temperature
- Wide power supply voltage
  - 1.7 to 5.5 V
  - 3.3 to 26.5 V
- AEC-Q100 Qualified for Automotive Applications
- Configurable output options
  - Analog (1.7 to 5.5V VDD)
  - PWM
  - SENT
- Industry-Standard Packaging
  - Surface-mount SOT-23 (3 or 5 pin)
  - TO92 and DFN packages (Coming Soon)





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1. Electrical Specifications

Unless otherwise specified, all min/max specifications apply over the recommended operating conditions.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply	V_{DD}	Si7211	2.25		5.5	V
Power Supply	V_{DD}	Si7212/3	1.71		5.5	V
Power Supply	V_{DD}	Si7214/5	3.3		26.5	V
Power Supply	V_{DD}	Si7216	4.0		26.5	V
Temperature	T_A	I grade	-40		+125	°C

Table 1.2. General Specification[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage High	V_{IH}	DIS or BIST pin	0.7 x V_{DD}	-	-	V
Input Voltage Low	V_{IL}	DIS or BIST pin	-	-	0.3 x V_{DD}	V
Input Voltage Range	V_{IN}	DIS or BIST pin	0		V_{DD}	V
Input Leakage	I_{IL}	DIS or BIST pin		< 0.1	1	µA
Current Consumption	I_{DD}	Conversion in progress Si7211 • V_{DD} = 3.3 V • V_{DD} = 5.0 V		 5.5 7	 6.5 9	mA
		Si7212/3 • V_{DD} = 1.8 V • V_{DD} = 3.3 V • V_{DD} = 5.0 V		 3.5 5.0 6.5	 4.5 6.0 8.5	mA
		Si7214/5		6.5	8.5	mA
		Si7216		7	9	mA
		Sleep Mode (DIS high)		50		nA
		Idle mode Si7212/3/7 Si7211 Si7214/5 Si7216		 360 860 900 1400	 700 1200 1200 1700	µA
Conversion Time	T_{CONV}	First conversion when waking from idle		11		µs
		Additional conversions in a burst		8.8		µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Idle Time[2]	T_{IDLE}	Minimum	11.9	13.2	14.5	µsec
		Maximum	185	206	227	msec
Wake Up Time	T_{WAKE}	Time from V_{DD} > 1.7 V to first measurement			1	msec

Note:

1. BIST and DIS pin specifications apply when the pin is present. These functions are only supported for the V_{DD} range of 1.7 – 5.5 V (Si7211/2/3).
2. Parts go to idle mode between measurements. Idle time can be factory programmed from 13.2 µsec to 206 msec ±10% or set to zero in which case conversions are done every 8.8 µsec. Normally idle time is only used at higher sample speeds.
3. For high voltage parts (V_{DD} = 26.5 V maximum), the power on ramp should be faster than 10 V per second in the start-up region from 2 to 3 V.

Table 1.3. Output Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si7211						
Offset[1]	B_{OFF}	V_{DD} = 2.25 - 5.5 V T = -40 to +125 °C		±300	±500	µT
		V_{DD} = 2.25 - 3.6 V T = 0 to +70 °C			±300	µT
Ratiometric Gain Error	RGE	Change in gain as function of supply for V_{DD} > 2.25.		±0.25		%/V
Gain Accuracy		-40 to +125 °C, V_{DD} = 2.25- 5.5 V 0 - 70 °C, V_{DD} = 2.25 - 3.6 V			12 6	%
Total Harmonic Distortion	THD	Vout inside 20-80% of V_{DD}, V_{DD} > 2.5 V		0.15		%
Short Circuit Protection	I_{SS}	Output shorted to ground of V_{DD}		±15		mA
Si7212/3						
Output Voltage Low Open Drain or Push Pull	V_{OL}	I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		I_{OL} = 2 mA V_{DD} > 1.7 V			0.2	V
		I_{OL} = 6 mA V_{DD} > 2 V			0.6	V
Leakage Output High Output Pin Open Drain	I_{OH}				1	µA
Output Voltage High Output Pin Push Pull	V_{OH}	I_{OH} = 2 mA V_{DD} > 2.25 V	V_{DD} – 0.4			V
Slew Rate	T_{SLEW}			5		$\%V_{DD}$/nS
Si7214/5						
Output Voltage Low	V_{OL}	I_{OL} = 11.4 mA V_{DD} > 6 V			0.4	V
Safe Continuous Sink Current					20	mA
Leakage Output High Output Pin Open Drain	I_{OH}				1	µA
Slew Rate Digital Output Mode	T_{SLEW}			5		$\%V_{DD}$/ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pin Shorted to VDD	I_{SHORT}	V_{DD} = 12 V Average current as pin cycles		4		mA
Si7216						
Zero Field Output	V_{OUT}	V_{DD} > 6 V	2.4		2.6	V
Gain		V_{DD} > 6 V		125		mV/mT

Note:
1. Deviation from VDD/2. To get voltage offset, divide by gain typically 40.96 mT/VDD.

Table 1.4. Magnetic Sensor PWM or SENT Output

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	B_{OFF}	20 mT scale Full temperature range		±250	+450, -350	µT
Gain Accuracy		0-70 °C			5	%
		Full temperature range			10	%
RMS Noise[1]		room Temp, 20 mT range, V_{DD} = 5 V		30		µT rms

Note:
1. For a single conversion. This can be reduced by the square root of N by filtering over N samples. See ordering guide for samples taken per measurement

Table 1.5. Temperature Compensation

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bop and Brp vs Temperature		No compensation 0-70°C		< ±0.05		%/°C
		Neodymium compensation		-0.12		%/°C
		Ceramic compensation		-0.2		%/°C

Table 1.6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Air Thermal Resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-5	212.8	°C/W
Junction to Board Thermal Resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-5	45	°C/W
Junction to Air Thermal Resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-3	254.6	°C/W
Junction to Board Thermal Resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-3	54.8	°C/W

Table 1.7. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature under Bias			-55		125	°C
Storage Temperature			-65		150	°C
Si7211/2/3						
Voltage on I/O Pins			-0.3		V_{DD}+0.3	V
Voltage on V_{DD} with Respect to GND			-0.3		6	V
ESD Tolerance		HBM			2	kV
		CDM			500	V
Si7214/5						
Voltage on Output Pin[2]			-21		40	V
Voltage on VDD withRespect to GND[3]			-21		40	V
ESD Tolerance		HBM			8	kV
		CDM			500	V
Si7216						
Voltage on Output Pin			-0.3		+5.5	V
V_{DD} withRespect to GND			-21		+40	V
ESD Tolerance		HBM output pin			2	kV
		HBM V_{DD}			8	kV
		CDM			500	V

Note:

1. Absolute maximum ratings are stress ratings only, operation at or beyond these conditions is not implied and may shorten the life of the device or alter its performance.
2. The output pin can withstand EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω to a local bypass cap of 0.1 µF and additional 22 Ω between the capacitor and ground.
3. VDD can withstand automotive EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω.

2. Functional Description

The Si7211/2/3/4/5 family of Hall Effect magnetic sensors digitize the component of the magnetic field in the z axis of the device (positive field is defined as pointing into the device from the bottom). The digitized field is then converted to an output format of analog, PWM or SENT and presented on the output pin.

Table 2.1. Part Description

Part Number	Description
Si7211	Low voltage analog output
Si7212	Low voltage PWM output
Si7213	Low voltage SENT output
Si7214	High voltage PWM output
Si7215	High voltage SENT output
Si7216	High voltage V_{DD}, low voltage analog out

Please see the selection guide for the two digit number after the die revision which gives more details about output, sampling frequency and other details.

Data output is always unsigned. That is, half scale (V_{DD}/2 for analog out parts, 50% duty cycle for PWM output parts and 2048 (0x800) for SENT output parts) corresponds to zero field.

The parts are preconfigured for the magnetic field measurement range, idle time, temperature compensation and digital filtering and will wake into this mode when first powered. The specific configuration output type (open collector or push pull) are determined by the part number.

Following is a list of configuration options:

- *Measurement Range* — This is normally set so that after temperature compensation the full scale output is ±20.47 mT or ±204.7 mT For convenience these are referred to as the 20 mT and 200 mT scales.
- *Digital Filtering* — To reduce noise in the output (normally 0.03 mT RMS on the 20 mT scale), digital filtering can be applied. The digital filtering can be done to a burst a measurements (FIR filter) or can be configured to average measurements in IIR style. The filtering can be done over a number of samples in powers of 2 (1,2,4,8,…) for up to 2^{12} (4096) samples.
- *Time between measurements* (or measurement bursts for the case of FIR filtering)
  - Idle times are variable from 11 µsec to 172 msec nominally. Analog output parts can also be configured to sample continuously (a new sample every 7 µsec)
  - For analog output parts the output pin is updated upon completion of each measurement.
  - For PWM output parts the output pin is update on the next PWM cycle
  - For SENT output parts a new SENT frame is output with each new measurement (for this reason the sample rate is always set less than the maximum frame rate)
  - For SENT operation, each new frame triggers a new measurement. For this reason the sample rate is set to maximum and is controlled by the SENT frame rate
- *Output Pin* — The direction in which the output signal goes in response to an increase in field.
- Temperature compensation of the magnetic field response to compensate for the nominal drop in magnetic field output of common magnets with increasing temperature.
  - In this case accuracy is defined at 25C and the sensitivity reduces at higher temperature
  - Standard compensations are -01.2%/C (Neodymium) and -0.2%/C (Ceramic)
- The PWM rate for PWM output parts (see also section 3)
- The SENT tick time and output format for SENT output parts. See also section 4.

3. Analog Output

For the Si7211, the analog output is $V_{DD}/2$ at zero field and goes from nearly zero at large negative field to nearly V_{DD} at large positive field.

$$B(mT) = (20.47 or 204.7) \times \left(2 \times \frac{Vout}{Vdd} - 1\right)$$

4- and 5-pin packages also have the option of a BISTb pin. When configured and detected low, the internal coil is turned on until the pin is detected high again. Each subsequent BISTb activation flips the polarity of the coil during BIST.

For high voltage parts (Si7216), the output is ratiometric to an internally derived V_{DD} of 5V (± 5%) so long as the input V_{DD} is > 6 V.

$$B(mT) = (20.47 or 204.7) \times \left(2 \times \frac{Vout}{5} - 1\right)$$

For V_{DD} < 6 V the internally derived reference drops 1 V for each 1 V drop in V_{DD} to the minimum recommended working voltage of 4.0 V.

4. PWM Output Description

The PWM output can be configured as open drain or push pull. High voltage parts can only be configured as open drain. The PWM duty cycle is factory configured and is normally set to in the range of 10 Hz to 1 KHz and is ±5%. See ordering guide for specific part numbers..

As each measurement completes, the next PWM cycle will be updated to reflect the last measurement result. The duty cycle varies from 0 to 100% where 50% duty cycle means zero field, 0 % duty cycle generally means maximum negative field (-20.47 mT or -204.7 mT) and 100% duty cycle generally means maximum positive field (+20.47 or +204.7 mT). The high portion of the PWM is output first so that

$$B(mT) = \left(20.47 \text{ or } 204.7\right) \times \left(2 \times \frac{Thigh}{Thigh + Tlow} - 1\right)$$

The host processor should look for a variation in the magnetic field to determine the entire system is working properly.

4- and 5-pin packages also have the option of a BISTb pin. When configured and detected low the internal coil is turned on until the pin is detected high again. Each subsequent BISTb activation flips the polarity of the coil during BIST.

5. SENT Output

The Si7213 and Si7215 output data in SENT (Single Edge Nibble transmission) format conforming to J2716 January 2010. All SENT output parts are configured as open collector.

SENT protocol messages consist of:

- A calibration/synchronization period consisting of 56 clock ticks
- A status and serial communication 4-bit nibble
- A sequence of up to six data nibbles
- A one nibble checksum
- Each nibble is 12 to 27 clock ticks
- An optional delay pause pulse

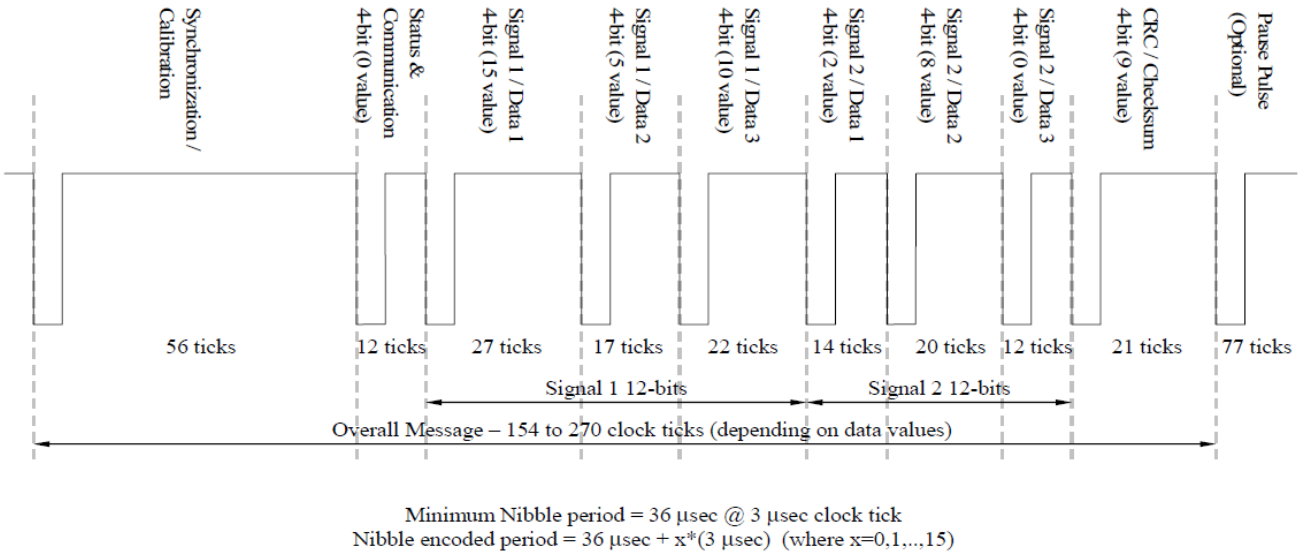


Figure 5.1. SENT Timing Diagram

As can be seen, each part of the sequence is determined by the timing between falling edges of the open drain sent output. First, a time of 56 clock ticks is produced so that the receiver can calibrate itself to the Si7213/5 speed. Then a total of 8 nibbles (4 bits per nibble) is produced. The edge to edge time of each nibble is 12 clock ticks for a data nibble of 0000b 13 ticks for a data value of 0001b and so on up to 27 ticks for a data value of 1111b.

The nominal tick time has been standardized at 5 µsec (±5%) however this is configurable.

5.1 tSENT Status Nibble

In the Si7200 the four bit status nibble is defined as follows:

- Bit 3 and Bit 2 always transmitted as zeroes (No serial message support)
- Bit 1 and Bit 0
  - 00 Normal; No error condition
  - 01 Error condition
  - 10 Positive field BIST active
  - 11 Negative field BIST active

5.2 SENT Data Nibbles

The Si7213 and Si7215 are configurable to support a variety of options. The standard option follows J2716 A.3 where:

Signal	Data	Description
1	1	MSB of the magnetic field data
1	2	MidSB of the magnetic field data
1	3	LSB of the magnetic field data
2	1	MSB of an 8 bit rolling counter
2	2	LSB of an 8 bit rolling counter
2	3	An inverted copy of signal 1 data 1

For magnetic field, 3 nibbles are put together for a total 12 bit data word with values that can range from 0 to 4095. For magnetic field data, 2048 corresponds to zero field. The Si7213 can be configured for ± 20.47 mT full scale or ± 204.7 mT full scale. On the 20.47 mT full scale 1 LSB is 0.01 mT and on the 204.7 mT full scale 1 LSB is 0.1 mT.

5.3 CRC Calculation

The CRC is calculated based on the 6 data nibble according to x4 +x3 + x2 + 1 with a seed value of 0101 as per the recommendations in J7216 section 5.4.2.2. The legacy CRC calculation is not supported.

5.4 SENT Pause Pulse

The Si7213 and Si7215 are configurable for a pause pulse that is 12 ticks low, 256 ticks wide. However, the standard offering is no pause pulse.

5.5 SENT Frame Rate

For the standard offering with no pause pulse, each message will be 154 to 270 ticks in length. At a tick time of 5 µsec this is 770 to 1350 µsec. This gives an average frame rate of approximately 1 msec for the standard tick time of 5 µsec. Conversion start is synchronized to the start of the synch pulse and is normally completed before the synch pulse completes so the data that is reported is the data obtained during the synch pulse time.

5.6 BIST Activation During SENT Operation

For 3-pin packages BIST can be activated by holding the output pin low for the entire message.

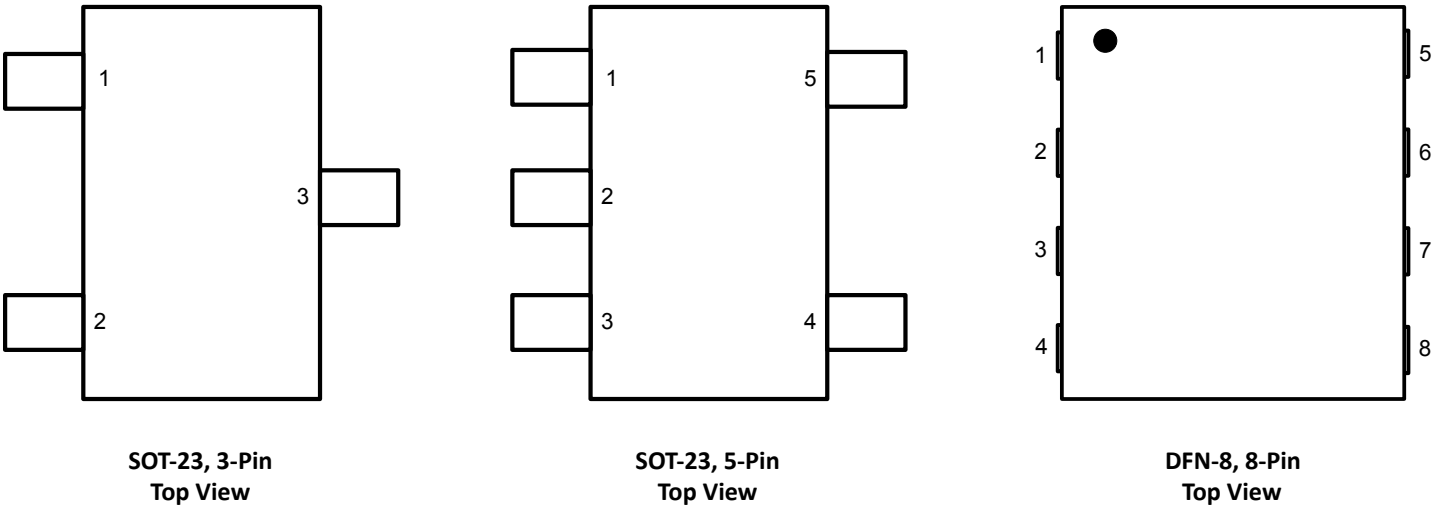
Once BIST is activated SENT messages resume 12 ticks after the SENT IO pin is detected high. Eight positive field BIST messages are followed by eight negative field BIST messages followed by a return to normal messages.

The magnetic field is generated by a small on chip coil that will generate a current of [TBD] mA and a magnetic field of [TBD] mT.

The host processor should look for a variation in the magnetic field output to determine the entire system is working properly.

4- and 5-pin packages also have the option of a BISTb pin. When configured and detected low the internal coil is turned on until the pin is detected high again. Each subsequent BISTb activation flips the polarity of the coil during BIST

6. Pin Description



SOT-23, 3-Pin Top View | **SOT-23, 5-Pin Top View** | **DFN-8, 8-Pin Top View**

Figure 6.1. Pin Assignments

Table 6.1. Three Pin SOT23 Package

Pin Name	Pin Number	Description
V_{DD}	1	Power +1.7 to +5.5 V or 3.3 to 26.5 V
OUT1	2	Output
GND	3	Ground

Table 6.2. Five Pin SOT23 Package

Pin Name	Pin Number	Description
BISTb	1	Logic low activates BIST
GND	2	Ground
DIS	3	Disables part (puts into sleep mode) when high. Measurement cycle will resume when pin goes low
V_{DD}	4	Power +1.7 to +5.5 V
OUT1	5	Switch/latch output

Table 6.3. DFN 8 Pin Package

Pin Name	Pin Number	Description
V_{DD}	8	Power +1.7 to +5.5 V
GND	1, 5	Ground
OUT1	6	Switch/latch output
BISTb	4	Activates Built in Self Test
DIS	2	Disable (puts part in lowest power mode with no sampling)

Table 6.4. TO-92 Package

Pin Name	Pin Number	Description
VDD	1	Power
GND	2	Ground
OUT1	3	Output

7. Ordering Guide

Part Number [1]	Output Type and Polarity	Package	I_{DD} Average	Sample Rate and Scale	Temp-Compen-sation	BIST	Digital Filtering
Analog output V_{DD} = 2.25 - 5.5 V							
Si7211-B-00-IV(R)	Analog, increasing field is increas-ing voltage	SOT23-3	5.5 mA	7 KHz 20 mT	No	No	16 sam-ples FIR
Si7217-B-01-IV(R)	Analog, increasing field is increas-ing voltage	SOT23-5	5.5 mA DIS low 50 nA DIS high	7 KHz 20 mT	No	Yes, sepa-rate pins	16 sam-ples FIR
PWM output V_{DD} = 1.7 - 5.5 V (Default PWM speed is 250 Hz)							
Si7212-B-00-IV(R)	Push pull. Increasing pulse width is increasing field	SOT23-3	560 µA	300 Hz 20 mT	No	No	16 sam-ples FIR
SENT output V_{DD} = 1.7 - 5.5 V (default is 5 µsec tick time 1 kHz frame rate A.3 signaling)							
Si7213-B-00-IV(R)	Open drain, increasing field gives increasing result	SOT23-3	1.02 mA	1 kHz 20 mT	No	Yes, by holding output low	16 sam-ples FIR
Si7214 PWM output V_{DD} = 3.3 - 26.5 V (Default PWM speed is 100 Hz)							
Si7214-B-00-IV(R)	Open Drain. Increasing pulse width is increasing field	SOT23-3	1.02 mA	150 Hz 20 mT	No	No	16 sam-ples FIR
SENT output V_{DD} = 3.3 - 26.5 V (default is 5 µsec tick time 1 kHz frame rate A.3 signaling)							
Si7215-B-00-IV(R)	Open drain, increasing field gives increasing result	SOT23-3	1.7 mA	1 kHz 20 mT	No	Yes, by holding output low	16 sam-ples FIR
Analog output V_{DD} = 4.0 to 26.5 V							
Si7216-B-00-IV(R)	Analog, increasing field is increas-ing voltagle	SOT23-3	2.2 mA	1 kHz 20 mT	No	No	16 sam-ples FIR

Note:

1. A is the die revision. The next two digits are used with this look up table to give more specific information. I is the temperature range (-40 to +125°C). B, M, or V is the package type (TO92, DFN8, or SOT23) the optional (R) is the designator for tape and reel (3000 pieces per reel). Parts not ordered by the full reel will be supplied in cut tape.
2. North pole of a magnet at the bottom of a SOT23 package is defined as positive field.

8. Package Outline

8.1 SOT23 3-Pin Package

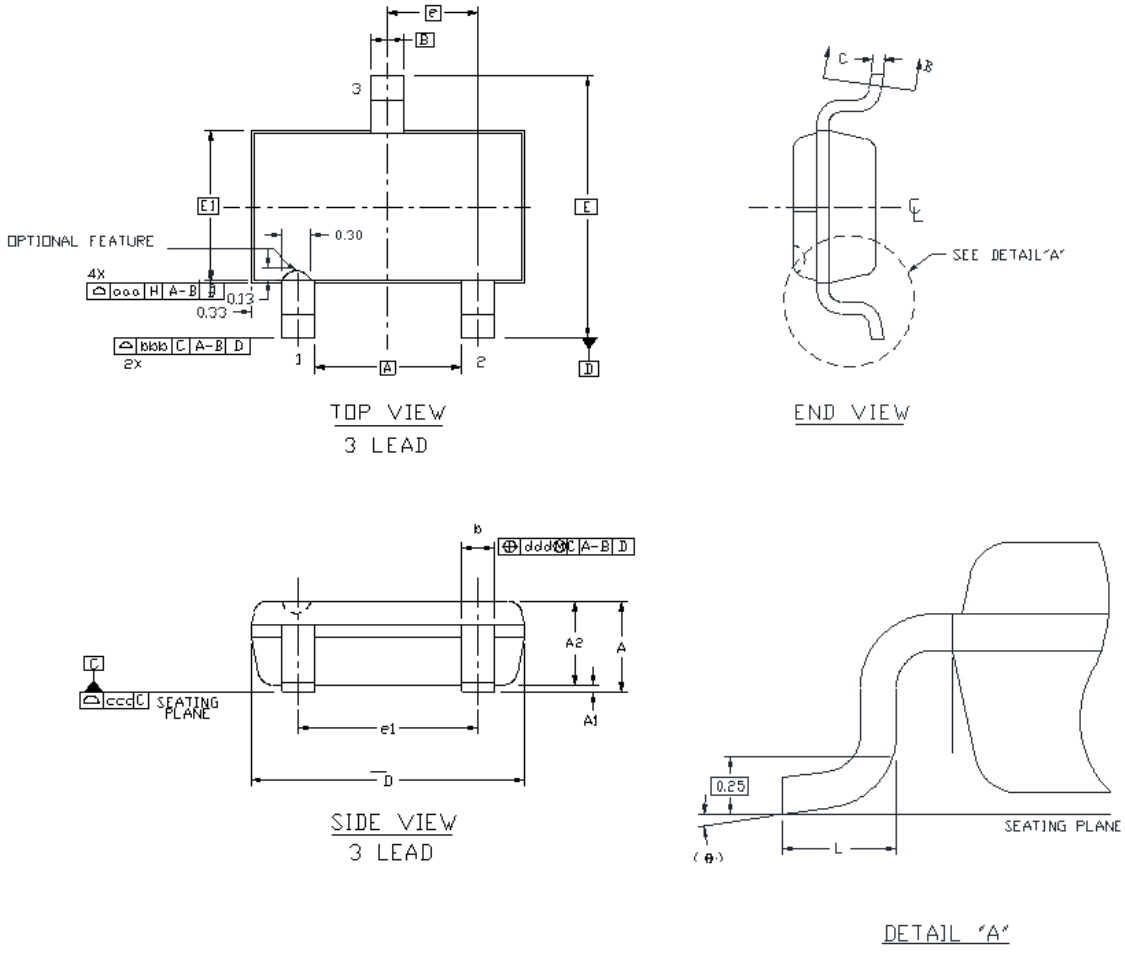


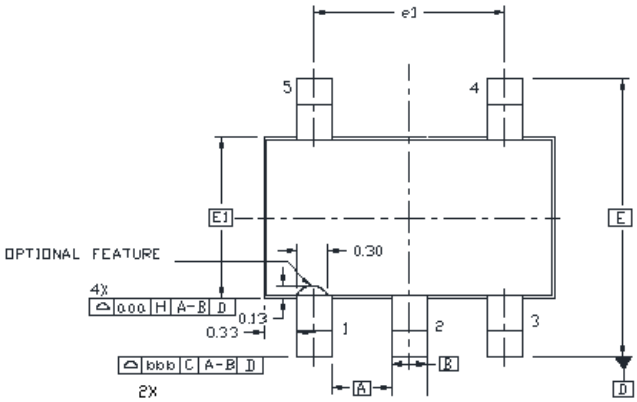
Table 8.1. SOT23 3-Pin Package Dimensions

Dimension	Min	Max
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.75 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
θ	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

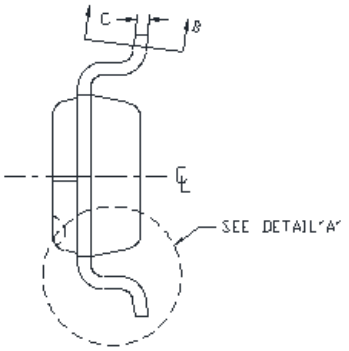
Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

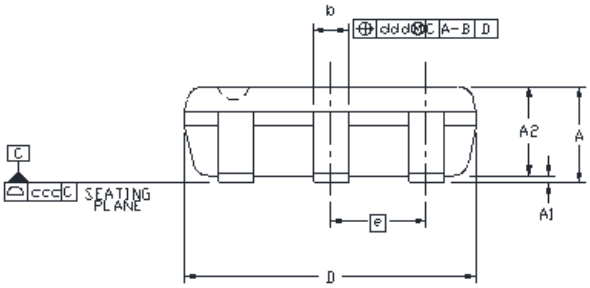
8.2 SOT23 5-Pin Package



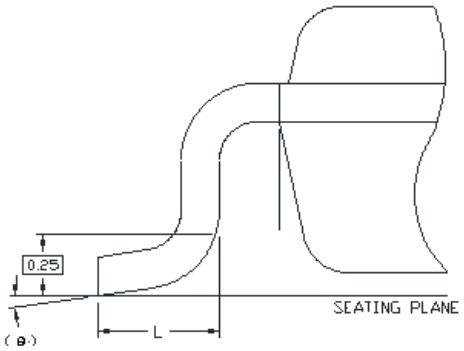
TOP VIEW
6 LEAD



END VIEW



SIDE VIEW
6 LEAD



DETAIL "A"

Table 8.2. SOT23 5-Pin Dimensions

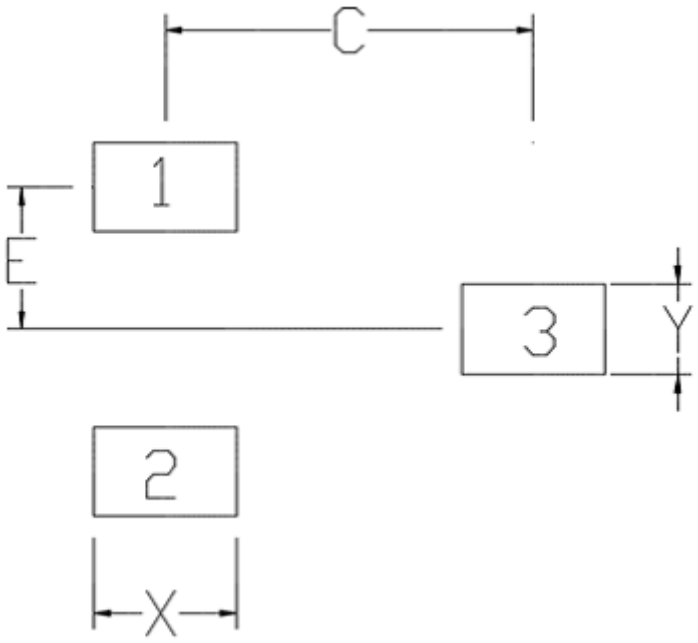
Dimension	Min	Max
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.75 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L2	0.25 BSC	
θ	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

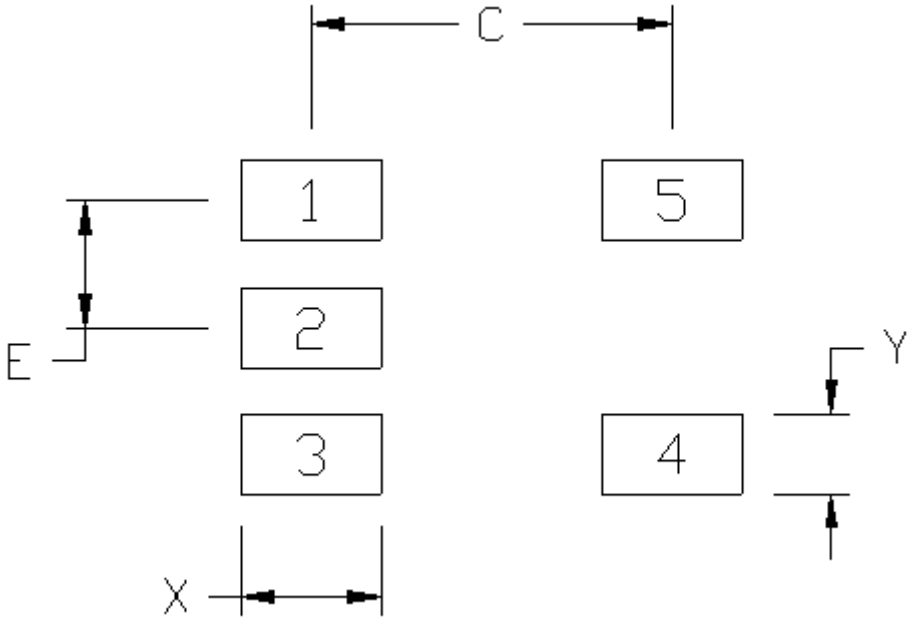
9. Land Patterns

9.1 SOT23 3-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

9.2 SOT23 5-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

Note:

General

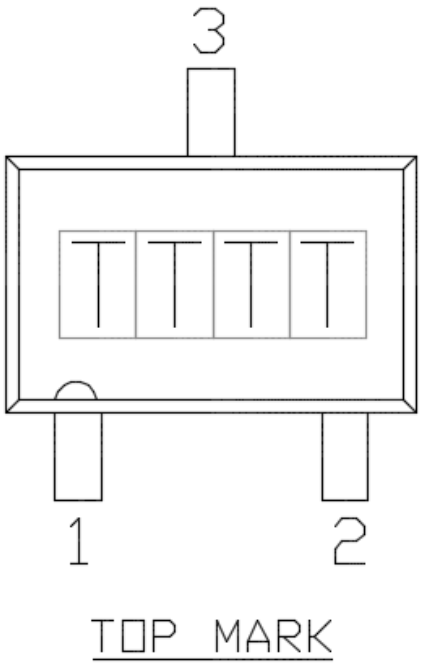
1. 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

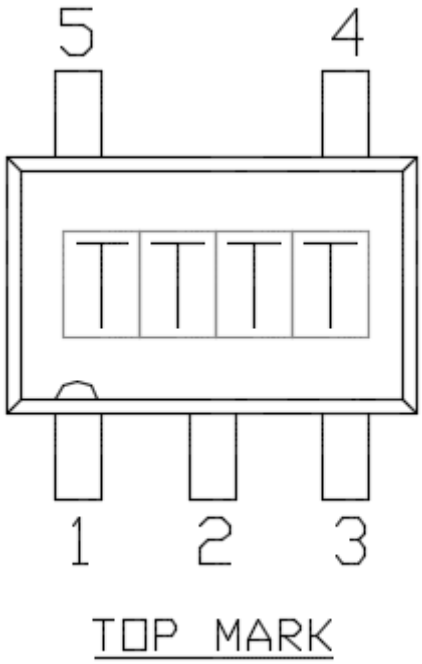
10. Top Marking

10.1 SOT23 3-Pin Top Marking



Note: TTTT is a manufacturing code.

10.2 SOT23 5-Pin Top Marking



Note: TTTT is a manufacturing code.

11. Revision History

11.1 Revision 0.1

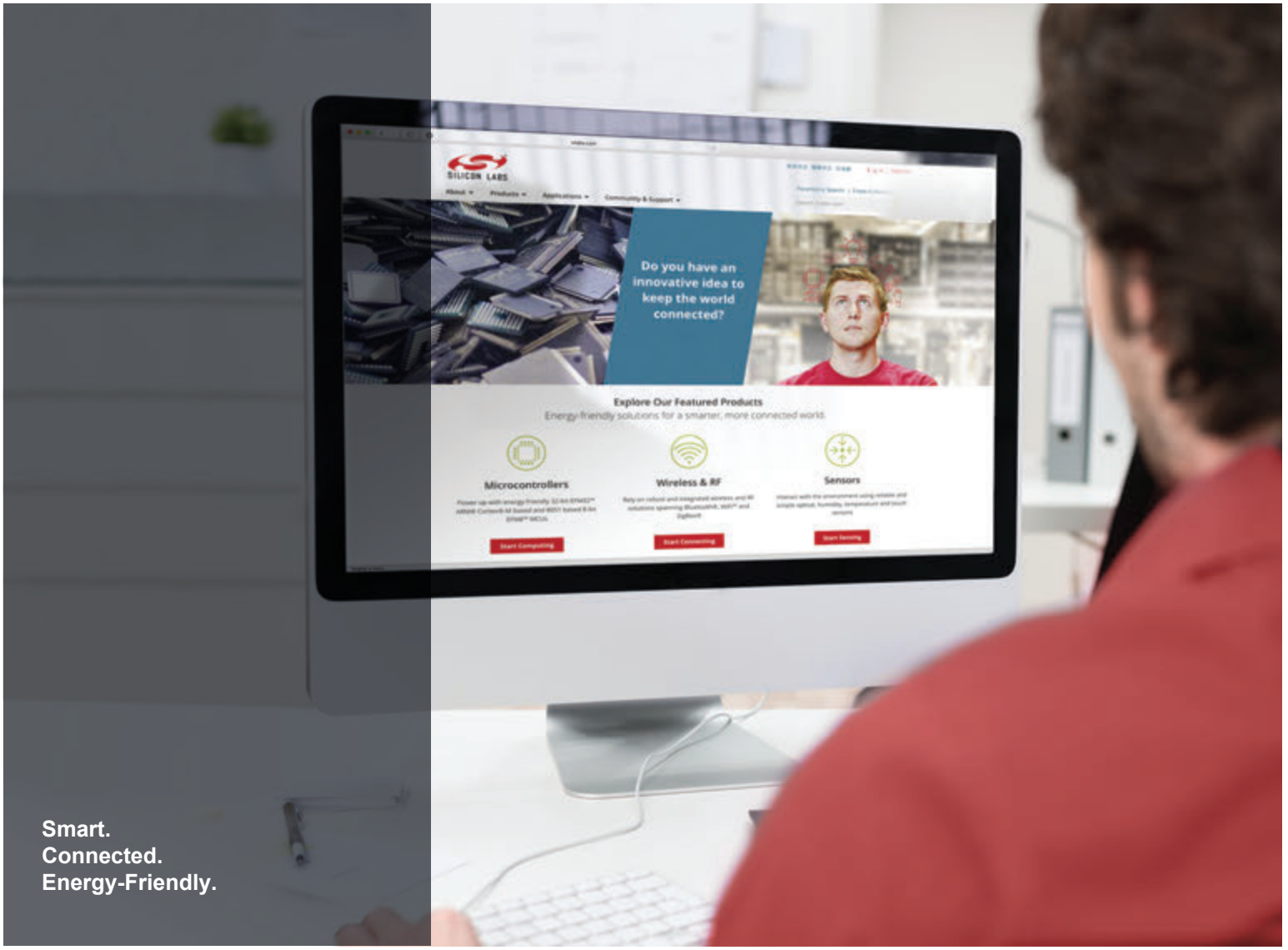
February 1, 2016

- Initial release.

11.2 Revision 0.9

June 30, 2017

- Updated 1. Electrical Specifications.
- Updated 7. Ordering Guide.
- Minor typo corrections.



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