LV58063MC

ON Semiconductor®

http://onsemi.com

Bi-CMOS IC
Step-down Switching Regulator

Overview

LV58063MC is a 1ch step-down switching regulator. 0.13Ω FET is incorporated on the upper side to achieve high-efficiency operation for large output current.

Low-heat resistance and compact-package SOP8L (200mil) employed.

Current mode control gives superior load current response with easy phase compensation.

EN pin, allowing the standby mode with the current drain of 70μA.

Pulse-by-pulse over-current protection and overheat protection available for protection of load devices.

Externally adjustable soft start time.

Function

- 3A 1ch step-down switching regulator
- Thermal shutdown
- Wide input range (8 to 28V)
- Reference voltage: 0.8V
- High efficiency (90% I_{OUT}=1A, V_{IN}=12V, V_{OUT}=5V)
- Fixed frequency: 370kHz
- Standby mode
- Soft start
- Over-current protection
- Compact package: SOP8L (200mil) with exposed pad
- Overshoot control after over-current protection event
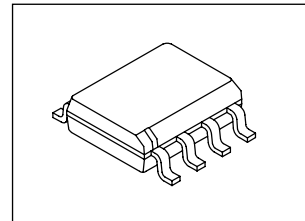
SOP8L (200mil)

Application

- LCD/PDP-TV
- STB
- White Goods
- Office equipment
- General consumer electronics

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input V_{IN} voltage	V_{IN} max		32	V
BOOT pin maximum voltage	V_{BT} max		37	V
SW pin maximum voltage	V_{SW} max		V_{IN} max	V
BOOT pin-SW pin maximum voltage	V_{BS-SW} max		7	V
FB, EN, COMP, SS pin maximum voltage	Vfs max		7	V
Allowable power dissipation	Pd max	Mount on a specified board *	2.05	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-40 to +150	°C

* Specified board: 46.4mm × 31.8mm ×1.7mm, glass epoxy.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{IN} pin voltage	V_{IN}		8 to 28	V
BOOT pin voltage	V_{BT}		-0.3 to 34	V
SW pin voltage	V_{SW}		-0.4 to V_{IN}	V
BOOT pin-SW pin voltage	V_{BS-SW}		6.5	V
FB, EN, COMP, SS pin voltage	V_{FSO}		6	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C V_{IN} = 12V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
IC current drain in standby	$I_{CC}1$	EN=0V		70		μA
IC current drain in operation	$I_{CC}2$	EN=open, FB=1V		5		mA
Efficiency	Effcy	V_{IN}=12V, I_{OUT}=1A, V_{OUT}=5V Design target: *1		90		%
Reference voltage	Vref	V_{IN}=8V to 28V (±2%)	-2%	0.8	+2%	V
FB pin bias current	Iref	FB=0.8V application		10	100	nA
High-side ON resistance	RonH	BOOT=5V		0.13		Ω
Low-side ON resistance	RonL			7		Ω
Oscillation frequency	F_{OSC}		296	370	444	kHz
Oscillation frequency during short-circuit protection	F_{OSCS}		30	38	46	kHz
EN high-threshold voltage	Venh				1.9	V
EN low-threshold voltage	Venl		0.8			V
EN pull-up corrent	Ien	EN=0V		16		μA
Maximum ON DUTY	D max			80		%
Current limit peak value	Icl	V_{IN}=12V, V_{OUT}=5V, L=10μH	3.8			A
Thermal shutdown temperature	Ttsd	*Design guarantee *2		160		°C
Thermal shutdown temperature hysteresis	Dtsd	*Design guarantee *2		40		°C
Soft start current	I_{SS}	SS=0V	6	10	14	μA

*1: Design target (not tested before shipment)

*2: Design guarantee (value guaranteed by design and not tested before shipment)
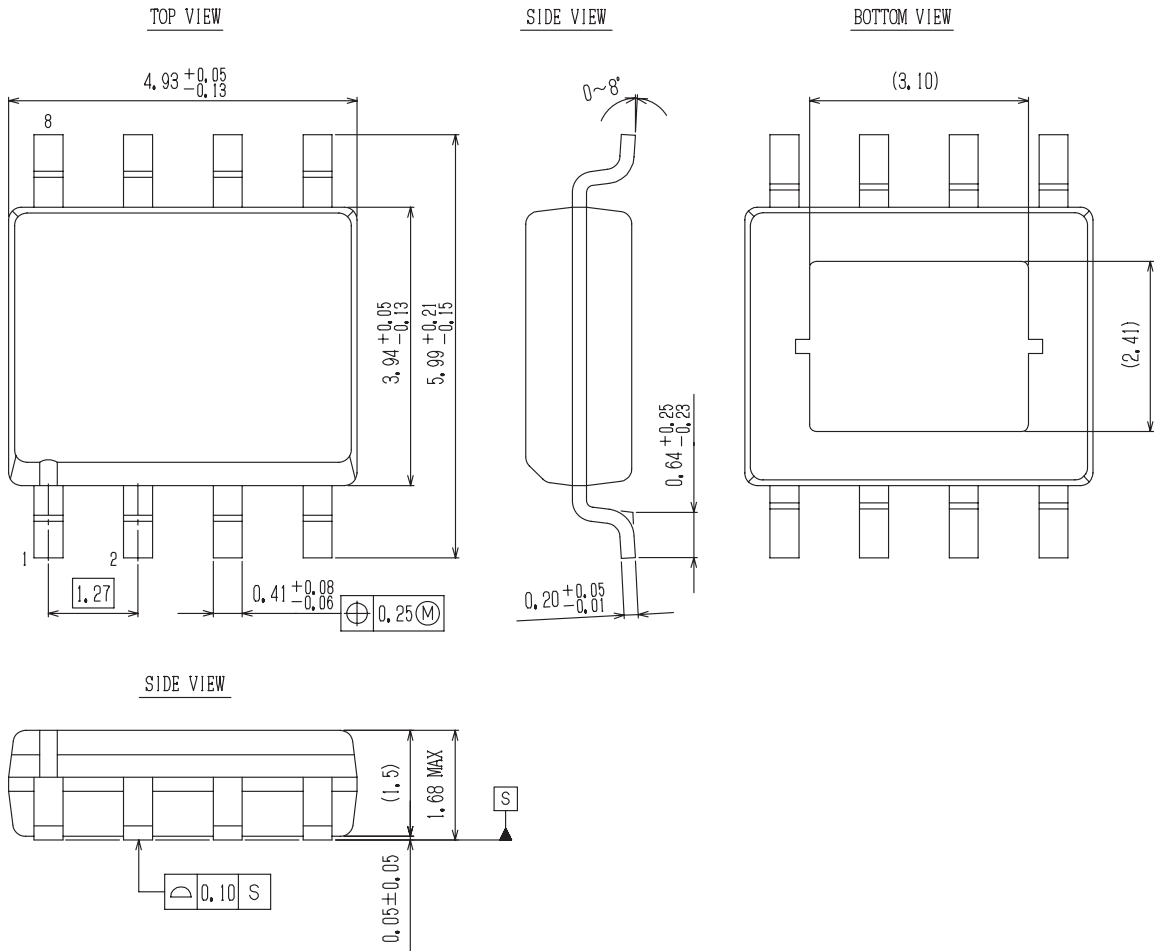
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
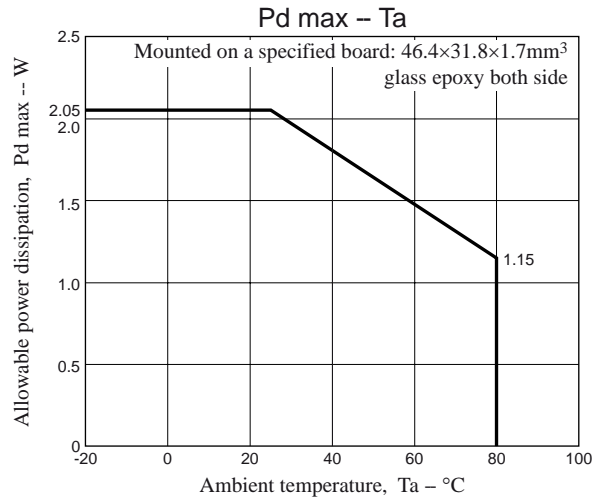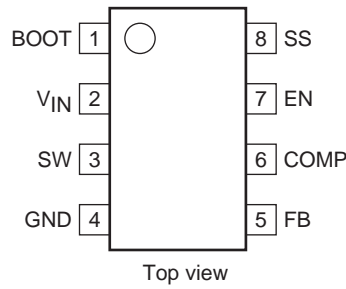
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Package Dimensions

unit : mm

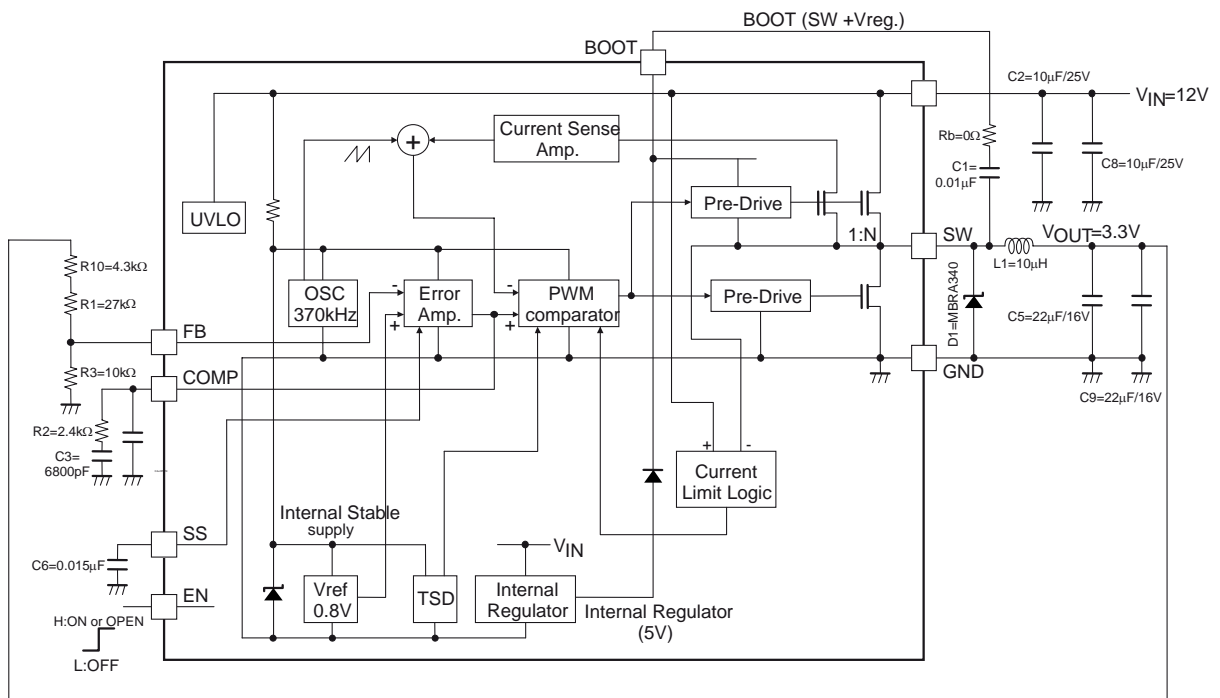**SOIC8 N EP / SOP8L (200 mil)**
CASE 751DM
ISSUE O

TOP VIEW

SIDE VIEW

BOTTOM VIEW

$4.93^{+0.05}_{-0.13}$

$3.94^{+0.05}_{-0.13}$

$5.99^{+0.21}_{-0.15}$

(3.10)

(2.41)

8

1   2

1.27

$0.41^{+0.08}_{-0.06}$

⊕ 0.25 Ⓜ

0~8°

$0.64^{+0.25}_{-0.23}$

$0.20^{+0.05}_{-0.01}$

SIDE VIEW

(1.5)

1.68 MAX

S

△ 0.10 S

$0.05±0.05$

Pd max – Ta

Pd max – Ta

Mounted on a specified board: 46.4×31.8×1.7mm^3 glass epoxy both side

Allowable power dissipation, Pd max – W (vertical axis): 0, 0.5, 1.0, 1.15, 1.5, 2.0, 2.05, 2.5

Ambient temperature, Ta – °C (horizontal axis): -20, 0, 20, 40, 60, 80, 100

Pin Assignment

BOOT	1	8 SS
V$_{IN}$	2	7 EN
SW	3	6 COMP
GND	4	5 FB

Top view

Block Diagram and Sample Application Circuit (3.3V output)

BOOT (SW +Vreg.)

BOOT

Current Sense Amp.

Pre-Drive

1:N

UVLO

Pre-Drive

OSC 370kHz

Error Amp.

PWM comparator

C2=10µF/25V

V$_{IN}$=12V

Rb=0Ω

C1= 0.01µF

C8=10µF/25V

SW

V$_{OUT}$=3.3V

L1=10µH

D1=MBRA340

C5=22µF/16V

GND

C9=22µF/16V

R10=4.3kΩ

R1=27kΩ

FB

R3=10kΩ

COMP

R2=2.4kΩ

C3= 6800pF

Current Limit Logic

SS

Internal Stable supply

C6=0.015µF

EN

Vref 0.8V

TSD

Internal Regulator

V$_{IN}$

Internal Regulator (5V)

H:ON or OPEN

L:OFF

- C1,C8,C5,C9 = Ceramic capacitor
- L1=CDRH105RNP-100NC (sumida)

Pin Function

Pin No.	Pin name	Description	Equivalent Circuit
1	BOOT	Internal high side mos fet boot strap capacitor Pin. Connect around 0.01μF capacitor or greater between SW and BOOT. To operate within absolute maximum rating of SW, to keep stable operation, and to reduce switching noise, please use a series resistor, Rb (value is around 100Ω) is recommended to use.	
2	V_{IN}	Input Voltage Pin. Large Filter Capacitor (equal or larger than 20μF) should be connected between V_{IN} and GND to eliminate noise on the input and to operate properly. When using electrolytic capacitors, it is recommended to add a ceramic capacitor of about 0.1uF between VIN-GND for stability.	See BOOT
3	SW	Power Switching Pin. Connect the output LC filter. Connect the above-mentioned capacitor between this pin and BOOT pin.	See BOOT
4	GND	Ground pin.	
5	FB	Feedback pin. Connect a voltage divider resistor across FB to set the regulated output voltage. The output voltage is given by next equation. $V_{OUT} = Vref \times \{ 1 + \frac{(R1 + R10)}{R3} \}$ Vref = 0.8V Example: 3.3V output voltage (See Block Diagram and Sample Application Circuit) $V_{OUT} = 0.8 \times \{ 1 + \frac{(27k + 4.3k)}{10k} \}$ =3.304V	
6	COMP	Phase compensation pin. Connect an external capacitor and a resistor for the DC DC converter close loop-phase compensation.	

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Pin No.	Pin name	Description	Equivalent Circuit
7	EN	Enable Pin. If applying logically high voltage, or left open, the converter operates. If connected to GND, the converter's operation stops. It is not applied to the EN before VIN is applied.	
8	SS	Soft start Pin Internal source current (10μA) and external capacitor will make soft start time. Soft start capacitor, C6 is given by next equation, $C6 = 10\mu A \times \dfrac{Tss}{Vref}$ Where, Tss : soft start time, 　　　　Vref : reference voltage 　Example : soft start time 1.2ms $C6 = 10\mu A \times \dfrac{1.2ms}{0.8\ V} = 0.015\mu F$	See FB

Considerations for the design

- Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage on SW pin deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. Please, do not insert beads as above described. Instead, remove noise by Rb resistor.
- Exposed pad on the bottom side of the IC should be soldered. We cannot recommend other usages of the exposed pad.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV58063MC-AH	SOP8L (200mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel
LV58063MCZ-AH	SOP8L (200mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel