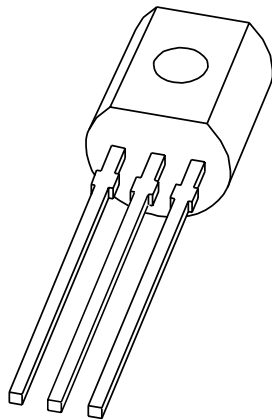


DATA SHEET



2N5401 PNP high-voltage transistor

Product specification
Supersedes data of 1999 Apr 08

2004 Oct 28

PNP high-voltage transistor

2N5401

FEATURES

- Low current (max. 300 mA)
- High voltage (max. 150 V).

APPLICATIONS

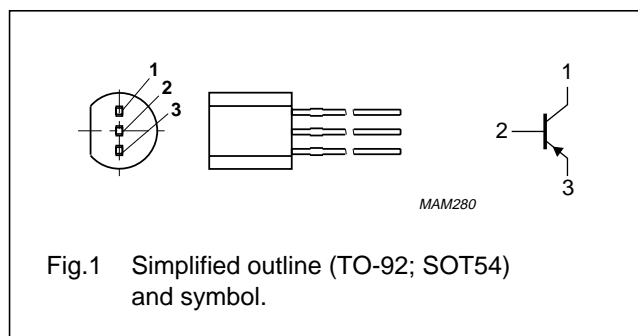
- General purpose switching and amplification
- Telephony applications.

DESCRIPTION

PNP high-voltage transistor in a TO-92; SOT54 plastic package. NPN complement: 2N5551.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
2N5401	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–160	V
V_{CEO}	collector-emitter voltage	open base	–	–150	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–300	mA
I_{CM}	peak collector current		–	–600	mA
I_{BM}	peak base current		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	630	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	200	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

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CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = -120 V; I _E = 0 A	-	-50	nA
		V _{CB} = -120 V; I _E = 0 A; T _j = 100 °C	-	-50	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = -4 V; I _C = 0 A	-	-50	nA
h _{FE}	DC current gain	V _{CE} = -5 V; see Fig.2 I _C = -1 mA I _C = -10 mA I _C = -50 mA	50 60 50	- 240 -	
V _{CEsat}	collector-emitter saturation voltage	I _C = -10 mA; I _B = -1 mA	-	-200	mV
		I _C = -50 mA; I _B = -5 mA	-	-500	mV
C _c	collector capacitance	V _{CB} = -10 V; I _E = i _e = 0 A; f = 1 MHz	-	6	pF
f _T	transition frequency	V _{CE} = -10 V; I _C = -10 mA; f = 100 MHz	100	300	MHz
F	noise figure	V _{CE} = -5 V; I _C = -200 μA; R _S = 2 kΩ; f = 10 Hz to 15.7 kHz	-	8	pF

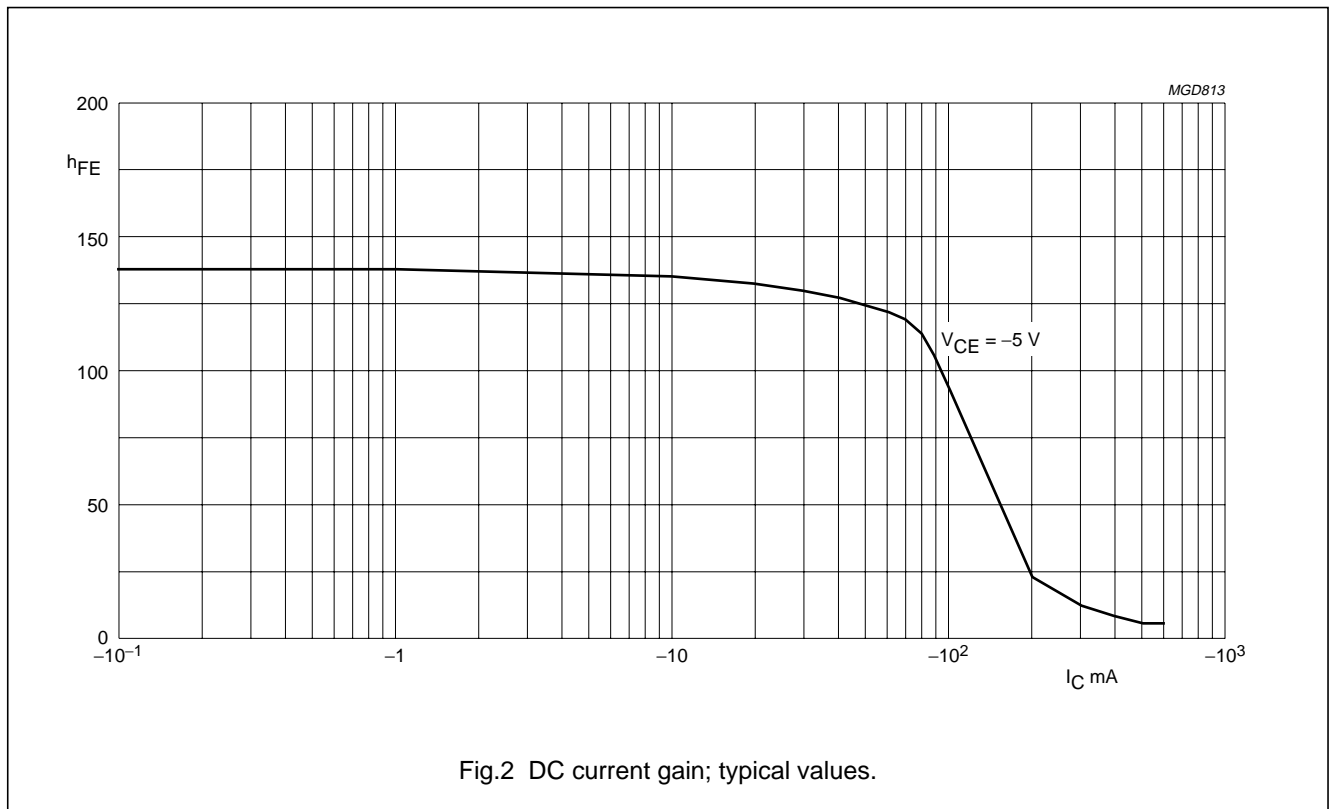


Fig.2 DC current gain; typical values.

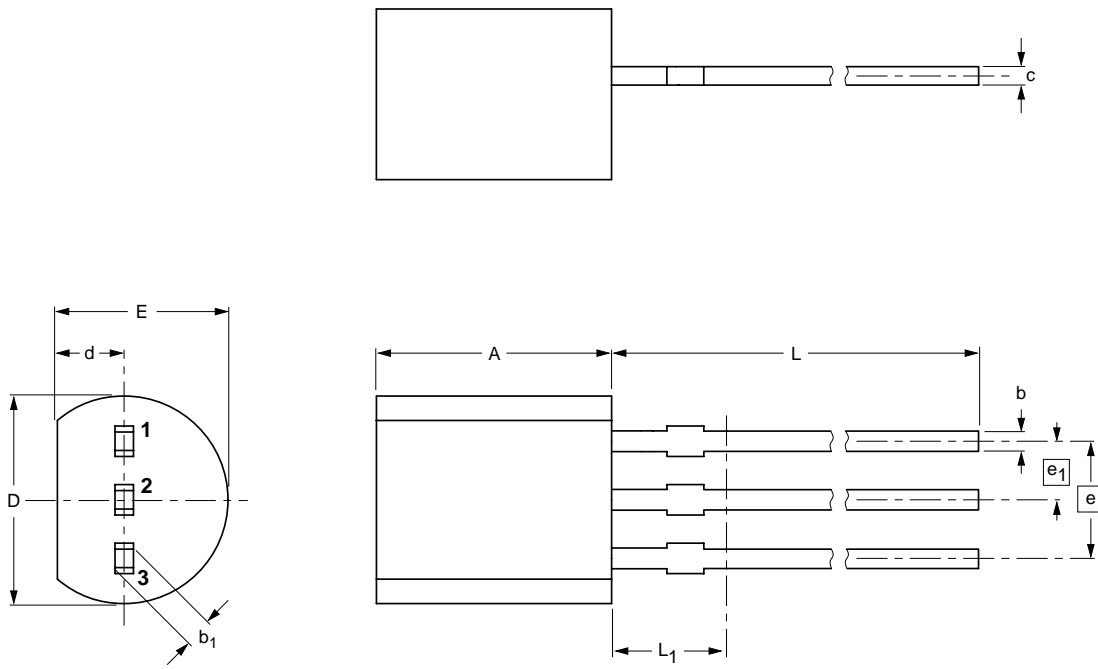
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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		97-02-28 04-06-28

PNP high-voltage transistor

2N5401

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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