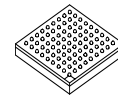


MSC7118

Low-Cost 16-bit DSP with DDR Controller



MAP-BGA-400
17 mm × 17 mm

- StarCore® SC1400 DSP extended core with one SC1400 DSP core, 256 Kbyte of internal SRAM M1 memory, 16 way 16 Kbyte instruction cache (ICache), four-entry write buffer, programmable interrupt controller (PIC), and low-power Wait and Stop processing modes.
- 192 Kbyte M2 memory for critical data and temporary data buffering.
- 8 Kbyte boot ROM.
- AHB-Lite crossbar switch that allows parallel data transfers between four master ports and six slave ports, where each port connects to an AHB-Lite bus; fixed or round robin priority programmable at each slave port; programmable bus parking at each slave port; low power mode.
- Internal PLL generates up to 300 MHz clock for the SC1400 core and up to 150 MHz for the crossbar switch, DMA channels, M2 memory, and other peripherals.
- Clock synthesis module provides predivision of PLL input clock; independent clocking of the internal timers and DDR module; programmable operation in the SC1400 low power Stop mode; independent shutdown of different regions of the device.
- Enhanced 16-bit wide host interface (HDI16) provides a glueless connection to industry-standard microcomputers, microprocessors, and DSPs and can also operate with an 8-bit host data bus, making it fully compatible with the DSP56300 HI08 from the external host side.
- DDR memory controller that supports byte enables for up to a 32-bit data bus; glueless interface to 150 MHz 14-bit page mode DDR-RAM; 14-bit external address bus supporting up to 1 Gbyte; and 16-bit or 32-bit external data bus.
- Programmable memory interface with independent read buffers, programmable predictive read feature for each buffer, and a write buffer.
- System control unit performs software watchdog timer function; includes programmable bus time-out monitors on AHB-Lite slave buses; includes bus error detection and programmable time-out monitors on AHB-Lite master buses; and has address out-of-range detection on each crossbar switch buses.
- Event port collects and counts important signal events including DMA and interrupt requests and trigger events such as interrupts, breakpoints, DMA transfers, or wake-up events; units operate independently, in sequence, or triggered externally; can be used standalone or with the OCE10.
- Multi-channel DMA controller with 32 time-multiplexed unidirectional channels, priority-based time-multiplexing between channels using 32 internal priority levels, fixed- or round-robin-priority operation, major-minor loop structure, and DONE or DRACK protocol from requesting units.
- Two independent TDM modules with independent receive and transmit, programmable sharing of frame sync and clock, programmable word size (8 or 16-bit), hardware-base A-law/ μ -law conversion, up to 50 Mbps data rate per TDM, up to 128 channels, with glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses.
- UART with full-duplex operation up to 5.0 Mbps.
- Up to 41 general-purpose input/output (GPIO) ports.
- I²C interface that allows booting from EEPROM devices up to 1 Mbyte.
- Two quad timer modules, each with sixteen configurable 16-bit timers.
- fieldBIST™ unit detects and provides visibility into unlikely field failures for systems with high availability to ensure structural integrity, that the device operates at the rated speed, is free from reliability defects, and reports diagnostics for partial or complete device inoperability.
- Standard JTAG interface allows easy integration to system firmware and internal on-chip emulation (OCE10) module.
- Optional booting external host via 8-bit or 16-bit access through the HDI16, I²C, or SPI using in the boot ROM to access serial SPI Flash/EEPROM devices; different clocking options during boot with the PLL on or off using a variety of input frequency ranges.

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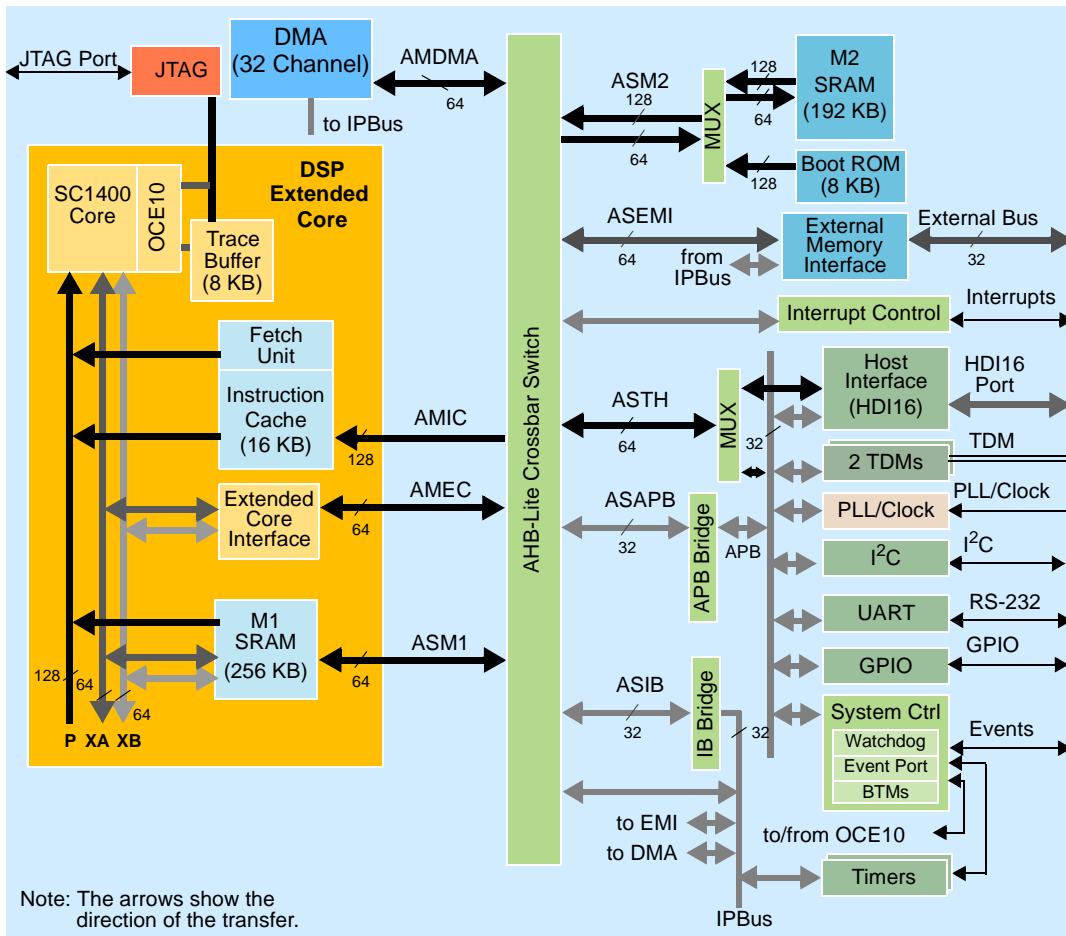


Figure 1. MSC7118 Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC7118 package ball grid array layouts and pinout allocation tables.

1.1 MAP-BGA Ball Layout Diagrams

Top and bottom views of the MAP-BGA package are shown in **Figure 2** and **Figure 3** with their ball location index numbers.

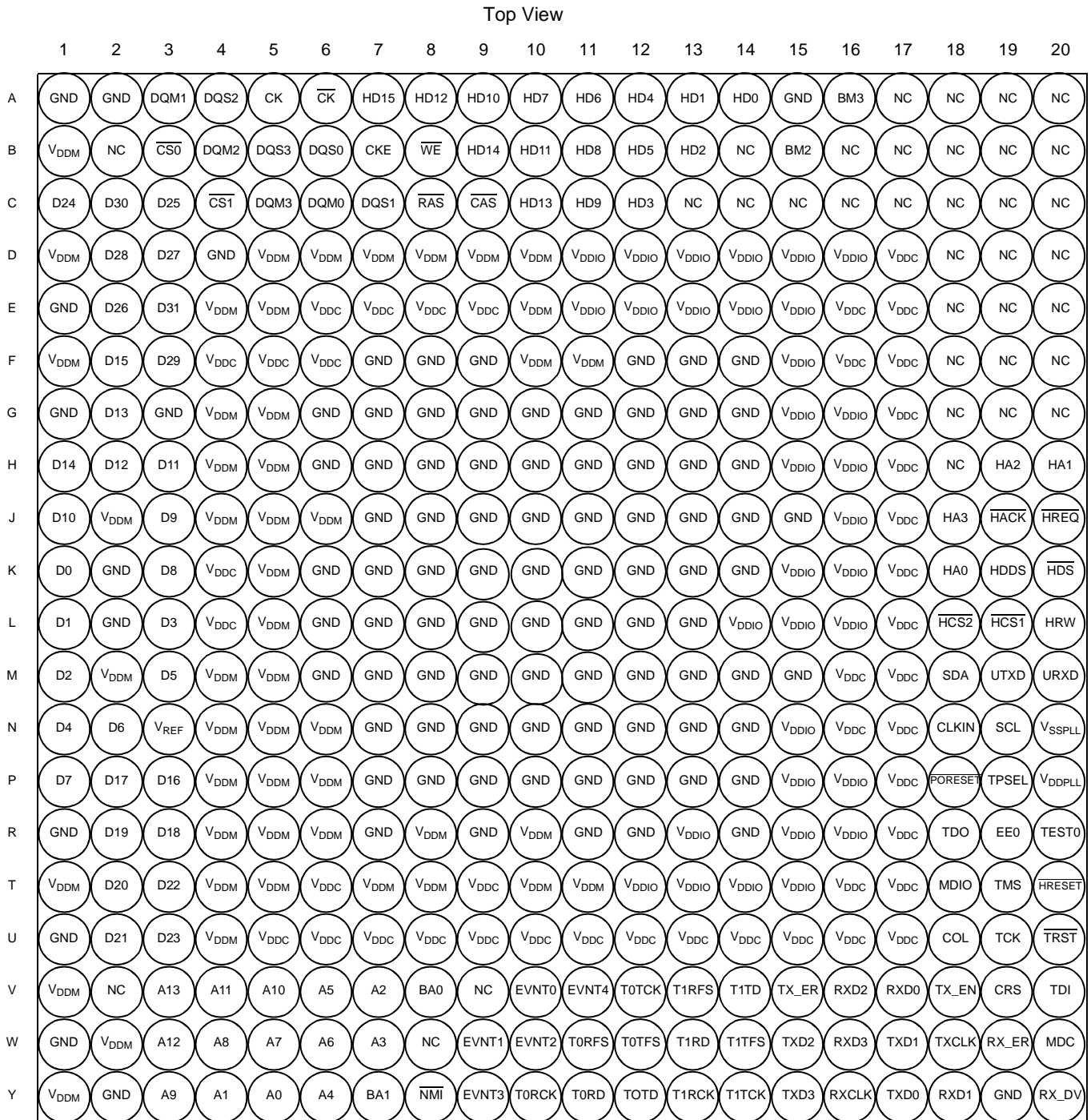


Figure 2. MSC7118 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

Bottom View

| | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---------------------|-------------------|----------------------|-----------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| A | NC | NC | NC | NC | BM3 | GND | HD0 | HD1 | HD4 | HD6 | HD7 | HD10 | HD12 | HD15 | \overline{CK} | CK | DQS2 | DQM1 | GND | GND |
| B | NC | NC | NC | NC | NC | BM2 | NC | HD2 | HD5 | HD8 | HD11 | HD14 | \overline{WE} | CKE | DQS0 | DQS3 | DQM2 | $\overline{CS0}$ | NC | V _{DDM} |
| C | NC | NC | NC | NC | NC | NC | NC | NC | HD3 | HD9 | HD13 | \overline{CAS} | \overline{RAS} | DQS1 | DQM0 | DQM3 | $\overline{CS1}$ | D25 | D30 | D24 |
| D | NC | NC | NC | V _{DD} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDM} | V _{DDM} | V _{DDM} | V _{DDM} | V _{DDM} | V _{DDM} | GND | D27 | D28 | V _{DDM} |
| E | NC | NC | NC | V _{DD} | V _{DD} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDM} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DDM} | V _{DDM} | D31 | D26 | GND |
| F | NC | NC | NC | V _{DD} | V _{DD} | V _{DDIO} | GND | GND | GND | V _{DDM} | V _{DDM} | GND | GND | GND | V _{DD} | V _{DD} | V _{DD} | D29 | D15 | V _{DDM} |
| G | NC | NC | NC | V _{DD} | V _{DDIO} | V _{DDIO} | GND | GND | GND | GND | GND | GND | GND | GND | GND | V _{DDM} | V _{DDM} | GND | D13 | GND |
| H | HA1 | HA2 | NC | V _{DD} | V _{DDIO} | V _{DDIO} | GND | GND | GND | GND | GND | GND | GND | GND | GND | V _{DDM} | V _{DDM} | D11 | D12 | D14 |
| J | \overline{HREQ} | \overline{HACK} | HA3 | V _{DD} | V _{DDIO} | GND | GND | GND | GND | GND | GND | GND | GND | GND | V _{DDM} | V _{DDM} | V _{DDM} | D9 | V _{DDM} | D10 |
| K | \overline{HDS} | HDDS | HA0 | V _{DD} | V _{DDIO} | V _{DDIO} | GND | GND | GND | GND | GND | GND | GND | GND | GND | V _{DDM} | V _{DD} | D8 | GND | D0 |
| L | HRW | $\overline{HCS1}$ | $\overline{HCS2}$ | V _{DD} | V _{DDIO} | V _{DDIO} | V _{DDIO} | GND | GND | GND | GND | GND | GND | GND | GND | V _{DDM} | V _{DD} | D3 | GND | D1 |
| M | URXD | UTXD | SDA | V _{DD} | V _{DD} | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | V _{DDM} | V _{DDM} | D5 | V _{DDM} | D2 |
| N | V _{SSPLL} | SCL | CLKIN | V _{DD} | V _{DD} | V _{DDIO} | GND | GND | GND | GND | GND | GND | GND | GND | V _{DDM} | V _{DDM} | V _{DDM} | V _{REF} | D6 | D4 |
| P | V _{DDPLL} | TPSEL | $\overline{PORESET}$ | V _{DD} | V _{DDIO} | V _{DDIO} | GND | GND | GND | GND | GND | GND | GND | GND | V _{DDM} | V _{DDM} | V _{DDM} | D16 | D17 | D7 |
| R | TEST0 | EE0 | TDO | V _{DD} | V _{DDIO} | V _{DDIO} | GND | V _{DDIO} | GND | GND | V _{DDM} | GND | V _{DDM} | GND | V _{DDM} | V _{DDM} | V _{DDM} | D18 | D19 | GND |
| T | \overline{HRESET} | TMS | MDIO | V _{DD} | V _{DD} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDIO} | V _{DDM} | V _{DDM} | V _{DD} | V _{DDM} | V _{DDM} | V _{DD} | V _{DDM} | V _{DDM} | D22 | D20 | V _{DDM} |
| U | \overline{TRST} | TCK | COL | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DD} | V _{DDM} | D23 | D21 | GND |
| V | TDI | CRS | TX_EN | RXD0 | RXD2 | TX_ER | T1TD | T1RFS | T0TCK | EVNT4 | EVNT0 | NC | BA0 | A2 | A5 | A10 | A11 | A13 | NC | V _{DDM} |
| W | MDC | RX_ER | TXCLK | TXD1 | RXD3 | TXD2 | T1TFS | T1RD | T0TFS | T0RFS | EVNT2 | EVNT1 | NC | A3 | A6 | A7 | A8 | A12 | V _{DDM} | GND |
| Y | RX_DV | GND | RXD1 | TXD0 | RXCLK | TXD3 | T1TCK | T1RCK | T0TD | T0RD | T0RCK | EVNT3 | \overline{NMI} | BA1 | A4 | A0 | A1 | A9 | GND | V _{DDM} |

Figure 3. MSC7118 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

1.2 Signal List By Ball Location

Table 1 lists the signals sorted by ball number and configuration.

Table 1. MSC7118 Signals by Ball Designator

| Number | Signal Names | | | | | |
|--------|--------------|-------------------------|-------------------|-------------|---------------------|-----------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| A1 | | GND | | | | |
| A2 | | GND | | | | |
| A3 | | DQM1 | | | | |
| A4 | | DQS2 | | | | |
| A5 | | CK | | | | |
| A6 | | $\overline{\text{CK}}$ | | | | |
| A7 | | GPIC7 | | GPOC7 | | HD15 |
| A8 | | GPIC4 | | GPOC4 | | HD12 |
| A9 | | GPIC2 | | GPOC2 | | HD10 |
| A10 | | reserved | | | | HD7 |
| A11 | | reserved | | | | HD6 |
| A12 | | reserved | | | | HD4 |
| A13 | | reserved | | | | HD1 |
| A14 | | reserved | | | | HD0 |
| A15 | | GND | | | | |
| A16 | BM3 | GPID8 | | GPOD8 | | reserved |
| A17 | | NC | | | | |
| A18 | | NC | | | | |
| A19 | | NC | | | | |
| A20 | | NC | | | | |
| B1 | | V_{DDM} | | | | |
| B2 | | NC | | | | |
| B3 | | $\overline{\text{CS0}}$ | | | | |
| B4 | | DQM2 | | | | |
| B5 | | DQS3 | | | | |
| B6 | | DQS0 | | | | |
| B7 | | CKE | | | | |
| B8 | | $\overline{\text{WE}}$ | | | | |
| B9 | | GPIC6 | | GPOC6 | | HD14 |
| B10 | | GPIC3 | | GPOC3 | | HD11 |
| B11 | | GPIC0 | | GPOC0 | | HD8 |
| B12 | | reserved | | | | HD5 |
| B13 | | reserved | | | | HD2 |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|-------------------------|-----------------------|-------------------|-------------|---------------------|-----------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| B14 | NC | | | | | |
| B15 | BM2 | GPID7 | | GPOD7 | reserved | |
| B16 | NC | | | | | |
| B17 | NC | | | | | |
| B18 | NC | | | | | |
| B19 | NC | | | | | |
| B20 | NC | | | | | |
| C1 | D24 | | | | | |
| C2 | D30 | | | | | |
| C3 | D25 | | | | | |
| C4 | $\overline{\text{CS1}}$ | | | | | |
| C5 | DQM3 | | | | | |
| C6 | DQM0 | | | | | |
| C7 | DQS1 | | | | | |
| C8 | $\overline{\text{RAS}}$ | | | | | |
| C9 | $\overline{\text{CAS}}$ | | | | | |
| C10 | GPIC5 | | | GPOC5 | HD13 | |
| C11 | GPIC1 | | | GPOC1 | HD9 | |
| C12 | reserved | | | | HD3 | |
| C13 | NC | | | | | |
| C14 | NC | | | | | |
| C15 | NC | | | | | |
| C16 | NC | | | | | |
| C17 | NC | | | | | |
| C18 | NC | | | | | |
| C19 | NC | | | | | |
| C20 | NC | | | | | |
| D1 | V_{DDM} | | | | | |
| D2 | D28 | | | | | |
| D3 | D27 | | | | | |
| D4 | GND | | | | | |
| D5 | V_{DDM} | | | | | |
| D6 | V_{DDM} | | | | | |
| D7 | V_{DDM} | | | | | |
| D8 | V_{DDM} | | | | | |
| D9 | V_{DDM} | | | | | |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|--------------|-----------------------|-------------------|-------------|---------------------|-------------------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| D10 | | | | | | V _{DDM} |
| D11 | | | | | | V _{DDIO} |
| D12 | | | | | | V _{DDIO} |
| D13 | | | | | | V _{DDIO} |
| D14 | | | | | | V _{DDIO} |
| D15 | | | | | | V _{DDIO} |
| D16 | | | | | | V _{DDIO} |
| D17 | | | | | | V _{DDC} |
| D18 | | | | | | NC |
| D19 | | | | | | NC |
| D20 | | | | | | NC |
| E1 | | | | | | GND |
| E2 | | | | | | D26 |
| E3 | | | | | | D31 |
| E4 | | | | | | V _{DDM} |
| E5 | | | | | | V _{DDM} |
| E6 | | | | | | V _{DDC} |
| E7 | | | | | | V _{DDC} |
| E8 | | | | | | V _{DDC} |
| E9 | | | | | | V _{DDC} |
| E10 | | | | | | V _{DDM} |
| E11 | | | | | | V _{DDIO} |
| E12 | | | | | | V _{DDIO} |
| E13 | | | | | | V _{DDIO} |
| E14 | | | | | | V _{DDIO} |
| E15 | | | | | | V _{DDIO} |
| E16 | | | | | | V _{DDC} |
| E17 | | | | | | V _{DDC} |
| E18 | | | | | | NC |
| E19 | | | | | | NC |
| E20 | | | | | | NC |
| F1 | | | | | | V _{DDM} |
| F2 | | | | | | D15 |
| F3 | | | | | | D29 |
| F4 | | | | | | V _{DDC} |
| F5 | | | | | | V _{DDC} |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|--------------|-----------------------|-------------------|-------------|---------------------|-------------------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| F6 | | | | | | V _{DDC} |
| F7 | | | | | | GND |
| F8 | | | | | | GND |
| F9 | | | | | | GND |
| F10 | | | | | | V _{DDM} |
| F11 | | | | | | V _{DDM} |
| F12 | | | | | | GND |
| F13 | | | | | | GND |
| F14 | | | | | | GND |
| F15 | | | | | | V _{DDIO} |
| F16 | | | | | | V _{DDC} |
| F17 | | | | | | V _{DDC} |
| F18 | | | | | | NC |
| F19 | | | | | | NC |
| F20 | | | | | | NC |
| G1 | | | | | | GND |
| G2 | | | | | | D13 |
| G3 | | | | | | GND |
| G4 | | | | | | V _{DDM} |
| G5 | | | | | | V _{DDM} |
| G6 | | | | | | GND |
| G7 | | | | | | GND |
| G8 | | | | | | GND |
| G9 | | | | | | GND |
| G10 | | | | | | GND |
| G11 | | | | | | GND |
| G12 | | | | | | GND |
| G13 | | | | | | GND |
| G14 | | | | | | GND |
| G15 | | | | | | V _{DDIO} |
| G16 | | | | | | V _{DDIO} |
| G17 | | | | | | V _{DDC} |
| G18 | | | | | | NC |
| G19 | | | | | | NC |
| G20 | | | | | | NC |
| H1 | | | | | | D14 |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|--------------|-----------------------|-------------------|-------------|---------------------|-----------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| H2 | | | | | D12 | |
| H3 | | | | | D11 | |
| H4 | | | | | V _{DDM} | |
| H5 | | | | | V _{DDM} | |
| H6 | | | | | GND | |
| H7 | | | | | GND | |
| H8 | | | | | GND | |
| H9 | | | | | GND | |
| H10 | | | | | GND | |
| H11 | | | | | GND | |
| H12 | | | | | GND | |
| H13 | | | | | GND | |
| H14 | | | | | GND | |
| H15 | | | | | V _{DDIO} | |
| H16 | | | | | V _{DDIO} | |
| H17 | | | | | V _{DDC} | |
| H18 | | | | | NC | |
| H19 | | reserved | | | | HA2 |
| H20 | | reserved | | | | HA1 |
| J1 | | | | | D10 | |
| J2 | | | | | V _{DDM} | |
| J3 | | | | | D9 | |
| J4 | | | | | V _{DDM} | |
| J5 | | | | | V _{DDM} | |
| J6 | | | | | V _{DDM} | |
| J7 | | | | | GND | |
| J8 | | | | | GND | |
| J9 | | | | | GND | |
| J10 | | | | | GND | |
| J11 | | | | | GND | |
| J12 | | | | | GND | |
| J13 | | | | | GND | |
| J14 | | | | | GND | |
| J15 | | | | | GND | |
| J16 | | | | | V _{DDIO} | |
| J17 | | | | | V _{DDC} | |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|-------------------|-----------------------|-------------------|--|--|-----------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| J18 | GPIC11 | | | GPOC11 | HA3 | |
| J19 | reserved | | | $\overline{\text{HACK}}/\text{HACK}$ or $\overline{\text{HRRQ}}/\text{HRRQ}$ | | |
| J20 | HDSP | reserved | | | $\overline{\text{HREQ}}/\text{HREQ}$ or $\overline{\text{HTRQ}}/\text{HTRQ}$ | |
| K1 | D0 | | | | | |
| K2 | GND | | | | | |
| K3 | D8 | | | | | |
| K4 | V_{DDC} | | | | | |
| K5 | V_{DDM} | | | | | |
| K6 | GND | | | | | |
| K7 | GND | | | | | |
| K8 | GND | | | | | |
| K9 | GND | | | | | |
| K10 | GND | | | | | |
| K11 | GND | | | | | |
| K12 | GND | | | | | |
| K13 | GND | | | | | |
| K14 | GND | | | | | |
| K15 | V_{DDIO} | | | | | |
| K16 | V_{DDIO} | | | | | |
| K17 | V_{DDC} | | | | | |
| K18 | reserved | | | HA0 | | |
| K19 | reserved | | | HDDS | | |
| K20 | reserved | | | $\overline{\text{HDS}}/\text{HDS}$ or $\overline{\text{HWR}}/\text{HWR}$ | | |
| L1 | D1 | | | | | |
| L2 | GND | | | | | |
| L3 | D3 | | | | | |
| L4 | V_{DDC} | | | | | |
| L5 | V_{DDM} | | | | | |
| L6 | GND | | | | | |
| L7 | GND | | | | | |
| L8 | GND | | | | | |
| L9 | GND | | | | | |
| L10 | GND | | | | | |
| L11 | GND | | | | | |
| L12 | GND | | | | | |
| L13 | GND | | | | | |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|-------------------|-----------------------|-------------------|----------------|---------------------|-----------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| L14 | V _{DDIO} | | | | | |
| L15 | V _{DDIO} | | | | | |
| L16 | V _{DDIO} | | | | | |
| L17 | V _{DDC} | | | | | |
| L18 | GPIB11 | | GPOB11 | HCS2/HCS2 | | |
| L19 | reserved | | | HCS1/HCS1 | | |
| L20 | reserved | | | HRW or HRD/HRD | | |
| M1 | D2 | | | | | |
| M2 | V _{DDM} | | | | | |
| M3 | D5 | | | | | |
| M4 | V _{DDM} | | | | | |
| M5 | V _{DDM} | | | | | |
| M6 | GND | | | | | |
| M7 | GND | | | | | |
| M8 | GND | | | | | |
| M9 | GND | | | | | |
| M10 | GND | | | | | |
| M11 | GND | | | | | |
| M12 | GND | | | | | |
| M13 | GND | | | | | |
| M14 | GND | | | | | |
| M15 | GND | | | | | |
| M16 | V _{DDC} | | | | | |
| M17 | V _{DDC} | | | | | |
| M18 | GPIA14 | IRQ15 | GPOA14 | SDA | | |
| M19 | GPIA12 | IRQ3 | GPOA12 | UTXD | | |
| M20 | GPIA13 | IRQ2 | GPOA13 | URXD | | |
| N1 | D4 | | | | | |
| N2 | D6 | | | | | |
| N3 | V _{REF} | | | | | |
| N4 | V _{DDM} | | | | | |
| N5 | V _{DDM} | | | | | |
| N6 | V _{DDM} | | | | | |
| N7 | GND | | | | | |
| N8 | GND | | | | | |
| N9 | GND | | | | | |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|-----------------------------|---------------------------|-------------------|-------------|---------------------|-----------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| N10 | GND | | | | | |
| N11 | GND | | | | | |
| N12 | GND | | | | | |
| N13 | GND | | | | | |
| N14 | GND | | | | | |
| N15 | V _{DDIO} | | | | | |
| N16 | V _{DDC} | | | | | |
| N17 | V _{DDC} | | | | | |
| N18 | CLKIN | | | | | |
| N19 | GPIA15 | $\overline{\text{IRQ14}}$ | GPOA15 | SCL | | |
| N20 | V _{SSPLL} | | | | | |
| P1 | D7 | | | | | |
| P2 | D17 | | | | | |
| P3 | D16 | | | | | |
| P4 | V _{DDM} | | | | | |
| P5 | V _{DDM} | | | | | |
| P6 | V _{DDM} | | | | | |
| P7 | GND | | | | | |
| P8 | GND | | | | | |
| P9 | GND | | | | | |
| P10 | GND | | | | | |
| P11 | GND | | | | | |
| P12 | GND | | | | | |
| P13 | GND | | | | | |
| P14 | GND | | | | | |
| P15 | V _{DDIO} | | | | | |
| P16 | V _{DDIO} | | | | | |
| P17 | V _{DDC} | | | | | |
| P18 | $\overline{\text{PORESET}}$ | | | | | |
| P19 | TPSEL | | | | | |
| P20 | V _{DDPLL} | | | | | |
| R1 | GND | | | | | |
| R2 | D19 | | | | | |
| R3 | D18 | | | | | |
| R4 | V _{DDM} | | | | | |
| R5 | V _{DDM} | | | | | |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|--------------|-----------------------|-------------------|-------------|---------------------|----------------------------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| R6 | | | | | | V _{DDM} |
| R7 | | | | | | GND |
| R8 | | | | | | V _{DDM} |
| R9 | | | | | | GND |
| R10 | | | | | | V _{DDM} |
| R11 | | | | | | GND |
| R12 | | | | | | GND |
| R13 | | | | | | V _{DDIO} |
| R14 | | | | | | GND |
| R15 | | | | | | V _{DDIO} |
| R16 | | | | | | V _{DDIO} |
| R17 | | | | | | V _{DDC} |
| R18 | | | | | | TDO |
| R19 | | reserved | | | | EE0/DBREQ |
| R20 | | | | | | TEST0 |
| T1 | | | | | | V _{DDM} |
| T2 | | | | | | D20 |
| T3 | | | | | | D22 |
| T4 | | | | | | V _{DDM} |
| T5 | | | | | | V _{DDM} |
| T6 | | | | | | V _{DDC} |
| T7 | | | | | | V _{DDM} |
| T8 | | | | | | V _{DDM} |
| T9 | | | | | | V _{DDC} |
| T10 | | | | | | V _{DDM} |
| T11 | | | | | | V _{DDM} |
| T12 | | | | | | V _{DDIO} |
| T13 | | | | | | V _{DDIO} |
| T14 | | | | | | V _{DDIO} |
| T15 | | | | | | V _{DDIO} |
| T16 | | | | | | V _{DDC} |
| T17 | | | | | | V _{DDC} |
| T18 | | reserved | | | | MDIO |
| T19 | | | | | | TMS |
| T20 | | | | | | $\overline{\text{HRESET}}$ |
| U1 | | | | | | GND |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|--------------|-----------------------|---------------------------|-------------|---------------------|--------------------------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| U2 | | | | | | D21 |
| U3 | | | | | | D23 |
| U4 | | | | | | V _{DDM} |
| U5 | | | | | | V _{DDC} |
| U6 | | | | | | V _{DDC} |
| U7 | | | | | | V _{DDC} |
| U8 | | | | | | V _{DDC} |
| U9 | | | | | | V _{DDC} |
| U10 | | | | | | V _{DDC} |
| U11 | | | | | | V _{DDC} |
| U12 | | | | | | V _{DDC} |
| U13 | | | | | | V _{DDC} |
| U14 | | | | | | V _{DDC} |
| U15 | | | | | | V _{DDC} |
| U16 | | | | | | V _{DDC} |
| U17 | | | | | | V _{DDC} |
| U18 | | reserved | | | | COL |
| U19 | | | | | | TCK |
| U20 | | | | | | $\overline{\text{TRST}}$ |
| V1 | | | | | | V _{DDM} |
| V2 | | | | | | NC |
| V3 | | | | | | A13 |
| V4 | | | | | | A11 |
| V5 | | | | | | A10 |
| V6 | | | | | | A5 |
| V7 | | | | | | A2 |
| V8 | | | | | | BA0 |
| V9 | | | | | | NC |
| V10 | | reserved | | | | EVNT0 |
| V11 | SWTE | GPIA16 | $\overline{\text{IRQ12}}$ | GPOA16 | | EVNT4 |
| V12 | | GPIA8 | $\overline{\text{IRQ6}}$ | GPOA8 | | T0TCK |
| V13 | | GPIA4 | $\overline{\text{IRQ1}}$ | GPOA4 | | T1RFS |
| V14 | | GPIA0 | $\overline{\text{IRQ11}}$ | GPOA0 | | T1TD |
| V15 | | GPIA28 | $\overline{\text{IRQ17}}$ | GPOA28 | TX_ER | reserved |
| V16 | | GPID6 | | GPOD6 | RXD2 | reserved |
| V17 | | GPIA22 | $\overline{\text{IRQ22}}$ | GPOA22 | | RXD0 |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|------------------|-----------------------|------------------------------|-------------|---------------------|-----------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| V18 | GPIA24 | | $\overline{\text{IRQ}}_{24}$ | GPOA24 | TX_EN | |
| V19 | reserved | | | | CRS | |
| V20 | TDI | | | | | |
| W1 | GND | | | | | |
| W2 | V_{DDM} | | | | | |
| W3 | A12 | | | | | |
| W4 | A8 | | | | | |
| W5 | A7 | | | | | |
| W6 | A6 | | | | | |
| W7 | A3 | | | | | |
| W8 | NC | | | | | |
| W9 | GPIA17 | | $\overline{\text{IRQ}}_{13}$ | GPOA17 | EVNT1 | CLKO |
| W10 | BM0 | GPIC14 | | GPOC14 | EVNT2 | |
| W11 | GPIA10 | | $\overline{\text{IRQ}}_{5}$ | GPOA10 | T0RFS | |
| W12 | GPIA7 | | $\overline{\text{IRQ}}_{7}$ | GPOA7 | T0TFS | |
| W13 | GPIA3 | | $\overline{\text{IRQ}}_{8}$ | GPOA3 | T1RD | |
| W14 | GPIA1 | | $\overline{\text{IRQ}}_{10}$ | GPOA1 | T1TFS | |
| W15 | GPID4 | | | GPOD4 | TXD2 | reserved |
| W16 | GPIA27 | | $\overline{\text{IRQ}}_{18}$ | GPOA27 | RXD3 | reserved |
| W17 | GPIA19 | | $\overline{\text{IRQ}}_{19}$ | GPOA19 | TXD1 | |
| W18 | GPIA23 | | $\overline{\text{IRQ}}_{23}$ | GPOA23 | TXCLK or REFCLK | |
| W19 | GPIA26 | | $\overline{\text{IRQ}}_{26}$ | GPOA26 | RX_ER | |
| W20 | H8BIT | reserved | | | MDC | |
| Y1 | V_{DDM} | | | | | |
| Y2 | GND | | | | | |
| Y3 | A9 | | | | | |
| Y4 | A1 | | | | | |
| Y5 | A0 | | | | | |
| Y6 | A4 | | | | | |
| Y7 | BA1 | | | | | |
| Y8 | reserved | | $\overline{\text{NMI}}$ | reserved | | |
| Y9 | BM1 | GPIC15 | | GPOC15 | EVNT3 | |
| Y10 | GPIA11 | | $\overline{\text{IRQ}}_{4}$ | GPOA11 | T0RCK | |
| Y11 | GPIA9 | | | GPOA9 | T0RD | |
| Y12 | GPIA6 | | | GPOA6 | T0TD | |
| Y13 | GPIA5 | | $\overline{\text{IRQ}}_{0}$ | GPOA5 | T1RCK | |

Table 1. MSC7118 Signals by Ball Designator (continued)

| Number | Signal Names | | | | | |
|--------|--------------|---------------------------|-------------------|-----------------|---------------------|-----------|
| | End of Reset | Software Controlled | | | Hardware Controlled | |
| | | GPI Enabled (Default) | Interrupt Enabled | GPO Enabled | Primary | Alternate |
| Y14 | GPIA2 | $\overline{\text{IRQ9}}$ | GPOA2 | T1TCK | | |
| Y15 | GPIA29 | $\overline{\text{IRQ16}}$ | GPOA29 | TXD3 | reserved | |
| Y16 | GPID5 | | GPOD5 | RXCLK | reserved | |
| Y17 | GPIA20 | $\overline{\text{IRQ20}}$ | GPOA20 | TXD0 | | |
| Y18 | GPIA21 | $\overline{\text{IRQ21}}$ | GPOA21 | RXD1 | | |
| Y19 | GND | | | | | |
| Y20 | GPIA25 | $\overline{\text{IRQ25}}$ | GPOA25 | RX_DV or CRS_DV | | |

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC711x Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC7118.

Table 2. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|-------------|--------------------|------|
| Core supply voltage | V_{DDC} | 1.5 | V |
| Memory supply voltage | V_{DDM} | 4.0 | V |
| PLL supply voltage | V_{DDPLL} | 1.5 | V |
| I/O supply voltage | V_{DDIO} | -0.2 to 4.0 | V |
| Input voltage | V_{IN} | (GND - 0.2) to 4.0 | V |
| Reference voltage | V_{REF} | 4.0 | V |
| Maximum operating temperature | T_J | 105 | °C |
| Minimum operating temperature | T_A | -40 | °C |
| Storage temperature range | T_{STG} | -55 to +150 | °C |
| Notes: <ol style="list-style-type: none"> 1. Functional operating conditions are given in Table 3. 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage. 3. Section 3.1, <i>Thermal Design Considerations</i> includes a formula for computing the chip junction temperature (T_J). | | | |

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

| Rating | Symbol | Value | Unit |
|-----------------------------|-------------|--------------|------|
| Core supply voltage | V_{DDC} | 1.14 to 1.26 | V |
| Memory supply voltage | V_{DDM} | 2.38 to 2.63 | V |
| PLL supply voltage | V_{DDPLL} | 1.14 to 1.26 | V |
| I/O supply voltage | V_{DDIO} | 3.14 to 3.47 | V |
| Reference voltage | V_{REF} | 1.19 to 1.31 | V |
| Operating temperature range | T_J | maximum: 105 | °C |
| | T_A | minimum: -40 | °C |

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC7118 for the MAP-BGA package.

Table 4. Thermal Characteristics for MAP-BGA Package

| Characteristic | Symbol | MAP-BGA 17 × 17 mm ⁵ | | Unit |
|---|-----------------|---------------------------------|----------------------------|------|
| | | Natural Convection | 200 ft/min (1 m/s) airflow | |
| Junction-to-ambient ^{1, 2} | $R_{\theta JA}$ | 39 | 31 | °C/W |
| Junction-to-ambient, four-layer board ^{1, 3} | $R_{\theta JA}$ | 23 | 20 | °C/W |
| Junction-to-board ⁴ | $R_{\theta JB}$ | 12 | | °C/W |
| Junction-to-case ⁵ | $R_{\theta JC}$ | 7 | | °C/W |
| Junction-to-package-top ⁶ | Ψ_{JT} | 2 | | °C/W |
| Notes: <ol style="list-style-type: none"> Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance). Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal. Per JEDEC JESD51-6 with the board horizontal. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. | | | | |

Section 3.1, *Thermal Design Considerations* explains these characteristics in detail.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC7118.

Note: The leakage current is measured for nominal voltage values must vary in the same direction (for example, both V_{DDIO} and V_{DDC} vary by +2 percent or both vary by -2 percent).

Table 5. DC Electrical Characteristics

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|--------------------------|-----------------------|-----------|-----------------------|------|
| Core and PLL voltage | V_{DDC} V_{DDPLL} | 1.14 | 1.2 | 1.26 | V |
| DRAM interface I/O voltage ¹ | V_{DDM} | 2.375 | 2.5 | 2.625 | V |
| I/O voltage | V_{DDIO} | 3.135 | 3.3 | 3.465 | V |
| DRAM interface I/O reference voltage ² | V_{REF} | $0.49 \times V_{DDM}$ | 1.25 | $0.51 \times V_{DDM}$ | V |
| DRAM interface I/O termination voltage ³ | VTT | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ | V |
| Input high CLKIN voltage | V_{IHCLK} | 2.4 | 3.0 | 3.465 | V |
| DRAM interface input high I/O voltage | V_{IHM} | $V_{REF} + 0.28$ | V_{DDM} | $V_{DDM} + 0.3$ | V |
| DRAM interface input low I/O voltage | V_{ILM} | -0.3 | GND | $V_{REF} - 0.18$ | V |
| Input leakage current, $V_{IN} = V_{DDIO}$ | I_{IN} | -1.0 | 0.09 | 1 | μA |
| V_{REF} input leakage current | I_{VREF} | — | — | 5 | μA |

Table 5. DC Electrical Characteristics (continued)

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|----------|------|---------|-----|---------|
| Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDIO}$ | I_{OZ} | -1.0 | 0.09 | 1 | μA |
| Signal low input current, $V_{IL} = 0.4 V$ | I_L | -1.0 | 0.09 | 1 | μA |
| Signal high input current, $V_{IH} = 2.0 V$ | I_H | -1.0 | 0.09 | 1 | μA |
| Output high voltage, $I_{OH} = -2 mA$, except open drain pins | V_{OH} | 2.0 | 3.0 | — | V |
| Output low voltage, $I_{OL} = 5 mA$ | V_{OL} | — | 0 | 0.4 | V |
| Typical power at 300 MHz ⁵ | P | — | 324.0 | — | mW |
| Notes: <ol style="list-style-type: none"> 1. The value of V_{DDM} at the MSC7118 device must remain within 50 mV of V_{DDM} at the DRAM device at all times. 2. V_{REF} must be equal to 50% of V_{DDM} and track V_{DDM} variations as measured at the receiver. Peak-to-peak noise must not exceed $\pm 2\%$ of the DC value. 3. V_{TT} is not applied directly to the MSC7118 device. It is the level measured at the far end signal termination. It should be equal to V_{REF}. This rail should track variations in the DC level of V_{REF}. 4. Output leakage for the memory interface is measured with all outputs disabled, $0 V \leq V_{OUT} \leq V_{DDM}$. 5. The core power values were measured using a standard EFR pattern at typical conditions (25°C, 300 MHz, 1.2 V core). | | | | | |

Table 6 lists the DDR DRAM capacitance.

Table 6. DDR DRAM Capacitance

| Parameter/Condition | Symbol | Max | Unit |
|--|-----------|-----|------|
| Input/output capacitance: DQ, DQS | C_{IO} | 30 | pF |
| Delta input/output capacitance: DQ, DQS | C_{DIO} | 30 | pF |
| Note: These values were measured under the following conditions: <ul style="list-style-type: none"> • $V_{DDM} = 2.5 V \pm 0.125 V$ • $f = 1 MHz$ • $T_A = 25^\circ C$ • $V_{OUT} = V_{DDM}/2$ • V_{OUT} (peak to peak) = 0.2 V | | | |

2.5 AC Timings

This section presents timing diagrams and specifications for individual signals and parallel I/O outputs and inputs. All AC timings are based on a 30 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, use the following equations to compute the delay:

- Standard interface: $2.45 + (0.054 \times C_{load})$ ns
- DDR interface: $1.6 + (0.002 \times C_{load})$ ns

2.5.1 Clock and Timing Signals

The following tables describe clock signal characteristics. **Table 6** shows the maximum frequency values for internal (core, reference, and peripherals) and external (CLKO) clocks. You must ensure that maximum frequency values are not exceeded (see **Section 2.5.2** for the allowable ranges when using the PLL).

Table 6. Maximum Frequencies

| Characteristic | Maximum in MHz |
|---|----------------|
| Core clock frequency (CLOCK) | 300 |
| External output clock frequency (CLKO) | 75 |
| Memory clock frequency (CK, \overline{CK}) | 150 |
| TDM clock frequency (TxRCK, TxTCK) | 50 |

Table 7. Clock Frequencies in MHz

| Characteristic | Symbol | Min | Max |
|---|-------------|-----|-----|
| CLKIN frequency | F_{CLKIN} | 10 | 100 |
| CLOCK frequency | F_{CORE} | — | 300 |
| CK, \overline{CK} frequency | F_{CK} | — | 150 |
| TDMxRCK, TDMxTCK frequency | F_{TDMCK} | — | 50 |
| CLKO frequency | F_{CKO} | — | 75 |
| AHB/IPBus/APB clock frequency | F_{BCK} | — | 150 |
| Note: The rise and fall time of external clocks should be 5 ns maximum | | | |

Table 8. System Clock Parameters

| Characteristic | Min | Max | Unit |
|---------------------------------------|-----|------|------|
| CLKIN frequency | 10 | 100 | MHz |
| CLKIN slope | — | 5 | ns |
| CLKIN frequency jitter (peak-to-peak) | — | 1000 | ps |
| CLKO frequency jitter (peak-to-peak) | — | 150 | ps |

2.5.2 Configuring Clock Frequencies

This section describes important requirements for configuring clock frequencies in the MSC7118 device when using the PLL block. To configure the device clocking, you must program four fields in the Clock Control Register (CLKCTL):

- *PLLDVF field.* Specifies the PLL division factor ($PLLDVF + 1$) to divide the input clock frequency F_{CLKIN} . The output of the divider block is the input to the multiplier block.
- *PLLMLTF field.* Specifies the PLL multiplication factor ($PLLMLTF + 1$). The output from the multiplier block is the loop frequency F_{LOOP} .
- *RNG field.* Selects the available PLL frequency range for F_{VCO} , either F_{LOOP} when the RNG bit is set (1) or $F_{LOOP}/2$ when the RNG bit is cleared (0).
- *CKSEL field.* Selects F_{CLKIN} , F_{VCO} , or $F_{VCO}/2$ as the source for the core clock.

There are restrictions on the frequency range permitted at the beginning of the multiplication portion of the PLL that affect the allowable values for the PLLDVF and PLLMLTF fields. The following sections define these restrictions and provide guidelines to configure the device clocking when using the PLL. Refer to the Clock and Power Management chapter in the *MSC711x Reference Manual* for details on the clock programming model.

2.5.2.1 PLL Multiplier Restrictions

There are two restrictions for correct usage of the PLL block:

- The input frequency to the PLL multiplier block (that is, the output of the divider) must be in the range 10–25 MHz.
- The output frequency of the PLL multiplier must be in the range 266–532 MHz.

When programming the PLL for a desired output frequency using the PLLDVF, PLLMLTF, and RNG fields, you must meet these constraints.

2.5.2.2 Input Division Factors and Corresponding CLKIN Frequency Range

The value of the PLLDVF field determines the allowable CLKIN frequency range, as shown in **Table 9**.

Table 9. CLKIN Frequency Ranges by Divide Factor Value

| PLLDVF Field Value | Input Divide Factor | CLKIN Frequency Range | Comments |
|--------------------|---------------------|-----------------------|----------------------|
| 0x00 | 1 | 10 to 25 MHz | Input Division by 1 |
| 0x01 | 2 | 20 to 50 MHz | Input Division by 2 |
| 0x02 | 3 | 30 to 75 MHz | Input Division by 3 |
| 0x03 | 4 | 40 to 100 MHz | Input Division by 4 |
| 0x04 | 5 | 50 to 100 MHz | Input Division by 5 |
| 0x05 | 6 | 60 to 100 MHz | Input Division by 6 |
| 0x06 | 7 | 70 to 100 MHz | Input Division by 7 |
| 0x07 | 8 | 80 to 100 MHz | Input Division by 8 |
| 0x08 | 9 | 90 to 100 MHz | Input Division by 9 |
| 0x09 | 10 | 100 MHz | Input Division by 10 |

Note: The maximum CLKIN frequency is 100 MHz. Therefore, the PLLDVF value must be in the range from 1–10.

2.5.2.3 Multiplication Factor Range

The multiplier block output frequency ranges depend on the divided input clock frequency as shown in **Table 10**.

Table 10. PLLMLTF Ranges

| Multiplier Block (Loop) Output Range | Minimum PLLMLTF Value | Maximum PLLMLTF Value |
|--|-------------------------|-------------------------|
| $266 \leq [\text{Divided Input Clock} \times (\text{PLLMLTF} + 1)] \leq 532 \text{ MHz}$ | 266/Divided Input Clock | 532/Divided Input Clock |
| Note: This table results from the allowed range for F_{Loop} . The minimum and maximum multiplication factors are dependent on the frequency of the Divided Input Clock. | | |

2.5.2.4 Allowed Core Clock Frequency Range

The frequency delivered to the core, extended core, and peripherals depends on the value of the CLKCTRL[RNG] bit as shown in **Table 11**.

Table 11. F_{VCO} Frequency Ranges

| CLKCTRL[RNG] Value | Allowed Range of F_{VCO} |
|--|--|
| 1 | $266 \leq F_{\text{VCO}} \leq 532 \text{ MHz}$ |
| 0 | $133 \leq F_{\text{VCO}} \leq 266 \text{ MHz}$ |
| Note: This table results from the allowed range for F_{VCO} , which is F_{Loop} modified by CLKCTRL[RNG]. | |

This bit along with the CKSEL determines the frequency range of the core clock.

Table 12. Resulting Ranges Permitted for the Core Clock

| CLKCTRL[CKSEL] | CLKCTRL[RNG] | Resulting Division Factor | Allowed Range of Core Clock | Comments |
|---|--------------|---------------------------|--|-----------------------------------|
| 11 | 1 | 1 | $266 \leq \text{core clock} \leq 300 \text{ MHz}$ | Limited by maximum core frequency |
| 11 | 0 | 2 | $133 \leq \text{core clock} \leq 266 \text{ MHz}$ | Limited by range of PLL |
| 01 | 1 | 2 | $133 \leq \text{core clock} \leq 266 \text{ MHz}$ | Limited by range of PLL |
| 01 | 0 | 4 | $66.5 \leq \text{core clock} \leq 133 \text{ MHz}$ | Limited by range of PLL |
| Note: This table results from the allowed range for F_{OUT} , which depends on clock selected via CLKCTRL[CKSEL]. | | | | |

2.5.2.5 Core Clock Frequency Range When Using DDR Memory

The core clock can also be limited by the frequency range of the DDR devices in the system. **Table 13** summarizes this restriction.

Table 13. Core Clock Ranges When Using DDR

| DDR Type | Allowed Frequency Range for DDR CK | Corresponding Range for the Core Clock | Comments |
|-------------------|------------------------------------|---|--|
| DDR 200 (PC-1600) | 83–100 MHz | $166 \leq \text{core clock} \leq 200 \text{ MHz}$ | Core limited to $2 \times$ maximum DDR frequency |
| DDR 266 (PC-2100) | 83–133 MHz | $166 \leq \text{core clock} \leq 266 \text{ MHz}$ | Core limited to $2 \times$ maximum DDR frequency |
| DDR 333 (PC-2600) | 83–150 MHz | $166 \leq \text{core clock} \leq 300 \text{ MHz}$ | Core limited to $2 \times$ maximum DDR frequency |

2.5.3 Reset Timing

The MSC7118 device has several inputs to the reset logic. All MSC7118 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 14** describes the reset sources.

Table 14. Reset Sources

| Name | Direction | Description |
|--------------------------------------|---------------|---|
| Power-on reset (PORESET) | Input | Initiates the power-on reset flow that resets the MSC7118 and configures various attributes of the MSC7118. On PORESET, the entire MSC7118 device is reset. SPL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted. |
| External Hard reset (HRESET) | Input/ Output | Initiates the hard reset flow that configures various attributes of the MSC7118. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset. |
| Software watchdog reset | Internal | When the MSC7118 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence. |
| Bus monitor reset | Internal | When the MSC7118 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence. |
| JTAG EXTEST, CLAMP, or HIGHZ command | Internal | When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence. |

Table 15 summarizes the reset actions that occur as a result of the different reset sources.

Table 15. Reset Actions for Each Reset Source

| Reset Action/Reset Source | Power-On Reset (PORESET) | Hard Reset (HRESET) | Soft Reset (SRESET) |
|---|--------------------------|---|---------------------------------------|
| | External only | External or Internal (Software Watchdog or Bus Monitor) | JTAG Command: EXTEST, CLAMP, or HIGHZ |
| Configuration pins sampled (refer to Section 2.5.3.1 for details). | Yes | No | No |
| PLL and clock synthesis states Reset | Yes | No | No |
| HRESET Driven | Yes | Yes | No |
| Software watchdog and bus time-out monitor registers | Yes | Yes | Yes |
| Clock synthesis modules (STOPCTRL, HLTREQ, and HLTACK) reset | Yes | Yes | Yes |
| Extended core reset | Yes | Yes | Yes |
| Peripheral modules reset | Yes | Yes | Yes |

2.5.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after external power to the MSC7118 reaches at least $2/3 V_{DD}$.

2.5.3.2 Reset Configuration

The MSC7118 has two mechanisms for writing the reset configuration:

- From a host through the host interface (HDI16)
- From memory through the I²C interface

Five signal levels (see **Chapter 1** for signal description details) are sampled on $\overline{\text{PORESET}}$ deassertion to define the boot and operating conditions:

- BM[0–1]
- SWTE
- H8BIT
- HDSP

2.5.3.3 Reset Timing Tables

Table 16 and **Figure 4** describe the reset timing for a reset configuration write.

Table 16. Timing for a Reset Configuration Write

| No. | Characteristics | Expression | Unit |
|-----|--|------------------------|--------|
| 1 | Required external $\overline{\text{PORESET}}$ duration minimum | $16/F_{\text{CLKIN}}$ | clocks |
| 2 | Delay from $\overline{\text{PORESET}}$ deassertion to $\overline{\text{HRESET}}$ deassertion | $521/F_{\text{CLKIN}}$ | clocks |

Note: Timings are not tested, but are guaranteed by design.

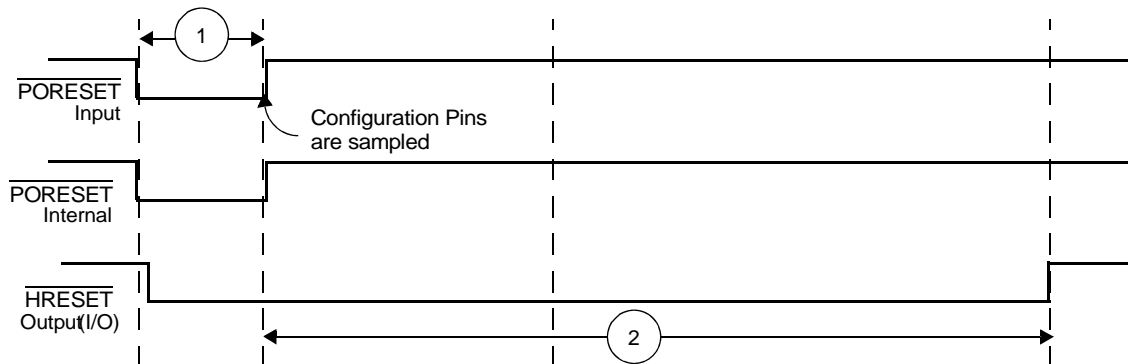


Figure 4. Timing Diagram for a Reset Configuration Write

2.5.4 DDR DRAM Controller Timing

This section provides the AC electrical characteristics for the DDR DRAM interface.

2.5.4.1 DDR DRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR DRAM interface.

Table 17. DDR DRAM Input AC Timing

| No. | Parameter | Symbol | Min | Max | Unit |
|-----|--|----------|------------------|------------------|------|
| — | AC input low voltage | V_{IL} | — | $V_{REF} - 0.31$ | V |
| — | AC input high voltage | V_{IH} | $V_{REF} + 0.31$ | $V_{DDM} + 0.3$ | V |
| 201 | Maximum Dn input setup skew relative to DQSn input | — | — | 900 | ps |
| 202 | Maximum Dn input hold skew relative to DQSn input | — | — | 900 | ps |

Notes:

1. Maximum possible skew between a data strobe (DQSn) and any corresponding bit of data (D[8n + {0...7}] if $0 \leq n \leq 7$).
2. See Table 18 for t_{CK} value.
3. Dn should be driven at the same time as DQSn. This is necessary because the DQSn centering on the DQn data tenure is done internally.

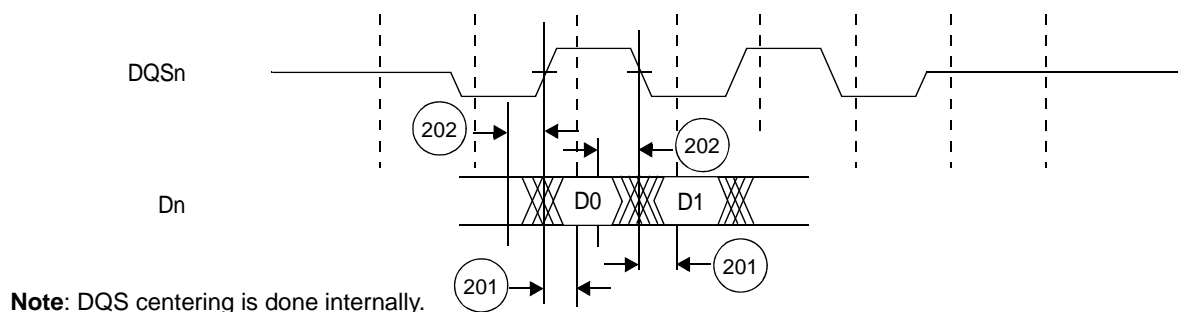


Figure 5. DDR DRAM Input Timing Diagram

2.5.4.2 DDR DRAM Output AC Timing Specifications

Table 18 and Table 19 list the output AC timing specifications and measurement conditions for the DDR DRAM interface.

Table 18. DDR DRAM Output AC Timing

| No. | Parameter | Symbol | Min | Max | Unit |
|-----|--|---------------|----------------------------|--------|----------|
| 200 | CK cycle time, (CK/ \overline{CK} crossing) ¹ • 100 MHz (DDR200) • 150 MHz (DDR300) | t_{CK} | 10 6.67 | — — | ns ns |
| 204 | $\overline{An}/\overline{RAS}/\overline{CAS}/\overline{WE}/\overline{CKE}$ output setup with respect to CK | t_{DDKHAS} | $0.5 \times t_{CK} - 1000$ | — | ps |
| 205 | $\overline{An}/\overline{RAS}/\overline{CAS}/\overline{WE}/\overline{CKE}$ output hold with respect to CK | t_{DDKHAX} | $0.5 \times t_{CK} - 1000$ | — | ps |
| 206 | \overline{CSn} output setup with respect to CK | t_{DDKHCS} | $0.5 \times t_{CK} - 1000$ | — | ps |
| 207 | \overline{CSn} output hold with respect to CK | $t_{DDKHCSX}$ | $0.5 \times t_{CK} - 1000$ | — | ps |
| 208 | CK to DQSn ² | t_{DDKHMH} | -600 | 600 | ps |

Table 18. DDR DRAM Output AC Timing (continued)

| No. | Parameter | Symbol | Min | Max | Unit |
|-----|--|--------------------------------|----------------------------|-----|------|
| 209 | Dn/DQMn output setup with respect to DQSn ³ | t_{DDKHDS} , t_{DDKLDS} | $0.25 \times t_{CK} - 750$ | — | ps |
| 210 | Dn/DQMn output hold with respect to DQSn ³ | t_{DDKHDX} , t_{DDKLDX} | $0.25 \times t_{CK} - 750$ | — | ps |
| 211 | DQSn preamble start ⁴ | t_{DDKHMP} | $-0.25 \times t_{CK}$ | — | ps |
| 212 | DQSn epilogue end ⁵ | t_{DDKHME} | -600 | 600 | ps |

- Notes:**
- All $\overline{CK}/\overline{CK}$ referenced measurements are made from the crossing of the two signals ± 0.1 V.
 - t_{DDKHMH} can be modified through the TCFG2[WRDD] DQSS override bits. The DRAM requires that the first write data strobe arrives 75–125% of a DRAM cycle after the write command is issued. Any skew between DQSn and CK must be considered when trying to achieve this 75%–125% goal. The TCFG2[WRDD] bits can be used to shift DQSn by 1/4 DRAM cycle increments. The skew in this case refers to an internal skew existing at the signal connections. By default, the $\overline{CK}/\overline{CK}$ crossing occurs in the middle of the control signal ($\overline{An}/\overline{RAS}/\overline{CAS}/\overline{WE}/\overline{CKE}$) tenure. Setting TCFG2[ACSM] bit shifts the control signal assertion 1/2 DRAM cycle earlier than the default timing. This means that the signal is asserted no earlier than 600 ps before the $\overline{CK}/\overline{CK}$ crossing and no later than 600 ps after the crossing time; the device uses 1200 ps of the skew budget (the interval from -600 to +600 ps). Timing is verified by referencing the falling edge of CK. See Chapter 10 of the *MSC711x Reference Manual* for details.
 - Determined by maximum possible skew between a data strobe (DQS) and any corresponding bit of data. The data strobe should be centered inside of the data eye.
 - Please note that this spec is in reference to the DQSn first rising edge. It could also be referenced from $\overline{CK}(r)$, but due to programmable delay of the write strobes (TCFG2[WRDD]), there pre-amble may be extended for a full DRAM cycle. For this reason, we reference from DQSn.
 - All outputs are referenced to the rising edge of CK. Note that this is essentially the $\overline{CK}/\overline{CK}$ skew in spec 208. In addition there is no real “maximum” time for the epilogue end. JEDEC does not require this is as a device limitation, but simply for the chip to guarantee fast enough write-to-read turn-around times. This is already guaranteed by the memory controller operation.

Figure 6 shows the DDR DRAM output timing diagram.

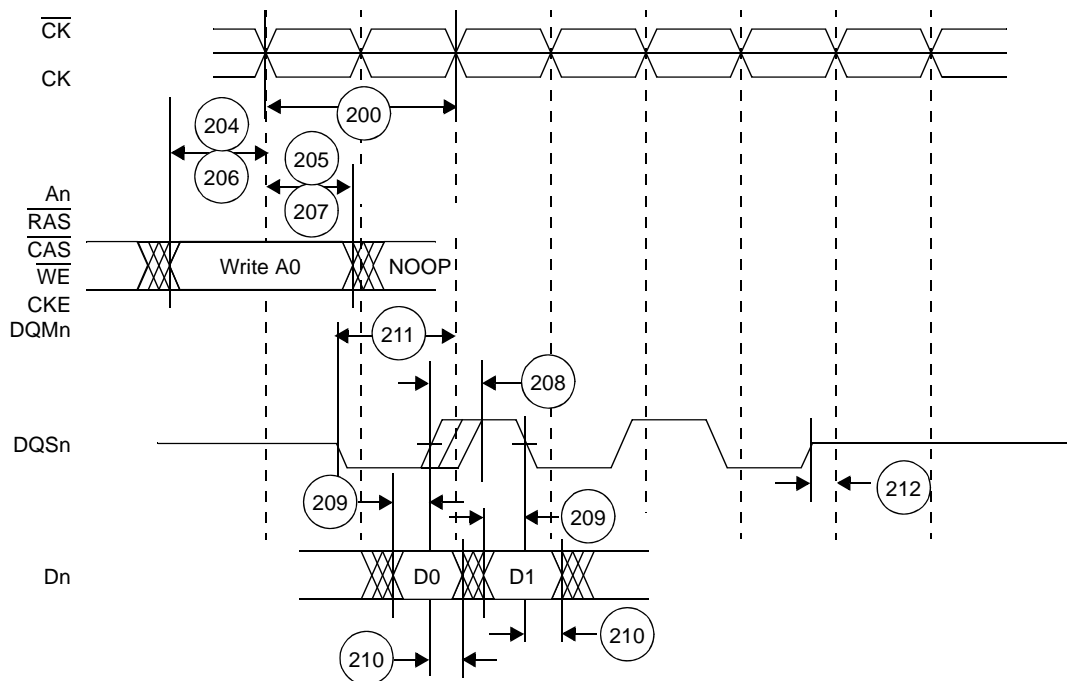


Figure 6. DDR DRAM Output Timing Diagram

Figure 7 provides the AC test load for the DDR DRAM bus.

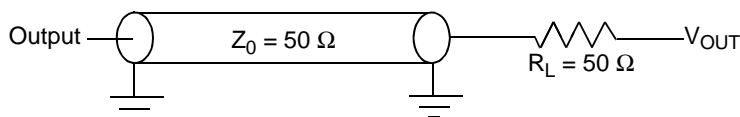


Figure 7. DDR DRAM AC Test Load

Table 19. DDR DRAM Measurement Conditions

| Symbol | DDR DRAM | Unit |
|-------------|----------------------|------|
| V_{TH}^1 | $V_{REF} \pm 0.31 V$ | V |
| V_{OUT}^2 | $0.5 \times V_{DDM}$ | V |

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

2.5.5 TDM Timing

Table 20. TDM Timing

| No. | Characteristic | Expression | Min | Max | Units |
|-----|--|-----------------|------|------|-------|
| 300 | TDMxRCK/TDMxTCK | TC | 20.0 | — | ns |
| 301 | TDMxRCK/TDMxTCK High Pulse Width | $0.4 \times TC$ | 8.0 | — | ns |
| 302 | TDMxRCK/TDMxTCK Low Pulse Width | $0.4 \times TC$ | 8.0 | — | ns |
| 303 | TDM all input Setup time | | 3.0 | — | ns |
| 304 | TDMxRD Hold time | | 3.5 | — | ns |
| 305 | TDMxTFS/TDMxRFS input Hold time | | 2.0 | — | ns |
| 306 | TDMxTCK High to TDMxTD output active | | 4.0 | — | ns |
| 307 | TDMxTCK High to TDMxTD output valid | | — | 14.0 | ns |
| 308 | TDMxTD hold time | | 2.0 | — | ns |
| 309 | TDMxTCK High to TDMxTD output high impedance | | — | 10.0 | ns |
| 310 | TDMxTFS/TDMxRFS output valid | | — | 13.5 | ns |
| 311 | TDMxTFS/TDMxRFS output hold time | | 2.5 | — | ns |

Notes:

1. Output values are based on 30 pF capacitive load.
2. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. Refer to the *MSC711x Reference Manual* for details. TDMxTCK and TDMxRCK are shown using the rising edge.

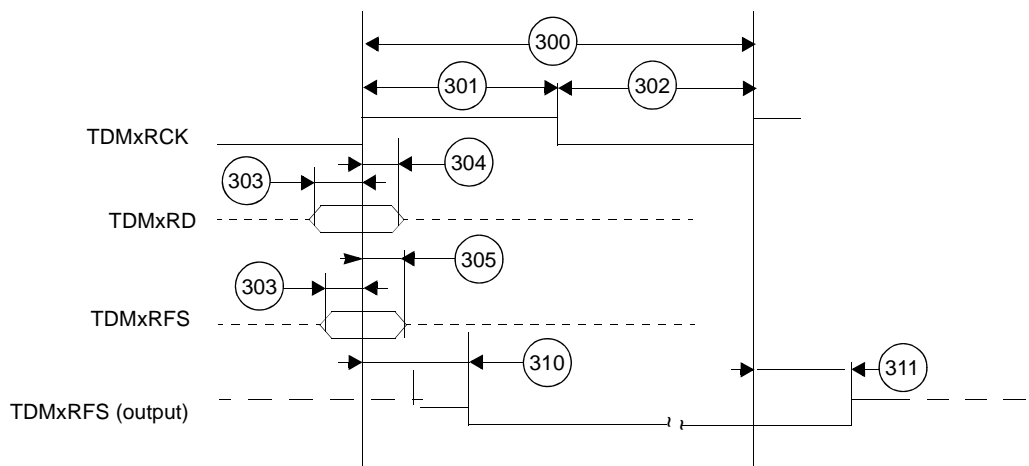


Figure 8. TDM Receive Signals

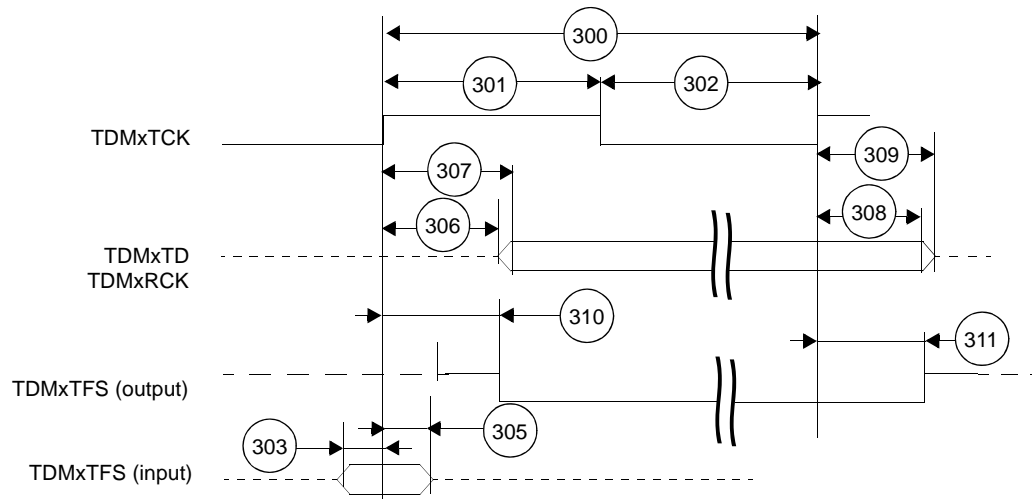


Figure 9. TDM Transmit Signals

2.5.6 HDI16 Signals

Table 21. Host Interface (HDI16) Timing^{1, 2}

| No. | Characteristics ³ | Expression | Value | Unit |
|-----|--|-------------------------------|---------|------|
| 40 | Host Interface Clock period | T_{CORE} | Note 1 | ns |
| 44a | Read data strobe minimum assertion width ⁴ HACK read minimum assertion width | $2.0 \times T_{CORE} + 9.0$ | Note 11 | ns |
| 44b | Read data strobe minimum deassertion width ⁴ HACK read minimum deassertion width | $1.5 \times T_{CORE}$ | Note 11 | ns |
| 44c | Read data strobe minimum deassertion width ⁴ after "Last Data Register" reads ^{5,6} , or between two consecutive CVR, ICR, or ISR reads ⁷ HACK minimum deassertion width after "Last Data Register" reads ^{5,6} | $2.5 \times T_{CORE}$ | Note 11 | ns |
| 45 | Write data strobe minimum assertion width ⁸ HACK write minimum assertion width | $1.5 \times T_{CORE}$ | Note 11 | ns |
| 46 | Write data strobe minimum deassertion width ⁸ HACK write minimum deassertion width after ICR, CVR and Data Register writes ⁵ | $2.5 \times T_{CORE}$ | Note 11 | ns |
| 47 | Host data input minimum setup time before write data strobe deassertion ⁸ Host data input minimum setup time before HACK write deassertion | — | 2.5 | ns |
| 48 | Host data input minimum hold time after write data strobe deassertion ⁸ Host data input minimum hold time after HACK write deassertion | — | 2.5 | ns |
| 49 | Read data strobe minimum assertion to output data active from high impedance ⁴ HACK read minimum assertion to output data active from high impedance | — | 1.0 | ns |
| 50 | Read data strobe maximum assertion to output data valid ⁴ HACK read maximum assertion to output data valid | $(2.0 \times T_{CORE}) + 8.0$ | Note 11 | ns |
| 51 | Read data strobe maximum deassertion to output data high impedance ⁴ HACK read maximum deassertion to output data high impedance | — | 9.0 | ns |
| 52 | Output data minimum hold time after read data strobe deassertion ⁴ Output data minimum hold time after HACK read deassertion | — | 1.0 | ns |
| 53 | HCS[1–2] minimum assertion to read data strobe assertion ⁴ | — | 0.5 | ns |
| 54 | HCS[1–2] minimum assertion to write data strobe assertion ⁸ | — | 0.0 | ns |
| 55 | HCS[1–2] maximum assertion to output data valid | $(2.0 \times T_{CORE}) + 6.0$ | Note 11 | ns |
| 56 | HCS[1–2] minimum hold time after data strobe deassertion ⁹ | — | 0.5 | ns |
| 57 | HA[0–2], HRW minimum setup time before data strobe assertion ⁹ | — | 5.0 | ns |
| 58 | HA[0–2], HRW minimum hold time after data strobe deassertion ⁹ | — | 5.0 | ns |
| 61 | Maximum delay from read data strobe deassertion to host request deassertion for "Last Data Register" read ^{4, 5, 10} | $(3.0 \times T_{CORE}) + 6.0$ | Note 11 | ns |
| 62 | Maximum delay from write data strobe deassertion to host request deassertion for "Last Data Register" write ^{5,8,10} | $(3.0 \times T_{CORE}) + 6.0$ | Note 11 | ns |
| 63 | Minimum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) deassertion to HREQ assertion. | $(2.0 \times T_{CORE}) + 1.0$ | Note 11 | ns |
| 64 | Maximum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) assertion to HREQ deassertion | $(5.0 \times T_{CORE}) + 6.0$ | Note 11 | ns |

- Notes:**
- T_{CORE} = core clock period. At 300 MHz, T_{CORE} = 3.333 ns.
 - In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
 - $V_{DD} = 3.3 \text{ V} \pm 0.15 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $C_L = 30 \text{ pF}$ for maximum delay timings and $C_L = 0 \text{ pF}$ for minimum delay timings.
 - The read data strobe is HRD/HRD in the dual data strobe mode and HDS/HDS in the single data strobe mode.
 - For 64-bit transfers, the "last data register" is the register at address 0x7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
 - This timing is applicable only if a read from the "last data register" is followed by a read from the RX[0–3] registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ/HREQ signal.
 - This timing is applicable only if two consecutive reads from one of these registers are executed.
 - The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
 - The data strobe is host read (HRD/HRD) or host write (HWR/HWR) in the dual data strobe mode and host data strobe (HDS/HDS) in the single data strobe mode.
 - The host request is HREQ/HREQ in the single host request mode and HRRQ/HRRQ and HTRQ/HTRQ in the double host request mode. HRRQ/HRRQ is deasserted only when HOTX fifo is empty, HTRQ/HTRQ is deasserted only if HORX fifo is full
 - Compute the value using the expression.
 - The read and write data strobe minimum deassertion width for non-"last data register" accesses in single and dual data strobe modes is based on timings 57 and 58.

Figure 10 and Figure 11 show HDI16 read signal timing. Figure 12 and Figure 13 show HDI16 write signal timing.

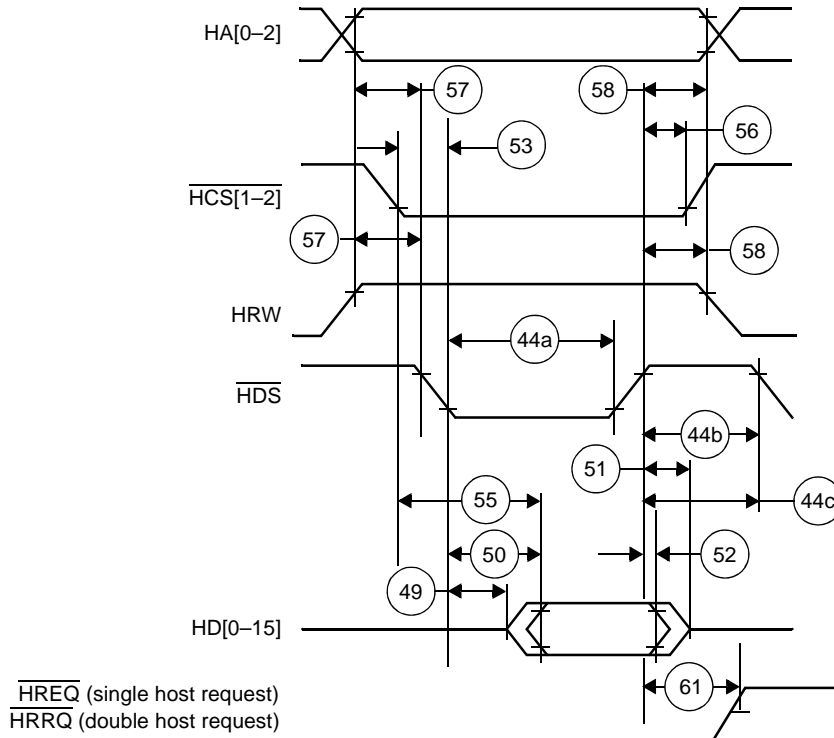


Figure 10. Read Timing Diagram, Single Data Strobe

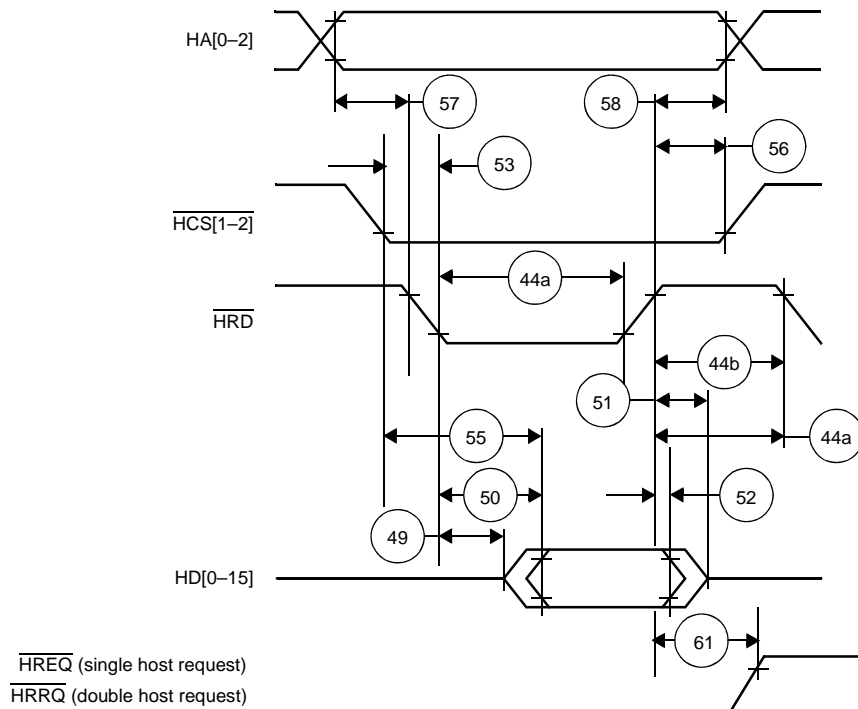


Figure 11. Read Timing Diagram, Double Data Strobe

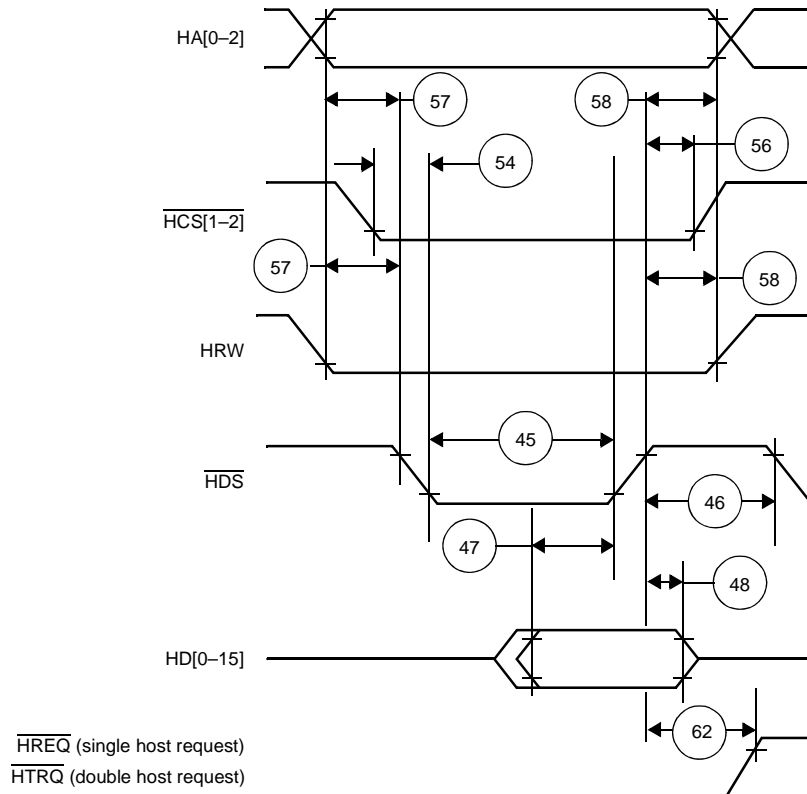


Figure 12. Write Timing Diagram, Single Data Strobe

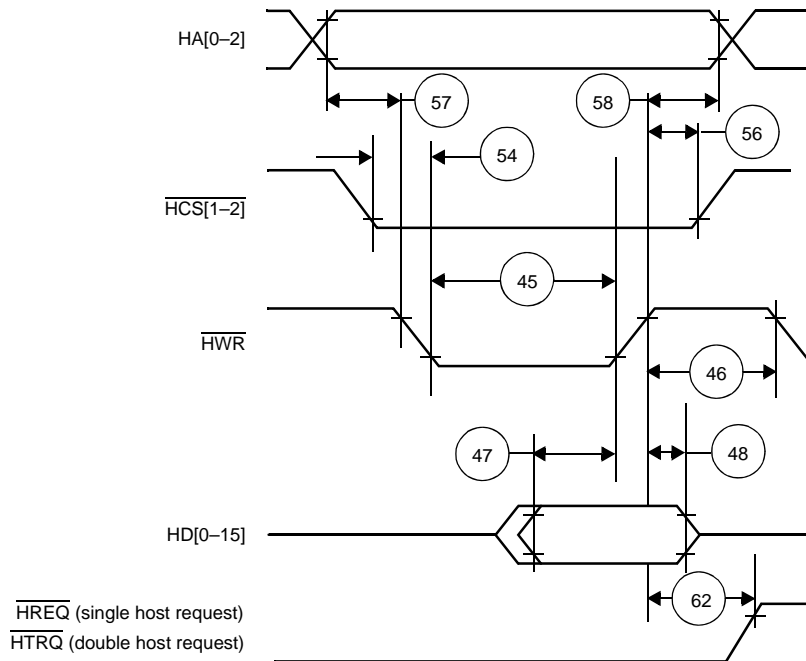


Figure 13. Write Timing Diagram, Double Data Strobe

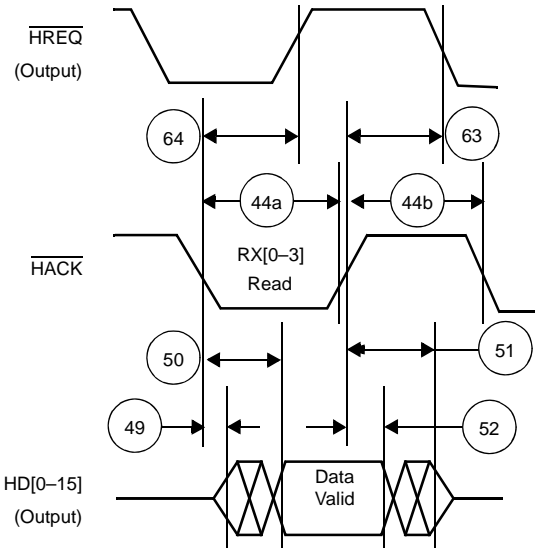


Figure 14. Host DMA Read Timing Diagram, HPCR[OAD] = 0

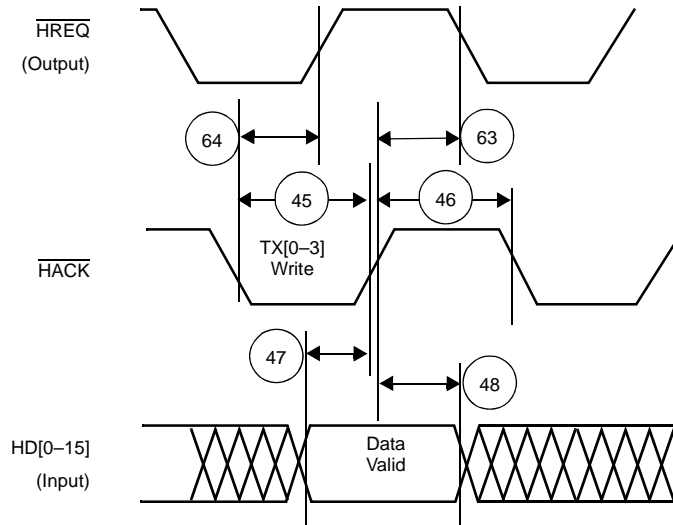


Figure 15. Host DMA Write Timing Diagram, HPCR[OAD] = 0

2.5.7 I²C Timing

Table 22. I²C Timing

| No. | Characteristic | Fast | | Unit |
|-----|--|-------------------------------------|-----|---------------|
| | | Min | Max | |
| 450 | SCL clock frequency | 0 | 400 | kHz |
| 451 | Hold time START condition | $(\text{SCL clock period}/2) - 0.3$ | — | μs |
| 452 | SCL low period | $(\text{SCL clock period}/2) - 0.3$ | — | μs |
| 453 | SCL high period | $(\text{SCL clock period}/2) - 0.1$ | — | μs |
| 454 | Repeated START set-up time (not shown in figure) | $2 \times 1/F_{\text{BCK}}$ | — | μs |
| 455 | Data hold time | 0 | — | μs |
| 456 | Data set-up time | 250 | — | ns |
| 457 | SDA and SCL rise time | — | 700 | ns |
| 458 | SDA and SCL fall time | — | 300 | ns |
| 459 | Set-up time for STOP | $(\text{SCL clock period}/2) - 0.7$ | — | μs |
| 460 | Bus free time between STOP and START | $(\text{SCL clock period}/2) - 0.3$ | — | μs |

Note: SDA set-up time is referenced to the rising edge of SCL. SDA hold time is referenced to the falling edge of SCL. Load capacitance on SDA and SCL is 400 pF.

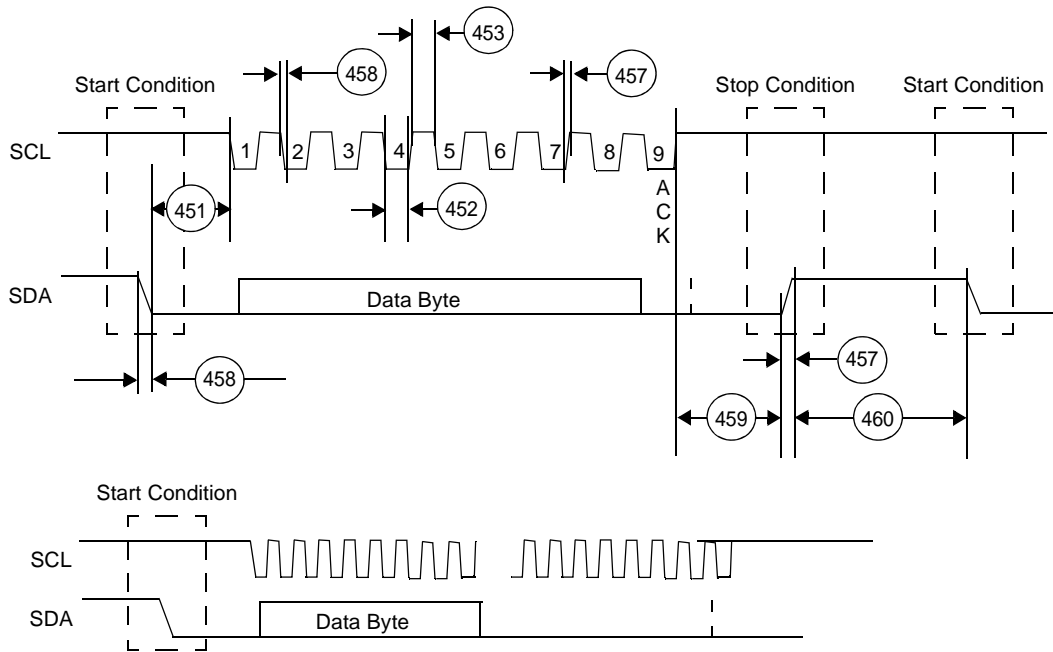


Figure 16. I²C Timing Diagram

2.5.8 UART Timing

Table 23. UART Timing

| No. | Characteristics | Expression | Min | Max | Unit |
|-----|--|------------------------|--------|-----|------|
| — | Internal bus clock (APBCLK) | $F_{CORE}/2$ | — | 150 | MHz |
| — | Internal bus clock period (1/APBCLK) | T_{APBCLK} | 6.67 | — | ns |
| 400 | URXD and UTXD inputs high/low duration | $16 \times T_{APBCLK}$ | 106.67 | — | ns |
| 401 | URXD and UTXD inputs rise/fall time | | — | 5 | ns |
| 402 | UTXD output rise/fall time | | — | 5 | ns |

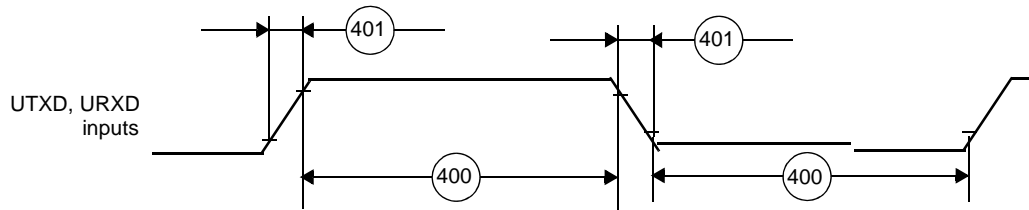


Figure 17. UART Input Timing

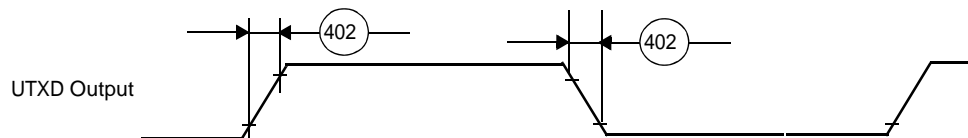


Figure 18. UART Output Timing

2.5.9 EE Timing

Table 24. EE0 Timing

| Number | Characteristics | Type | Min |
|--------|--------------------------|---------------------------|----------------------|
| 65 | EE0 input to the core | Asynchronous | 4 core clock periods |
| 66 | EE0 output from the core | Synchronous to core clock | 1 core clock period |

Notes:

1. The core clock is the SC1400 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Configure the direction of the EE pin in the EE_CTRL register (see the *SC140/SC1400 Core Reference Manual* for details).
3. Refer to **Table 1-11** on page 1-16 for details on EE pin functionality.

Figure 20 shows the signal behavior of the EE pin.

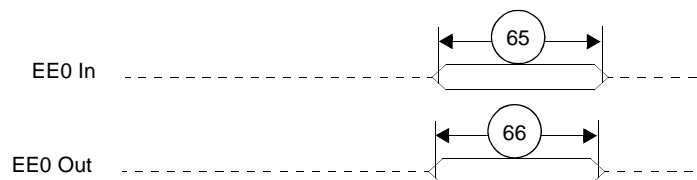


Figure 19. EE Pin Timing

2.5.10 Event Timing

Table 25. EVNT Signal Timing

| Number | Characteristics | Type | Min |
|--------|-----------------|---------------------------|----------------------|
| 67 | EVNT as input | Asynchronous | 1.5 × APBCLK periods |
| 68 | EVNT as output | Synchronous to core clock | 1 APBCLK period |

Notes:

1. Refer to **Table 23** for a definition of the APBCLK period.
2. Direction of the EVNT signal is configured through the GPIO and Event port registers.
3. Refer to the signal chapter in the *MSC711x Reference Manual* for details on EVNT pin functionality.

Figure 20 shows the signal behavior of the EVNT pins.

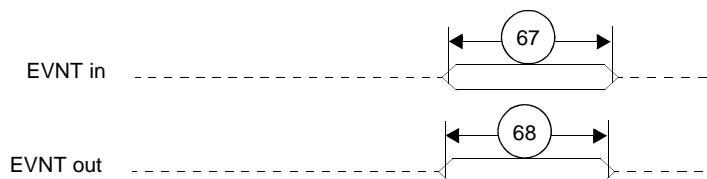


Figure 20. EVNT Pin Timing

2.5.11 GPIO Timing

Table 26. GPIO Signal Timing^{1,2,3}

| Number | Characteristics | Type | Min |
|--------|----------------------------------|---------------------------|---------------------------------|
| 601 | GPI ^{4,5} | Asynchronous | 1.5 × APBCLK periods |
| 602 | GPO ⁵ | Synchronous to core clock | 1 APBCLK period |
| 603 | Port A edge-sensitive interrupt | Asynchronous | 1.5 × APBCLK periods |
| 604 | Port A level-sensitive interrupt | Asynchronous | 3 × APBCLK periods ⁶ |

Notes:

1. Refer to **Table 23** for a definition of the APBCLK period.
2. Direction of the GPIO signal is configured through the GPIO port registers.
3. Refer to **Section 1.5** for details on GPIO pin functionality.
4. GPI data is synchronized to the APBCLK internally and the minimum listed is the capability of the hardware to capture data into a register when the GPADR is read. The specification is not tested due to the asynchronous nature of the input and dependence on the state of the DSP core. It is guaranteed by design.
5. The output signals cannot toggle faster than 75 MHz.
6. Level-sensitive interrupts should be held low until the system determines (via the service routine) that the interrupt is acknowledged.

Figure 21 shows the signal behavior of the GPI/GPO pins.

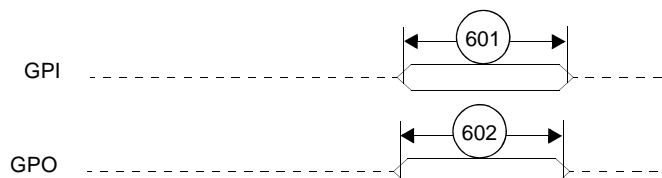


Figure 21. GPI/GPO Pin Timing

2.5.12 JTAG Signals

Table 27. JTAG Timing

| No. | Characteristics | All frequencies | | Unit |
|-----|--|-----------------|------|------|
| | | Min | Max | |
| 700 | TCK frequency of operation ($1/(T_C \times 3)$) Note: $T_C = 1/\text{CLOCK}$ which is the period of the core clock. The TCK frequency must less than 1/3 of the core frequency with an absolute maximum limit of 40 MHz. | 0.0 | 40.0 | MHz |
| 701 | TCK cycle time | 25.0 | — | ns |
| 702 | TCK clock pulse width measured at $V_M = 1.6\text{ V}$ | 11.0 | — | ns |
| 703 | TCK rise and fall times | 0.0 | 3.0 | ns |
| 704 | Boundary scan input data set-up time | 5.0 | — | ns |
| 705 | Boundary scan input data hold time | 14.0 | — | ns |
| 706 | TCK low to output data valid | 0.0 | 20.0 | ns |
| 707 | TCK low to output high impedance | 0.0 | 20.0 | ns |
| 708 | TMS, TDI data set-up time | 5.0 | — | ns |
| 709 | TMS, TDI data hold time | 14.0 | — | ns |
| 710 | TCK low to TDO data valid | 0.0 | 24.0 | ns |
| 711 | TCK low to TDO high impedance | 0.0 | 10.0 | ns |
| 712 | $\overline{\text{TRST}}$ assert time | 100.0 | — | ns |

Note: All timings apply to OCE module data transfers as the OCE module uses the JTAG port as an interface.

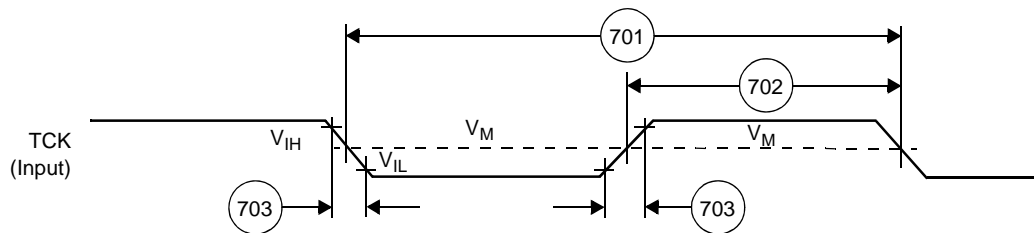


Figure 22. Test Clock Input Timing Diagram

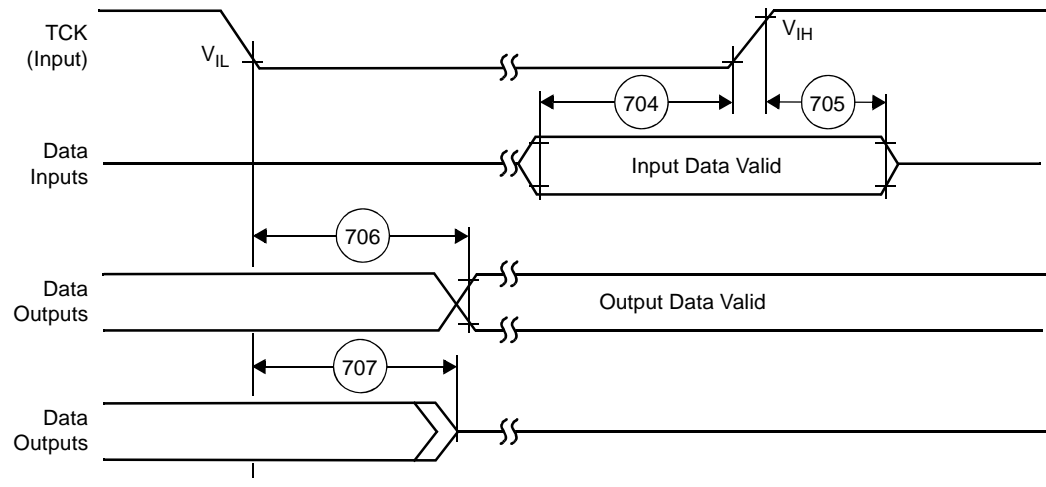


Figure 23. Boundary Scan (JTAG) Timing Diagram

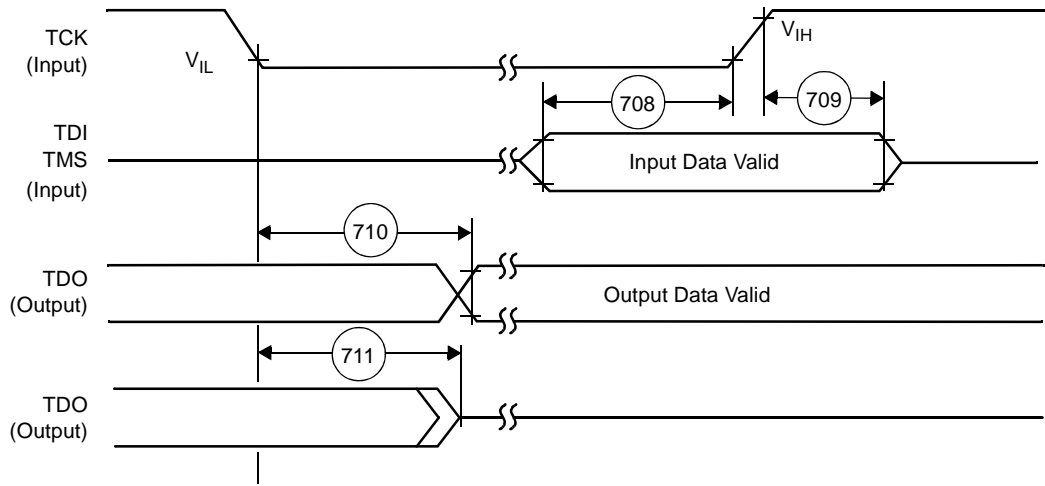


Figure 24. Test Access Port Timing Diagram



Figure 25. TRST Timing Diagram

3 Hardware Design Considerations

This section described various areas to consider when incorporating the MSC7118 device into a system design.

3.1 Thermal Design Considerations

An estimation of the chip-junction temperature, T_J , in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)

$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)

$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC7118 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm² with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip.

You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case. Use the following equation to determine T_J :

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

3.2 Power Supply Design Considerations

This section outlines the MSC7118 power considerations: power supply, power sequencing, power planes, decoupling, power supply filtering, and power consumption. It also presents a recommended power supply design and options for low-power consumption. For information on AC/DC electrical specifications and thermal characteristics, refer to **Section 2**.

3.2.1 Power Supply

The MSC7118 requires four input voltages, as shown in **Table 28**.

Table 28. MSC7118 Voltages

| Voltage | Symbol | Value |
|-----------|------------|--------|
| Core | V_{DDC} | 1.2 V |
| Memory | V_{DDM} | 2.5 V |
| Reference | V_{REF} | 1.25 V |
| I/O | V_{DDIO} | 3.3 V |

You should supply the MSC7118 core voltage via a variable switching supply or regulator to allow for compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied with 1.2 V (+5% and -10%) across V_{DDC} and GND and the I/O section is supplied with 3.3 V ($\pm 10\%$) across V_{DDIO} and GND. The memory and reference voltages supply the DDR memory controller block. The memory voltage is supplied with 2.5 V across V_{DDM} and GND. The reference voltage is supplied across V_{REF} and GND and must be between $0.49 \times V_{DDM}$ and $0.51 \times V_{DDM}$. Refer to the JEDEC standard JESD8 (*Stub Series Terminated Logic for 2.5 Volts (STTL_2)*) for memory voltage supply requirements.

3.2.2 Power Sequencing

One consequence of multiple power supplies is that the voltage rails ramp up at different rates when power is initially applied. The rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. It is extremely important to observe the power up and power down sequences at the board level to avoid latch-up, forward biasing of ESD devices, and excessive currents, which all lead to severe device damage.

Note: There are five possible power-up/power-down sequence cases. The first four cases listed in the following sections are recommended for new designs. The fifth case is not recommended for new designs and must be carefully evaluated for current spike risks based on actual information for the specific application.

3.2.2.1 Case 1

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 26** for relative timing for power sequencing case 1.

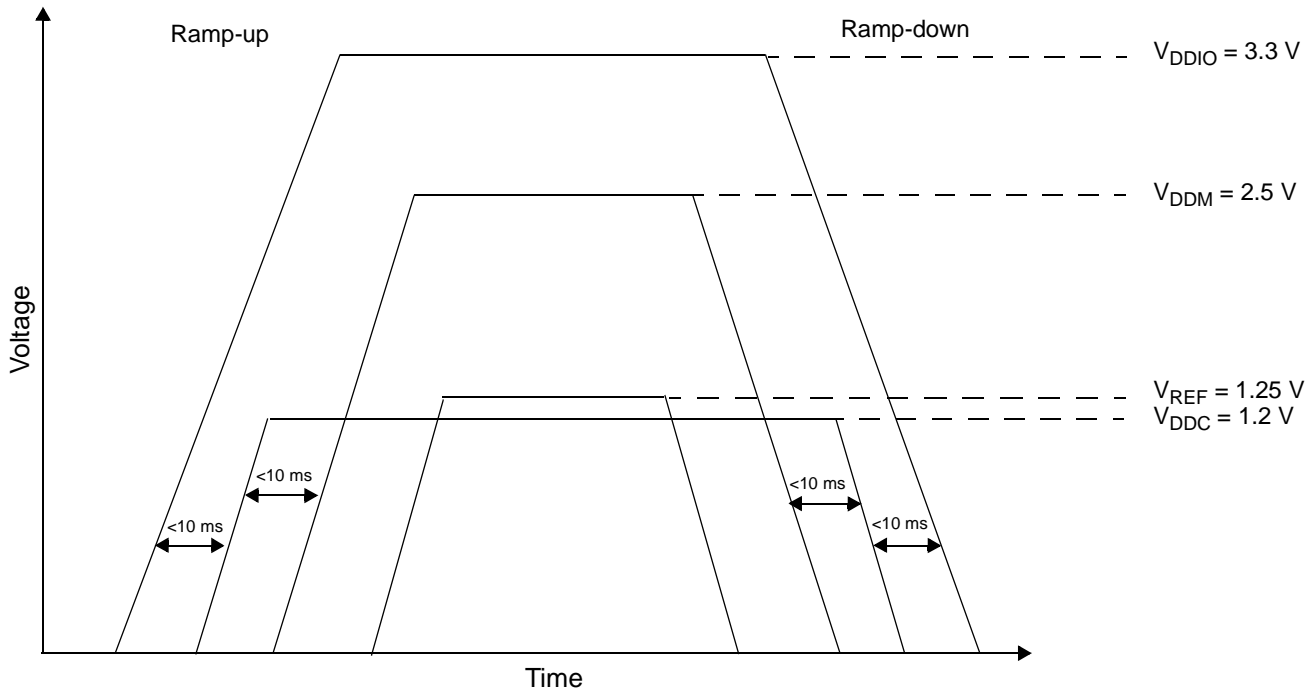


Figure 26. Voltage Sequencing Case 1

3.2.2.2 Case 2

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) and V_{DDM} (2.5 V) supplies simultaneously (second).
3. Turn on the V_{REF} (1.25 V) supply last (third).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC}/V_{DDM} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down for V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 27** for relative timing for Case 2.

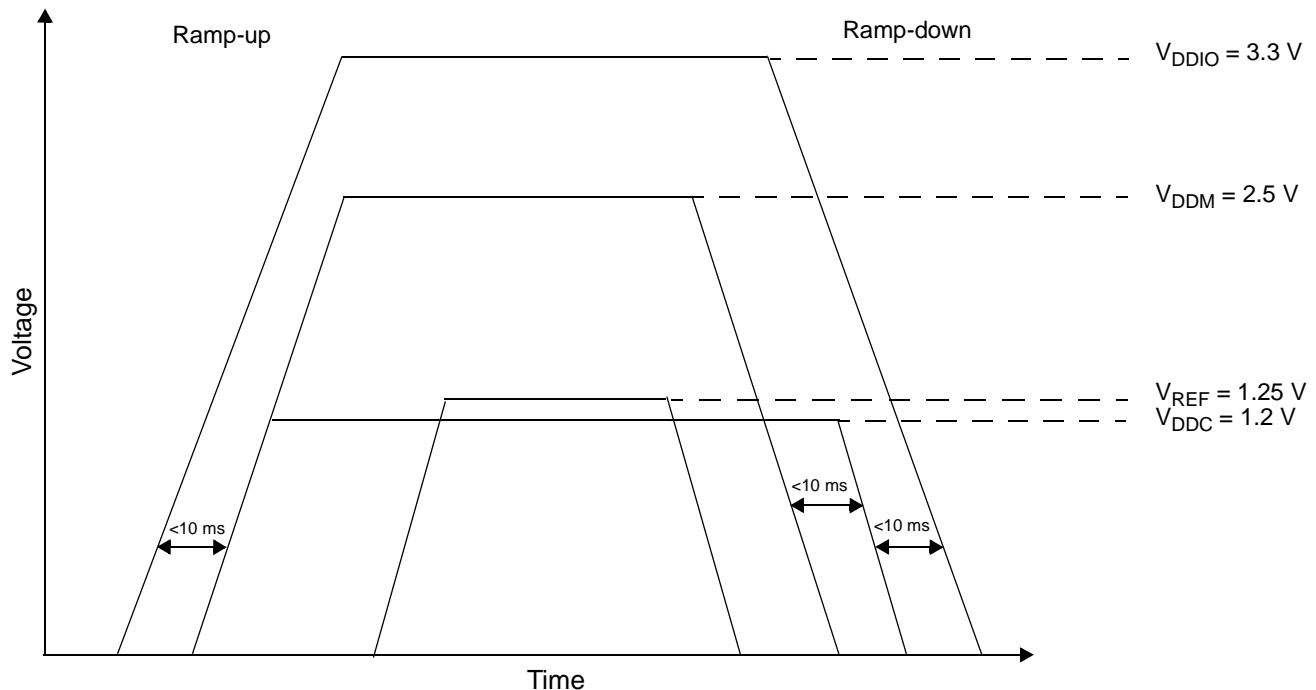


Figure 27. Voltage Sequencing Case 2

3.2.2.3 Case 3

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) and V_{REF} (1.25 V) supplies simultaneously (third).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDM} (2.5 V) and V_{REF} (1.25 V) supplies simultaneously (first).
2. Turn off the V_{DDC} (1.2 V) supply second.
3. Turn of the V_{DDIO} (3.3 V) supply third (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down for V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 28** for relative timing for Case 3.

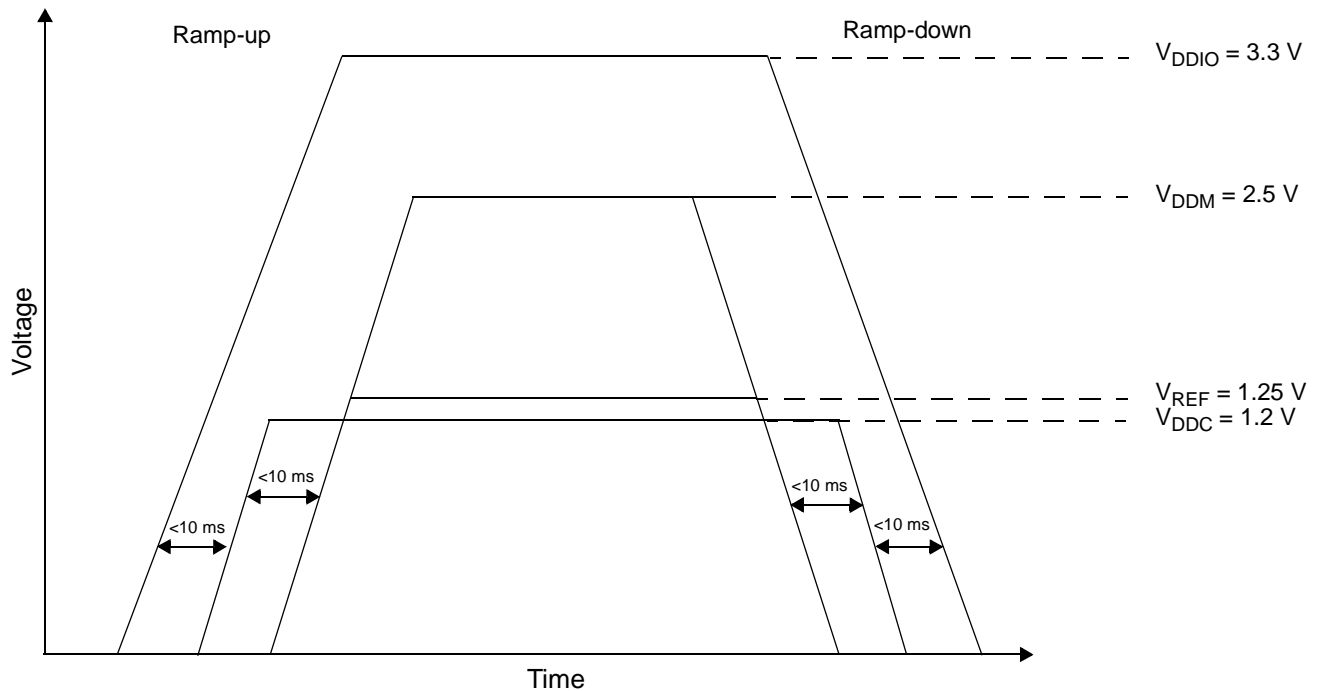


Figure 28. Voltage Sequencing Case 3

3.2.2.4 Case 4

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V), V_{DDM} (2.5 V), and V_{REF} (1.25 V) supplies simultaneously (second).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDC} (1.2 V), V_{REF} (1.25 V), and V_{DDM} (2.5 V) supplies simultaneously (first).
2. Turn of the V_{DDIO} (3.3 V) supply last.

Use the following guidelines:

- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 29** for relative timing for Case 4.

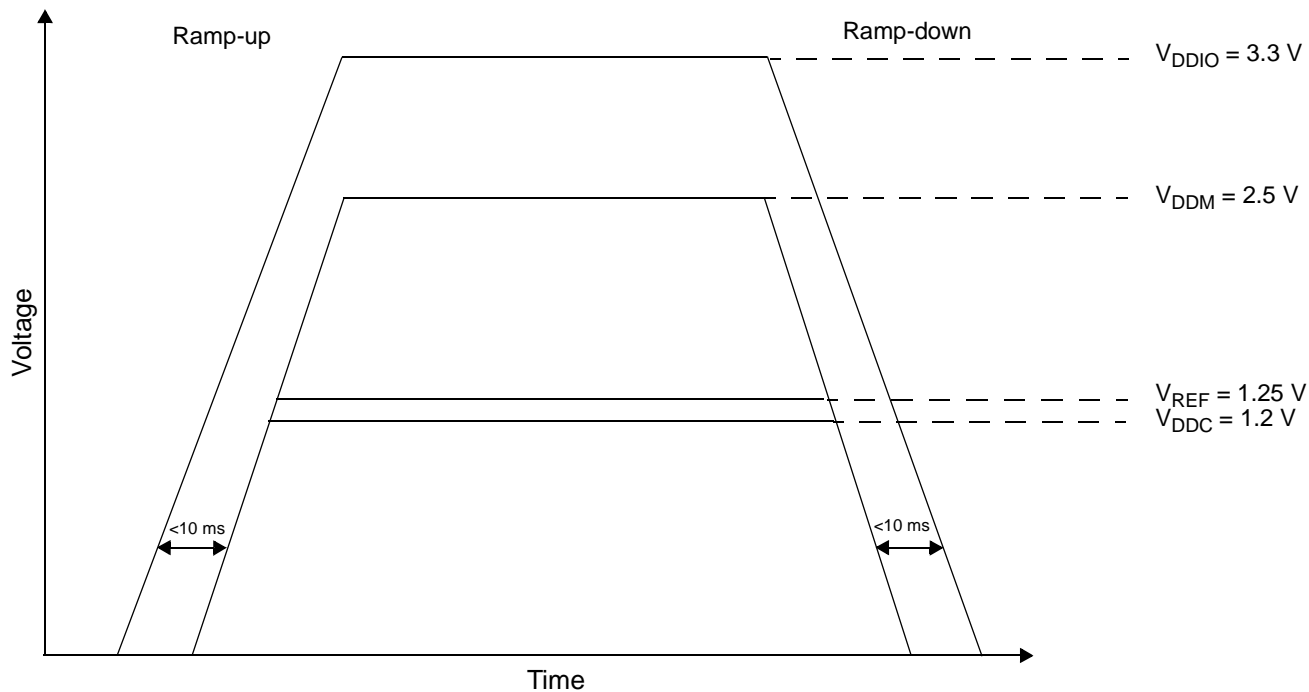


Figure 29. Voltage Sequencing Case 4

3.2.2.5 Case 5 (not recommended for new designs)

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDM} (2.5 V) supply second.
3. Turn on the V_{DDC} (1.2 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDM} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDC} (1.2 V) supply second.
3. Turn off the V_{DDM} (2.5 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDM} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 2 ms for power-up and power-down.
- Refer to **Figure 30** for relative timing for power sequencing case 5.

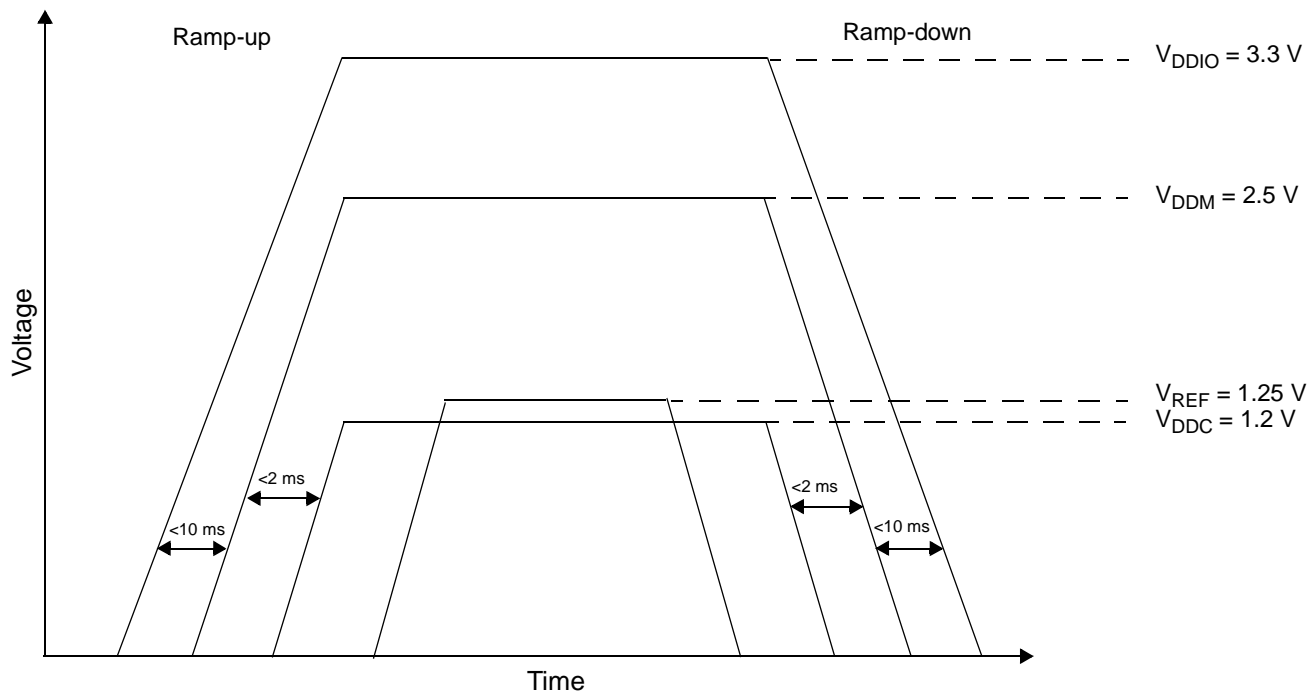


Figure 30. Voltage Sequencing Case 5

Note: Cases 1, 2, 3, and 4 are recommended for system design. Designs that use Case 5 may have large current spikes on the V_{DDM} supply at startup and is not recommended for most designs. If a design uses case 5, it must accommodate the potential current spikes. Verify risks related to current spikes using actual information for the specific application.

3.2.3 Power Planes

Each power supply pin (V_{DDC} , V_{DDM} , and V_{DDIO}) should have a low-impedance path to the board power supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The MSC7118 V_{DDC} power supply pins should be bypassed to ground using decoupling capacitors. The capacitor leads and associated printed circuit traces connecting to device power pins and GND should be kept to less than half an inch per capacitor lead. A minimum four-layer board that employs two inner layers as power and GND planes is recommended. See **Section 3.5** for DDR Controller power guidelines.

3.2.4 Decoupling

Both the I/O voltage and core voltage should be decoupled for switching noise. For I/O decoupling, use standard capacitor values of $0.01 \mu\text{F}$ for every two to three voltage pins. For core voltage decoupling, use two levels of decoupling. The first level should consist of a $0.01 \mu\text{F}$ high frequency capacitor with low effective series resistance (ESR) and effective series inductance (ESL) for every two to three voltage pins. The second decoupling level should consist of two bulk/tantalum decoupling capacitors, one $10 \mu\text{F}$ and one $47 \mu\text{F}$, (with low ESR and ESL) mounted as closely as possible to the MSC7118 voltage pins. Additionally, the maximum drop between the power supply and the DSP device should be 15 mV at 1 A .

3.2.5 PLL Power Supply Filtering

The MSC7118 V_{DDPLL} power signal provides power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to this pin should be filtered with capacitors that have low and high frequency filtering characteristics. V_{DDPLL} can be connected to V_{DDC} through a 2Ω resistor. V_{SSPLL} can be tied directly to the GND plane. A circuit similar to the one shown in **Figure 31** is recommended. The PLL loop filter should be placed as closely as possible to the V_{DDPLL} pin (which are located on the outside edge of the silicon package) to minimize noise coupled from nearby circuits. The $0.01 \mu\text{F}$ capacitor should be closest to V_{DDPLL} , followed by the $0.1 \mu\text{F}$ capacitor, the $10 \mu\text{F}$ capacitor, and finally the $2\text{-}\Omega$ resistor to V_{DDC} . These traces should be kept short.

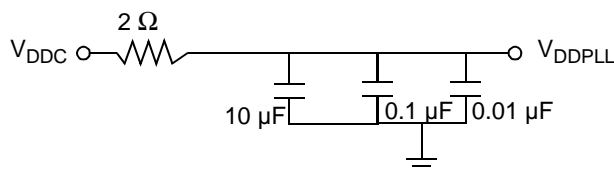


Figure 31. PLL Power Supply Filter Circuits

3.2.6 Power Consumption

You can reduce power consumption in your design by controlling the power consumption of the following regions of the device:

- *Extended core.* Use the SC1400 Stop and Wait modes by issuing a **stop** or **wait** instruction.
- *Clock synthesis module.* Disable the PLL, timer, watchdog, or DDR clocks or disable the CLKO pin.
- *AHB subsystem.* Freeze or shut down the AHB subsystem using the GPSCTL[XBR_HRQ] bit.
- *Peripheral subsystem.* Halt the individual on-device peripherals such as the DDR memory controller, HDI16, TDM, UART, I²C, and timer modules.

For details, see the “Clocks and Power Management” chapter of the *MSC711x Reference Manual*.

3.2.7 Power Supply Design

One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3 V supply can be used. However, a separate adjustable linear regulator supply for the core voltage V_{DDC} should be implemented. For the memory power supply, regulators are available that take care of all DDR power requirements.

Table 29. Recommended Power Supply Ratings

| Supply | Symbol | Nominal Voltage | Current Rating |
|-----------|------------|-----------------|-----------------------|
| Core | V_{DDC} | 1.2 V | 1.5 A per device |
| Memory | V_{DDM} | 2.5 V | 0.5 A per device |
| Reference | V_{REF} | 1.25 V | 10 μ A per device |
| I/O | V_{DDIO} | 3.3 V | 1.0 A per device |

3.3 Estimated Power Usage Calculations

The following equations permit estimated power usage to be calculated for individual design conditions. Overall power is derived by totaling the power used by each of the major subsystems:

$$P_{TOTAL} = P_{CORE} + P_{PERIPHERALS} + P_{DDRIO} + P_{IO} + P_{LEAKAGE} \quad \text{Eqn. 3}$$

This equation combines dynamic and static power. Dynamic power is determined using the generic equation:

$$C \times V^2 \times F \times 10^{-3} \text{ mW} \quad \text{Eqn. 4}$$

where,

C = load capacitance in pF

V = peak-to-peak voltage swing in V

F = frequency in MHz

3.3.1 Core Power

Estimation of core power is straightforward. It uses the generic dynamic power equation and assumes that the core load capacitance is 750 pF, core voltage swing is 1.2 V, and the core frequency is 300 MHz. This yields:

$$P_{CORE} = 750 \text{ pF} \times (1.2 \text{ V})^2 \times 300 \text{ MHz} \times 10^{-3} = 324.0 \text{ mW} \quad \text{Eqn. 5}$$

This equation allows for adjustments to voltage and frequency if necessary.

3.3.2 Peripheral Power

Peripherals include the DDR memory controller, DMA controller, HDI16, TDM, UART, timers, GPIOs, and the I²C module. Basic power consumption by each module is assumed to be the same and is computed by using the following equation which assumes an effective load of 20 pF, core voltage swing of 1.2 V, and a switching frequency of 100 MHz. This yields:

$$P_{PERIPHERAL} = 20 \text{ pF} \times (1.2 \text{ V})^2 \times 150 \text{ MHz} \times 10^{-3} = 4.32 \text{ mW per peripheral} \quad \text{Eqn. 6}$$

Multiply this value by the number of peripherals used in the application to compute the total peripheral power consumption.

3.3.3 External Memory Power

Estimation of power consumption by the DDR memory system is complex. It varies based on overall system signal line usage, termination and load levels, and switching rates. Because the DDR memory includes terminations external to the MSC7118 device, the 2.5 V power source provides the power for the termination, which is a static value of 16 mA per signal driven high. The dynamic power is computed, however, using a differential voltage swing of ±0.200 V, yielding a peak-to-peak swing of 0.4 V. The equations for computing the DDR power are:

$$P_{DDRIO} = P_{STATIC} + P_{DYNAMIC} \quad \text{Eqn. 7}$$

$$P_{STATIC} = (\text{unused pins} \times \% \text{ driven high}) \times 16 \text{ mA} \times 2.5 \text{ V} \quad \text{Eqn. 8}$$

$$P_{DYNAMIC} = (\text{pin activity value}) \times 20 \text{ pF} \times (0.4 \text{ V})^2 \times 300 \text{ MHz} \times 10^{-3} \text{ mW} \quad \text{Eqn. 9}$$

$$\text{pin activity value} = (\text{active data lines} \times \% \text{ activity} \times \% \text{ data switching}) + (\text{active address lines} \times \% \text{ activity}) \quad \text{Eqn. 10}$$

As an example, assume the following:

- unused pins = 16 (DDR uses 16-pin mode)
- % driven high = 50%
- active data lines = 16
- % activity = 60%
- % data switching = 50%
- active address lines = 3

In this example, the DDR memory power consumption is:

$$P_{DDRIO} = ((16 \times 0.5) \times 16 \times 2.5) + (((16 \times 0.6 \times 0.5) + (3 \times 0.6)) \times 20 \times (0.4)^2 \times 300 \times 10^{-3}) = 326.3 \text{ mW} \quad \text{Eqn. 11}$$

3.3.4 External I/O Power

The estimation of the I/O power is similar to the computation of the peripheral power estimates. The power consumption per signal line is computed assuming a maximum load of 20 pF, a voltage swing of 3.3 V, and a switching frequency of 25 MHz, which yields:

$$P_{IO} = 20 \text{ pF} \times (3.3 \text{ V})^2 \times 25 \text{ MHz} \times 10^{-3} = 5.44 \text{ mW per I/O line} \quad \text{Eqn. 12}$$

Multiply this number by the number of I/O signal lines used in the application design to compute the total I/O power.

Note: The signal loading depends on the board routing. For systems using a single DDR device, the load could be as low as 7 pF.

3.3.5 Leakage Power

The leakage power is for all power supplies combined at a specific temperature. The value is temperature dependent. The observed leakage value at room temperature is 64 mW.

3.3.6 Example Total Power Consumption

Using the examples in this section and assuming four peripherals and 10 I/O lines active, a total power consumption value is estimated as the following:

$$P_{TOTAL} = 324.0 + (4 \times 4.32) + 326.3 + (10 \times 5.44) + 64 = 784.98 \text{ mW} \quad \text{Eqn. 13}$$

3.4 Reset and Boot

This section describes the recommendations for configuring the MSC7118 at reset and boot.

3.4.1 Reset Circuit

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC7118 output current, the pull-up value should not be too small (a 1 K Ω pull-up resistor is used in the MSC711xADS reference design).

3.4.2 Reset Configuration Pins

Table 30 shows the MSC7118 reset configuration signals. These signals are sampled at the deassertion (rising edge) of $\overline{\text{PORESET}}$. For details, refer to the Reset chapter of the *MSC711x Reference Manual*.

Table 30. Reset Configuration Signals

| Signal | Description | Settings |
|---------|------------------------------------|---|
| BM[3–0] | Determines boot mode. | See Table 31 for details. |
| SWTE | Determines watchdog functionality. | 0 Watchdog timer disabled. 1 Watchdog timer enabled. |
| HDSP | Configures HDI16 strobe polarity. | 0 Host Data strobes active low. 1 Host Data strobes active high. |
| H8BIT | Configures HDI16 operation mode. | 0 HDI16 port configured for 16-bit operation. 1 HDI16 port configured for 8-bit operation. |

Table 31. Boot Mode Source Selection

| BM[3–0] | Boot Port | Input Clock Frequency | Clock Divide | PLL | CKSEL | RNG Bit | Core Clock Frequency | Comments |
|--|---|-----------------------|--------------|-----|-------|---------|----------------------|---|
| HDI Boot Modes | | | | | | | | |
| 0000 | HDI16 | < F _{max} | N/A | N/A | 00 | 0 | < F _{max} | Not clocked by the PLL. Can boot as 8- or 16-bit HDI. |
| 0101 | HDI16 | 22.2-25 MHz | 1 | 12 | 11 | 1 | 266–300 MHz | Can boot as 8- or 16-bit HDI. |
| 0010 | HDI16 | 25-33.3 MHz | 2 | 32 | 01 | 1 | 200–266 MHz | |
| 0111 | HDI16 | 33-66 MHz | 3 | 12 | 11 | 1 | 132–264 MHz | |
| 0100 | HDI16 | 44.3-50 MHz | 2 | 12 | 11 | 1 | 266–300 MHz | |
| SPI Boot Modes - Using HA3, HCS2, BM3, BM2 Pins | | | | | | | | |
| 1000 | SPI (SW) | < F _{max} | N/A | N/A | 00 | 0 | < F _{max} | The boot program automatically determines whether EEPROM or Flash memory. |
| 1001 | SPI (SW) | 15.6-25 MHz | 1 | 17 | 11 | 0 | 133–212.5 MHz | |
| 1010 | SPI (SW) | 33-50 MHz | 2 | 16 | 11 | 0 | 132–200 MHz | |
| 1011 | SPI (SW) | 44.3-75 MHz | 3 | 18 | 11 | 0 | 133–225 MHz | |
| SPI Boot Modes - Using URXD, UTXD, SCL, SDA Pins | | | | | | | | |
| 1100 | SPI (SW) | < F _{max} | N/A | N/A | 00 | 0 | < F _{max} | Boots through different set of pins. |
| I ² C Boot Modes | | | | | | | | |
| 0001 | I ² C | < 100 MHz | N/A | N/A | 00 | 0 | < 100 MHz | Not clocked by the PLL. I ² C is limited to a maximum bit rate of 400 Kbps. With a clock divider of 128, this limits the maximum input clock frequency to 100 MHz. |
| Reserved | | | | | | | | |
| 0011 | Reserved | — | — | — | — | — | — | — |
| 0110 | Reserved | — | — | — | — | — | — | — |
| 1101 | Reserved | — | — | — | — | — | — | — |
| 1110 | Reserved | — | — | — | — | — | — | — |
| 1111 | Reserved | — | — | — | — | — | — | — |
| Notes: | <ol style="list-style-type: none"> 1. The clock divider determines the value used in the clock module CLKCTRL[PLLDVDF] field. 2. The clock multiplier determines the value used in the clock module CLKCTRL[PLLMLTF] field. 3. F_{max} is determined by the maximum frequency of the peripheral and of the SC1400 core as specified in the data sheet. | | | | | | | |

3.4.3 Boot

After a power-on reset, the PLL is bypassed and the device is directly clocked from the CLKIN pin. Thus, the device operates slowly during the boot process. After the boot program is loaded, it can enable the PLL and start the device operating at a higher speed. The MSC7118 can boot from an external host through the HDI16 or download a user program through the I²C port. The boot operating mode is set by configuring the BM[0–3] signals sampled at the rising edge of PORESET, as shown in **Table 31**. See the *MSC711x Reference Manual* for details of boot program operation.

3.4.3.1 HDI16 Boot

If the MSC7118 device boots from an external host through the HDI16, the port is configured as follows:

- Operate in Non-DMA mode.
- Operate in polled mode on the device side.
- Operate in polled mode on the external host side.
- External host must write four 16-bit values at a time with the first word as the most significant and the fourth word as the least significant.

When booting from a power-on reset, the HDI16 is additionally configurable as follows:

- 8- or 16-bit mode as specified by the H8BIT pin.
- Data strobe as specified by the HDSP and HDDS pins.

These pins are sampled only on the deassertion of power-on reset. During a boot from a hard reset, the configuration of these pins is unaffected.

Note: When the HDI16 is used for booting or other purposes, bit 0 is the least significant bit and not the most significant bit as for other DSP products.

3.4.3.2 I²C Boot

When the MSC7118 device is configured to boot from the I²C port, the boot program configures the GPIO pins for I²C operation. Then the MSC7118 device initiates accesses to the I²C module, downloading data to the MSC7118 device. The I²C interface is configured as follows:

- PLL is disabled and bypassed so that the I²C module is clocked with the IPBus clock.
- I²C interface operates in master mode and polling is used.
- EPROM operates in slave mode.
- Clock divider is set to 128.
- Address of slave during boot is 0xA0.

The IPBus clock is internally divided to generate the bit clock, as follows:

- CLKIN must be a maximum of 100 MHz
- PLL is bypassed.
- IPBus clock = CLKIN/2 is a maximum of 50 MHz.
- I²C bit clock must be less than or equal to:
 - IPBus clock/I²C clock divider
 - 50 MHz (max)/128
 - 390.6 KHz

This satisfies the maximum clock rate requirement of 400 kbps for the I²C interface. For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

3.4.3.3 SPI Boot

When the MSC7118 device is configured to boot from the SPI port, the boot program configures the GPIO pins for SPI operation. Then the MSC7118 device initiates accesses to the SPI module, downloading data to the MSC7118 device. When the SPI routines run in the boot ROM, the MSC7118 is always configured as the SPI master. Booting through the SPI is supported for serial EEPROM devices and serial Flash devices. When a READ_ID instruction is issued to the serial memory device and the device returns a value of 0x00 or 0xFF, the routines for accessing a serial EEPROM are used, at a maximum frequency of 4 Mbps. Otherwise, the routines for accessing a serial Flash are used, and they can run at faster speeds. Booting is performed through one of two sets of pins:

- Main set: BM[2–3], HA3, and HCS2, which allow use of the PLL.
- Alternate set: UTXD, URXD, SDA, and SCL, which cannot be used with the PLL.

In either configuration, an error during SPI boot is flagged on the EVNT3 pin. For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

3.5 DDR Memory System Guidelines

MSC7118 devices contain a memory controller that provides a glueless interface to external double data rate (DDR) SDRAM memory modules with Class 2 Series Stub Termination Logic 2.5 V (SSTL_2). There are two termination techniques, as shown in Figure 32. Technique B is the most popular termination technique.

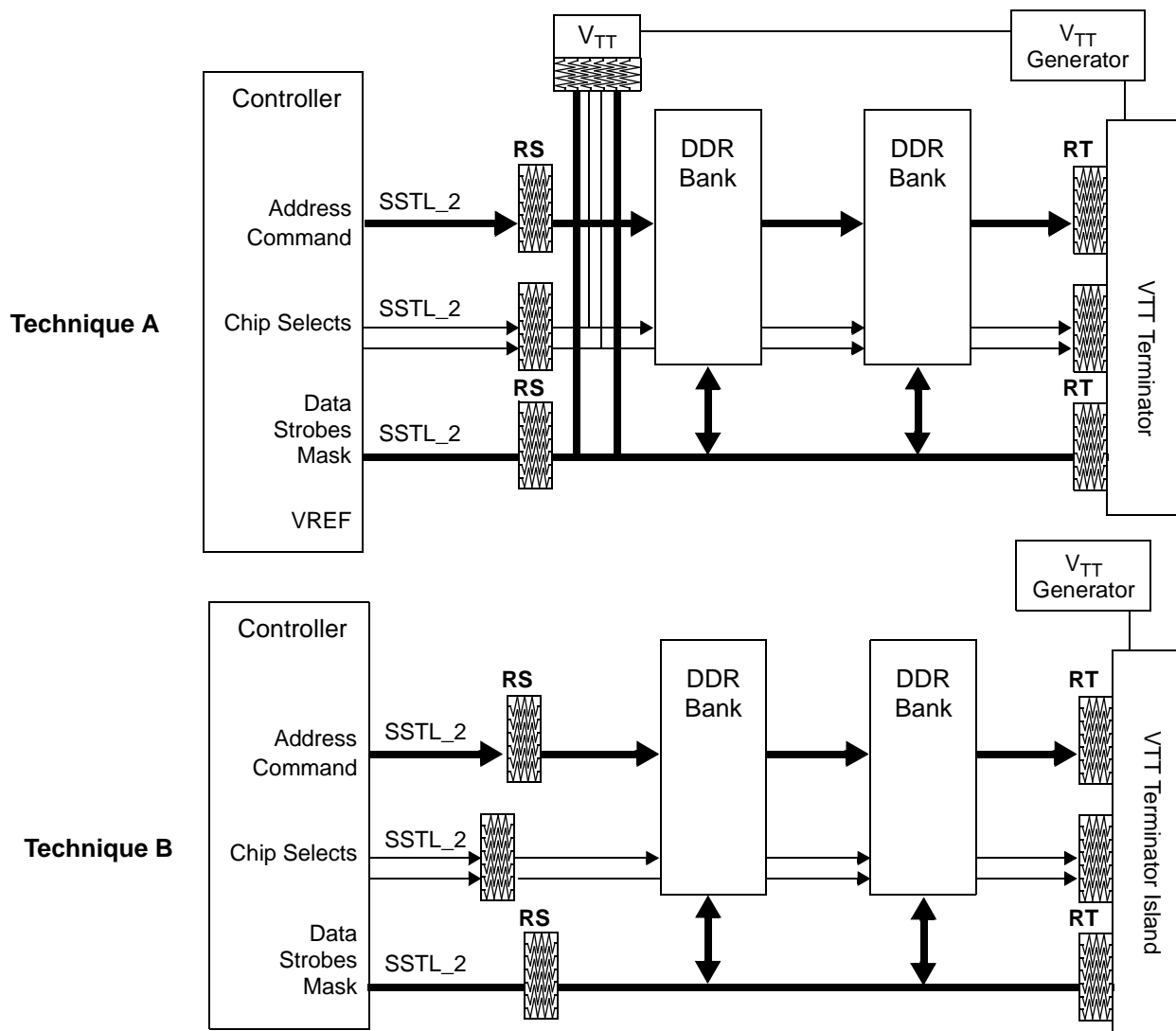


Figure 32. SSTL Termination Techniques

Figure 33 illustrates the power wattage for the resistors. Typical values for the resistors are as follows:

- RS = 22 Ω
- RT = 24 Ω

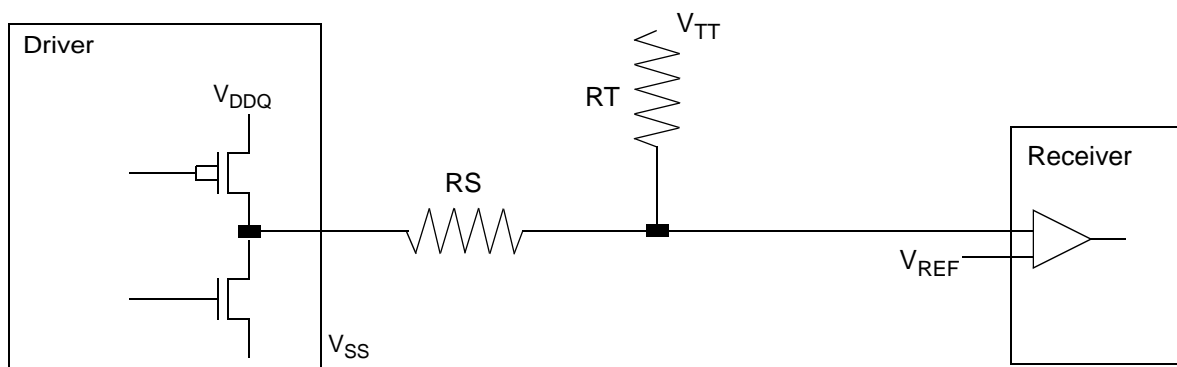


Figure 33. SSTL Power Value

3.5.1 V_{REF} and V_{TT} Design Constraints

V_{TT} and V_{REF} are isolated power supplies at the same voltage, with V_{TT} as a high current power source. This section outlines the voltage supply design needs and goals:

- Minimize the noise on both rails.
- V_{TT} must track variation in the V_{REF} DC offsets. Although they are isolated supplies, one possible solution is to use a single IC to generate both signals.
- Both references should have minimal drift over temperature and source supply.
- It is important to minimize the noise from coupling onto V_{REF} as follows:
 - Isolate V_{REF} and shield it with a ground trace.
 - Use 15–20 mm track.
 - Use 20–30 mm clearance between other traces for isolating.
 - Use the outer layer route when possible.
 - Use distributed decoupling to localize transient currents and return path and decouple with an inductance less than 3 nH.
- Max source/sink transient currents of up to 1.8 A for a 32-bit data bus.
- Use a wide island trace on the outer layer:
 - Place the island at the end of the bus.
 - Decouple both ends of the bus.
 - Use distributed decoupling across the island.
 - Place SSTL termination resistors inside the V_{TT} island and ensure a good, solid connection.
- Place the V_{TT} regulator as closely as possible to the termination island.
 - Reduce inductance and return path.
 - Tie current sense pin at the midpoint of the island.

3.5.2 Decoupling

The DDR decoupling considerations are as follows:

- DDR memory requires significantly more burst current than previous SDRAMs.
- In the worst case, up to 64 drivers may be switching states.
- Pay special attention and decouple discrete ICs per manufacturer guidelines.
- Leverage V_{TT} island topology to minimize the number of capacitors required to supply the burst current needs of the termination rail.
- See the Micron DesignLine publication entitled *Decoupling Capacitor Calculation for a DDR Memory Channel* (<http://download.micron.com/pdf/pubs/designline/3Q00d11-4.pdf>).

3.5.3 General Routing

The general routing considerations for the DDR are as follows:

- All DDR signals must be routed next to a solid reference:
 - For data, next to solid ground planes.
 - For address/command, power planes if necessary.
- All DDR signals must be impedance controlled. This is system dependent, but typical values are 50–60 ohm.
- Minimize other cross-talk opportunities. As possible, maintain at least a four times the trace width spacing between all DDR signals to non-DDR signals.
- Keep the number of vias to a minimum to eliminate additional stubs and capacitance.
- Signal group routing priorities are as follows:
 - DDR clocks.
 - Route MVTT/MVREF.
 - Data group.
 - Command/address.
- Minimize data bit jitter by trace matching.

3.5.4 Routing Clock Distribution

The DDR clock distribution considerations are as follows:

- DDR controller supports six clock pairs:
 - 2 DIMM modules.
 - Up to 36 discrete chips.
- For route traces as for any other differential signals:
 - Maintain proper difference pair spacing.
 - Match pair traces within 25 mm.
- Match all clock traces to within 100 mm.
- Keep all clocks equally loaded in the system.
- Route clocks on inner critical layers.

3.5.5 Data Routing

The DDR data routing considerations are as follows:

- Route each data group (8-bits data + DQS + DM) on the same layer. Avoid switching layers within a byte group.
- Take care to match trace lengths, which is extremely important.
- To make trace matching easier, let adjacent groups be routed on alternate critical layers.
- Pin swap bits within a byte group to facilitate routing (discrete case).
- Tight trace matching is recommended within the DDR data group. Keep each 8-bit datum and its DM signal within ± 25 mm of its respective strobe.
- Minimize lengths across the entire DDR channel:
 - Between all groups maintain a delta of no more than 500 mm.
 - Allows greater flexibility in the design for readjustments as needed.
- DDR data group separation:
 - If stack-up allows, keep DDR data groups away from the address and control nets.
 - Route address and control on separate critical layers.
 - If resistor networks (RNs) are used, attempt to keep data and command lines in separate packages.

3.6 Connectivity Guidelines

This section summarizes the connections and special conditions, such as pull-up or pull-down resistors, for the MSC7118 device. Following are guidelines for signal groups and configuration settings:

- *Clock and reset signals.*
 - SWTE is used to configure the MSC7118 device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{DDC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$, this signal can be left floating.
 - BM[0–1] configure the MSC7118 device and are sampled until $\overline{\text{PORESET}}$ is deasserted, so they should be tied to V_{DDIO} or GND either directly or through pull-up or pull-down resistors.
 - $\overline{\text{HRESET}}$ should be pulled up.
- *Interrupt signals.* When used, $\overline{\text{IRQ}}$ pins must be pulled up.
- *HDI16 signals.*
 - When they are configured for open-drain, the $\overline{\text{HREQ/HREQ}}$ or $\overline{\text{HTRQ/HTRQ}}$ signals require a pull-up resistor. However, these pins are also sampled at power-on reset to determine the HDI16 boot mode and may need to be pulled down. When these pins must be pulled down on reset and pulled up otherwise, a buffer can be used with the $\overline{\text{HRESET}}$ signal as the enable.
 - When the device boots through the HDI16, the HDDS, HDSP and H8BIT pins should be pulled up or down, depending on the required boot mode settings.
- *I²C signals.* The SCL and SDA signals, when programmed for I²C, requires an external pull-up resistor.
- *General-purpose I/O (GPIO) signals.* An unused GPIO pin can be disconnected. After boot, program it as an output pin.
- *Other signals.*
 - The $\overline{\text{TEST0}}$ pin must be connected to ground.
 - The $\overline{\text{TPSEL}}$ pin should be pulled up to enable debug access via the EOnCE port and pulled down for boundary scan.
 - Pins labelled NO CONNECT (NC) must not be connected.
 - When a 16-pin double data rate (DDR) interface is used, the 16 unused data pins should be no connects (floating) if the used lines are terminated.
 - Do not connect DBREQ to DONE (as you would for the MSC8101 device). Connect DONE to one of the EVNT pins, and DBREQ to HRRQ.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

| Part | Supply Voltage | Package Type | Pin Count | Core Frequency (MHz) | Solder Spheres | Order Number |
|---------|---|--|-----------|----------------------|----------------|---------------|
| MSC7118 | 1.2 V core 2.5 V memory 3.3 V I/O | Molded Array Process-Ball Grid Array (MAP-BGA) | 400 | 300 | Lead-free | MSC7118VM1200 |
| | | | | | Lead-bearing | MSC7118VF1200 |

5 Package Information

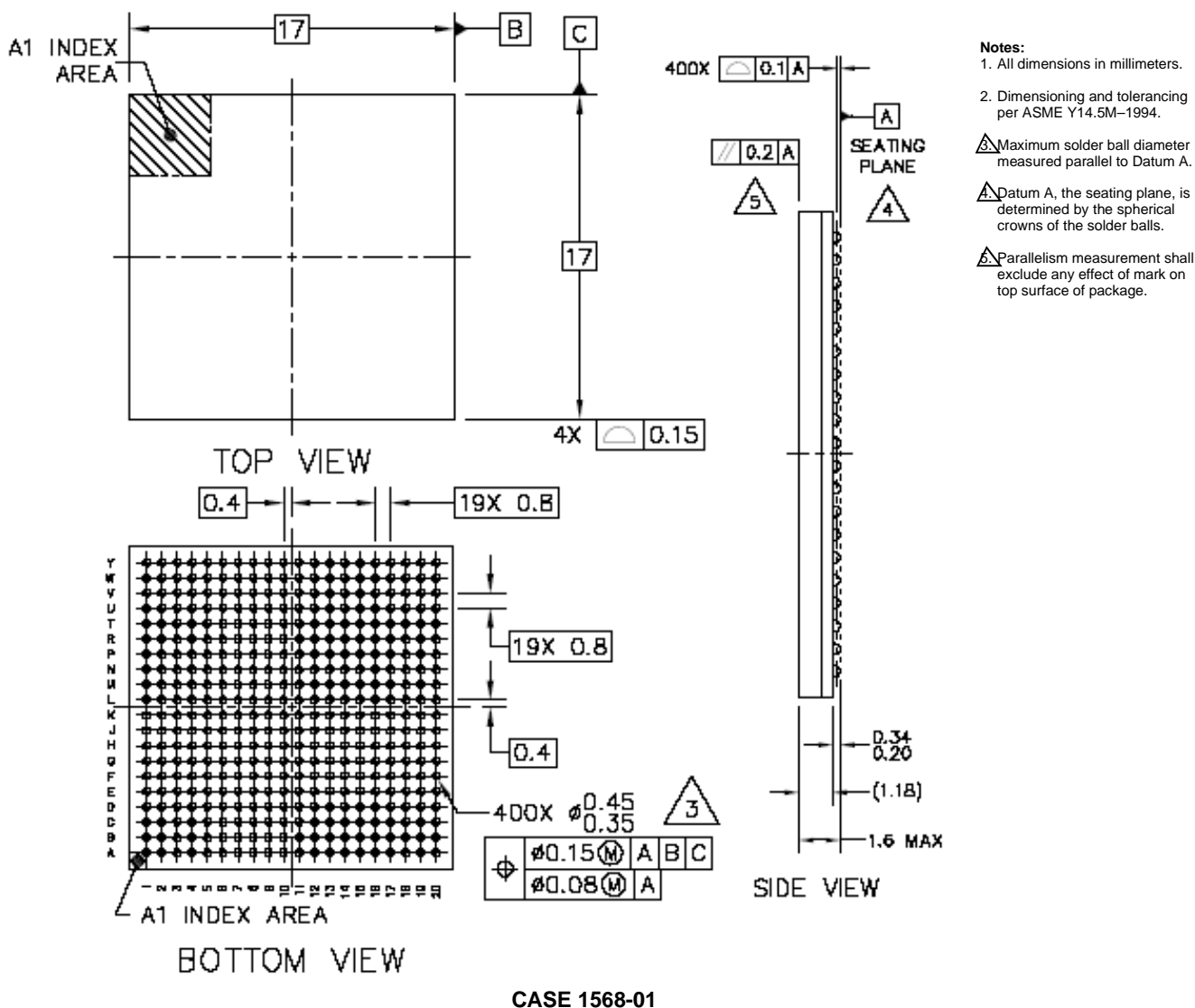


Figure 34. MSC7118 Mechanical Information, 400-pin MAP-BGA Package

6 Product Documentation

- *MSC711x Reference Manual* (MSC711xRM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC7118 device.
- *SC140/SC1400 DSP Core Reference Manual*. Covers the SC140 and SC1400 core architecture, control registers, clock registers, program control, and instruction set.

7 Revision History

Table 32 provides a revision history for this data sheet.

Table 32. Document Revision History

| Revision | Date | Description |
|----------|-----------|---|
| 0 | Sep. 2005 | <ul style="list-style-type: none"> Initial public release. |
| 1 | Oct 2005 | <ul style="list-style-type: none"> Added explanatory note to HDI16 timing table. |
| 2 | Oct. 2005 | <ul style="list-style-type: none"> Added information about signals GPIOB11, GPIOC11, GPIOD7, and GPIOD8 to the signal descriptions and pinout location lists. |
| 3 | Dec. 2005 | <ul style="list-style-type: none"> Added information about signals GPIOA16, GPIOA17, GPIOA27, GPIOA28, and GPIOA29 to signal description and pinout location lists. |
| 4 | Nov. 2006 | <ul style="list-style-type: none"> Updated Reference Manual reference to MSC711x Reference Manual. Updated arrows in Host DMA Writing Timing figure. |
| 5 | Jul. 2007 | <ul style="list-style-type: none"> Updated to new data sheet format. Reorganized and renumbered sections, figures, and tables. Added a note to clarify the definition of TCK timing 700 in new Table 31. Removed references to V_{CCSYN} and V_{CCSYN1} in the new power supply design recommendation Section 3.2. |
| 6 | Aug 2007 | <ul style="list-style-type: none"> The power-up and power-down sequences described in Section 3.2 starting on page 42 have been expanded to five possible design scenarios/cases. These cases replace the previously recommended power-up/power-down sequence recommendations. Section 3.2 has been clarified by adding subsection headings. |
| 7 | Apr 2008 | <ul style="list-style-type: none"> Change the PLL filter resistor from 20 Ω to 2 Ω in Section 3.2.5. |



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