DRF13XX Evaluation Board

Gui Choi
Sr. Application Engineer
Phone: 541-382-8028, ext. 1205
gchoi@microsemi.com

Figure 1 shows a simplified circuit diagram for the DRF13XX series of devices. The Hybrid consists of two MOSFET Drivers and two Power MOSFETs in a Push-Pull configuration. For U1, the control signal is applied to internal driver through pin 4 (IN) and referenced to pin 5 (GND) a Ground return. The pin 3 (FN) allows the user to select either Inverting or Non-inverting mode. The output of the driver is internally applied to the gate of the Power MOSFET. U2 is controlled in the same method. For more information on the specific DRF13XX, refer to the device data sheet.

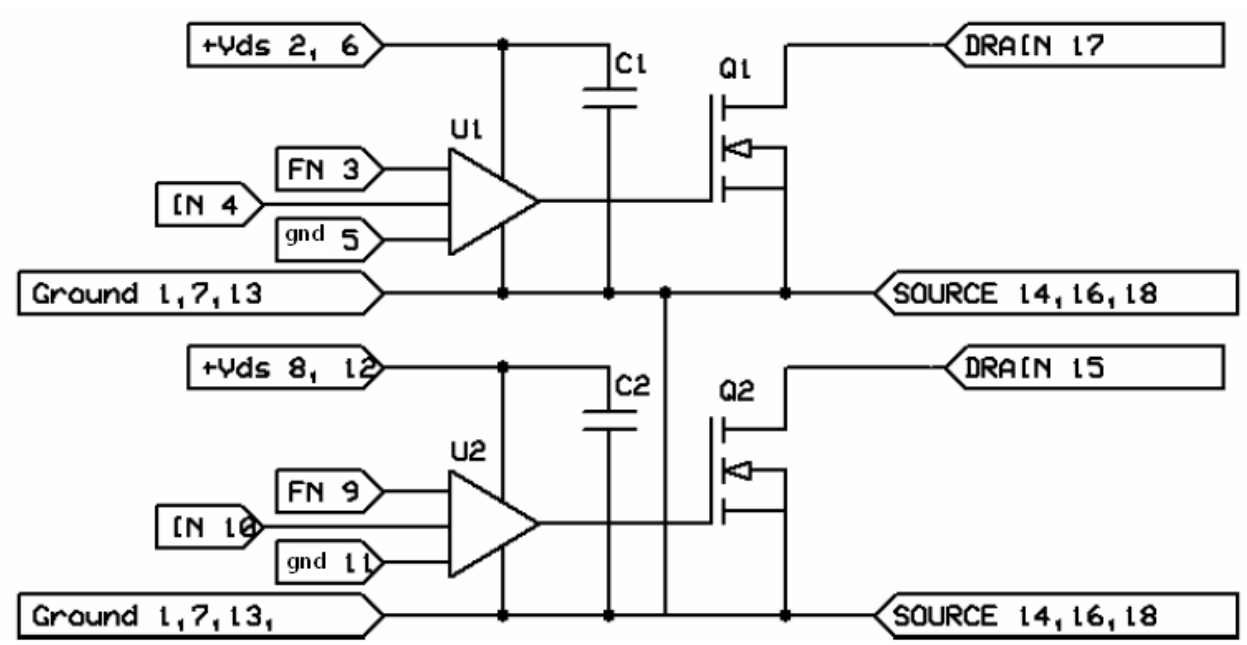

Figure 1. DRF13XX

The control logic for the DRF1300 is shown in Table 1. Each section is independent in function and control.

FN (pin 3,9) Invert/Non-invert	IN (pin 4,10) Control	MOSFET
High	High	On
High	Low	Off
Low	High	Off
Low	Low	On

Table 1

The DRF13XX Evaluation Board is a generic PCB which will allow the design engineer to prototype a circuit of their choice. It is initially configured as shown in Figure 2 allowing the user to evaluate the switching performance of a DRF13XX. The 50Ω load resistors (RL1or RL2) have a power limit of 4 watts. In this configuration, the DRF13XX evaluation board should only be operated at a reduced duty cycle to avoid damaging the output resistor. The DRF13XX must also be attached to a heat sink when configured for dissipation greater than 4 watts.

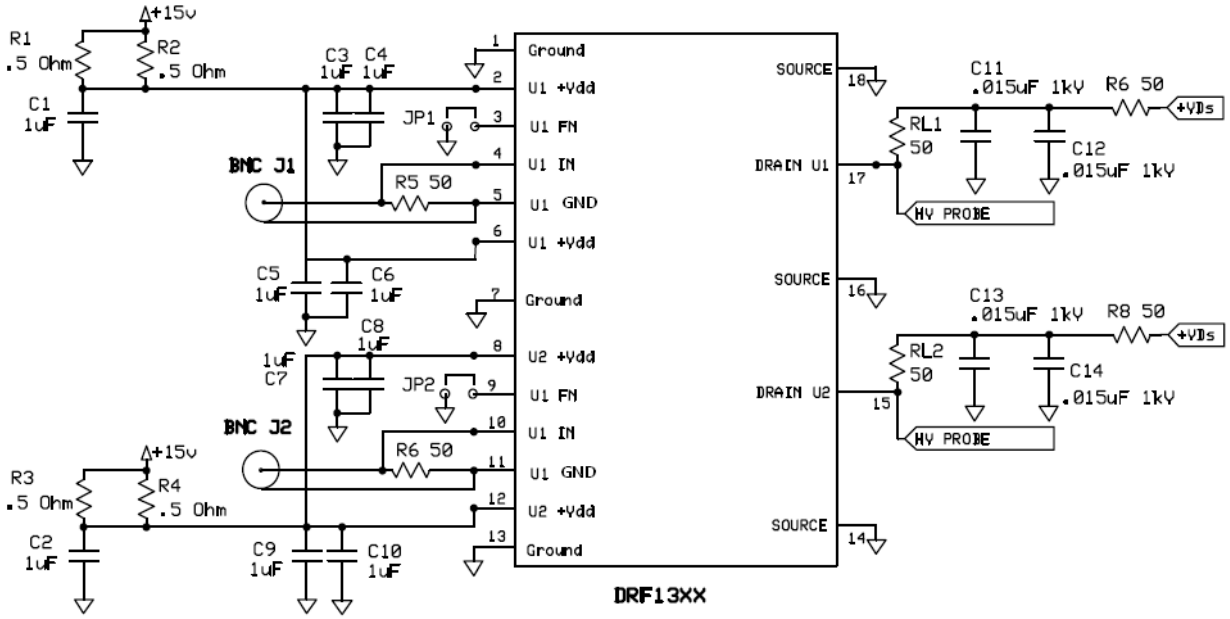

Figure 2. DRF13XX Evaluation Board

A 5V max signal input is applied to either J1 or J2. Using the Ground (GND) for the BNC shielding provides a connection for the input increasing noise immunity. The driver supply from the +15V (VCC) input is applied to U1 Vdd pins 2 and 6 that are both externally and internally connected to help balance pulse currents in the hybrid. The same applies for U2 Vdd pins 8 and 12. U1 section and the U2 section do not share an internal power connection.

Connecting the Jumper JP1 will cause the U1 side of the DRF1300 to operate in the Inverting mode, while JP2 provides this function for the U2 side.

The output sections as configured have 50Ω resistive pull-up circuits with on board filtering for the High Voltage power supply. High currents should be restricted to the source and drain pins.

Table 2 shows Evaluation board inputs and outputs and the highly recommended Common Mode Chokes (CMC) that should be used for the test bench set-up. These devices provide the best stability and the most accurate measurements.

Inputs	Parameter	Remarks
GND	Driver Ground	(Green)
+15V	Driver supply	CMC suggested (VCC White)
IN	+5V max signal	BNC w/ 50Ω termination, CMC suggested
GND	(IN) Signal Rtn.	BNC, Rtn, CMC suggested
Drain Probe	X10 or X100 Probe	Tek P6139A or P5100, CMC suggested on probe lead
VDS	+250V Max	CMC suggested (Red)
Power GND	Power GND	Connected to MOSFET Source (Black)

Table 2

Construction of both CMCs is illustrated in Figure 3. The CMC on the left should be used for both the +15V input and the +HV VDS input. These lines are tightly twisted pairs (5-8 twists per inch). The CMC on the right should be used for the control signal Input and on the Scope Probe Cable. Three to five turns on each is sufficient. The CMCs should be placed as close to the DRF13XX Evaluation Board as practical.

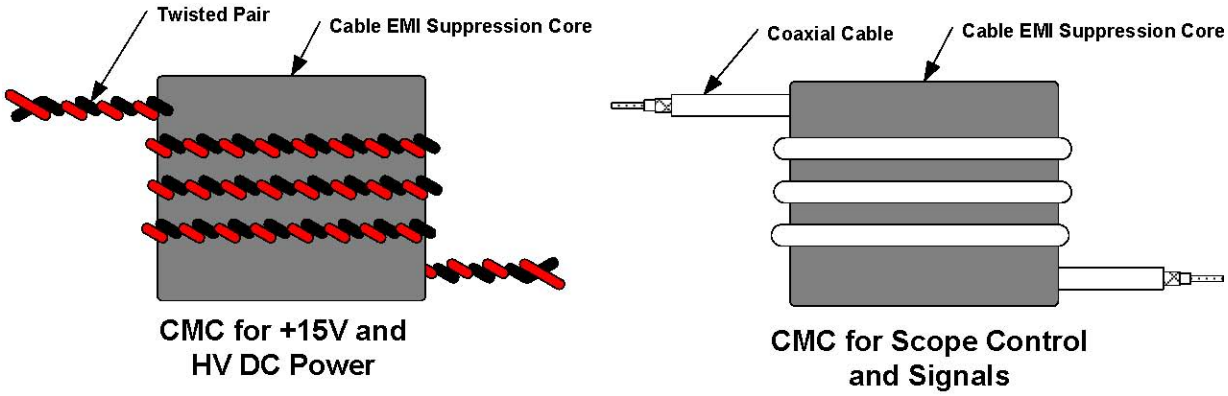

Figure 3. Common Mode Choke (CMC)
FairRite part number 0431164181

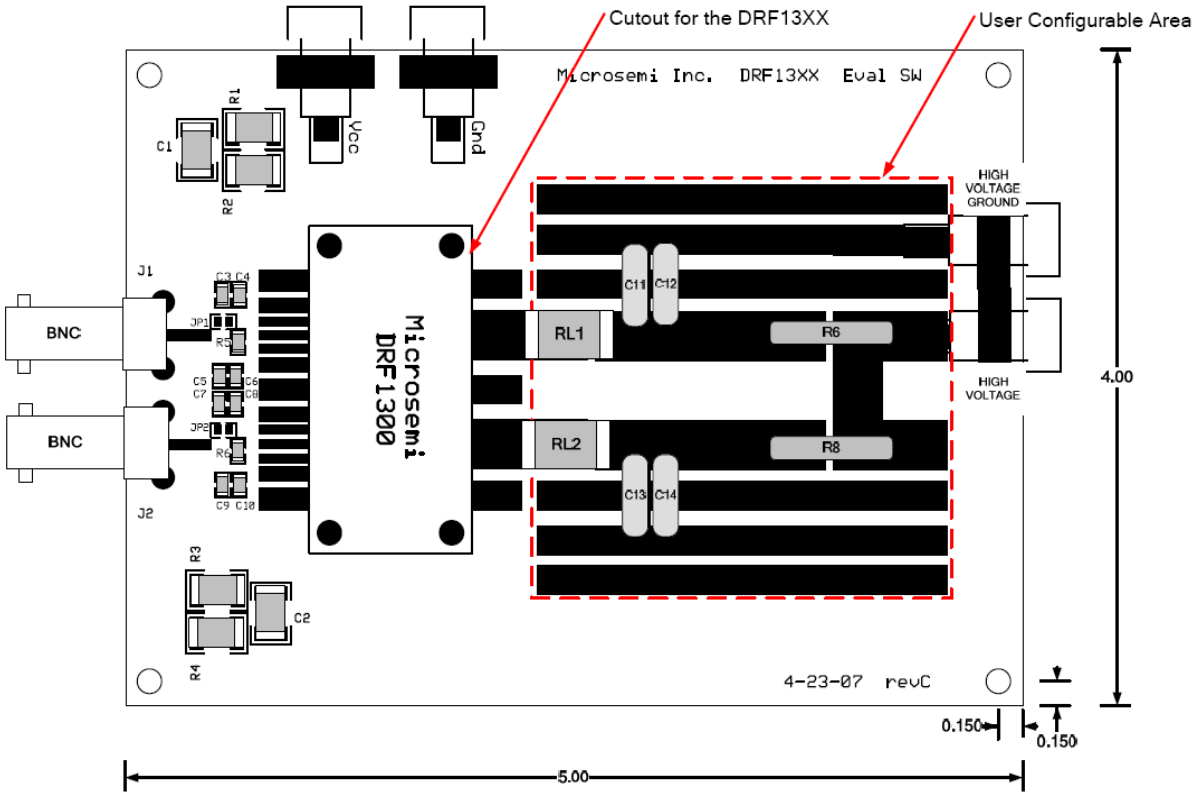

Figure 4. DRF13XX Evaluation Board
All Dimensions are ± 0.010 In. Max.

Figure 4 shows the mechanical layout of the DRF13XX. The user configurable area is illustrated by the dashed red line. The main purpose of the board is to verify SWITCHING PERFORMANCE for DRF13xx devices.

Mounting Instructions for Flangeless Devices: Refer to Application Note 1810 “DRF Device Mounting Procedures And Power Dissipation”.