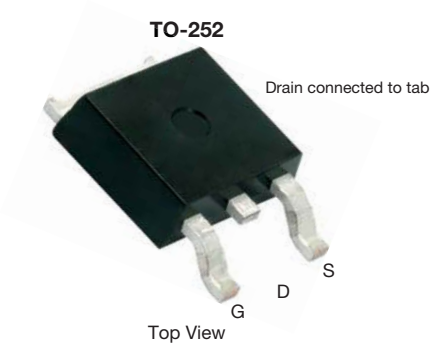
P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (TYP.)
-40	0.0081 at V_{GS} = -10 V	-50 [d]	60
	0.0117 at V_{GS} = -4.5 V	-48 [d]	



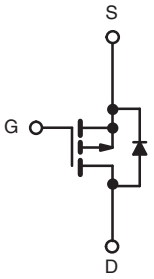
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Power switch
- Load switch in high current applications
- DC/DC converters



P-Channel MOSFET

Ordering Information:
SUD50P04-08-GE3 (lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	-50 [d]	A
	T_C = 70 °C		-50 [d]	
Pulsed Drain Current		I_{DM}	-100	
Avalanche Current		I_{AS}	-46	
Single Avalanche Energy [a]	L = 0.1 mH	E_{AS}	106	mJ
Maximum Power Dissipation [a]	T_C = 25 °C	P_D	73.5 [b]	W
	T_A = 25 °C [c]		2.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount) [c]	R_{thJA}	50	°C/W
Junction-to-Case (Drain)	R_{thJC}	1.7	

Notes
a. Duty cycle ≤ 1 %.
b. See SOA curve for voltage derating.
c. When mounted on 1" square PCB (FR-4 material).
d. Package limited.

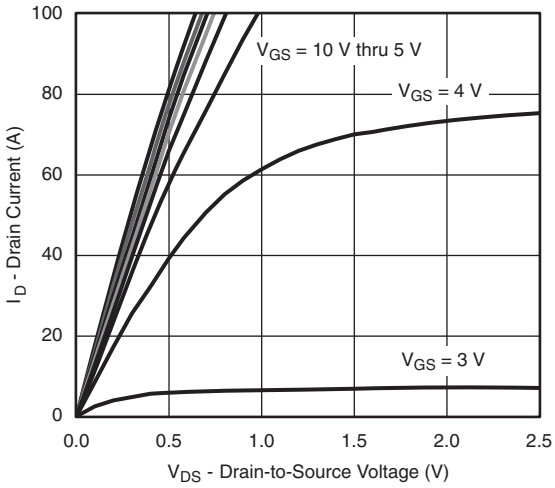
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-1	-	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40 V, V_{GS} = 0 V	-	-	-1	µA
		V_{DS} = -40 V, V_{GS} = 0 V, T_J = 125 °C	-	-	-50	
		V_{DS} = -40 V, V_{GS} = 0 V, T_J = 150 °C	-	-	-250	
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} \leq$ -10 V, V_{GS} = -10 V	-50	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -22 A	-	0.0067	0.0081	Ω
		V_{GS} = -4.5 V, I_D = -19 A	-	0.0097	0.0117	
Forward Transconductance [a]	g_{fs}	V_{DS} = -15 V, I_D = -22 A	-	45	-	S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -20 V, f = 1 MHz	-	5380	-	pF
Output Capacitance	C_{oss}		-	570	-	
Reverse Transfer Capacitance	C_{rss}		-	500	-	
Total Gate Charge [c]	Q_g	V_{DS} = -20 V, V_{GS} = -10 V, I_D = -20 A	-	106	159	nC
		V_{DS} = -20 V, V_{GS} = -4.5 V, I_D = -20 A	-	60	90	
Gate-Source Charge [c]	Q_{gs}		-	22	-	
Gate-Drain Charge [c]	Q_{gd}		-	27	-	
Gate Resistance	R_g	f = 1 MHz	0.4	1.8	3.6	Ω
Turn-On Delay Time [c]	$t_{d(on)}$	V_{DD} = -20 V, R_L = 2 Ω $I_D \cong$ -10 A, V_{GEN} = -10 V, R_g = 1 Ω	-	15	23	ns
Rise Time [c]	t_r		-	12	18	
Turn-Off Delay Time [c]	$t_{d(off)}$		-	70	105	
Fall Time [c]	t_f		-	18	27	
Drain-Source Body Diode Ratings and Characteristics (T_C = 25 °C) [b]						
Continuous Current	I_S		-	-	-50	A
Pulsed Current	I_{SM}		-	-	-100	
Forward Voltage [a]	V_{SD}	I_F = -10 A, V_{GS} = 0 V	-	-0.8	-1.5	V
Reverse Recovery Time	trr	I_F = -10 A, dI/dt = 100 A/µs	-	35	53	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$		-	-2	-3	A
Reverse Recovery Charge	Q_{rr}		-	33	50	nC

Notes

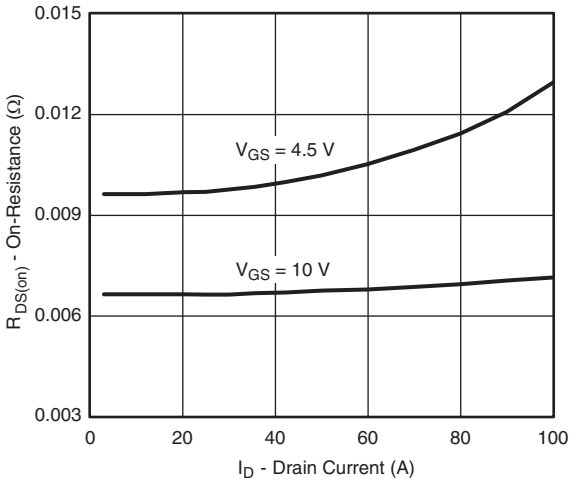
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

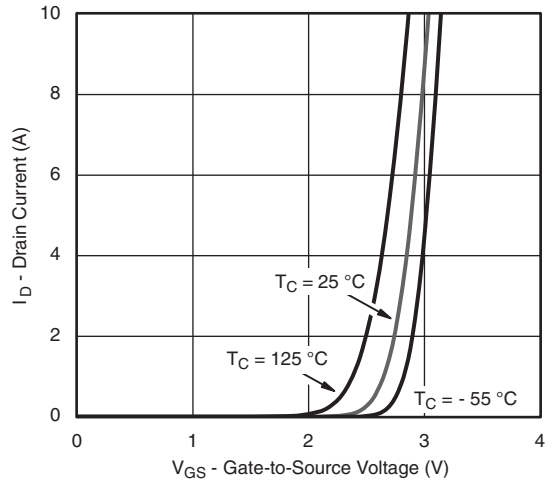
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



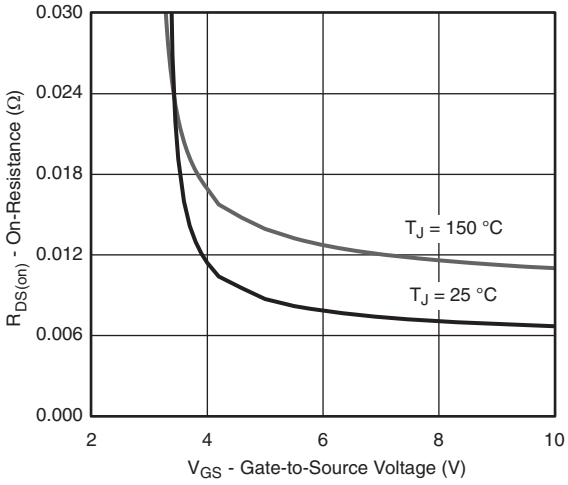
Output Characteristics



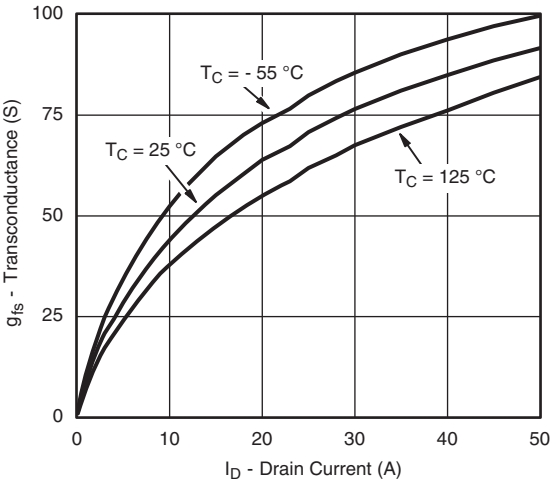
On-Resistance vs. Drain Current



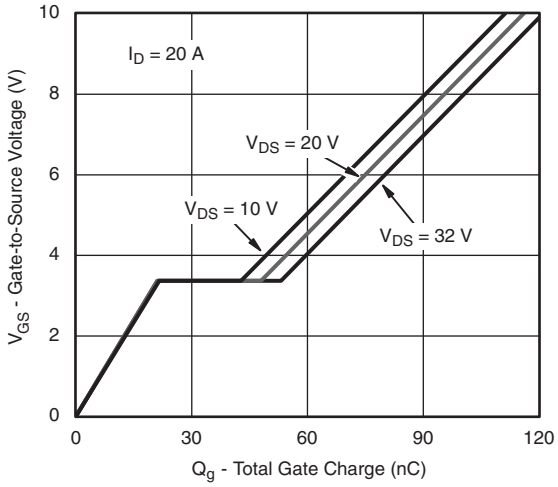
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage

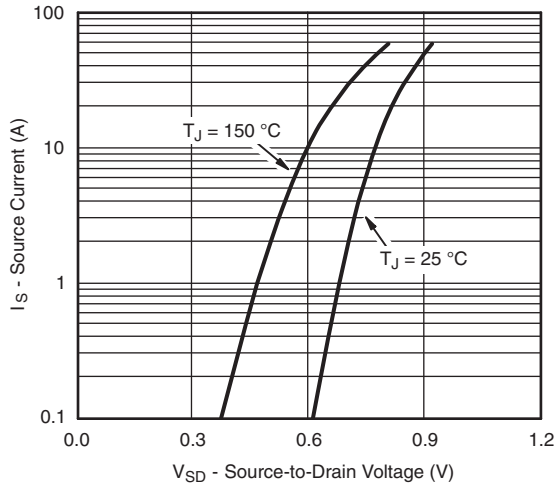


Transconductance

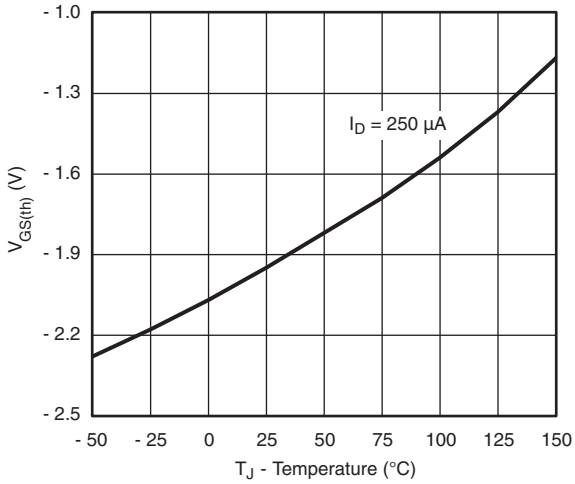


Gate Charge

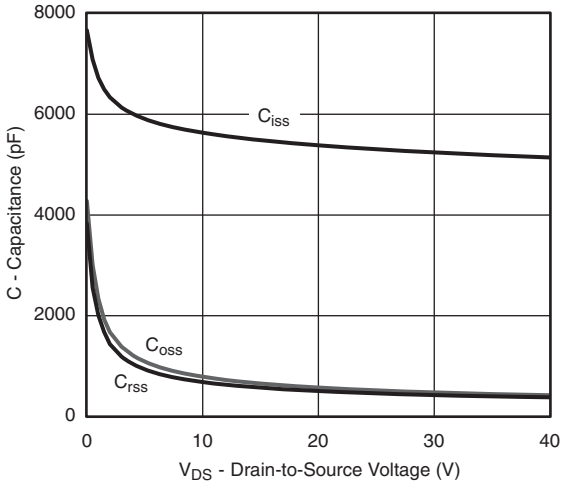
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



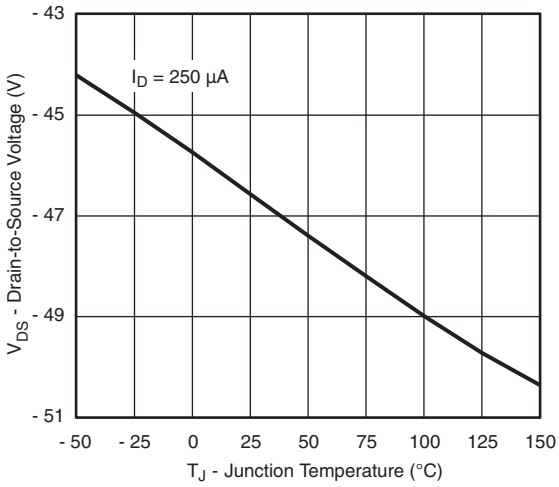
Source-Drain Diode Forward Voltage



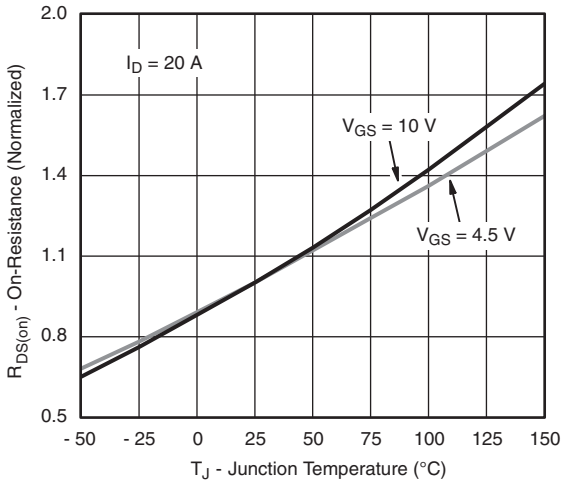
Threshold Voltage



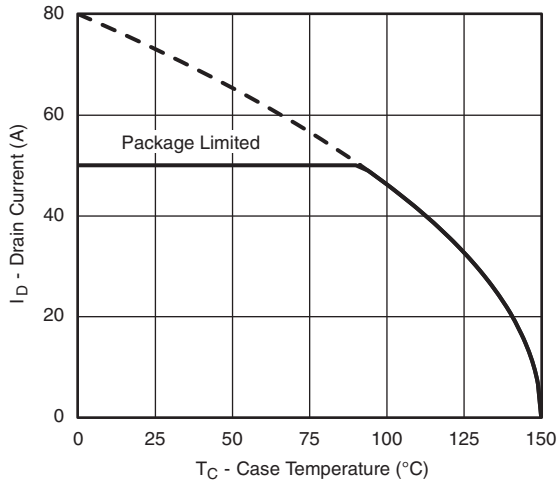
Capacitance



Drain Source Breakdown vs. Junction Temperature

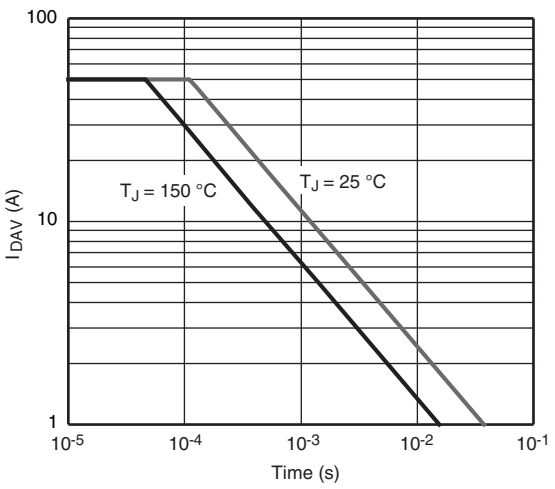


On-Resistance vs. Junction Temperature

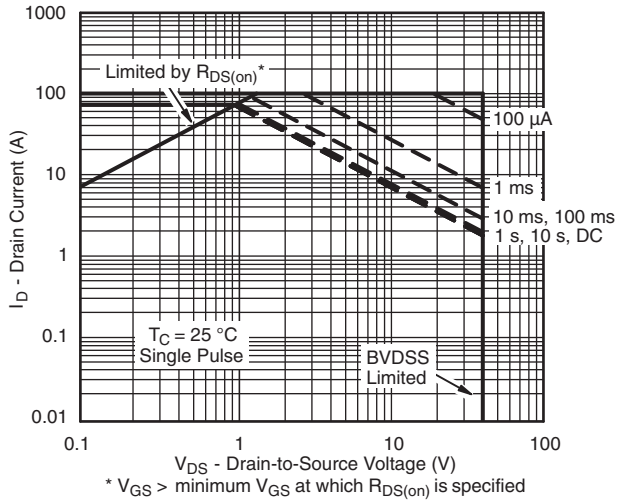


Current Derating

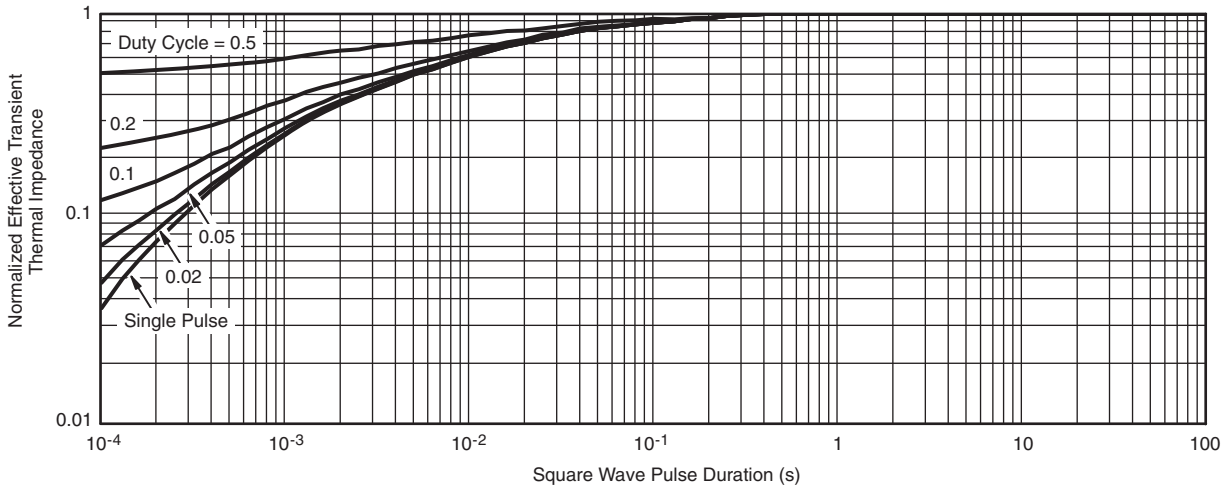
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Single Pulse Avalanche Current Capability vs. Time



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

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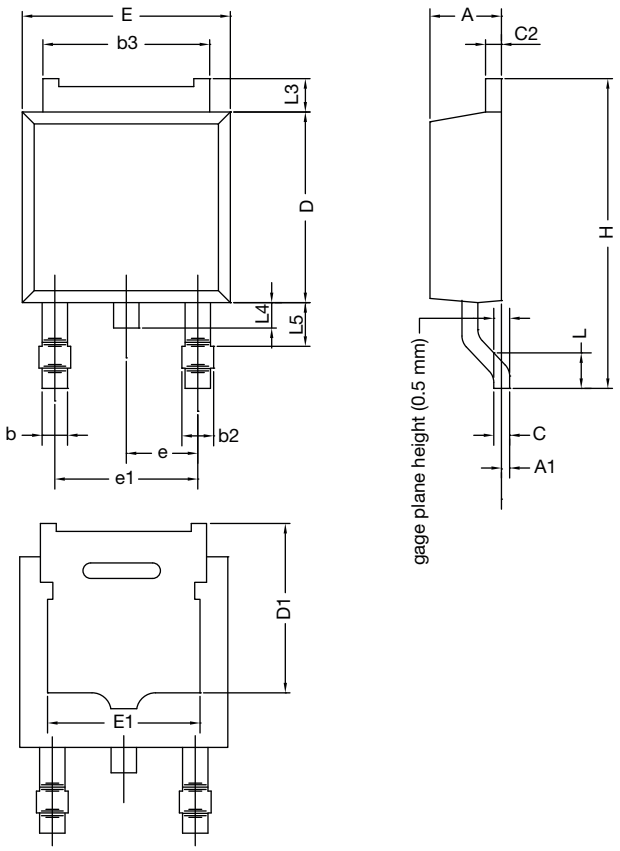
TO-252AA Case Outline

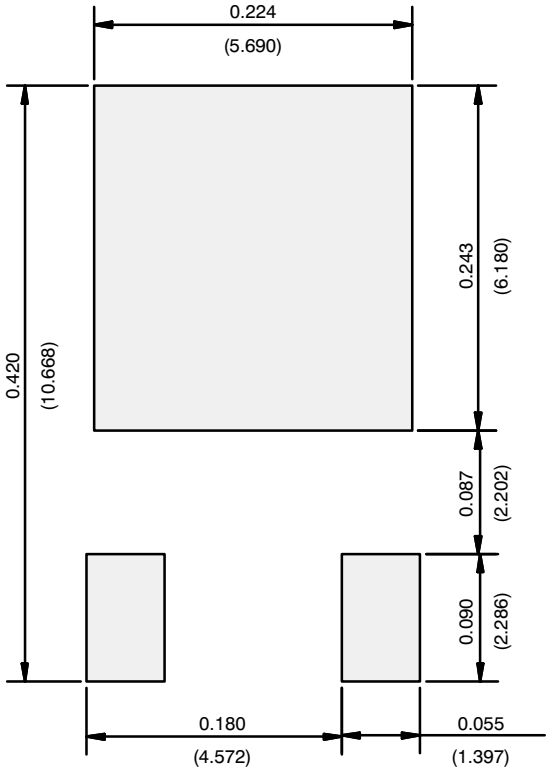


	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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