FAIRCHILD SEMICONDUCTOR™

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SSTV16859
Dual Output 13-Bit Register with SSTL-2 Compatible I/O and Reset

General Description

The SSTV16859 is a dual output 13-bit register designed for use with 184 and 232 pin DDR-1 memory modules. The device has a differential input clock, SSTL-2 compatible data inputs and a LVCMOS compatible RESET input. The device has been designed to meet the JEDEC DDR module register specifications.

The device has been fabricated on an advanced submicron CMOS process and is designed to operate at power supplies of less than 3.6V's.

Features

- Compliant with DDR-I registered module specifications
- Operates at 2.5V ± 0.2V V_{DD}
- SSTL-2 compatible input structure
- SSTL-2 compliant output structure
- Differential SSTL-2 compatible clock inputs
- Low power mode when device is reset
- Industry standard 64 pin TSSOP package
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Ordering Code:

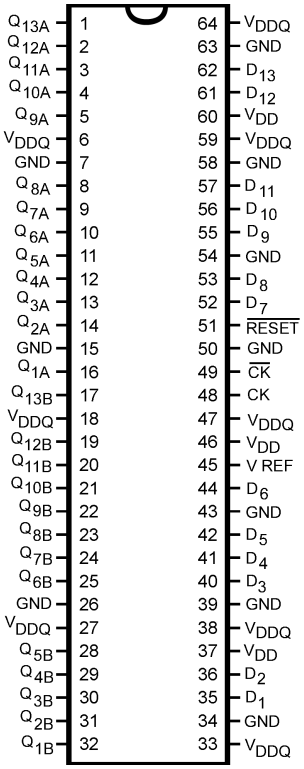
Order Number	Package Number	Package Description
SSTV16859G (Note 1)(Note 2)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
SSTV16859MTD (Note 2)	MTD64	64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 1: Ordering code "G" indicates Trays.

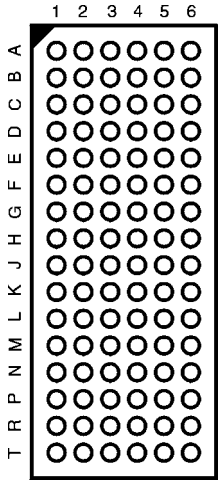
Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Name	Description
Q_{1A}-Q_{13A} Q_{1B}-Q_{13B}	SSTL-2 Compatible Register Outputs
D_1-D_{13}	SSTL-2 Compatible Register Inputs
$\overline{RESET}$	Asynchronous LVCMOS Reset Input
CK	Positive Master Clock Input
$\overline{CK}$	Negative Master Clock Input
V_{REF}	Voltage Reference Pin for SSTL level inputs
V_{DDQ}	Power Supply Voltage for Output Signals
V_{DD}	Power Supply Voltage for Inputs
NC	Electrically Isolated No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	NC	NC	NC	NC	NC	NC
B	Q_{12A}	Q_{13A}	GND	GND	NC	NC
C	Q_{10A}	Q_{11A}	GND	GND	NC	NC
D	Q_{8A}	Q_{9A}	V_{DDQ}	V_{DDQ}	D_{13}	D_{12}
E	Q_{6A}	Q_{7A}	V_{DDQ}	V_{DD}	D_{11}	D_{10}
F	Q_{4A}	Q_{5A}	V_{DDQ}	V_{DD}	D_9	D_8
G	Q_{2A}	Q_{3A}	GND	GND	D_7	$\overline{RESET}$
H	Q_{1A}	Q_{13B}	GND	GND	NC	$\overline{CK}$
J	Q_{12B}	Q_{11B}	GND	V_{REF}	NC	CK
K	Q_{10B}	Q_{9B}	V_{DDQ}	V_{DD}	NC	NC
L	Q_{8B}	Q_{7B}	V_{DDQ}	V_{DD}	D_5	D_6
M	Q_{6B}	Q_{5B}	V_{DDQ}	V_{DDQ}	D_3	D_4
N	Q_{4B}	Q_{3B}	GND	GND	D_1	D_2
P	Q_{2B}	Q_{1B}	GND	GND	NC	NC
R	NC	NC	NC	NC	NC	NC
T	NC	NC	NC	NC	NC	NC

Truth Table

$\overline{RESET}$	D_n	CK	$\overline{CK}$	Q_n
L	X or Floating	X or Floating	X or Floating	L
H	L	↑	↓	L
H	H	↑	↓	H
H	X	L	H	Q_{n-1}
H	X	H	L	Q_{n-1}

L = Logic LOW
H = Logic HIGH
X = Don't Care but not floating unless noted
↑ = LOW-to-HIGH Clock Transition
↓ = HIGH-to-LOW Clock Transition
Q_{n-1} = Output Remains in Previously Clocked State

Functional Description

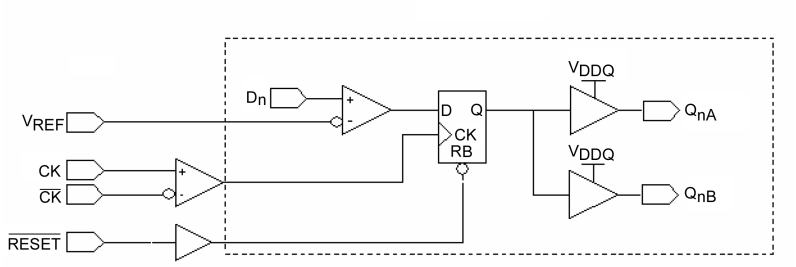
The SSTV16859 is a 13-bit dual register with SSTL-2 compatible inputs and outputs. Input data is transferred to output data on the rising edge of the differential clock pair. When the $\overline{\text{RESET}}$ signal is asserted LOW all outputs are placed into the LOW logic state and all input comparators are disabled for power savings. Output glitches are prevented by disabling the internal registers more quickly than the input comparators. When $\overline{\text{RESET}}$ is removed, the system designer must insure the clock and data inputs to the device are stable during the rising transition of the $\overline{\text{RESET}}$ signal.

The SSTL-2 data inputs transition based on the value of V_{REF}. V_{REF} is a stable system reference used for setting the trip point of the input buffers of the SSTV16859 and other SSTL-2 compatible devices.

The $\overline{\text{RESET}}$ signal is a standard CMOS compatible input and is not referenced to the V_{REF} signal.

Logic Diagram

For n = 1 to 13



Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{DDQ})	−0.5V to +3.6V
Supply Voltage (V_{DD})	−0.5V to +3.6V
Reference Voltage (V_{REF})	−0.5V to +3.6V
Input Voltage (V_I)	−0.5V to V_{DD} +0.5V
Output Voltage (V_O)	
Outputs Active (Note 4)	−0.5V to V_{DDQ} + 0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
V_I > V_{DD}	+50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{DDQ}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{DD} or Ground Current per Supply Pin (I_{DD} or Ground)	±100 mA
Storage Temperature Range (T_{stg})	−65°C to +150°C
ESD (Human Body Model)	≥ 7000V

Recommended Operating Conditions (Note 5)

Power Supply (V_{DDQ})	2.3V to 2.7V
Power Supply (V_{DD})	
Operating Range	V_{DDQ} to 2.7V
Reference Supply (V_{REF} = V_{DDQ}/2)	1.15 to 1.35
Termination Voltage (V_{TT})	V_{REF} ± 40 mV
Input Voltage	0 to V_{DD}
Output Voltage (V_O)	
Output in Active States	0V to V_{DDQ}
Output Current I_{OH}/I_{OL}	
V_{DD} = 2.3V to 2.7V	±20 mA
Free Air Operating Temperature (T_A)	0°C to +70°C

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: IO Absolute Maximum Rating must be observed.

Note 5: The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is asserted LOW.

DC Electrical Characteristics ($2.3V \le V_{DD} \le 2.7V$)

Symbol	Parameter	Conditions	V_{DD} (V)	Min	Typ	Max	Units
V_{IKL}	Input LOW Clamp Voltage	I_I = −18 mA	2.3			−1.2	V
V_{IKH}	Input HIGH Clamp Voltage	I_I = +18 mA	2.3			3.5	V
$V_{IH\text{-}AC}$	AC HIGH Level Input Voltage	Data Inputs		V_{REF}+310mV			V
$V_{IL\text{-}AC}$	AC LOW Level Input Voltage	Data Inputs				V_{REF}−310mV	V
$V_{IH\text{-}DC}$	DC HIGH Level Input Voltage	Data Inputs		V_{REF}+150mV			V
$V_{IL\text{-}DC}$	DC LOW Level Input Voltage	Data Inputs				V_{REF}−150mV	V
V_{IH}	HIGH Level Input Voltage	$\overline{\text{RESET}}$		1.7			V
V_{IL}	LOW Level Input Voltage	$\overline{\text{RESET}}$				0.7	V
V_{ICR}	Common Mode Input Voltage Range	CK, $\overline{\text{CK}}$		0.97		1.53	V
$V_{I(PP)}$	Peak to Peak Input Voltage	CK, $\overline{\text{CK}}$		360			mV
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA I_{OH} = −16 mA	2.3 to 2.7 2.3	V_{DD} − 0.2 1.95			V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA I_{OL} = 16 mA	2.3 to 2.7 2.3			0.2 0.35	V
I_I	Input Leakage Current	V_I = V_{DD} or GND	2.7			±5.0	µA
I_{DD}	Static Standby	$\overline{\text{RESET}}$ = GND, I_O = 0	2.7			10	µA
	Static Operating	$\overline{\text{RESET}}$ = V_{DD}, I_O = 0 V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$				25	mA
I_{DDD}	Dynamic Operating Current Clock Only	$\overline{\text{RESET}}$ = V_{DD}, I_O = 0 V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$ CK, $\overline{\text{CK}}$ Duty Cycle 50%	2.7			120	µA/MHz
	Dynamic Operating Current per Data Input	$\overline{\text{RESET}}$ = V_{DD}, I_O = 0 V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$ CK, $\overline{\text{CK}}$ Duty Cycle 50% Data Input = ½ Clock Rate 50% Duty Cycle				15	µA/MHz

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{DD} (V)	Min	Typ	Max	Units
R_{OH}	Output HIGH On Resistance	I_{OH} = −20 mA	2.3 to 2.7	7		20	Ω
R_{OL}	Output LOW On Resistance	I_{OL} = 20 mA	2.3 to 2.7	7		20	Ω
$R_{O\Delta}$	$\lvert R_{OH} - R_{OL} \rvert$	I_O = 20 mA, T_A = 25°C	2.5			4	Ω

AC Electrical Characteristics (Note 6)

Symbol	Parameter	T_A = 0°C to +70°C, C_L = 30 pF, R_L = 50Ω; V_{DD} = 2.5V ± 0.2V; V_{DDQ} = 2.5V ± 0.2V			Units
		Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency	200			MHz
t_W	Pulse Duration, CK, $\overline{CK}$ HIGH or LOW (Figure 2)	2.5			ns
t_{ACT} (Note 7)	Differential Inputs Activation Time, data inputs must be LOW after $\overline{RESET}$ HIGH (Figure 3)	22			ns
t_{INACT} (Note 7)	Differential Inputs De-activation Time, data and clock inputs must be held at valid levels (not floating) after $\overline{RESET}$ LOW	22			ns
t_S	Setup Time, Fast Slew Rate (Note 8)(Note 9) (Figure 5)	0.75			ns
	Setup Time, Slow Slew Rate (Note 9)(Note 10) (Figure 5)	0.9			
t_H	Hold Time, Fast Slew Rate (Note 8)(Note 10) (Figure 5)	0.75			ns
	Hold Time, Slow Slew Rate (Note 9)(Note 10) (Figure 5)	0.9			
t_{REM}	Reset Removal Time (Figure 7)	10			ns
t_{PHL}, t_{PLH}	Propagation Delay CK, $\overline{CK}$ to Q_n (Figure 4)	1.1		2.8	ns
t_{PHL}	Propagation Delay $\overline{RESET}$ to Q_n (Figure 6)			5.0	ns

Note 6: Refer to Figure 1 through Figure 7.

Note 7: This parameter is not production tested.

Note 8: For data signal input slew rate ≥ 1 V/ns.

Note 9: For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.

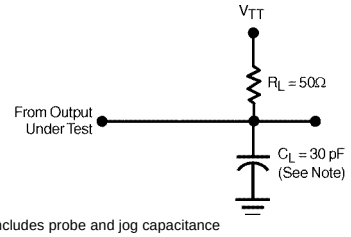
Note 10: For CK, $\overline{CK}$ signals input slew rates are ≥ 1 V/ns.

Capacitance (Note 11)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Data Pin Input Capacitance	2.2		3.2	pF	V_{DD} = 2.5V, V_I = V_{REF} ± 310 mV
	CK, $\overline{CK}$ - Input Capacitance	2.2		3.2	pF	V_{DD} = 2.5V, V_{ICR} = 1.25, $V_{I(PP)}$ = 360 mV
	$\overline{RESET}$	2.3		3.3	pF	V_{DD} = 2.5V, V_I = V_{DD} or GND

Note 11: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms (See Notes A through F below)



Note: C_L includes probe and jog capacitance

FIGURE 1. AC Test Circuit

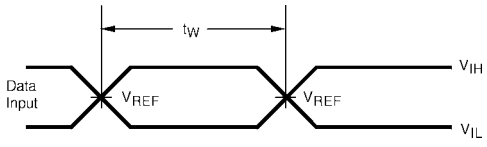
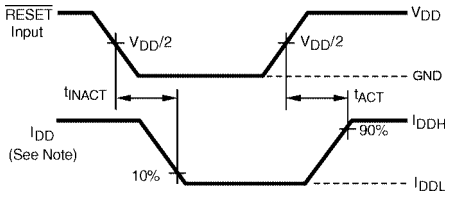


FIGURE 2. Voltage Waveforms - Pulse Duration



Note: I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_O = 0$ mA.

FIGURE 3. Voltage and Current Waveforms Inputs Active and Inactive Times

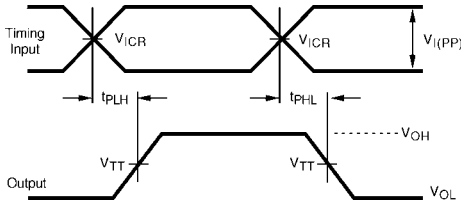


FIGURE 4. Voltage Waveforms - Propagation Delay Times

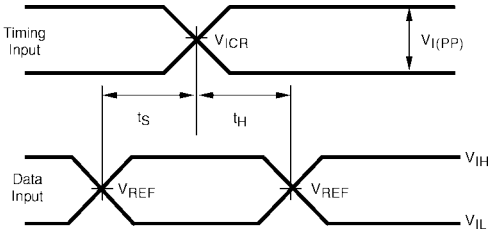


FIGURE 5. Voltage Waveforms - Setup and Hold Times

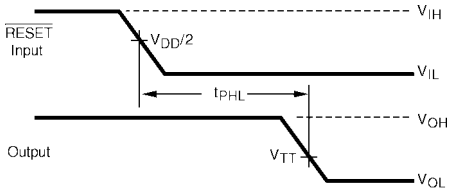


FIGURE 6. Voltage Waveforms - RESET Propagation Delay Times

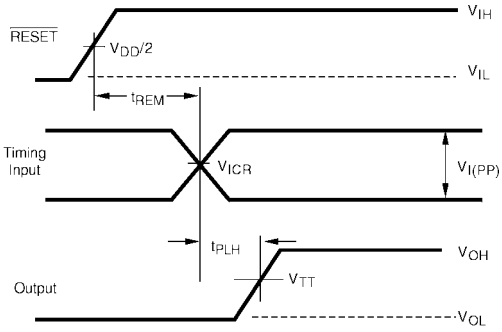


FIGURE 7. Voltage Waveforms - RESET Removal Delay Times

Note A: All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz, $Z_0 = 50\Omega$, input slew rate = 1V/ns ± 20% (unless otherwise specified).

Note B: The outputs are measured one at a time with one transition per measurement.

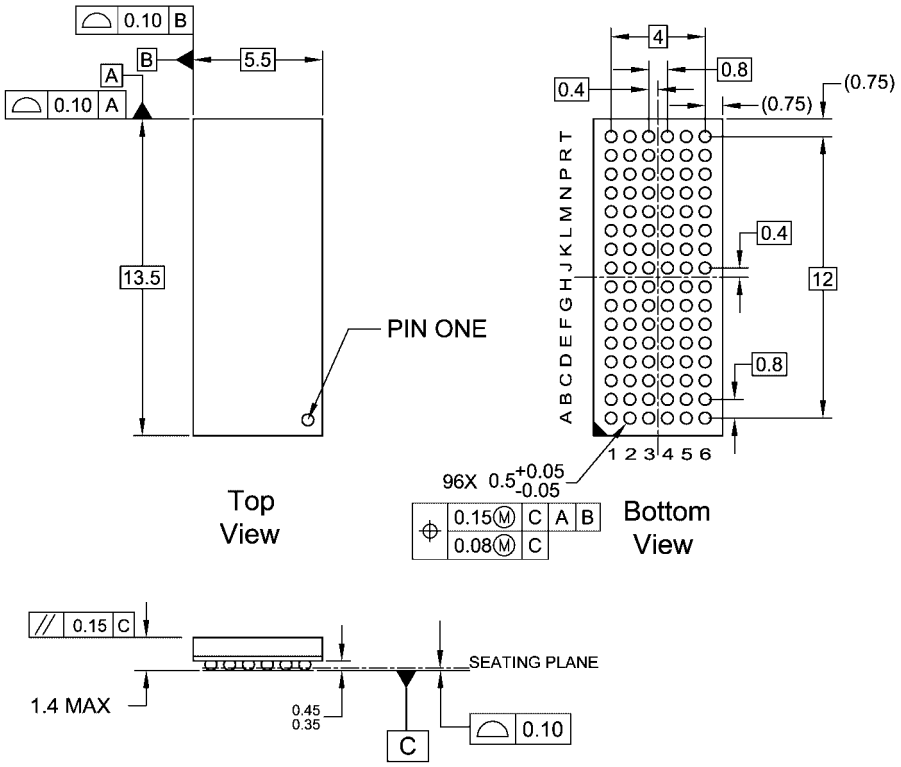
Note C: $V_{TT} = V_{REF} = V_{DD}/2$.

Note D: $V_{IH} = V_{REF} + 310$ mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

Note E: $V_{IL} = V_{REF} - 310$ mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

Note F: Removal time (t_{REM}) is tested with one data input held active HIGH. The propagation time from CK to the corresponding output must meet valid timing specifications for the measurement to be accurate.

Physical Dimensions inches (millimeters) unless otherwise noted



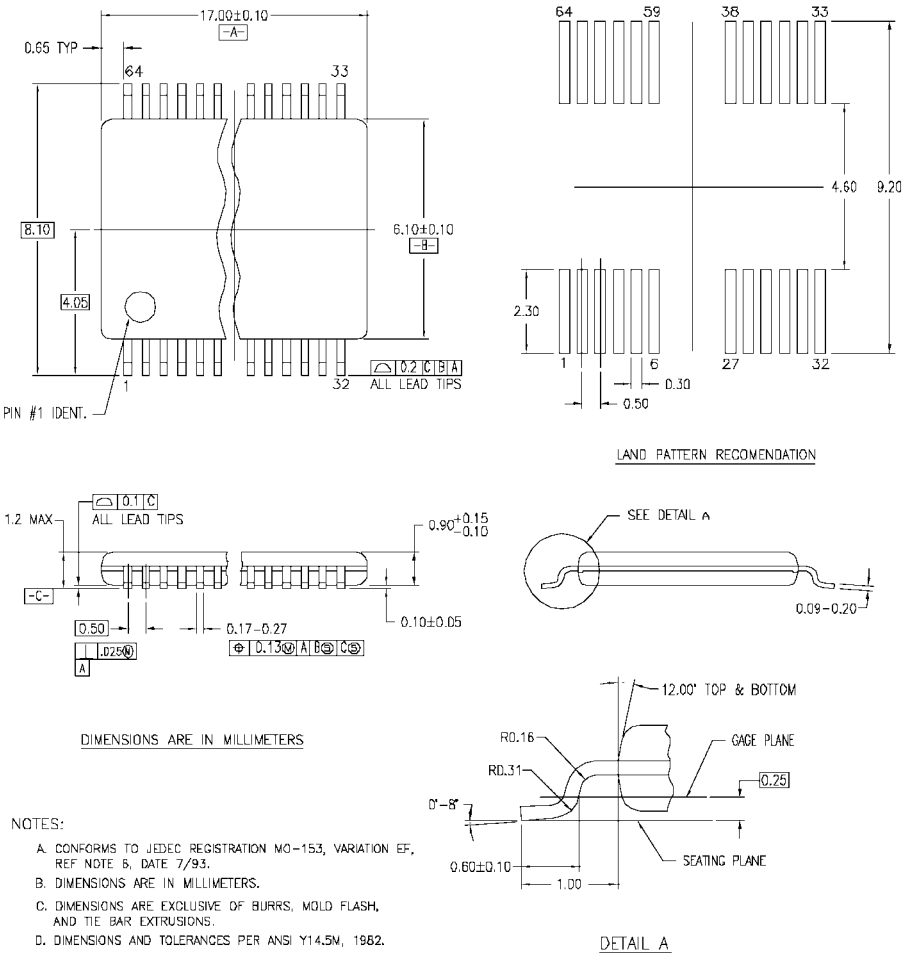
NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD64

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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