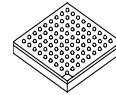


MSC8144E



FC-PBGA-783
29 mm × 29 mm

Quad Core Digital Signal Processor

- Four StarCore® SC3400 DSP subsystems, each with an SC3400 DSP core, 16 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, memory management unit (MMU), extended programmable interrupt controller (EPIC), two general-purpose 32-bit timers, debug and profiling support, and low-power Wait and Stop processing modes.
- Chip-level arbitration and system (CLASS) that provides full fabric non-blocking arbitration between the processing elements and other initiators and the M2 memory, DDR SRAM controller, device configuration control and status registers, and other targets.
- 128 Kbyte L2 shared instruction cache.
- 512 Kbyte M2 memory for critical data and temporary data buffering.
- 10 Mbyte 128-bit wide M3 memory.
- 96 Kbyte boot ROM.
- Three input clocks (shared, global, and differential).
- Four PLLs (system, core, global, and serial RapidIO).
- Security Engine (SEC0 optimized to process all the algorithms associated with IPsec, IKE, WTLS/WAP, SSL/TLS, and 3GPP using 4 crypto-channels with multi-command chains, integrated controller for assignment of the six execution units (PKEU, DEU, AESU, AFEU, MDEU, and KEU0) and the random number generator (RNG), and XOR engine to accelerate parity checking for RAID storage applications.
- DDR controller with up to a 200 MHz clock (400 MHz data rate), 16/32 bit data bus, supporting up to 1 Gbyte in up to two banks and support for DDR1 and DDR2.
- DMA controller with 16 bidirectional channels with up to 1024 buffer descriptors, and programmable priority, buffer, and multiplexing configuration.
- Up to eight independent TDM modules with programmable word size (2, 4, 8, or 16-bit), hardware-base A-law/ μ -law conversion, up to 128 Mbps data rate for all channels, with glueless interface to E1 or T1 framers, and can interface with H-MVIP/H.110 devices, TSI, and codecs such as AC-97.
- QUICC Engine™ technology subsystem with dual RISC processors, 48 Kbyte multi-master RAM, 48 Kbyte instruction RAM, supporting three communication controllers with one ATM and two Gigabit Ethernet interfaces, to offload scheduling tasks from the DSP cores.
- The two Ethernet controllers support 10/100/1000 Mbps operations via MII/RMII/SMII/RGMII/SGMII and the SGMII protocol using a 4-pin SerDes interface at 1000 Mbps data rate only.
- The ATM controller supports UTOPIA level II 8/16 bits at 25/50 MHz in UTOPIA/POS mode with adaptation layer support AAL0, AAL2, and AAL5.
- PCI designed to comply with the PCI specification revision 2.2 at 33 MHz or 66 MHz with access to all PCI address spaces.
- Serial RapidIO® 1x/4x endpoint corresponds to Specification 1.2 of the RapidIO trade association, and supports read, write, messages, doorbells, and maintenance accesses in inbound mode, and messages and doorbells in outbound mode.
- I/O interrupt concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes them to $\overline{\text{INT_OUT}}$, $\overline{\text{NMI_OUT}}$, and the cores.
- UART that permits full-duplex operation with a bit rate of up to 6.25 Mbps.
- Serial peripheral interface (SPI).
- Four timer modules, each with four configurable 16-bit timers.
- Four software watchdog timer (SWT) modules.
- Up to 32 general-purpose input/output (GPIO) ports, 16 of which can be configured as maskable interrupt inputs.
- I²C interface that allows booting from EEPROM devices.
- Eight programmable hardware semaphores.
- Thirty two virtual maskable interrupts and one virtual $\overline{\text{NMI}}$ that can be generated by a simple write access.
- Optional booting via serial RapidIO port, PCI, I²C, SPI, or Ethernet interfaces.

Note: This document supports mask set M31H.

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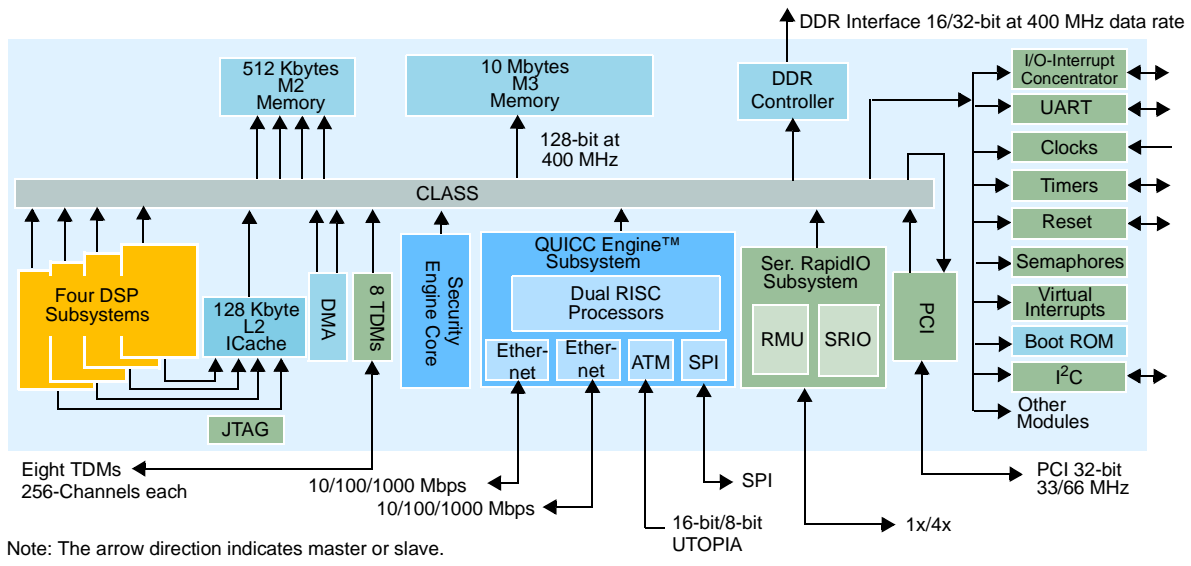


Figure 1. MSC8144E Block Diagram

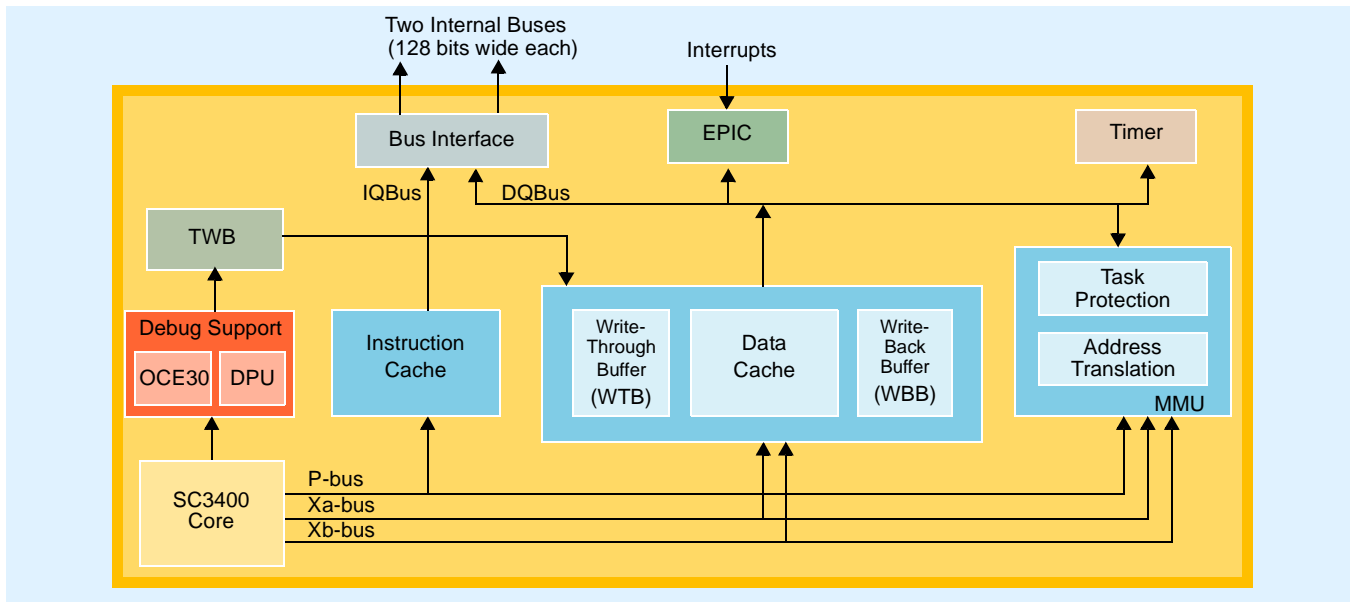


Figure 2. StarCore SC3400 DSP Core Subsystem Block Diagram

1 Pin Assignments and Reset States

This section includes diagrams of the MSC8144E package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in [Figure 3](#) and [Figure 4](#) with their ball location index numbers.

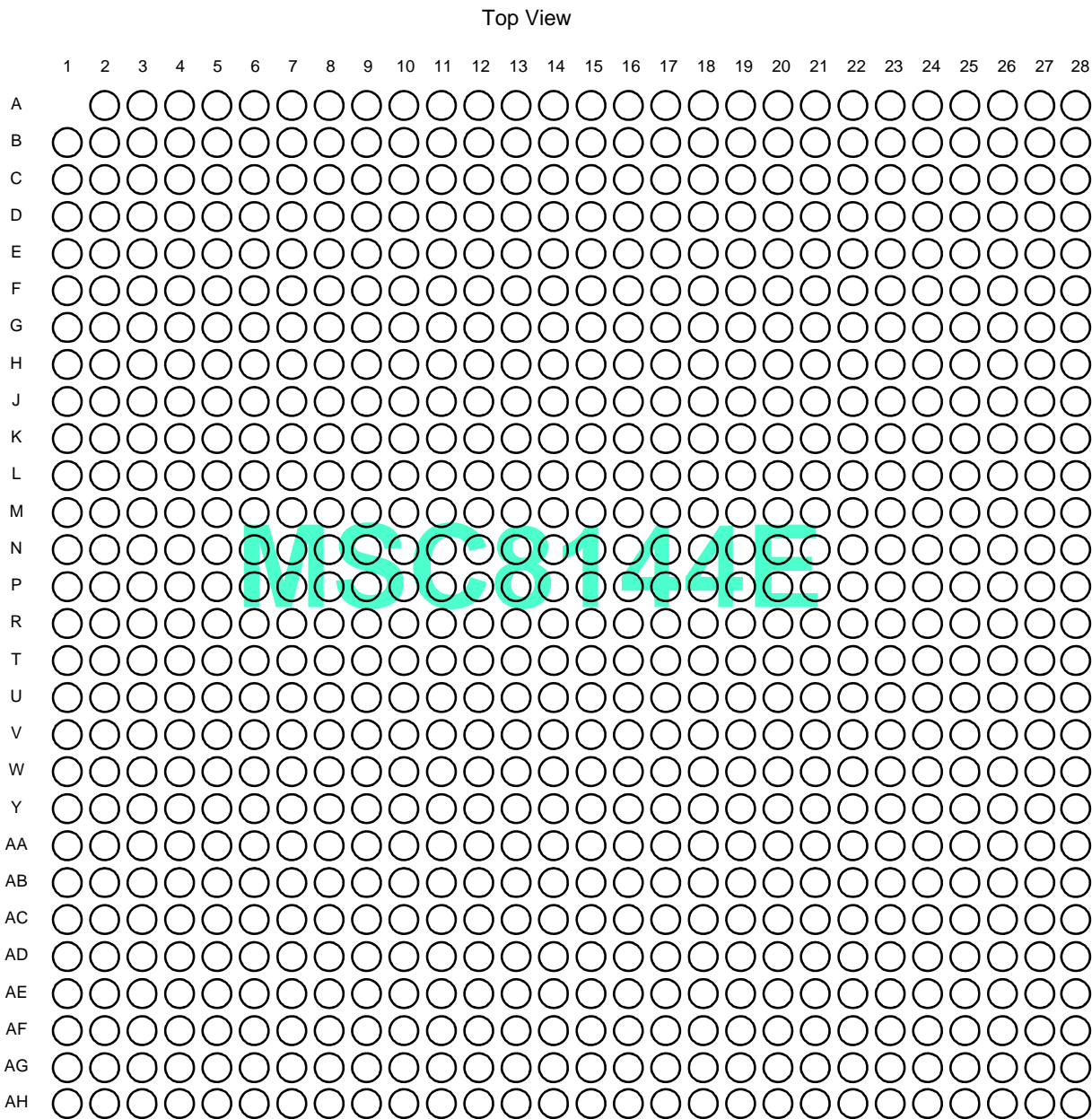


Figure 3. MSC8144E FC-PBGA Package, Top View

Bottom View

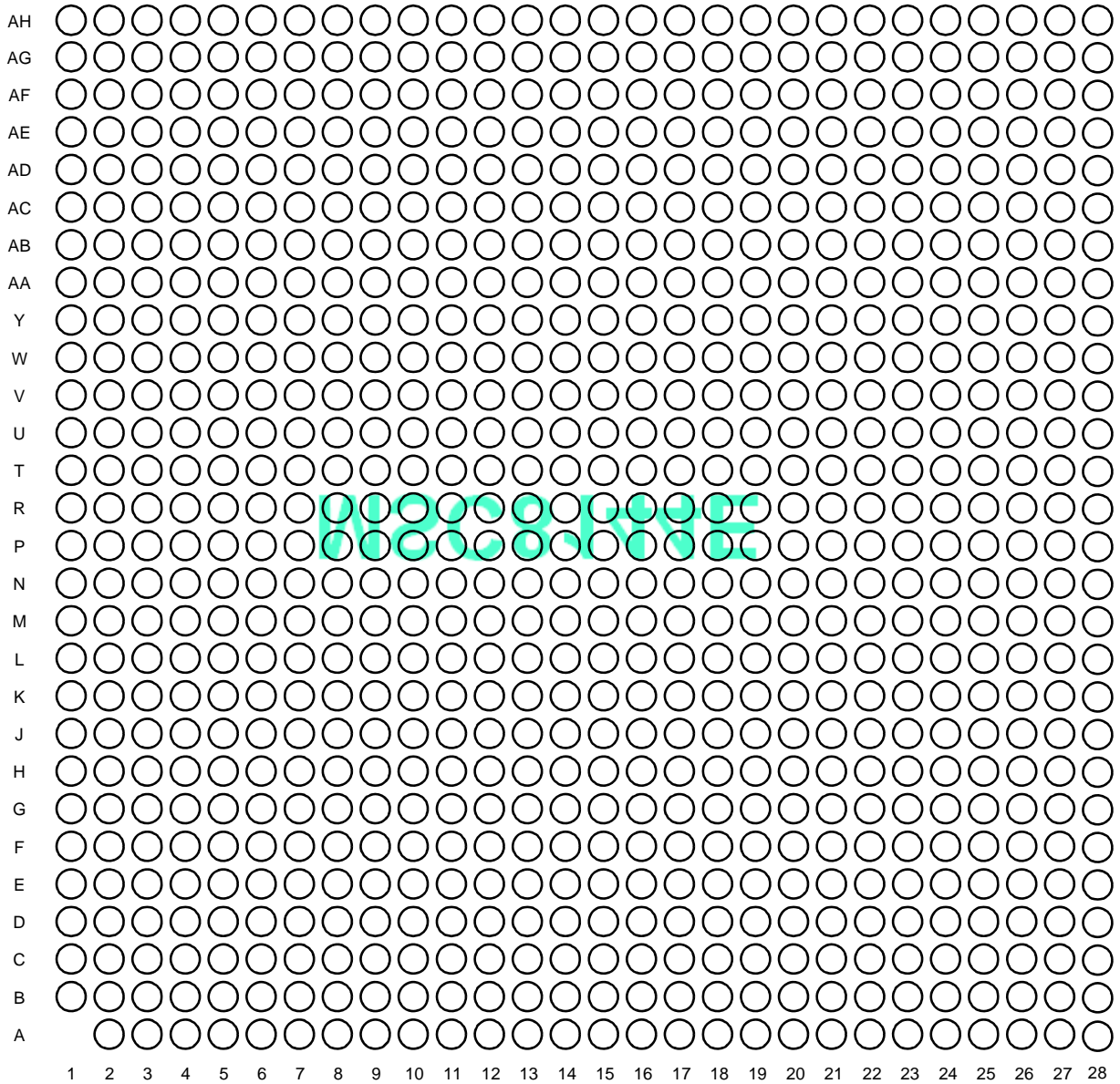


Figure 4. MSC8144E FC-PBGA Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
A2	GND									GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}
A4	V _{DDGE2}									V _{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}
A6	GE2_TD0/PCI_CBE0		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}
A7	SRIO_IMP_CAL_RX									V _{DDSDXC}
A8	Reserved ¹									—
A9	Reserved ¹									—
A10	Reserved ¹									—
A11	Reserved ¹									—
A12	SRIO_RXD0									V _{DDSDXC}
A13	V _{DDSDXC}									V _{DDSDXC}
A14	SRIO_RXD1									V _{DDSDXC}
A15	V _{DDSDXC}									V _{DDSDXC}
A16	SRIO_REF_CLK									V _{DDSDXC}
A17	V _{DDRIOPLL}									GND _{RIOPLL}
A18	GND _{SXC}									GND _{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DDSDXC}
A20	V _{DDSDXC}									V _{DDSDXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DDSDXC}
A22	V _{DDSDXC}									V _{DDSDXC}
A23	SRIO_IMP_CAL_TX									V _{DDSDXP}
A24	MDQ28									V _{DDDDR}
A25	MDQ29									V _{DDDDR}
A26	MDQ30									V _{DDDDR}
A27	MDQ31									V _{DDDDR}
A28	MDQS3									V _{DDDDR}
B1	Reserved ¹									—
B2	GE2_TD1/PCI_CBE1		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}
B3	GE2_TX_EN/PCI_CBE2		Ethernet 2			PCI	Ethernet 2			V _{DDGE2}
B4	GE_MDIO		Ethernet							V _{DDGE2}
B5	GND									GND
B6	GE_MDC		Ethernet							V _{DDGE2}
B7	GND _{SXC}									GND _{SXC}
B8	Reserved ¹									—
B9	Reserved ¹									—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
B10	Reserved ¹									—
B11	Reserved ¹									—
B12	$\overline{\text{SRIO_RXD0}}$									V _{DD} SXC
B13	GND _{SXC}									GND _{SXC}
B14	SRIO_RXD1									V _{DD} SXC
B15	GND _{SXC}									GND _{SXC}
B16	SRIO_REF_CLK									V _{DD} SXC
B17	Reserved ¹									—
B18	V _{DD} SXC									V _{DD} SXC
B19	$\overline{\text{SRIO_RXD2}}/\overline{\text{GE1_SGMII_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXC
B20	GND _{SXC}									GND _{SXC}
B21	$\overline{\text{SRIO_RXD3}}/\overline{\text{GE2_SGMII_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXC
B22	GND _{SXC}									GND _{SXC}
B23	GND _{SXP}									GND _{SXP}
B24	MDQ27									V _{DD} DDR
B25	V _{DD} DDR									V _{DD} DDR
B26	GND									GND
B27	V _{DD} DDR									V _{DD} DDR
B28	MDQS3									V _{DD} DDR
C1	Reserved ¹									—
C2	GE2_RX_CLK/PCI_AD29		Ethernet 2			PCI	Ethernet 2			V _{DD} GE2
C3	V _{DD} GE2									V _{DD} GE2
C4	TDM7RSYN/GE2_TD2/PCI_AD2/UTP_TER		TDM	PCI			Ethernet 2	UTOPIA	V _{DD} GE2	
C5	TDM7RCLK/GE2_RD2/PCI_AD0/UTP_RVL		TDM	PCI			Ethernet 2	UTOPIA	V _{DD} GE2	
C6	V _{DD} GE2									V _{DD} GE2
C7	GE2_RD0/PCI_AD27		Ethernet 2			PCI	Ethernet 2			V _{DD} GE2
C8	Reserved ¹									—
C9	Reserved ¹									—
C10	Reserved ¹									—
C11	Reserved ¹									—
C12	V _{DD} SXP									V _{DD} SXP
C13	$\overline{\text{SRIO_TXD0}}$									V _{DD} SXP
C14	V _{DD} SXP									V _{DD} SXP
C15	$\overline{\text{SRIO_TXD1}}$									V _{DD} SXP
C16	GND _{SXC}									GND _{SXC}
C17	GND _{RIOPLL}									GND _{RIOPLL}
C18	Reserved ¹									—
C19	V _{DD} SXP									V _{DD} SXP
C20	$\overline{\text{SRIO_TXD2}}/\overline{\text{GE1_SGMII_TX}}$		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXP

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply	
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)		7 (111)
C21	V _{DD} SXP										V _{DD} SXP
C22	SRIO_TXD3/GE2_SGMII_T X		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXP	
C23	V _{DD} SXP										V _{DD} SXP
C24	MDQ26										V _{DD} DDR
C25	MDQ25										V _{DD} DDR
C26	MDM3										V _{DD} DDR
C27	GND										GND
C28	MDQ24										V _{DD} DDR
D1	Reserved ¹										—
D2	GE2_RD1/PCI_AD28		Ethernet 2			PCI	Ethernet 2			V _{DD} GE2	
D3	GND										GND
D4	TDM7TDAT/GE2_TD3/ PCI_AD3/UTP_TMD		TDM		PCI		Ethernet 2		UTOPIA	V _{DD} GE2	
D5	TDM7RDAT/GE2_RD3/ PCI_AD1/UTP_STA		TDM		PCI		Ethernet 2		UTOPIA	V _{DD} GE2	
D6	GE1_RD0/UTP_RD2/ PCI_CBE2		UTOPIA	Ethernet 1		PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DD} GE1	
D7	TDM7TCLK/GE2_TCK/ PCI_IDS/UTP_RER		TDM		PCI		Ethernet 2		UTOPIA	V _{DD} GE2	
D8	Reserved ¹										—
D9	Reserved ¹										—
D10	Reserved ¹										—
D11	Reserved ¹										—
D12	GND _{SXP}										GND _{SXP}
D13	SRIO_TXD0										V _{DD} SXP
D14	GND _{SXP}										GND _{SXP}
D15	SRIO_TXD1										V _{DD} SXP
D16	V _{DD} SXC										V _{DD} SXC
D17	Reserved ¹										—
D18	Reserved ¹										—
D19	GND _{SXP}										GND _{SXP}
D20	SRIO_TXD2/GE1_SGMII_T X		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXP	
D21	GND _{SXP}										GND _{SXP}
D22	SRIO_TXD3/GE2_SGMII_T X		SGMII support on SERDES is enabled by Reset Configuration Word							V _{DD} SXP	
D23	GND _{SXP}										GND _{SXP}
D24	MDQ23										V _{DD} DDR
D25	V _{DD} DDR										V _{DD} DDR
D26	MDQ22										V _{DD} DDR
D27	MDQ21										V _{DD} DDR
D28	MDQS2										V _{DD} DDR
E1	Reserved ¹										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E6	V _{DDGE1}								V _{DDGE1}	
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
E8	Reserved ¹								—	
E9	Reserved ¹								—	
E10	GND								GND	
E11	V _{DD}								V _{DD}	
E12	GND								GND	
E13	V _{DD}								V _{DD}	
E14	GND								GND	
E15	V _{DD}								V _{DD}	
E16	GND								GND	
E17	V _{DD}								V _{DD}	
E18	GND								GND	
E19	V _{DD}								V _{DD}	
E20	GND								GND	
E21	V _{DD}								V _{DD}	
E22	GND								GND	
E23	V _{DDDDR}								V _{DDDDR}	
E24	MDQ20								V _{DDDDR}	
E25	GND								GND	
E26	V _{DDDDR}								V _{DDDDR}	
E27	GND								GND	
E28	MDQS2								V _{DDDDR}	
F1	Reserved ¹								—	
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
F3	V _{DDGE1}								V _{DDGE1}	
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
F6	GND								GND	
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
F8	V _{DDGE1}								V _{DDGE1}	
F9	GND								GND	

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
F10	V _{DD}									V _{DD}
F11	GND									GND
F12	V _{DD}									V _{DD}
F13	GND									GND
F14	V _{DD}									V _{DD}
F15	GND									GND
F16	V _{DD}									V _{DD}
F17	GND									GND
F18	V _{DD}									V _{DD}
F19	GND									GND
F20	V _{DD}									V _{DD}
F21	Reserved ¹									—
F22	V _{DDDDR}									V _{DDDDR}
F23	GND									GND
F24	MDQ19									V _{DDDDR}
F25	MDQ18									V _{DDDDR}
F26	MDM2									V _{DDDDR}
F27	MDQ17									V _{DDDDR}
F28	MDQ16									V _{DDDDR}
G1	Reserved ¹									—
G2	$\overline{\text{SRESET}}^4$									V _{DDIO}
G3	GND									GND
G4	$\overline{\text{PORESET}}^4$									V _{DDIO}
G5	GE1_COL/UTP_RD1		UTOPIA	Ethernet 1	UTOPIA		Ethernet 1	UTOPIA	V _{DDIO}	
G6	GE1_TD2/UTP_TD4/ PCI_AD29		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
G7	GE1_RX_DV/UTP_RD7		UTOPIA	Ethernet 1	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}	
G8	GE1_TX_ER/UTP_TD7/ PCI_CBE1		UTOPIA	Ethernet 1	PCI	UTOPIA	Ethernet 1	UTOPIA	V _{DDGE1}	
G9	V _{DD}									V _{DD}
G10	GND									GND
G11	V _{DD}									V _{DD}
G12	GND									GND
G13	V _{DD}									V _{DD}
G14	GND									GND
G15	V _{DD}									V _{DD}
G16	GND									GND
G17	V _{DD}									V _{DD}
G18	GND									GND
G19	V _{DD}									V _{DD}
G20	GND									GND
G21	Reserved ¹	—								—
G22	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
G23	MBA1									V _{DDDDR}
G24	MA3									V _{DDDDR}
G25	MA8									V _{DDDDR}
G26	V _{DDDDR}									V _{DDDDR}
G27	GND									GND
G28	$\overline{\text{MCK0}}$									V _{DDDDR}
H1	Reserved ¹									—
H2	CLKIN									V _{DDIO}
H3	$\overline{\text{HRESET}}$									V _{DDIO}
H4	PCI_CLK_IN									V _{DDIO}
H5	NMI									V _{DDIO}
H6	URXD/GPIO14/ $\overline{\text{IRQ8}}$ / RC_LDF ^{3, 6}	$\overline{\text{RC_LDF}}$	UART/GPIO/IRQ							V _{DDIO}
H7	GE1_RX_ER/PCI_AD6/ GPIO25/ $\overline{\text{IRQ15}}$ ^{3, 6}		GPIO/ IRQ	Ethernet 1	PCI		GPIO/ IRQ	Ethernet 1		V _{DDIO}
H8	GE1_CRSS/PCI_AD5		PCI	Ethernet 1	PCI		Ethernet 1		V _{DDIO}	
H9	GND									GND
H10	V _{DD}									V _{DD}
H11	GND									GND
H12	V _{DD}									V _{DD}
H13	GND									GND
H14	V _{DD}									V _{DD}
H15	V _{DD}									V _{DD}
H16	V _{DD}									V _{DD}
H17	GND									GND
H18	V _{DD}									V _{DD}
H19	GND									GND
H20	V _{DD}									V _{DD}
H21	V _{DD}									V _{DD}
H22	V _{DDDDR}									V _{DDDDR}
H23	MBA0									V _{DDDDR}
H24	MA15									V _{DDDDR}
H25	V _{DDDDR}									V _{DDDDR}
H26	MA9									V _{DDDDR}
H27	MA7									V _{DDDDR}
H28	MCK0									V _{DDDDR}
J1	Reserved ¹									—
J2	GND									GND
J3	V _{DDIO}									V _{DDIO}
J4	STOP_BS									V _{DDIO}
J5	$\overline{\text{NMI_OUT}}$ ⁴									V _{DDIO}
J6	$\overline{\text{INT_OUT}}$ ⁴									V _{DDIO}
J7	SDA/GPIO27 ^{3, 4, 6}		I2C/GPIO							V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
J8	VDDIO									VDDIO
J9	VDD									VDD
J10	GND									GND
J11	VDD									VDD
J12	GND									GND
J13	VDD									VDD
J14	GND									GND
J15	GND									GND
J16	GND									GND
J17	VDD									VDD
J18	GND									GND
J19	VDD									VDD
J20	GND									GND
J21	GND									GND
J22	GND									GND
J23	GND									GND
J24	VDDDDR									VDDDDR
J25	GND									GND
J26	VDDDDR									VDDDDR
J27	GND									GND
J28	VDDDDR									VDDDDR
K1	Reserved ¹									—
K2	Reserved ¹									—
K3	Reserved ¹									—
K4	Reserved ¹									—
K5	VDDPLL2A									VDDPLL2A
K6	GND									GND
K7	VDDPLL0A									VDDPLL0A
K8	VDDPLL1A									VDDPLL1A
K9	VDD									VDD
K10	GND									GND
K11	VDD									VDD
K12	GND									GND
K13	VDD									VDD
K14	VDD									VDD
K15	VDD									VDD
K16	VDD									VDD
K17	VDD									VDD
K18	GND									GND
K19	VDD									VDD
K20	GND									GND
K21	VDD									VDD
K22	VDDDDR									VDDDDR

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply	
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)		7 (111)
K23	MBA2										V _{DDDDR}
K24	MA10										V _{DDDDR}
K25	MA12										V _{DDDDR}
K26	MA14										V _{DDDDR}
K27	MA4										V _{DDDDR}
K28	MV _{REF}										V _{DDDDR}
L1	Reserved ¹										—
L2	CLKOUT										V _{DDIO}
L3	TMR1/UTP_IR/PCI_CBE3/ GPIO17 ^{3, 6}		UTOPIA	TMR/ GPIO	UTOPIA	PCI	UTOPIA			V _{DDIO}	
L4	TMR4/PCI_PAR/GPIO20 ^{3, 6} / UTP_REOP		TIMER/GPIO			PCI	TIMER/GPIO			V _{DDIO}	
L5	GND										GND
L6	TMR2/PCI_FRAME/ GPIO18 ^{3, 6}		TIMER/GPIO			PCI	TIMER/GPIO	UTOPIA		V _{DDIO}	
L7	SCL/GPIO26 ^{3, 4, 6}		I ² C/GPIO							V _{DDIO}	
L8	UTXD/GPIO15/IRQ ^{3, 6}		UART/GPIO/IRQ							V _{DDIO}	
L9	GND										GND
L10	V _{DD}										V _{DD}
L11	GND										GND
L12	V _{DD}										V _{DD}
L13	GND										GND
L14	V _{DD}										V _{DD}
L15	Reserved ¹										GND
L16	V _{DD}										V _{DD}
L17	GND										GND
L18	V _{DD}										V _{DD}
L19	GND										GND
L20	V _{DD}										V _{DD}
L21	GND										GND
L22	GND										GND
L23	MCKE1										V _{DDDDR}
L24	MA1										V _{DDDDR}
L25	V _{DDDDR}										V _{DDDDR}
L26	GND										GND
L27	V _{DDDDR}										V _{DDDDR}
L28	MCK1										V _{DDDDR}
M1	Reserved ¹										—
M2	TRST										V _{DDIO}
M3	EE0										V _{DDIO}
M4	EE1										V _{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA	PCI	UTOPIA					V _{DDIO}	
M6	UTP_RADDR0/PCI_AD7		UTOPIA	PCI	UTOPIA					V _{DDIO}	
M7	UTP_TD8/PCI_AD30		UTOPIA	PCI	UTOPIA					V _{DDIO}	

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
M8	V _{DDIO}									V _{DDIO}
M9	V _{DD}									V _{DD}
M10	GND									GND
M11	V _{DD}									V _{DD}
M12	GND									GND
M13	V _{DD}									V _{DD}
M14	GND									GND
M15	V _{DD}									V _{DD}
M16	GND									GND
M17	V _{DD}									V _{DD}
M18	GND									GND
M19	V _{DD}									V _{DD}
M20	GND									GND
M21	V _{DD}									V _{DD}
M22	V _{DDDDR}									V _{DDDDR}
M23	MCS1									V _{DDDDR}
M24	MA13									V _{DDDDR}
M25	MA2									V _{DDDDR}
M26	MA0									V _{DDDDR}
M27	GND									GND
M28	MCK1									V _{DDDDR}
N1	Reserved ¹									—
N2	V _{DDIO}									V _{DDIO}
N3	TMS									V _{DDIO}
N4	UTP_RD10/PCI_AD14 ⁵		UTOPIA	PCI	UTOPIA				V _{DDIO}	
N5	V _{DDIO}		Power						V _{DDIO}	
N6	UTP_RADDR1/PCI_AD8		UTOPIA	PCI	UTOPIA				V _{DDIO}	
N7	UTP_TD9/PCI_AD31		UTOPIA	PCI	UTOPIA				V _{DDIO}	
N8	TMR3/PCI_IRDY/GPIO19 ^{3,6} /UTP_TEOP		TIMER/GPIO			PCI	TIMER/GPIO	UTOPIA	V _{DDIO}	
N9	GND									GND
N10	V _{DDM3}									V _{DDM3}
N11	V _{DD}									V _{DD}
N12	V _{DDM3}									V _{DDM3}
N13	V _{DD}									V _{DD}
N14	V _{DDM3}									V _{DDM3}
N15	V _{DD}									V _{DD}
N16	V _{DDM3}									V _{DDM3}
N17	V _{DD}									V _{DD}
N18	V _{DDM3}									V _{DDM3}
N19	V _{DD}									V _{DD}
N20	V _{DDM3}									V _{DDM3}
N21	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply	
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)		7 (111)
N22	GND										GND
N23	MODT1										V _{DDDDR}
N24	MCKE0										V _{DDDDR}
N25	V _{DDDDR}										V _{DDDDR}
N26	MA5										V _{DDDDR}
N27	MA6										V _{DDDDR}
N28	MA11										V _{DDDDR}
P1	Reserved ¹										—
P2	TDI ⁵										V _{DDIO}
P3	UTP_RD11/PCI_AD15		UTOPIA		PCI	UTOPIA				V _{DDIO}	
P4	GND										GND
P5	UTP_RADDR3/PCI_AD10		UTOPIA		PCI	UTOPIA				V _{DDIO}	
P6	UTP_RADDR2/PCI_AD9		UTOPIA		PCI	UTOPIA				V _{DDIO}	
P7	PCI_GNT/GPIO29/IRQ7 ^{3, 6}		GPIO/IRQ		PCI		GPIO/IRQ			V _{DDIO}	
P8	PCI_STOP/GPIO30/IRQ2 ^{3, 6}		GPIO/IRQ		PCI		GPIO/IRQ			V _{DDIO}	
P9	GND										GND
P10	GND										GND
P11	V _{DDM3}										V _{DDM3}
P12	GND										GND
P13	V _{DDM3}										V _{DDM3}
P14	GND										GND
P15	V _{DDM3}										V _{DDM3}
P16	GND										GND
P17	V _{DDM3}										V _{DDM3}
P18	GND										GND
P19	V _{DDM3}										V _{DDM3}
P20	GND										GND
P21	GND										GND
P22	V _{DDDDR}										V _{DDDDR}
P23	MCS0										V _{DDDDR}
P24	MRAS										V _{DDDDR}
P25	GND										GND
P26	V _{DDDDR}										V _{DDDDR}
P27	GND										GND
P28	MCK2										V _{DDDDR}
R1	Reserved ¹										—
R2	TCK										V _{DDIO}
R3	TDO										V _{DDIO}
R4	UTP_RD12/PCI_AD16		UTOPIA		PCI	UTOPIA				V _{DDIO}	
R5	UTP_RCLAV_PDRPA/PCI_AD12		UTOPIA		PCI	UTOPIA				V _{DDIO}	
R6	UTP_RADDR4/PCI_AD11		UTOPIA		PCI	UTOPIA				V _{DDIO}	

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
R7	V _{DDIO}									V _{DDIO}
R8	PCI_REQ		PCI							V _{DDIO}
R9	GND									GND
R10	GND									GND
R11	GND									GND
R12	GND									GND
R13	GND									GND
R14	GND									GND
R15	GND									GND
R16	GND									GND
R17	GND									GND
R18	GND									GND
R19	GND									GND
R20	GND									GND
R21	GND									GND
R22	GND									GND
R23	MODT0									V _{DDDDR}
R24	MDIC1									V _{DDDDR}
R25	MDIC0									V _{DDDDR}
R26	MCAS									V _{DDDDR}
R27	$\overline{\text{MWE}}$									V _{DDDDR}
R28	MCK2									V _{DDDDR}
T1	Reserved ¹									—
T2	UTP_RPRTY/PCI_AD21		UTOPIA	PCI	UTOPIA				V _{DDIO}	
T3	UTP_RD13/PCI_AD17		UTOPIA	PCI	UTOPIA				V _{DDIO}	
T4	V _{DDIO}									V _{DDIO}
T5	UTP_RD14/PCI_AD18		UTOPIA	PCI	UTOPIA				V _{DDIO}	
T6	UTP_RD15/PCI_AD19		UTOPIA	PCI	UTOPIA				V _{DDIO}	
T7	PCI_TRDY		PCI							V _{DDIO}
T8	$\overline{\text{PCI_DEVSEL}}$ /GPIO31/ IRQ ^{3, 6}		GPIO/IRQ		PCI		GPIO/IRQ			V _{DDIO}
T9	GND									GND
T10	GND									GND
T11	GND									GND
T12	GND									GND
T13	GND									GND
T14	GND									GND
T15	GND									GND
T16	GND									GND
T17	GND									GND
T18	GND									GND
T19	GND									GND
T20	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
T21	GND									GND
T22	V _{DDDDR}									V _{DDDDR}
T23	GND									GND
T24	V _{DDDDR}									V _{DDDDR}
T25	GND									GND
T26	V _{DDDDR}									V _{DDDDR}
T27	GND									GND
T28	V _{DDDDR}									V _{DDDDR}
U1	Reserved ¹									—
U2	UTP_TCLK/PCI_AD29		UTOPIA	PCI	UTOPIA					V _{DDIO}
U3	UTP_TADDR4/PCI_AD27		UTOPIA	PCI	UTOPIA					V _{DDIO}
U4	UTP_TADDR2		UTOPIA							V _{DDIO}
U5	GND									GND
U6	UTP_REN/PCI_AD20		UTOPIA	PCI	UTOPIA					V _{DDIO}
U7	PCI_AD26		PCI							V _{DDIO}
U8	PCI_AD25		PCI							V _{DDIO}
U9	Reserved ¹									V _{DDIO}
U10	V _{D_{DM3}}									V _{D_{DM3}}
U11	GND									GND
U12	V _{D_{DM3}}									V _{D_{DM3}}
U13	GND									GND
U14	V _{D_{DM3}}									V _{D_{DM3}}
U15	GND									GND
U16	V _{D_{DM3}}									V _{D_{DM3}}
U17	GND									GND
U18	V _{D_{DM3}}									V _{D_{DM3}}
U19	GND									GND
U20	V _{D_{DM3}}									V _{D_{DM3}}
U21	GND									GND
U22	GND									GND
U23	MDQ7									V _{DDDDR}
U24	MDQ3									V _{DDDDR}
U25	MDQ4									V _{DDDDR}
U26	MDQ5									V _{DDDDR}
U27	MDQ1									V _{DDDDR}
U28	MDQ0									V _{DDDDR}
V1	Reserved ¹									—
V2	UTP_TD10/PCI_CBE0		UTOPIA	PCI	UTOPIA					V _{DDIO}
V3	UTP_TADDR3		UTOPIA							V _{DDIO}
V4	UTP_TD11/PCI_PERR		UTOPIA	PCI	UTOPIA					V _{DDIO}
V5	UTP_TADDR0/PCI_AD23		UTOPIA	PCI	UTOPIA					V _{DDIO}
V6	UTP_TADDR1/PCI_AD24		UTOPIA	PCI	UTOPIA					V _{DDIO}
V7	UTP_TCLAV/PCI_AD28		UTOPIA	PCI	UTOPIA					V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
V8	VDDIO									VDDIO
V9	Reserved ¹									VDDIO
V10	GND									GND
V11	VDDM3									VDDM3
V12	GND									GND
V13	VDDM3									VDDM3
V14	GND									GND
V15	VDDM3									VDDM3
V16	GND									GND
V17	VDDM3									VDDM3
V18	GND									GND
V19	VDDM3									VDDM3
V20	GND									GND
V21	GND									GND
V22	VDDDDR									VDDDDR
V23	MDQ2									VDDDDR
V24	VDDDDR									VDDDDR
V25	MDQ6									VDDDDR
V26	GND									GND
V27	VDDDDR									VDDDDR
V28	MDQS0									VDDDDR
W1	Reserved ¹									—
W2	UTP_TD12/ <u>PCI_CBE2</u>		UTOPIA	PCI	UTOPIA				VDDIO	
W3	UTP_TD11/ <u>PCI_CBE1</u>		UTOPIA	PCI	UTOPIA				VDDIO	
W4	VDDIO									VDDIO
W5	GND									GND
W6	UTP_TD15/ <u>PCI_IRDY</u>		UTOPIA	PCI	UTOPIA				VDDIO	
W7	UTP_TD0/ <u>PCI_SERR</u>		UTOPIA	PCI	UTOPIA				VDDIO	
W8	UTP_RSOC/ <u>PCI_AD22</u>		UTOPIA	PCI	UTOPIA				VDDIO	
W9	Reserved ¹									VDDIO
W10	VDDM3									VDDM3
W11	GND									GND
W12	V _{25M3}									V _{25M3}
W13	GND									GND
W14	VDDM3									VDDM3
W15	V _{25M3}									V _{25M3}
W16	VDDM3									VDDM3
W17	GND									GND
W18	V _{25M3}									V _{25M3}
W19	GND									GND
W20	VDDM3									VDDM3
W21	GND									GND
W22	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
W23	MDQ10									VDDDDR
W24	GND									GND
W25	MDQ11									VDDDDR
W26	MDM0									VDDDDR
W27	GND									GND
W28	MDQS0									VDDDDR
Y1	Reserved ¹									-
Y2	UTP_TD14/PCI_FRAME		UTOPIA	PCI	UTOPIA					VDDIO
Y3	TDM5TSYN/PCI_AD18/ GPIO12 ^{3,6}		TDM/GPIO		PCI	TDM/GPIO				VDDIO
Y4	TDM5TCLK/PCI_AD16		TDM		PCI	TDM				VDDIO
Y5	TDM4RCLK/PCI_AD7		TDM		PCI	TDM				VDDIO
Y6	TDM4TSYN/PCI_AD12		TDM		PCI	TDM				VDDIO
Y7	UTP_TPRTY/RC14	RC14	UTOPIA							VDDIO
Y8	UTP_TEN/PCI_PAR		UTOPIA	PCI	UTOPIA				VDDIO	
Y9	Reserved ¹									VDDIO
Y10	GND									GND
Y11	VDDM3									VDDM3
Y12	GND									GND
Y13	VDDM3									VDDM3
Y14	GND									GND
Y15	VDDM3									VDDM3
Y16	GND									GND
Y17	VDDM3									VDDM3
Y18	GND									GND
Y19	VDDM3									VDDM3
Y20	GND									GND
Y21	GND									GND
Y22	VDDDDR									VDDDDR
Y23	MDQ13									VDDDDR
Y24	VDDDDR									VDDDDR
Y25	GND									GND
Y26	MDQ9									VDDDDR
Y27	VDDDDR									VDDDDR
Y28	MDQ8									VDDDDR
AA1	Reserved ¹									—
AA2	UTP_TD13/PCI_CBE3		UTOPIA	PCI	UTOPIA				VDDIO	
AA3	TDM5RSYN/PCI_AD15/ GPIO10 ^{3,6}		TDM/GPIO		PCI	TDM/GPIO			VDDIO	
AA4	TDM5TDAT, AT/PCI_AD17/ GPIO11 ⁶		TDM/GPIO		PCI	TDM/GPIO			VDDIO	
AA5	TDM5RCLK/PCI_AD13/ GPIO28 ^{3,6}		TDM/GPIO		PCI	TDM/GPIO			VDDIO	
AA6	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AA7	TDM4TCLK/PCI_AD10		TDM			PCI	TDM			V _{DDIO}
AA8	TDM4TDAT/PCI_AD11		TDM			PCI	TDM			V _{DDIO}
AA9	V _{DDIO}									V _{DDIO}
AA10	V _{DDM3}									V _{DDM3}
AA11	GND									GND
AA12	V _{DDM3}									V _{DDM3}
AA13	GND									GND
AA14	V _{DDM3}									V _{DDM3}
AA15	GND									GND
AA16	V _{DDM3}									V _{DDM3}
AA17	GND									GND
AA18	V _{DDM3}									V _{DDM3}
AA19	GND									GND
AA20	V _{DDM3}									V _{DDM3}
AA21	GND									GND
AA22	GND									GND
AA23	MDQ15									V _{DDDDR}
AA24	MDQ14									V _{DDDDR}
AA25	MDM1									V _{DDDDR}
AA26	MDQ12									V _{DDDDR}
AA27	MDQS ¹									V _{DDDDR}
AA28	MDQS1									V _{DDDDR}
AB1	Reserved ¹									-
AB2	UTP_TSOC/RC15	RC15	UTOPIA							V _{DDIO}
AB3	V _{DDIO}									V _{DDIO}
AB4	TDM6RDAT/PCI_AD20/ GPIO5/IRQ11 ^{3, 6}		TDM/GPIO/IRQ			PCI	TDM/GPIO/IRQ			V _{DDIO}
AB5	TDM5RDAT/PCI_AD14/ GPIO9 ^{3, 6}		TDM/GPIO			PCI	TDM/GPIO			V _{DDIO}
AB6	TDM6TSYN/PCI_AD24/ GPIO8/IRQ14 ^{3, 6}		TDM/GPIO/IRQ			PCI	TDM/GPIO/IRQ			V _{DDIO}
AB7	TDM6RCLK/PCI_AD19/ GPIO4/IRQ10 ^{3, 6}		TDM/GPIO/IRQ			PCI	TDM/GPIO/IRQ			V _{DDIO}
AB8	TDM4RSYN/PCI_AD9		TDM			PCI	TDM			V _{DDIO}
AB9	TDM4RDAT/PCI_AD8		TDM			PCI	TDM			V _{DDIO}
AB10	GND									GND
AB11	V _{DDM3}									V _{DDM3}
AB12	GND									GND
AB13	V _{DDM3}									V _{DDM3}
AB14	GND									GND
AB15	V _{DDM3}									V _{DDM3}
AB16	GND									GND
AB17	V _{DDM3}									V _{DDM3}
AB18	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AB19	V _{DDM3}									V _{DDM3}
AB20	GND									GND
AB21	GND									GND
AB22	V _{DDDDR}									V _{DDDDR}
AB23	MECC7									V _{DDDDR}
AB24	MECC1									V _{DDDDR}
AB25	MECC4									V _{DDDDR}
AB26	MECC5									V _{DDDDR}
AB27	MECC2									V _{DDDDR}
AB28	ECC_MDQS									V _{DDDDR}
AC1	Reserved ¹									—
AC2	UTP_RD9/RC13	RC13	UTOPIA							V _{DDIO}
AC3	UTP_RD8/RC12	RC12	UTOPIA							V _{DDIO}
AC4	TDM6TCLK/PCI_AD22		TDM		PCI		TDM			V _{DDIO}
AC5	TDM6RSYN/PCI_AD21/ GPIO6/IRQ12 ^{3, 6}		TDM/GPIO/IRQ		PCI		TDM/GPIO/IRQ			V _{DDIO}
AC6	V _{DDIO}									V _{DDIO}
AC7	TDM3TSYN/RC11	RC11	TDM							V _{DDIO}
AC8	PCI_AD23/GPIO7/IRQ13/ TDM6TDAT ^{3, 6} /UTP_RMOD		TDM/GPIO/IRQ		PCI		TDM/GPIO/IRQ		UTOPIA	V _{DDIO}
AC9	TDM7TSYN/PCI_AD4		TDM		PCI		reserved			V _{DDIO}
AC10	V _{DDM3IO}									V _{DDM3IO}
AC11	GND									GND
AC12	V _{DDM3}									V _{DDM3}
AC13	GND									GND
AC14	V _{DDM3}									V _{DDM3}
AC15	GND									GND
AC16	V _{DDM3}									V _{DDM3}
AC17	GND									GND
AC18	V _{DDM3}									V _{DDM3}
AC19	GND									GND
AC20	V _{DDM3IO}									V _{DDM3IO}
AC21	Reserved ¹									—
AC22	MECC6									V _{DDDDR}
AC23	MECC3									V _{DDDDR}
AC24	ECC_MDM									V _{DDDDR}
AC25	V _{DDDDR}									V _{DDDDR}
AC26	MECC0									V _{DDDDR}
AC27	V _{DDDDR}									V _{DDDDR}
AC28	ECC_MDQS									V _{DDDDR}
AD1	Reserved ¹									—
AD2	GPIO1 ^{3, 6}		GPIO							V _{DDIO}
AD3	TMR0/GPIO13		TIMER/GPIO							V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AD4	GPIO2 ^{3, 6}		GPIO							V _{DDIO}
AD5	GND									GND
AD6	TDM1TCLK		TDM							V _{DDIO}
AD7	TDM3TDAT/RC10	RC10	TDM							V _{DDIO}
AD8	TDM3RSYN/RC9	RC9	TDM							V _{DDIO}
AD9	TDM3RDAT/RC8	RC8	TDM							V _{DDIO}
AD10	GND									GND
AD11	V _{25M3}									V _{25M3}
AD12	GND									GND
AD13	V _{DDM3}									V _{DDM3}
AD14	GND									GND
AD15	V _{25M3}									V _{25M3}
AD16	GND									GND
AD17	V _{DDM3}									V _{DDM3}
AD18	GND									GND
AD19	V _{25M3}									V _{25M3}
AD20	GND									GND
AD21	Reserved ¹									—
AD22	V _{DDDDR}									V _{DDDDR}
AD23	GND									GND
AD24	V _{DDDDR}									V _{DDDDR}
AD25	GND									GND
AD26	V _{DDDDR}									V _{DDDDR}
AD27	GND									GND
AD28	V _{DDDDR}									V _{DDDDR}
AE1	Reserved ¹									—
AE2	GPIO0 ^{3, 6}		GPIO							V _{DDIO}
AE3	GPIO3 ^{3, 6}		GPIO							V _{DDIO}
AE4	TDM1RCLK		TDM							V _{DDIO}
AE5	TDM1TSYN/RC3	RC3	TDM							V _{DDIO}
AE6	TDM1TDAT/RC2	RC2	TDM							V _{DDIO}
AE7	TDM1RSYN/RC1	RC1	TDM							V _{DDIO}
AE8	TDM3RCLK/RC16	RC16	TDM							V _{DDIO}
AE9	TDM3TCLK		TDM							V _{DDIO}
AE10	TDM2TDAT/RC6	RC6	TDM							V _{DDIO}
AE11	GPIO21/ $\overline{\text{IRQ1}}$ ^{3, 6} /SPICKL		GPIO/IRQ/SPI							V _{DDIO}
AE12	GND									GND
AE13	Reserved ¹									—
AE14	GND									GND
AE15	Reserved ¹									—
AE16	Reserved ¹									—
AE17	Reserved ¹									—
AE18	GND									GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AE19	GND									GND
AE20	V _{DDM3IO}									V _{DDM3IO}
AE21	Reserved ¹									—
AE22	GND									GND
AE23	GND									GND
AE24	GND									GND
AE25	V _{DDDDR}									V _{DDDDR}
AE26	GND									GND
AE27	V _{DDDDR}									V _{DDDDR}
AE28	GND									GND
AF1	Reserved ¹									—
AF2	V _{DDIO}									V _{DDIO}
AF3	GND									GND
AF4	TDM0RDAT/ RCFG_CLKIN_RNG	RCFG_ CLKIN_ RNG	TDM							V _{DDIO}
AF5	TDM0TSYN/RCW_SRC2	RCW_ SRC2	TDM							V _{DDIO}
AF6	TDM1RDAT/RC0	RC0	TDM							V _{DDIO}
AF7	V _{DDIO}									V _{DDIO}
AF8	GND									GND
AF9	TDM2RDAT/RC4	RC4	TDM							V _{DDIO}
AF10	TDM2TCLK		TDM							V _{DDIO}
AF11	GPIO22/ $\overline{\text{IRQ}}4^{3, 6}$ /SPIMOSI		GPIO/IRQ/SPI							V _{DDIO}
AF12	GND									GND
AF13	GND									GND
AF14	V _{DDM3IO}									V _{DDM3IO}
AF15	GND									GND
AF16	GND									GND
AF17	Reserved ¹									—
AF18	V _{DDM3IO}									V _{DDM3IO}
AF19	GND									GND
AF20	Reserved ¹									—
AF21	Reserved ¹									—
AF22	$\overline{\text{M3_RESET}}$									V _{DDM3IO}
AF23	GND									GND
AF24	V _{DDDDR}									V _{DDDDR}
AF25	GND									GND
AF26	V _{DDDDR}									V _{DDDDR}
AF27	GND									GND
AF28	V _{DDDDR}									V _{DDDDR}
AG1	Reserved ¹									—
AG2	GPIO16/ $\overline{\text{IRQ}}0^{3, 6}$		GPIO/IRQ							V _{DDIO}
AG3	TDM0TCLK		TDM							V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	
AG4	TDM0RSYN/RCW_SRC0	RCW_SRC0	TDM							V _{DDIO}
AG5	TDM0RCLK		TDM							V _{DDIO}
AG6	TDM0TDAT/RCW_SRC1	RCW_SRC1	TDM							V _{DDIO}
AG7	TDM2TSYN/RC7	RC7	TDM							V _{DDIO}
AG8	TDM2RCLK		TDM							V _{DDIO}
AG9	TDM2RSYN/RC5	RC5	TDM							V _{DDIO}
AG10	GPIO24/IRQ6 ^{3, 6} /SPISEL		GPIO/IRQ/SPI							V _{DDIO}
AG11	GPIO23/IRQ5 ^{3, 6} /SPIMISO		GPIO/IRQ/SPI							V _{DDIO}
AG12	Reserved ¹									—
AG13	GND									GND
AG14	GND									GND
AG15	GND									GND
AG16	GND									GND
AG17	Reserved ¹									—
AG18	Reserved ¹									—
AG19	GND									GND
AG20	GND									GND
AG21	V _{DDM3IO}									V _{DDM3IO}
AG22	GND									GND
AG23	GND									GND
AG24	GND									GND
AG25	V _{DDDDR}									V _{DDDDR}
AG26	GND									GND
AG27	V _{DDDDR}									V _{DDDDR}
AG28	GND									GND
AH1	Reserved ¹									—
AH2	Reserved ¹									—
AH3	Reserved ¹									—
AH4	Reserved ¹									—
AH5	Reserved ¹									—
AH6	Reserved ¹									—
AH7	Reserved ¹									—
AH8	Reserved ¹									—
AH9	Reserved ¹									—
AH10	Reserved ¹									—
AH11	Reserved ¹									—
AH12	Reserved ¹									—
AH13	Reserved ¹									—
AH14	Reserved ¹									—
AH15	Reserved ¹									—
AH16	Reserved ¹									—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²							Ref. Supply	
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)		7 (111)
AH17	Reserved ¹										—
AH18	Reserved ¹										—
AH19	Reserved ¹										—
AH20	Reserved ¹										—
AH21	Reserved ¹										—
AH22	Reserved ¹										—
AH23	Reserved ¹										—
AH24	Reserved ¹										—
AH25	Reserved ¹										—
AH26	Reserved ¹										—
AH27	Reserved ¹										—
AH28	Reserved ¹										—

Notes:

1. Reserved signals should be disconnected for compatibility with future revisions of the device.
2. For signals with same functionality in all modes the appropriate cells are empty.
3. The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see **Chapter 23, GPIO** in the *MSC8144E Reference Manual*.
4. Open-drain signal.
5. Internal 20 K Ω pull-up resistor.
6. For signals with GPIO functionality, the open-drain and internal 20 K Ω pull-up resistor can be configured by GPIO register programming. See **Chapter 23, GPIO** of the *MSC8144E Reference Manual* for configuration details.

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8144E Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8144E.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{dd}	-0.3 to 1.1	V
PLL supply voltage ³	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	-0.3 to 1.1	V
M3 memory Internal voltage	V_{DDM3}	-0.3 to 1.32	V
DDR memory supply voltage	V_{DDDDR}	-0.3 to 2.75 -0.3 to 1.98	V V
• DDR mode			
• DDR2 mode			
DDR reference voltage	MV_{REF}	-0.3 to $0.51 \times V_{DDDDR}$	V
Input DDR voltage	V_{INDDR}	-0.3 to $V_{DDDDR} + 0.3$	V
Ethernet 1 I/O voltage	V_{DDGE1}	-0.3 to 3.465	V
Input Ethernet 1 I/O voltage	V_{INGE1}	-0.3 to $V_{DDGE1} + 0.3$	V
Ethernet 2 I/O voltage	V_{DDGE2}	-0.3 to 3.465	V
Input Ethernet 2 I/O voltage	V_{INGE2}	-0.3 to $V_{DDGE2} + 0.3$	V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	-0.3 to 3.465	V
Input I/O voltage	V_{INIO}	-0.3 to $V_{DDIO} + 0.3$	V

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
M3 memory I/O and M3 memory charge pump voltage	V_{DDM3IO} V_{25M3}	-0.3 to 2.75	V
Input M3 memory I/O voltage	V_{INM3IO}	-0.3 to $V_{DDM3IO} + 0.3$	V
Rapid I/O C voltage	V_{DDSXC}	-0.3 to 1.21	V
Rapid I/O P voltage	V_{DSDXP}	-0.3 to 1.26	V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	-0.3 to 1.21	V
Operating temperature	T_J	-40 to 105	°C
Storage temperature range	T_{STG}	-55 to +150	°C
Notes: <ol style="list-style-type: none"> Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage. PLL supply voltage is specified at input of the filter and not at pin of the MSC8144E (see Figure 43) 			

2.2 Recommended Operating Conditions

[Table 3](#) lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage	V_{DD}				
• 800 MHz (VT, SVT, TVT) and 1000 MHz (VT)		0.97	1.0	1.05	V
• 1000 MHz (SVT, TVT)		0.97	1.0	1.03	V
PLL supply voltage	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}				
• 800 MHz (VT, SVT, TVT) and 1000 MHz (VT)		0.97	1.0	1.05	V
• 1000 MHz (SVT, TVT)		0.97	1.0	1.03	V
M3 memory Internal voltage	V_{DDM3}	1.213	1.25	1.313	V
DDR memory supply voltage	V_{DDDDR}				
• DDR mode		2.375	2.5	2.625	V
• DDR2 mode		1.71	1.8	1.89	V
DDR reference voltage	MV_{REF}	$0.49 \times V_{DDDDR}$ (nom)	$0.5 \times V_{DDDDR}$ (nom)	$0.51 \times V_{DDDDR}$ (nom)	V
Ethernet 1 I/O voltage	V_{DDGE1}				
• 2.5 V mode		2.375	2.5	2.625	V
• 3.3 V mode		3.135	3.3	3.465	V
Ethernet 2 I/O voltage	V_{DDGE2}				
• 2.5 V mode		2.375	2.5	2.625	V
• 3.3 V mode		3.135	3.3	3.465	V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	3.135	3.3	3.465	V
M3 memory I/O and M3 charge pump voltage	V_{DDM3IO} V_{25M3}	2.375	2.5	2.625	V
Rapid I/O C voltage	V_{DDSXC}	0.97	1.0	1.05	V
Rapid I/O P voltage	V_{DSDXP}				
• Short run (haul) mode		0.97	1.0	1.05	V
• Long run (haul) mode		1.14	1.2	1.26	V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	0.97	1.0	1.05	V
Operating temperature range:					
• Standard (VT)	T_J	0		90	°C
• Intermediate (SVT)	T_J	0		105	°C
• Extended (TVT)	T_A	-40		—	°C
	T_J	—		105	°C
Note: PLL supply voltage is specified at input of the filter and not at pin of the MSC8144E (see Figure 43).					

2.3 Default Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths.

Table 4. Output Drive Impedance

Driver Type	Output Impedance (Ω)
DDR signal	18
DDR2 signal	18 35 (half strength mode)

2.4 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8144E for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8144E

Characteristic	Symbol	FC-PBGA 29 × 29 mm ⁵		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient ^{1, 2}	$R_{\theta JA}$	20	15	°C/W
Junction-to-ambient, four-layer board ^{1, 3}	$R_{\theta JA}$	15	12	°C/W
Junction-to-board (bottom) ⁴	$R_{\theta JB}$	7		°C/W
Junction-to-case ⁵	$R_{\theta JC}$	0.8		°C/W
Notes: <ol style="list-style-type: none"> Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. 				

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8144E.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8144E.

Note: DDR SDRAM uses $V_{DDDDR}(typ) = 2.5\text{ V}$ and DDR2 SDRAM uses $V_{DDDDR}(typ) = 1.8\text{ V}$.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MSC8144E when $V_{DDDDR}(typ) = 1.8\text{ V}$.

Table 6. DDR2 SDRAM DC Electrical Characteristics for $V_{DDDDR}(typ) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage ¹	V_{DDDDR}	1.7	1.9	V
I/O reference voltage ²	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage ³	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V
Output leakage current ⁴	I_{OZ}	-50	50	μA
Output high current ($V_{OUT} = 1.420\text{ V}$)	I_{OH}	-13.4	—	mA
Output low current ($V_{OUT} = 0.280\text{ V}$)	I_{OL}	13.4	—	mA
Notes: <ol style="list-style-type: none"> V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}. Output leakage is measured with all outputs are disabled, $0\text{ V} \leq V_{OUT} \leq V_{DDDDR}$. 				

2.5.1.2 DDR (2.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM component(s) of the MSC8144E when $V_{DDDDR}(typ) = 2.5\text{ V}$.

Table 7. DDR SDRAM DC Electrical Characteristics for $V_{DDDDR}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage ¹	V_{DDDDR}	2.3	2.7	V
I/O reference voltage ²	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage ³	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.15$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.15$	V
Output leakage current ⁴	I_{OZ}	-50	50	μA
Output high current ($V_{OUT} = 1.95\text{ V}$)	I_{OH}	-16.2	—	mA
Output low current ($V_{OUT} = 0.35\text{ V}$)	I_{OL}	16.2	—	mA
Notes: <ol style="list-style-type: none"> V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}. Output leakage is measured with all outputs are disabled, $0\text{ V} \leq V_{OUT} \leq V_{DDDDR}$. 				

Table 8 lists the current draw characteristics for MV_{REF} .

Table 8. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REF}	I_{MVREF}	—	500	μA
Note: The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.				

2.5.2 Serial RapidIO DC Electrical Characteristics

DC receiver logic levels are not defined since the receiver is AC-coupled.

2.5.2.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks `SRIO_REF_CLK` and `$\overline{\text{SRIO_REF_CLK}}$` are AC-coupled differential inputs. Each differential clock input has an internal $50\ \Omega$ termination to GND_{SXC} . The reference clock must be able to drive this termination. The recommended minimum operating voltage is $-0.4\ \text{V}$; the recommended maximum operating voltage is $1.32\ \text{V}$; and the maximum absolute voltage is $1.72\ \text{V}$.

The maximum average current allowed in each input is $8\ \text{mA}$. This current limitation sets the maximum common mode input voltage to be less than $0.4\ \text{V}$ ($0.4\ \text{V}/50\ \Omega = 8\ \text{mA}$) while the minimum common mode input level is GND_{SXC} . For example, a clock with a 50/50 duty cycle can be driven by a current source output that ranges from $0\ \text{mA}$ to $16\ \text{mA}$ (0 – $0.8\ \text{V}$). The input is AC-coupled internally, so, therefore, the exact common mode input voltage is not critical.

Note: This internal AC-couple network does not function correctly with reference clock frequencies below $90\ \text{MHz}$.

If the device driving the `$\overline{\text{SRIO_REF_CLK}}$` inputs cannot drive $50\ \Omega$ to GND_{SXC} , or if it exceeds the maximum input current limitations, then it must use external AC-coupling. The minimum differential peak-to-peak amplitude of the input clock is $0.4\ \text{V}$ ($0.2\ \text{V}$ peak-to-peak per phase). The maximum differential peak-to-peak amplitude of the input clock is $1.6\ \text{V}$ peak-to-peak (see [Figure 5](#)). The termination to GND_{SXC} allows compatibility with HCSL type reference clocks specified for PCI-Express applications. Many other low voltage differential type outputs can be used but will probably need to be AC-coupled due to the limited common mode input range. LVPECL outputs can produce too large an amplitude and may need to be source terminated with a divider network to reduce the amplitude. The amplitude of the clock must be at least a $400\ \text{mV}$ differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive $100\ \text{mV}$ around common mode voltage. The differential reference clock (`$\overline{\text{SRIO_REF_CLK}}$` / `$\text{SRIO_REF_CLK}$`) input is HCSL-compatible DC coupled or LVDS-compatible with AC-coupling.

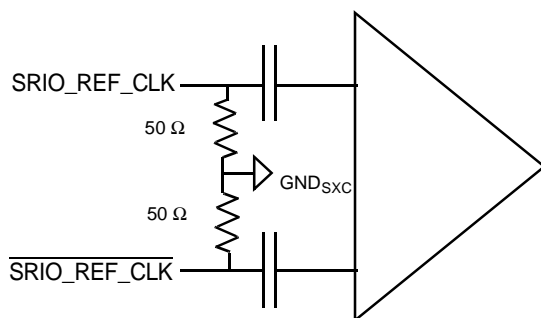


Figure 5. SerDes Reference Clocks Input Stage

2.5.2.2 Spread Spectrum Clock

SRIO_REF_CLK/SRIO_REF_CLK is designed to work with a spread spectrum clock (0 to 0.5% spreading at 3033 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

2.5.3 PCI DC Electrical Characteristics

Table 9. PCI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDPCI}	3.135	3.465	V
Input high voltage	V_{IH}	$0.5 \times V_{DDPCI}$	3.465	V
Input low voltage	V_{IL}	-0.5	$0.3 \times V_{DDPCI}$	V
Input Pull-up voltage ²	V_{IPU}	$0.7 \times V_{DDPCI}$		
Input leakage current, $0 < V_{IN} < V_{DDPCI}$	I_{IN}	-30	30	μA
Tri-state (high impedance off state) leakage current, $0 < V_{IN} < V_{DDPCI}$	I_{OZ}	-30	30	μA
Signal low input current, $V_{IL} = 0.4 V^1$	I_L	-30	30	μA
Signal high input current, $V_{IH} = 2.0 V^1$	I_H	-30	30	μA
Output high voltage, $I_{OH} = -0.5 mA$, except open drain pins	V_{OH}	$0.9 \times V_{DDPCI}$	—	V
Output low voltage, $I_{OL} = 1.5 mA$	V_{OL}	—	$0.1 \times V_{DDPCI}$	V
Input Pin Capacitance ²	C_{IN}		10	pF

Notes: 1. Not tested. Guaranteed by design.

2.5.4 TDM DC Electrical Characteristics

Table 10. TDM DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDTDM}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	-0.3	0.8	V
Input leakage current $0 < V_{IN} < V_{DDTDM}$	I_{IN}	-30	30	μA
Tri-state (high impedance off state) leakage current	I_{OZ}	-30	30	μA
Output high voltage, $I_{OH} = -1.6 mA$	V_{OH}	2.4	—	V
Output low voltage, $I_{OL} = 0.4 mA$	V_{OL}	—	0.4	V

2.5.5 Ethernet DC Electrical Characteristics

2.5.5.1 MII, SMII and RMII DC Electrical Characteristics

Table 11. MII, SMII and RMII DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDGE1} V_{DDGE2}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	-0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	-30	30	μ A
Signal low input current, $V_{IL} = 0.4 V^1$	I_L	-30	30	μ A
Signal high input current, $V_{IH} = 2.4 V^1$	I_H	-30	30	μ A
Output high voltage, $I_{OH} = -4$ mA	V_{OH}	2.4	3.465	V
Output low voltage, $I_{OL} = 4$ mA	V_{OL}	—	0.4	V
Input Pin Capacitance ¹	C_{IN}		8	pF
Note: 1. Not tested. Guaranteed by design.				

2.5.5.2 RGMII DC Electrical Characteristics

Table 12. RGMII DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 2.5 V	V_{DDGE1} V_{DDGE2}	2.375	2.625	V
Input high voltage	V_{IH}	1.7	2.625	V
Input low voltage	V_{IL}	-0.3	0.7	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	-30	30	μ A
Output high voltage, $I_{OH} = -1$ mA	V_{OH}	2.0	2.625	V
Output low voltage, $I_{OL} = 1$ mA	V_{OL}	—	0.4	V
Input Pin Capacitance ¹	C_{IN}		8	pF
Note: 1. Not tested. Guaranteed by design.				

2.5.6 ATM/UTOPIA/POS DC Electrical Characteristics

Table 13. ATM/UTOPIA/POS DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	-0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	-30	30	μ A
Signal low input current, $V_{IL} = 0.4$ V ¹	I_L	-30	30	μ A
Signal high input current, $V_{IH} = 2.4$ V ¹	I_H	-30	30	μ A
Output high voltage, $I_{OH} = -4$ mA	V_{OH}	2.4	3.465	V
Output low voltage, $I_{OL} = 4$ mA	V_{OL}	—	0.5	V

Notes: 1. Not tested. Guaranteed by design.

2.5.7 SPI DC Electrical Characteristics

Table 14 provides the SPI DC electrical characteristics.

Table 14. SPI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	-0.3	0.8	V
Input current	I_{IN}		30	μ A
Output high voltage, $I_{OH} = -4.0$ mA	V_{OH}	2.4	—	V
Output low voltage, $I_{OL} = 4.0$ mA	V_{OL}	—	0.5	V

2.5.8 GPIO, UART, TIMER, EE, STOP_BS, I²C, \overline{IRQn} , $\overline{NMI_OUT}$, $\overline{INT_OUT}$, CLKIN, JTAG Ports DC Electrical Characteristics

 Table 15. GPIO, UART, Timer, EE, STOP_BS, I²C, \overline{IRQn} , $\overline{NMI_OUT}$, $\overline{INT_OUT}$, CLKIN, and JTAG Port¹ DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	-0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	-30	30	μ A
Tri-state (high impedance off state) leakage current, V_{IN} = supply voltage	I_{OZ}	-30	30	μ A
Signal low input current, $V_{IL} = 0.4$ V ²	I_L	-30	30	μ A
Signal high input current, $V_{IH} = 2.0$ V ²	I_H	-30	30	μ A
Output high voltage, $I_{OH} = -2$ mA, except open drain pins	V_{OH}	2.4	3.465	V
Output low voltage, $I_{OL} = 3.2$ mA	V_{OL}	—	0.4	V

Notes: 1. This does not include TDI and TMS, which have internal pullup resistors.
2. Not tested. Guaranteed by design.

2.6 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs.

2.6.1 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.6.2** describes the clocking characteristics. **Section 2.6.3** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8144E device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence using the V_{DDIO} (3.3 V) supply. See [Table 19](#) for timing. $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct initialization of the Security Engine.

Note: For applications that use M3 memory, $\overline{\text{M3_RESET}}$ should replicate the $\overline{\text{PORESET}}$ sequence timing, but using the V_{DDM3IO} (2.5 V) supply. See **Section 3.1.1, Power-on Sequence** for additional design information.

- CLKIN should start toggling at least 32 cycles before the $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see [Figure 6](#)). 32 cycles should be accounted only after V_{DDIO} reaches its nominal value.
- CLKIN and PCI_CLK_IN should either be stable low during the power-up of V_{DDIO} supply and start their swings after power-up or should swing within V_{DDIO} range during V_{DDIO} power-up., so their amplitude grows as V_{DDIO} grows during power-up.

[Figure 6](#) shows a sequence in which V_{DDIO} is raised after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

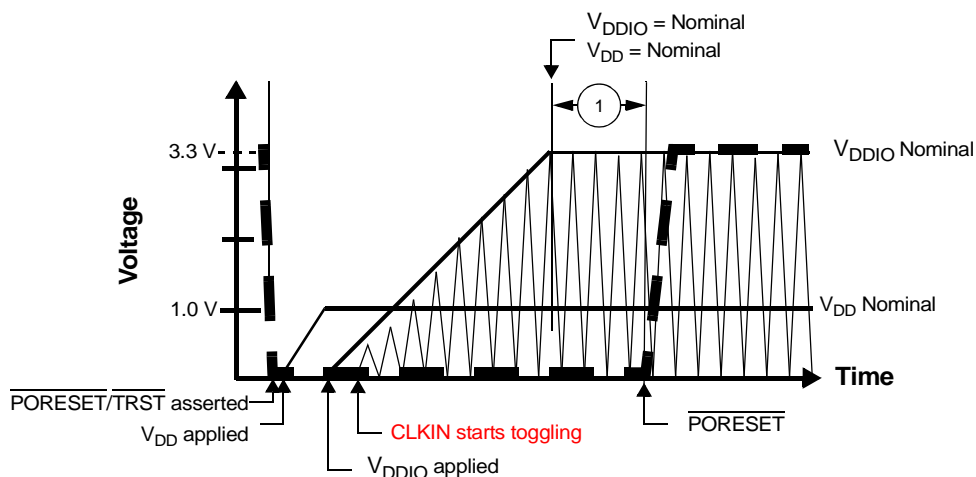


Figure 6. Start-Up Sequence with V_{DD} Raised Before V_{DDIO} with CLKIN Started with V_{DDIO}

2.6.2 Clock and Timing Signals

The following sections include a description of clock signal characteristics. [Table 16](#) shows the maximum frequency values for CLKIN and PCI_CLK_IN. The user must ensure that maximum frequency values are not exceeded.

Table 16. Clock Frequencies

Characteristic	Symbol	Min	Max	Unit
CLKIN frequency	F_{CLKIN}	33	133	MHz
PCI_CLK_IN frequency	$F_{\text{PCI_CLK_IN}}$	33	133	MHz
CLKIN duty cycle	D_{CLKIN}	40	60	%
PCI_CLK_IN duty cycle	$D_{\text{PCI_CLK_IN}}$	40	60	%

2.6.3 Reset Timing

The MSC8144E has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- JTAG reset
- RapidIO reset
- Software hard reset
- Software soft reset

All MSC8144E reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. [Table 17](#) describes the reset sources.

Table 17. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8144E and configures various attributes of the MSC8144E. On $\overline{\text{PORESET}}$, the entire MSC8144E device is reset. All PLLs states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the extended cores are reset, and system configuration is sampled. The reset source and word are configured only when $\overline{\text{PORESET}}$ is asserted.
External hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8144E. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the extended cores are reset, and system configuration is sampled. Note that the RCW (reset Configuration Word) is not reloaded during $\overline{\text{HRESET}}$ assertion after out of power on reset sequence. The reset configuration word is described in the Reset chapter in the <i>MSC8144E Reference Manual</i> .
External soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8144E detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8144E is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the extended cores are reset, and system configuration is maintained.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.
Software watchdog reset	Internal	When the MSC8144E watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
RapidIO reset	Internal	When the RapidIO logic asserts the RapidIO hard reset signal, it generates an internal hard reset sequence.
Software hard reset	Internal	A hard reset sequence can be initialized by writing to a memory mapped register (RCR)
Software soft reset	Internal	A soft reset sequence can be initialized by writing to a memory mapped register (RCR)

[Table 18](#) summarizes the reset actions that occur as a result of the different reset sources.

Table 18. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset ($\overline{\text{PORESET}}$)	Hard Reset ($\overline{\text{HRESET}}$)	Soft Reset ($\overline{\text{SRESET}}$)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to Section 2.6.3.2 for details).	Yes	No	No	No
PLL state reset	Yes	No	No	No
Select reset configuration source	Yes	No	No	No
System reset configuration write	Yes	No	No	No

Table 18. Reset Actions for Each Reset Source (continued)

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset ($\overline{\text{HRESET}}$)	Soft Reset ($\overline{\text{SRESET}}$)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
$\overline{\text{HRESET}}$ driven	Yes	Yes	No	No
IPBus modules reset (TDM, UART, SWT, DDRC, IPBus master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
$\overline{\text{SRESET}}$ driven	Yes	Yes	Yes	Depends on command
Extended cores reset	Yes	Yes	Yes	Yes
CLASS registers reset	Yes	Yes	Some registers	Some registers
Timers, Performance Monitor	Yes	Yes	No	No
QUICC Engine Subsystem, PCI, DMA	Yes	Yes	Most registers	Most registers

2.6.3.1 Power-On Reset ($\overline{\text{PORESET}}$) Pin

Asserting $\overline{\text{PORESET}}$ initiates the power-on reset flow. $\overline{\text{PORESET}}$ must be asserted externally for at least 32 CLKIN cycles after V_{DD} and V_{DDIO} are both at their nominal levels.

2.6.3.2 Reset Configuration

The MSC8144E has two mechanisms for writing the reset configuration:

- Through the I²C port
- Through external pins
- Through internal hard coded

Twenty-three signals (see **Section 1** for signal description details) are sampled during the power-on reset sequence to define the Reset Word Configuration Source and operating conditions:

- RCW_SRC[2–0]
- RC[16–0]

The RCFG_CLKIN_RNG pin must be valid during power-on or hard reset sequence. The STOP_BS pin must be always valid and is also sampled during power-on reset sequence for RCW loading from an I²C EEPROM.

2.6.3.3 Reset Timing Tables

Table 19 and Figure 7 describe the reset timing for a reset configuration.

Table 19. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Max	Min	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum <ul style="list-style-type: none"> • 33 MHz \leq CLKIN < 44 MHz • 44 MHz \leq CLKIN < 66 MHz • 66 MHz \leq CLKIN < 100 MHz • 100 MHz \leq CLKIN < 133 MHz 	32/CLKIN	1280 728 485 320	727 484 320 241	ns ns ns ns

Table 19. Timing for a Reset Configuration Write (continued)

No.	Characteristics	Expression	Max	Min	Unit
2	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for external pins and hard coded RCW	$15369/\text{CLKIN}$ $34825/\text{CLKIN}$	615 528	233 262	μs μs
	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for loading RCW the I ² C interface	$92545/\text{CLKIN}$ $107435/\text{CLKIN}$ $124208/\text{CLKIN}$ $157880/\text{CLKIN}$	3702 2441 1882 1579	2103 1627 1242 1187	μs μs μs μs
3	Delay from $\overline{\text{HRESET}}$ deassertion to $\overline{\text{SRESET}}$ deassertion	$16/\text{CLKIN}$	640	120	ns

Note: Timings are not tested, but are guaranteed by design.

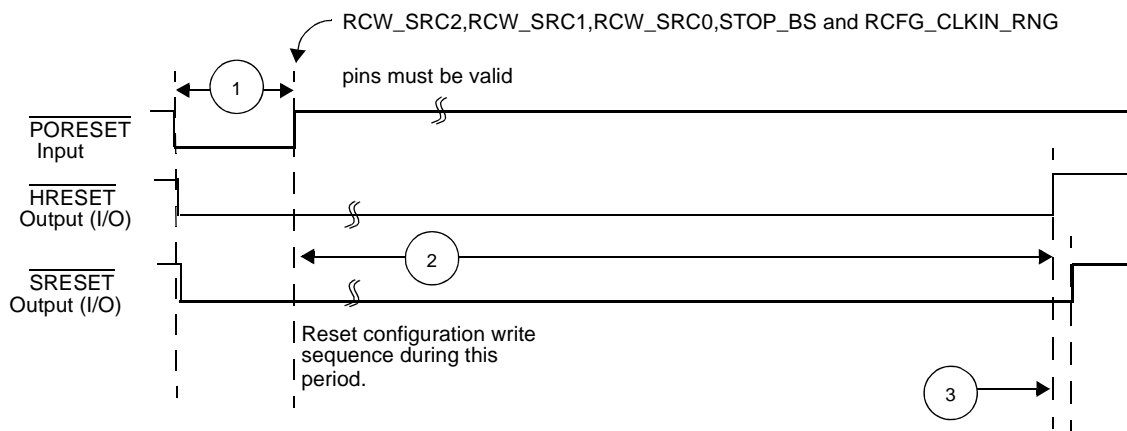


Figure 7. Timing for a Reset Configuration Write

See also Reset Errata for PLL lock and reset duration.

2.6.4 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.4.1 DDR SDRAM Input Timings

Table 20 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 2.5 V.

Table 20. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V
Note: At recommended operating conditions with V_{DDDDR} of $2.5 \pm 5\%$.				

Table 21 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 21. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V
Note: At recommended operating conditions with V_{DDDDR} of $1.8 \pm 5\%$.				

Table 22 provides the input AC timing specifications for the DDR SDRAM interface.

Table 22. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit
Controller Skew for MDQS—MDQ/MECC/MDM ¹	t_{CISKEW}			
• 400 MHz		–365	365	ps
• 333 MHz		–390	390	ps
• 266 MHz		–428	428	ps
• 200 MHz		–490	490	ps
Notes:				
1.	t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.			
2.	At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) $\pm 5\%$			

2.6.4.2 DDR SDRAM Output AC Timing Specifications

Table 23 provides the output AC timing specifications for the DDR SDRAM interface.

Table 23. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol ¹	Min	Max	Unit
MCK[n] cycle time, (MCK[n]/MCK[n] crossing) ²	t_{MCK}	5	10	ns
ADDR/CMD output setup with respect to MCK ³ <ul style="list-style-type: none"> • 400 MHz • 333 MHz • 266 MHz • 200 MHz 	t_{DDKHAS}	1.95 2.40 3.15 4.20	— — — —	ns ns ns ns
ADDR/CMD output hold with respect to MCK ³ <ul style="list-style-type: none"> • 400 MHz • 333 MHz • 266 MHz • 200 MHz 	t_{DDKHAX}	1.85 2.40 3.15 4.20	— — — —	ns ns ns ns
MCSn output setup with respect to MCK ³ <ul style="list-style-type: none"> • 400 MHz • 333 MHz • 266 MHz • 200 MHz 	t_{DDKHCS}	1.95 2.40 3.15 4.20	— — — —	ns ns ns ns
MCSn output hold with respect to MCK ³ <ul style="list-style-type: none"> • 400 MHz • 333 MHz • 266 MHz • 200 MHz 	t_{DDKHXC}	1.95 2.40 3.15 4.20	— — — —	ns ns ns ns
MCK to MDQS Skew ⁴	t_{DDKMHM}	-0.6	0.6	ns
MDQ/MECC/MDM output setup with respect to MDQS ⁵ <ul style="list-style-type: none"> • 400 MHz • 333 MHz • 266 MHz • 200 MHz 	t_{DDKHDS} , t_{DDKLDS}	700 900 1100 1200	— — — —	ps ps ps ps
MDQ/MECC/MDM output hold with respect to MDQS ⁵ <ul style="list-style-type: none"> • 400 MHz • 333 MHz • 266 MHz • 200 MHz 	t_{DDKHDX} , t_{DDKLDX}	700 900 1100 1200	— — — —	ps ps ps ps
MDQS preamble start ⁶	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns
MDQS epilogue end ⁶	t_{DDKHME}	-0.6	0.6	ns

- Notes:**
1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ± 0.1 V.
 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
 4. Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MSC8144 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
 6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
 7. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) \pm 5%.

Figure 8 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

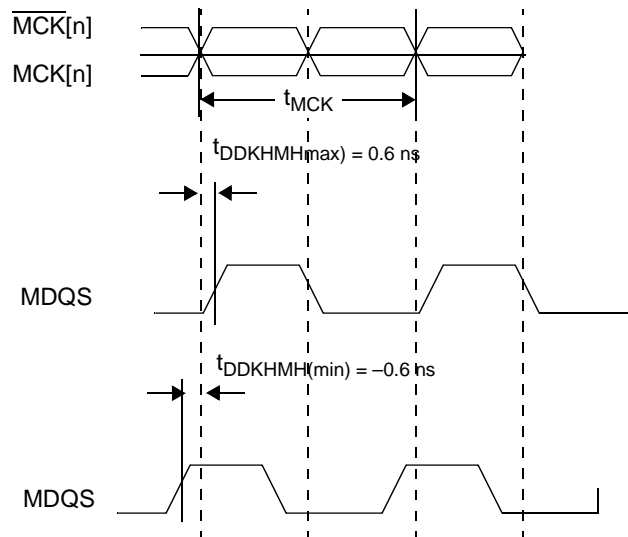


Figure 8. Timing for t_{DDKHMH}

Figure 9 shows the DDR SDRAM output timing diagram.

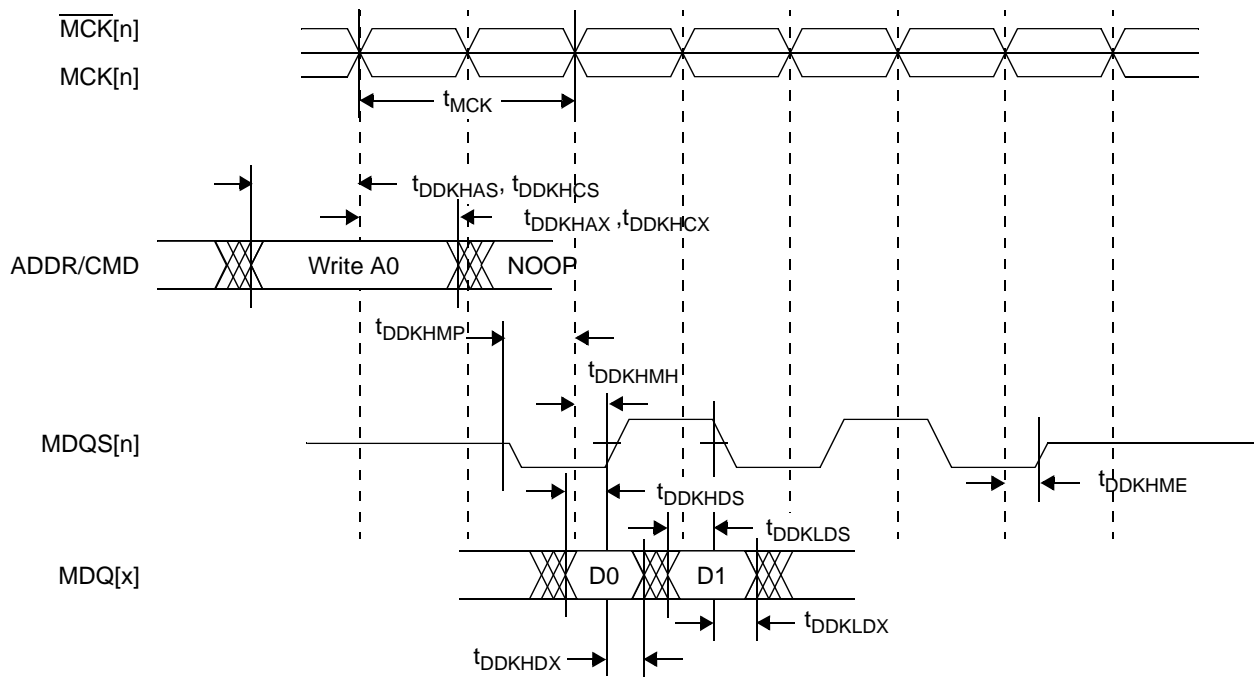


Figure 9. DDR SDRAM Output Timing

Figure 10 provides the AC test load for the DDR bus.

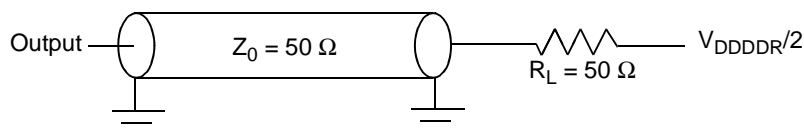


Figure 10. DDR AC Test Load

2.6.5 Serial RapidIO Timing and SGMII Timing

2.6.5.1 AC Requirements for $\overline{\text{SRIO_REF_CLK}}$ and $\overline{\text{SRIO_REF_CLK}}$

Table 24 lists AC signal specifications.

Table 24. $\overline{\text{SDn_REF_CLK}}$ and $\overline{\text{SDn_REF_CLK}}$ AC Signal Specifications

Parameter Description	Symbol	Min	Typical	Max	Units	Comments
REFCLK cycle time	t_{REF}	—	10 (8, 6.4)	—	ns	8 ns applies only to serial RapidIO system with 125-MHz reference clock. 6.4 ns applies only to serial RapidIO systems with a 156.25 MHz reference clock. Note: SGMII uses the 8 ns (125 MHz) value only.

2.6.5.2 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 11 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between voltage levels A and B, where $A > B$.

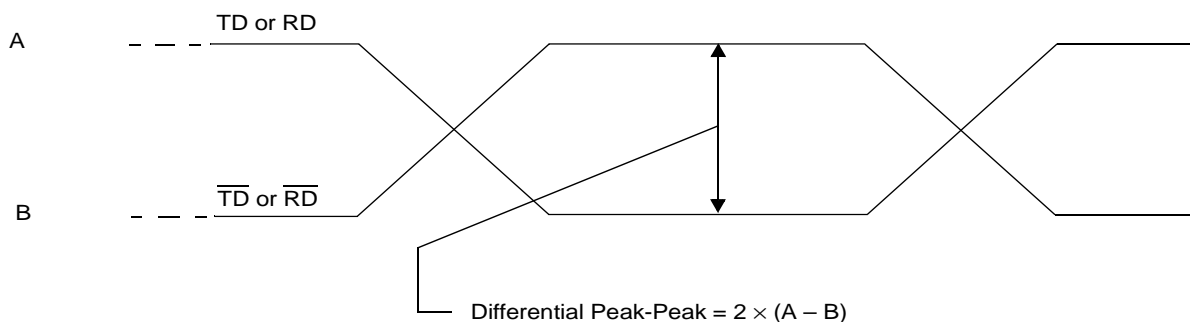


Figure 11. Differential V_{PP} of Transmitter or Receiver

Note: This explanation uses generic TD/ $\overline{\text{TD}}$ /RD/ $\overline{\text{RD}}$ signal names. These correspond to SRIO_TXD/ $\overline{\text{SRIO_TXD}}$ /SRIO_RXD/ $\overline{\text{SRIO_RXD}}$ respectively.

Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals T_D , $\overline{T_D}$, R_D and $\overline{R_D}$ each have a peak-to-peak voltage (V_{PP}) swing of $A - B$.
2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{T_D} - V_{\overline{T_D}}$.
3. The differential input signal of the receiver, V_{ID} , is defined as $V_{R_D} - V_{\overline{R_D}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$.
5. The peak value of the differential transmitter output signal and the differential receiver input signal is $A - B$.
6. The value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A - B) V_{PP}$.

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, T_D and $\overline{T_D}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals T_D and $\overline{T_D}$ is 500 mV_{PP}. The differential output signal ranges between 500 mV and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV_{PP}.

Note: AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described. The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE™ Std 802.3ae-2002™. XAUI has similar application goals to serial RapidIO. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

2.6.5.3 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

2.6.5.4 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section. The differential return loss, S11, of the transmitter in each case shall be better than

- -10 dB for (baud frequency)/10 < freq(f) < 625 MHz, and
- -10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ freq(f) ≤ baud frequency

The reference impedance for the differential return loss measurements is 100 Ω resistive. Differential return loss includes contributions from internal circuitry, packaging, and any external components related to the driver. The output impedance requirement applies to all valid output levels. It is recommended that the 20–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case. It is also recommended that the timing skew at the output of an LP-Serial transmitter between the two signals comprising a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Table 25. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV _{PP}	
Deterministic Jitter	J_D		0.17	UI _{PP}	
Total Jitter	J_T		0.35	UI _{PP}	

Table 25. Short Run Transmitter AC Timing Specifications—1.25 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S _{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 26. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV _{PP}	
Deterministic Jitter	J _D		0.17	UI _{PP}	
Total Jitter	J _T		0.35	UI _{PP}	
Multiple Output skew	S _{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 27. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV _{PP}	
Deterministic Jitter	J _D		0.17	UI _{PP}	
Total Jitter	J _T		0.35	UI _{PP}	
Multiple output skew	S _{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

Table 28. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V _O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	800	1600	mV _{PP}	
Deterministic Jitter	J _D		0.17	UI _{PP}	
Total Jitter	J _T		0.35	UI _{PP}	
Multiple output skew	S _{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 29. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV _{PP}	
Deterministic Jitter	J_D		0.17	UI _{PP}	
Total Jitter	J_T		0.35	UI _{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 30. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV _{PP}	
Deterministic Jitter	J_D		0.17	UI _{PP}	
Total Jitter	J_T		0.35	UI _{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in [Figure 12](#) with the parameters specified in [Table 31](#) when measured at the output pins of the device and the device is driving a $100\ \Omega \pm 5\%$ differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

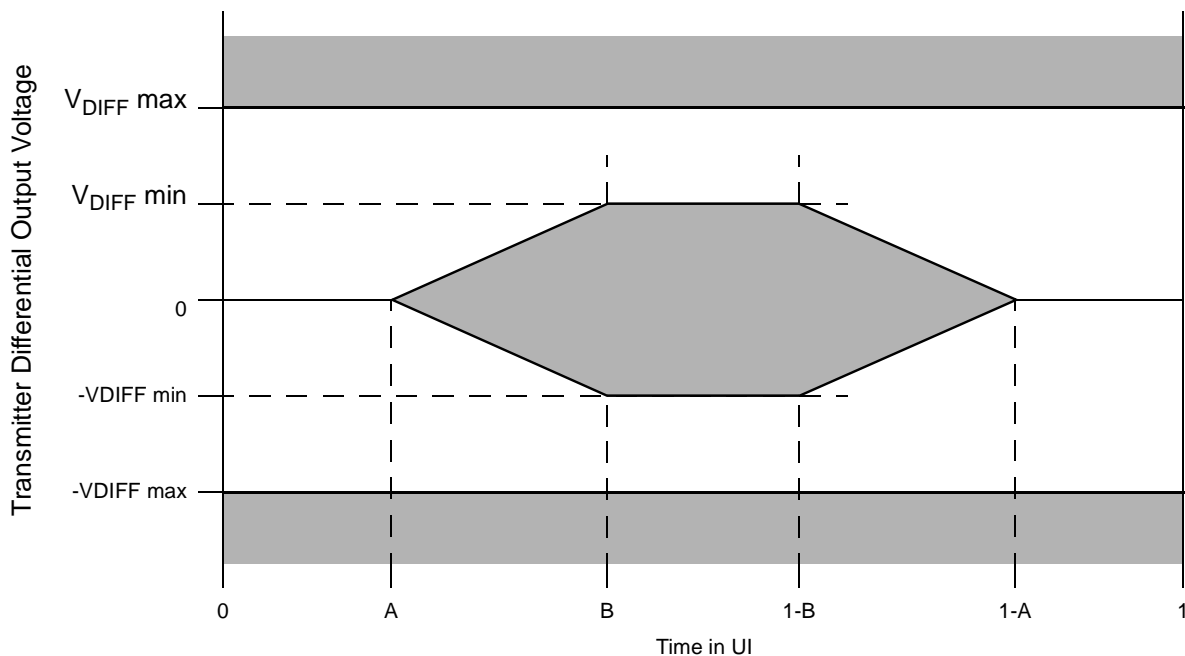


Figure 12. Transmitter Output Compliance Mask

Table 31. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

2.6.5.5 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section. Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to $0.8 \times$ baud frequency. This includes contributions from internal circuitry, the package, and any external components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω resistive for differential return loss and 25 Ω resistive for common mode.

Table 32. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV _{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI _{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI _{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI _{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	800	800	ps	± 100 ppm

Table 33. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV _{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI _{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI _{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI _{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	400	400	ps	± 100 ppm

Table 34. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV _{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI _{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI _{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI _{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	± 100 ppm

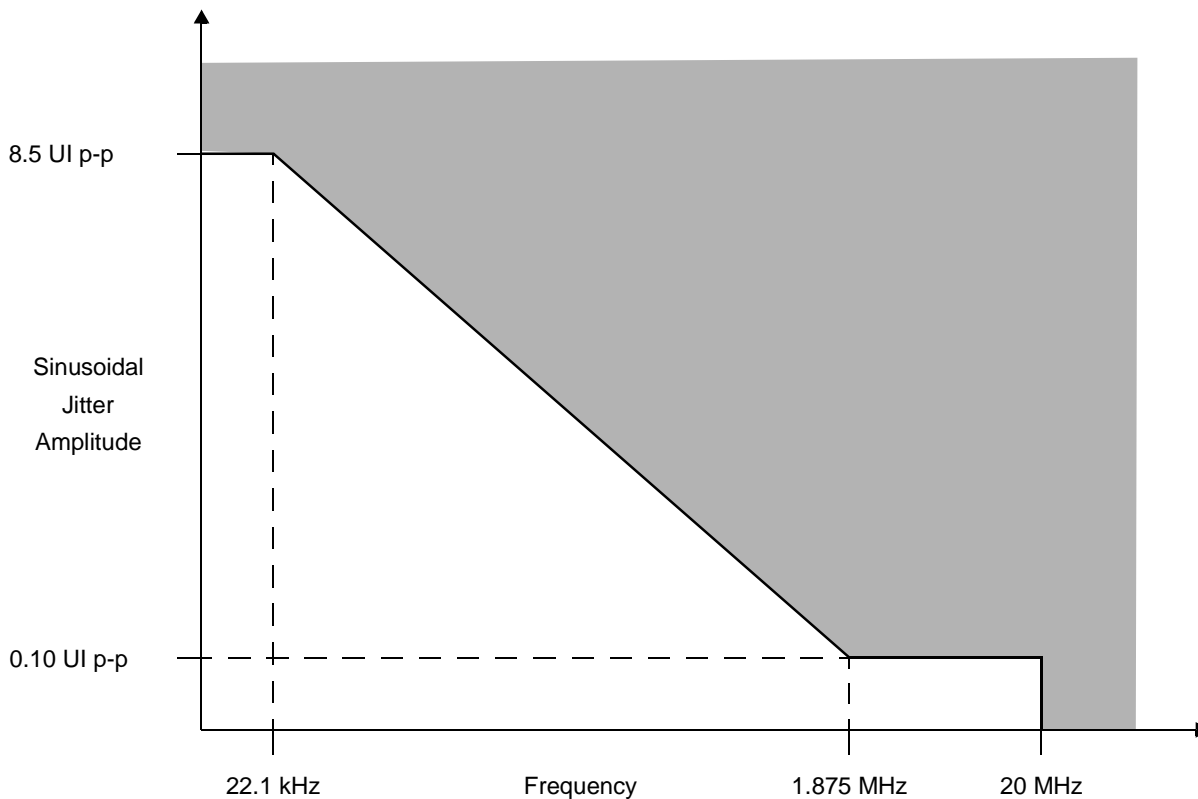


Figure 13. Single Frequency Sinusoidal Jitter Limits

2.6.5.6 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 32, Table 33, and Table 34) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 14 with the parameters specified in Table 35. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100\ \Omega \pm 5\%$ differential resistive load.

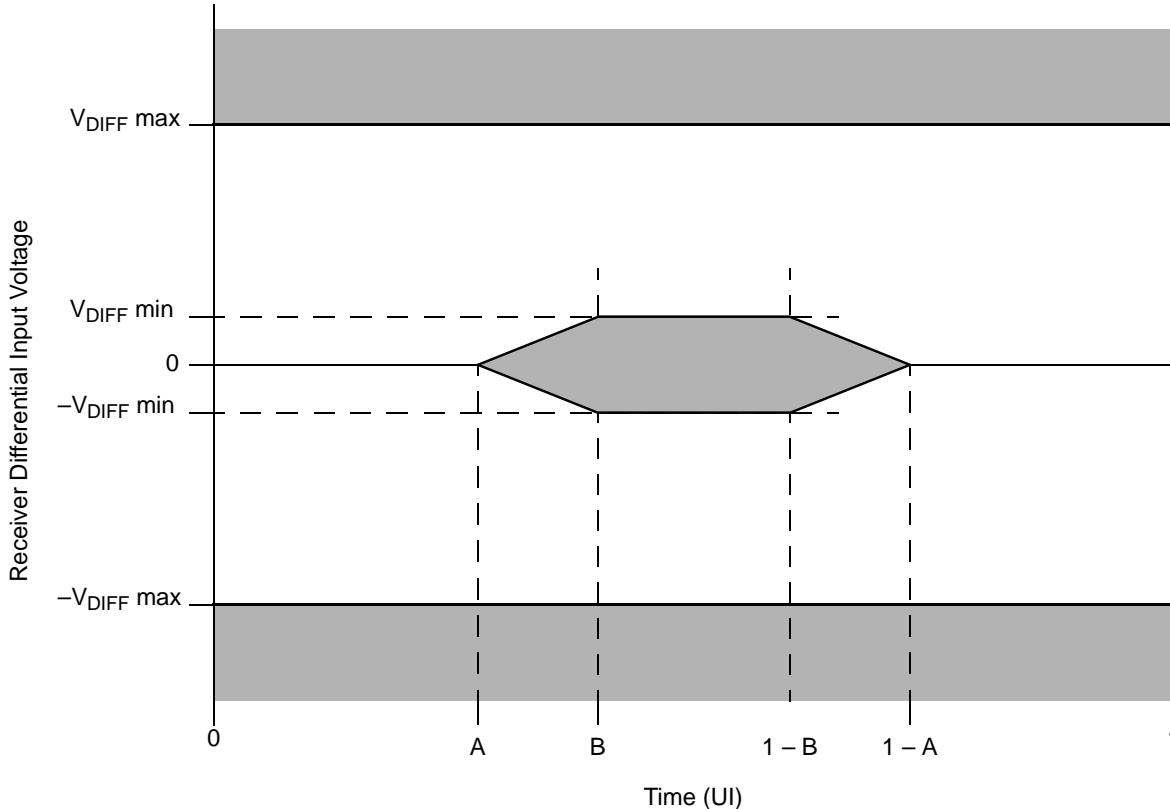


Figure 14. Receiver Input Compliance Mask

Table 35. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

2.6.5.7 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of **IEEE** Std. 802.3ae-2002™, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of **IEEE** Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of **IEEE** Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

2.6.5.8 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12} . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive $\pm 5\%$ differential to 2.5 GHz.

2.6.5.9 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of **IEEE** Std. 802.3ae.

2.6.5.10 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive $\pm 5\%$ differential to 2.5 GHz.

2.6.5.11 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in **Section 2.6.5.9** and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in **Figure 14** and **Table 35**. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

2.6.6 PCI Timing

This section describes the general AC timing parameters of the PCI bus. **Table 36** provides the PCI AC timing specifications.

Table 36. PCI AC Timing Specifications

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Output delay	t_{PCVAL}	2.0	11.0	1.0	6.0	ns
High-Z to Valid Output delay	t_{PCON}	2.0	—	1.0	—	ns
Valid to High-Z Output delay	t_{PCOFF}	—	28	—	14	ns
Input setup	t_{PCSU}	7.0	—	3.0	—	ns
Input hold	t_{PCH}	0	—	0	—	ns

Table 36. PCI AC Timing Specifications (continued)

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Notes: <ol style="list-style-type: none"> 1. See the timing measurement conditions in the <i>PCI 2.2 Local Bus Specifications</i>. 2. All PCI signals are measured from $0.5 \times V_{DDIO}$ of the rising edge of PCI_CLK_IN to $0.4 \times V_{DDIO}$ of the signal in question for 3.3-V PCI signaling levels. 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification. 4. Input timings are measured at the pin. 5. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is in Table 19 and Figure 7 						

Figure 15 provides the AC test load for the PCI.

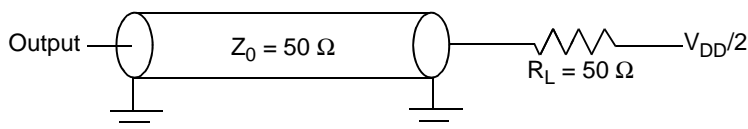

Figure 15. PCI AC Test Load

Figure 16 shows the PCI input AC timing conditions.

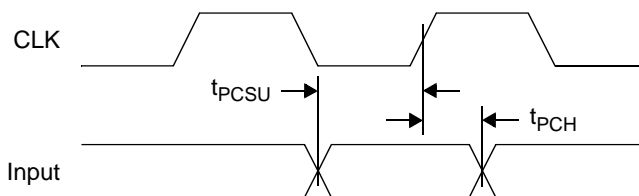
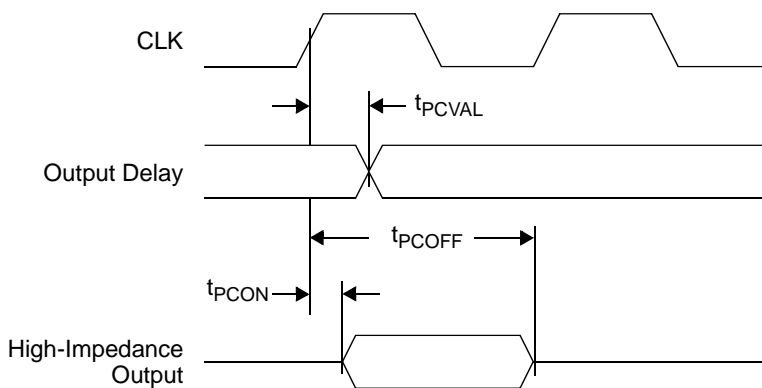

Figure 16. PCI Input AC Timing Measurement Conditions

Figure 17 shows the PCI output AC timing conditions.


Figure 17. PCI Output AC Timing Measurement Condition

2.6.7 TDM Timing

Table 37. TDM Timing

Characteristic	Symbol	Expression	Min	Max	Units
TDMxRCLK/TDMxTCLK	t_{TDMC}	TC^1	16	—	ns
TDMxRCLK/TDMxTCLK high pulse width	t_{TDMCH}	$(0.5 \pm 0.1) \times TC^4$	7	—	ns
TDMxRCLK/TDMxTCLK low pulse width	t_{TDMCL}	$(0.5 \pm 0.1) \times TC^4$	7	—	ns
TDM receive all input setup time related to TDMxRCLK TDMxTSYN input setup time related to TDMxTCLK in TSO=0 mode	t_{TDMVKH}		3.6	—	ns
TDM receive all input hold time related to TDMxRCLK TDMxTSYN input hold time related to TDMxTCLK in TSO=0 mode	t_{TDMXKH}		1.9	—	ns
TDMxTCLK high to TDMxTDAT output active ²	$t_{TDMDHox}$		2.5	—	ns
TDMxTCLK high to TDMxTDAT output valid ²	$t_{TDMDHov}$		—	9.8	ns
All output hold time (except TDMxTSYN) ³	t_{TDMHox}		2.5	—	ns
TDMxTCLK high to TDMxTDAT output high impedance ²	$t_{TDMDHOZ}$		—	9.8	ns
TDMxTCLK high to TDMxTSYN output valid ²	$t_{TDMShov}$		—	9.25	ns
TDMxTSYN output hold time ³	$t_{TDMShox}$		2.0	—	ns

Notes:

1. Values are based on a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz.
2. Values are based on 20 pF capacitive load.
3. Values are based on 10 pF capacitive load.
4. The expression is for common calculations only.

Figure 18 shows the TDM input AC timing.

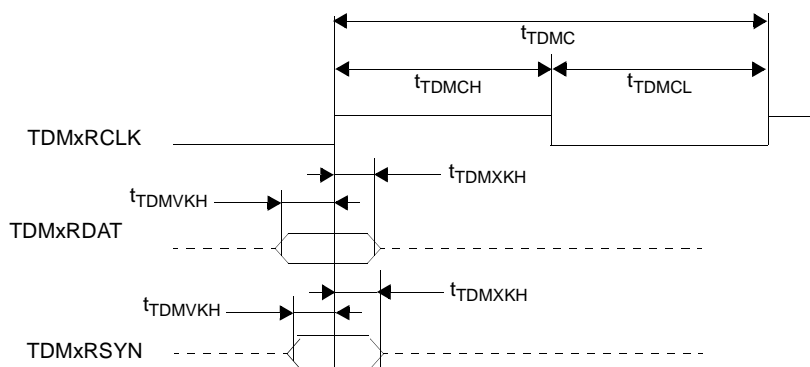


Figure 18. TDM Inputs Signals

Note: For some TDM modes, receive data and receive sync are input on other pins. This timing is also valid for them. See the *MSC8144E Reference Manual*.

Figure 19 shows TDMxTSYN AC timing in TSO=0 mode.

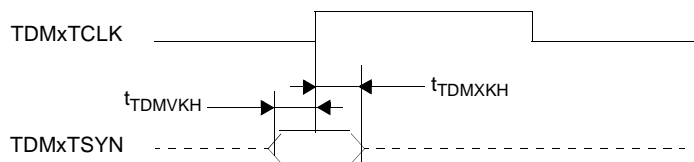


Figure 19. TDMxTSYN in TSO=0 mode

Figure 20 shows the TDM Output AC timing

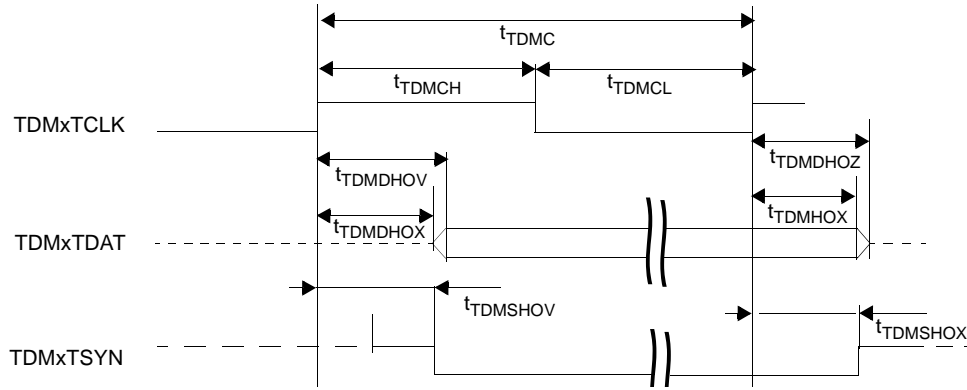


Figure 20. TDM Output Signals

Note: For some TDM modes, transmit data is output on other pins. This timing is also valid for those pins. See the *MSC8144E Reference Manual*

2.6.8 UART Timing

Table 38. UART Timing

Characteristics	Symbol	Expression	Min	Max	Unit
URXD and UTXD inputs high/low duration	$T_{UREFCLK}$	$16 \times T_{REFCLK}$	160	—	ns
Note: $T_{UREFCLK} = T_{REFCLK}$ is guaranteed by design.					

Figure 21 shows the UART input AC timing

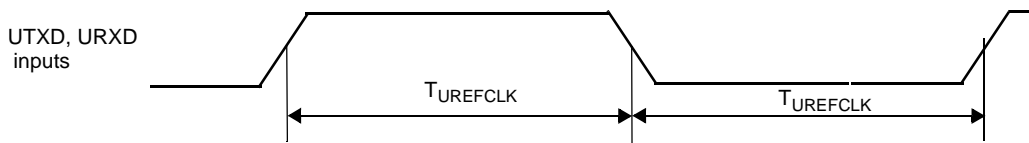


Figure 21. UART Input Timing

Figure 22 shows the UART output AC timing



Figure 22. UART Output Timing

2.6.9 Timer Timing

Table 39. Timer Timing

Characteristics	Symbol	Min	Unit
TIMERx frequency	$T_{TMREFCLK}$	10.0	ns
TIMERx Input high phase	T_{TMCH}	4.0	ns
TIMERx Output low phase	T_{TMCL}	4.0	ns

Figure 23 shows the timer input AC timing

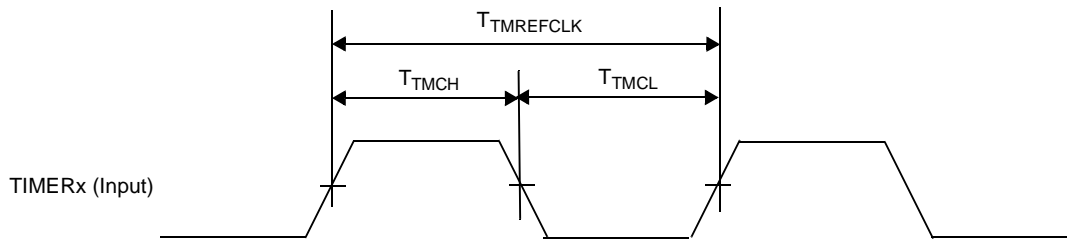


Figure 23. Timer Timing

2.6.10 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each Interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8144E Reference Manual*.

2.6.10.1 Management Interface Timing

Table 40. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
ETHMDC to ETHMDIO delay ²	t_{MDKHDX}	10	70	ns
ETHMDIO to ETHMDC rising edge setup time	t_{MDDVKH}	7	—	ns
ETHMDC rising edge to ETHMDIO hold time	t_{MDDXKH}	0	—	ns
Notes: <ol style="list-style-type: none"> 1. Program the ETHMDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz, to achieve $f_{MDC} = 2.5$ MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the <i>MSC8144E Reference Manual</i> for configuration details. 2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns. 				

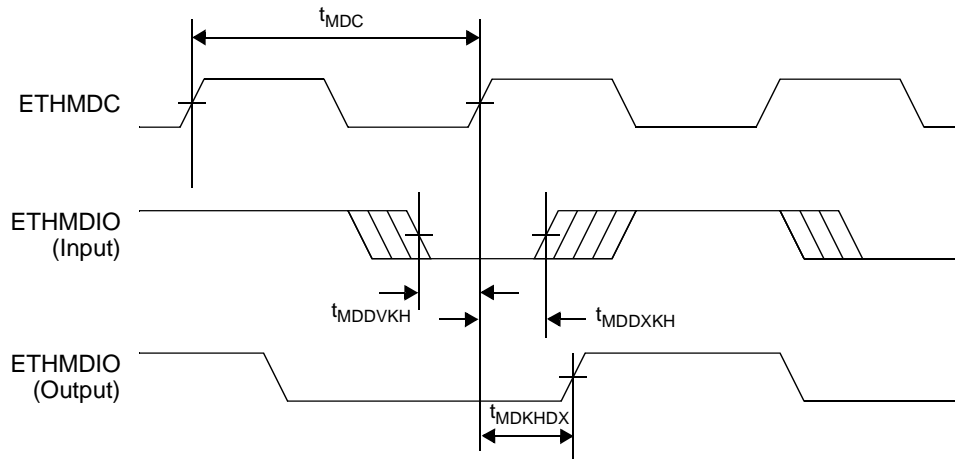


Figure 24. MII Management Interface Timing

2.6.10.2 MII Transmit AC Timing Specifications

Table 41 provides the MII transmit AC timing specifications.

Table 41. MII Transmit AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Max	Unit
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	25	ns
Notes: 1. Typical TX_CLK period (t_{MTX}) for 10 Mbps is 400 ns and for 100 Mbps is 40 ns. 2. Program GCR4 as 0x00030CC3.				

Figure 25 shows the MII transmit AC timing diagram.

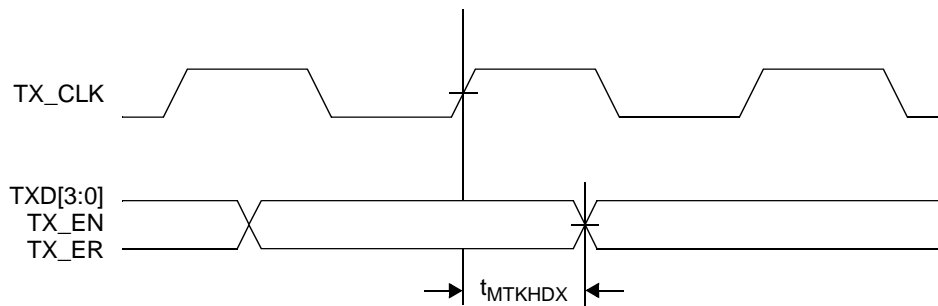


Figure 25. MII Transmit AC Timing

2.6.10.3 MII Receive AC Timing Specifications

Table 42 provides the MII receive AC timing specifications.

Table 42. MII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Max	Unit
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	2	—	ns
Notes: 1. Typical RX_CLK period (t_{MRX}) for 10 Mbps is 400 ns and for 100 Mbps is 40 ns. 2. Program GCR4 as 0x00030CC3.				

Figure 26 provides the AC test load.

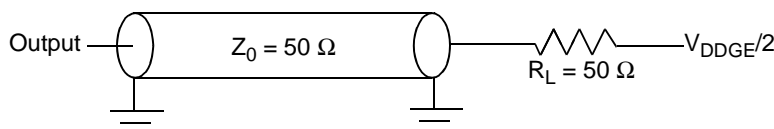


Figure 26. AC Test Load

Figure 27 shows the MII receive AC timing diagram.

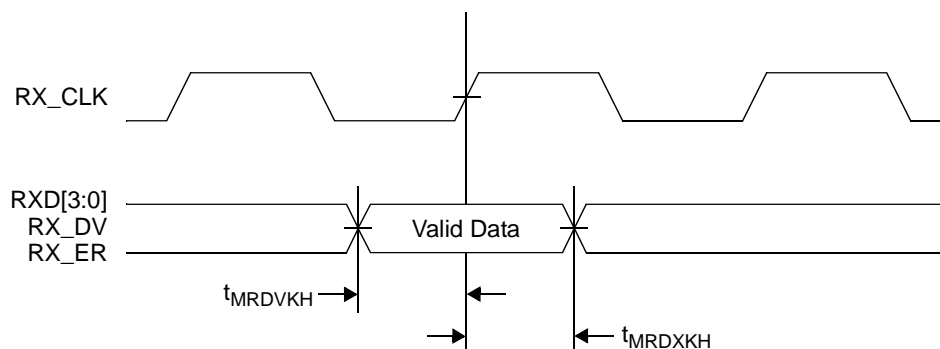


Figure 27. MII Receive AC Timing

2.6.10.4 RMI Transmit and Receive AC Timing Specifications

Table 43 provides the RMI transmit and receive AC timing specifications.

Table 43. RMI Transmit and Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Max	Unit
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	65	%
REF_CLK to RMI data TXD[1–0], TX_EN delay	$t_{RMTKHDX}$	2	10	ns
RXD[1–0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	ns
RXD[1–0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	ns
REF_CLK data clock rise	t_{RMXR}	1.0	4.0	ns
REF_CLK data clock fall	t_{RMXF}	1.0	4.0	ns
Typical REF_CLK clock period (t_{RMX}) is 20 ns				
Notes: <ol style="list-style-type: none"> 1. Typical REF_CLK clock period (t_{RMX}) is 20 ns 2. Program GCR4 as 0x00001405 				

Figure 28 shows the RMIIT transmit and receive AC timing diagram.

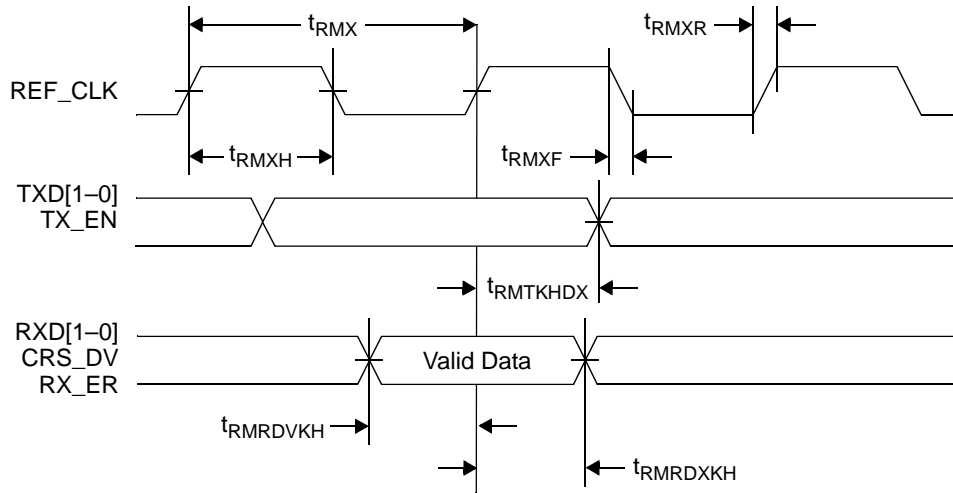


Figure 28. RMIIT Transmit and Receive AC Timing

Figure 29 provides the AC test load.

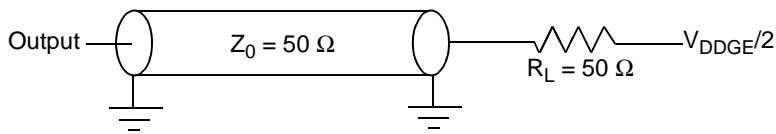


Figure 29. AC Test Load

2.6.10.5 SMII AC Timing Specification

Table 44. SMII Mode Signal Timing

Characteristics	Symbol	Min	Max	Unit
ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge setup time	t_{SMDVKH}	1.5	—	ns
ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	t_{SMDXKH}	1.0	—	ns
ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	t_{SMXR}	1.5	5.0	ns
Notes: <ol style="list-style-type: none"> 1. Typical REF_CLK clock period is 8ns 2. Measured using a 5 pF load. 3. Measured using a 15 pF load 4. Program GCR4 as 0x00002008 				

Figure 30 shows the SMII Mode signal timing.

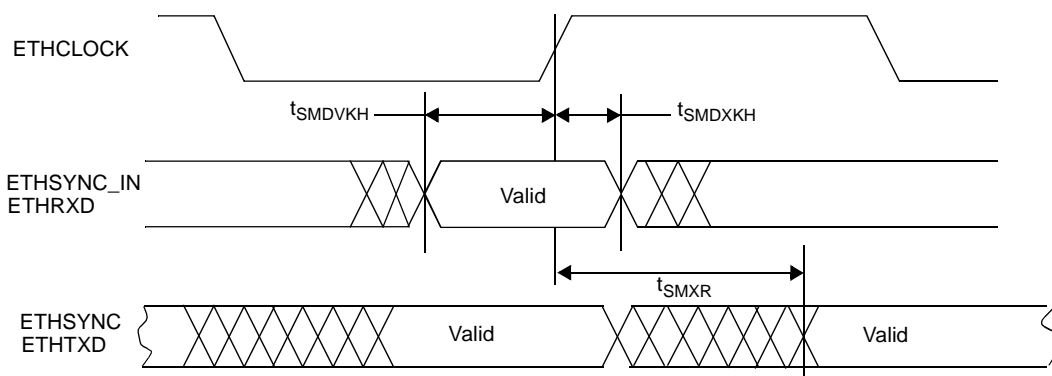


Figure 30. SMI Mode Signal Timing

2.6.10.6 RGMII AC Timing Specifications

Table 45 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 45. RGMII with On-Board Delay AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKEWT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ²	t_{SKEWR}	0.9	—	2.6	ns
Clock cycle duration ³	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12}^6	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	45	—	55	%

Notes:

- At recommended operating conditions with L_{VDD} of 2.5 V +/- 5%.
- This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns +/- 40 ns and 40 ns +/- 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Duty cycle reference is $L_{Vdd}/2$.
- This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- GCR4 should be programmed as 0x00001004.

Table 46 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 46. RGMII with No On-Board Delay AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKEWT}	-2.6	—	-0.9	ns
Data to clock input skew (at receiver) ²	t_{SKEWR}	-0.5	—	0.5	ns

Notes:

- At recommended operating conditions with L_{VDD} of 2.5 V +/- 5%.
- This implies that PC board design will require clocks to be routed with no additional trace delay
- GCR4 should be programmed as 0x0004C130.

Figure 31 shows the RGMII AC timing and multiplexing diagrams.

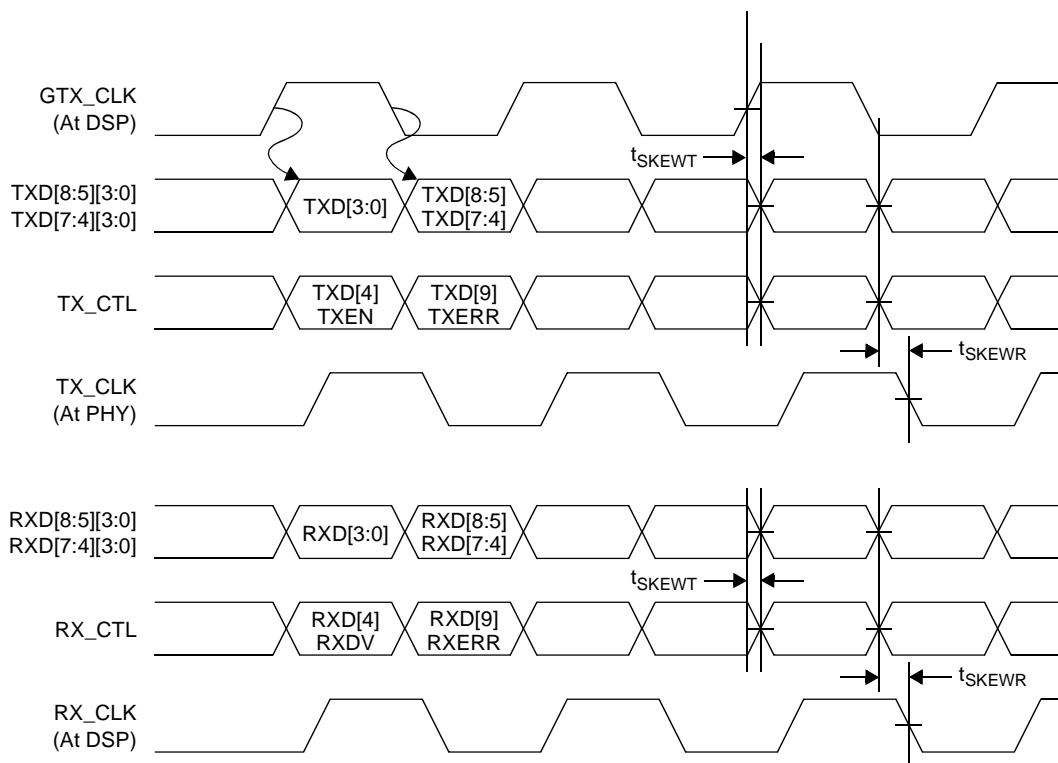


Figure 31. RGMII AC Timing and Multiplexing

2.6.11 ATM/UTOPIA/POS Timing

Table 47 provides the ATM/UTOPIA/POS input and output AC timing specifications.

Table 47. ATM/UTOPIA/POS AC Timing (External Clock) Specifications

Characteristic	Symbol	Min	Max	Unit
Outputs—External clock delay	t_{UEKHOV}	1	9	ns
Outputs—External clock High Impedance ¹	t_{UEKHOX}	1	9	ns
Inputs—External clock input setup time	t_{UEIVKH}	4		ns
Inputs—External clock input hold time	t_{UEIXKH}	1		ns

Notes:

1. Not tested. Guaranteed by design.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 32 provides the AC test load for the ATM/UTOPIA/POS.

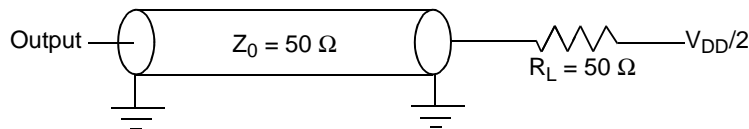


Figure 32. ATM/UTOPIA/POS AC Test Load

Figure 33 shows the ATM/UTOPIA/UTOPIA timing with external clock.

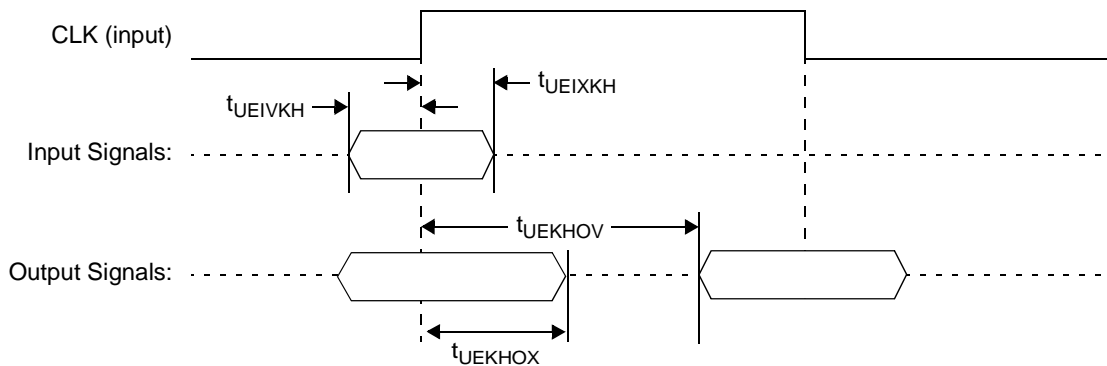


Figure 33. ATM/UTOPIA/POS AC Timing (External Clock)

2.6.12 SPI Timing

Table 48 lists the SPI input and output AC timing specifications.

Table 48. SPI AC Timing Specifications ¹

Characteristic	Symbol ²	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	$t_{NIKH OV}$		6	ns
SPI outputs hold—Master mode (internal clock) delay	$t_{NIKH OX}$	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	$t_{NEKH OV}$		8	ns
SPI outputs hold—Slave mode (external clock) delay	$t_{NEKH OX}$	2		ns
SPI inputs—Master mode (internal clock) input setup time	$t_{NIIV KH}$	4		ns
SPI inputs—Master mode (internal clock) input hold time	$t_{NIIX KH}$	0		ns
SPI inputs—Slave mode (external clock) input setup time	$t_{NEIV KH}$	4		ns
SPI inputs—Slave mode (external clock) input hold time	$t_{NEIX KH}$	2		ns

Notes:

- Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
- The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{NIKH OX}$ symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 34 provides the AC test load for the SPI.

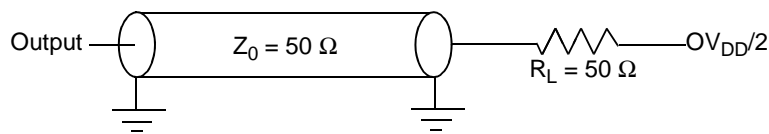
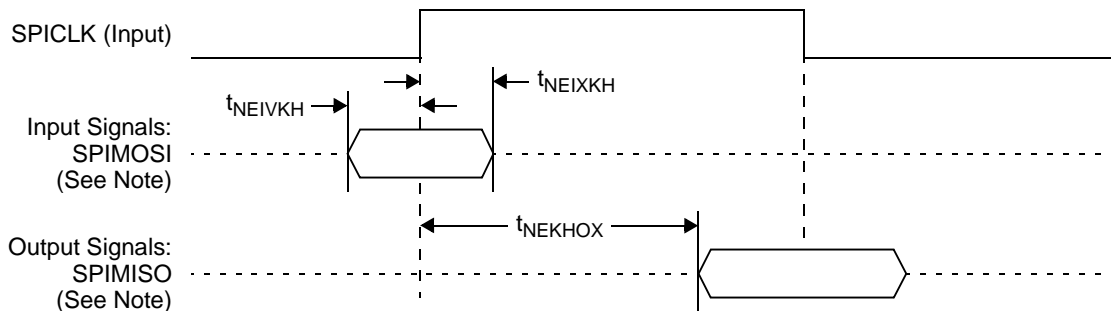


Figure 34. SPI AC Test Load

Figure 35 and Figure 36 represent the AC timings from Table 48. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

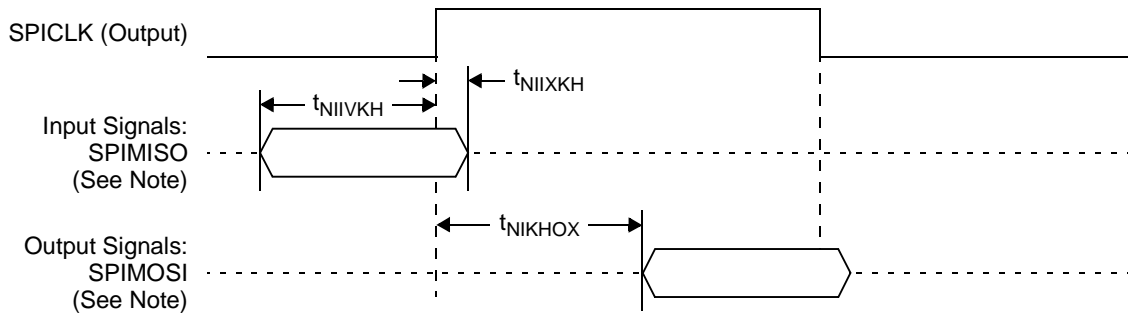
Figure 35 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Slave Mode (External Clock)

Figure 36 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC Timing in Master Mode (Internal Clock)

2.6.13 Asynchronous Signal Timing

Table 49. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN cycle ¹
Output	t_{OUT}	Asynchronous	Application dependent

Note: 1. Relevant for EE0, $\overline{IRQ[15-0]}$, and \overline{NMI} only.

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a GPI, the input should be driven until it is acknowledged by the device; the GPIO input status is read from a register.

- *EE port*. Signals EE0, EE1, EE2_0, EE2_1, EE2_2, and EE2_3.
- *Boot function*. Signal STOP_BS.
- *I²C interface*. Signals I2C_SCL and I2C_SDA.
- *Interrupt inputs*. Signals $\overline{IRQ[15-0]}$ and \overline{NMI} .
- *Interrupt outputs*. Signals $\overline{INT_OUT}$ and $\overline{NMI_OUT}$ (pulse width is 10 ns).

Figure 37 shows the behavior of the asynchronous signals.

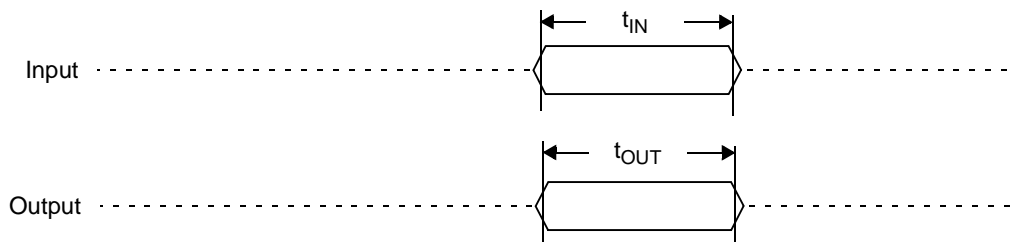


Figure 37. Asynchronous Signal Timing

2.6.14 JTAG Signals

Table 50. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at $V_M = 1.6\text{ V}$	t_{TCKH}	15.0	—	ns
TCK rise and fall times	t_{TCKR}	—	3.0	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
TRST assert time	t_{TRST}	100.0	—	ns

Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.

Figure 38 Shows the Test Clock Input Timing Diagram

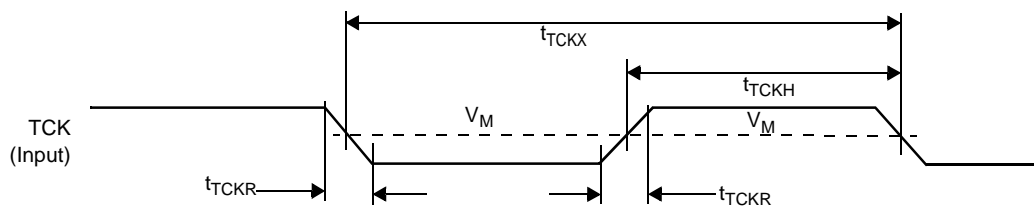


Figure 38. Test Clock Input Timing

Figure 39 Shows the boundary scan (JTAG) timing diagram.

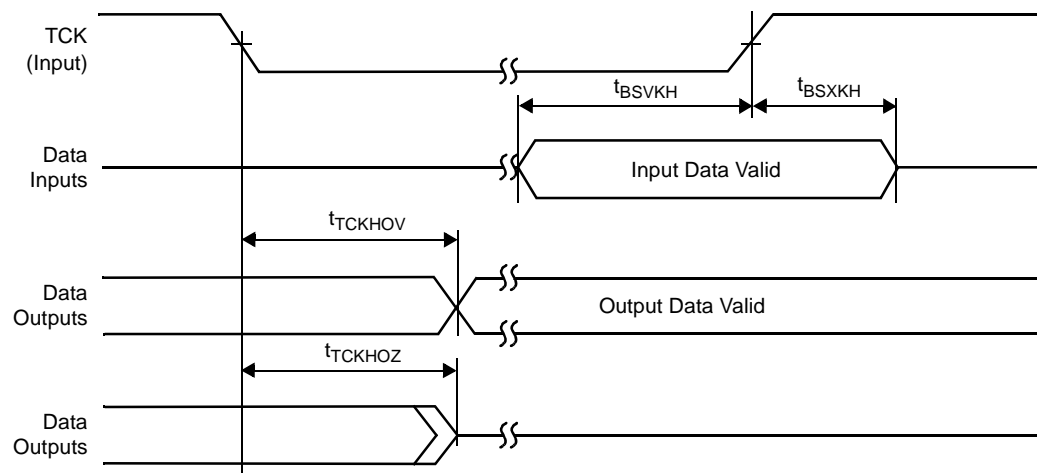


Figure 39. Boundary Scan (JTAG) Timing

Figure 40 Shows the test access port timing diagram

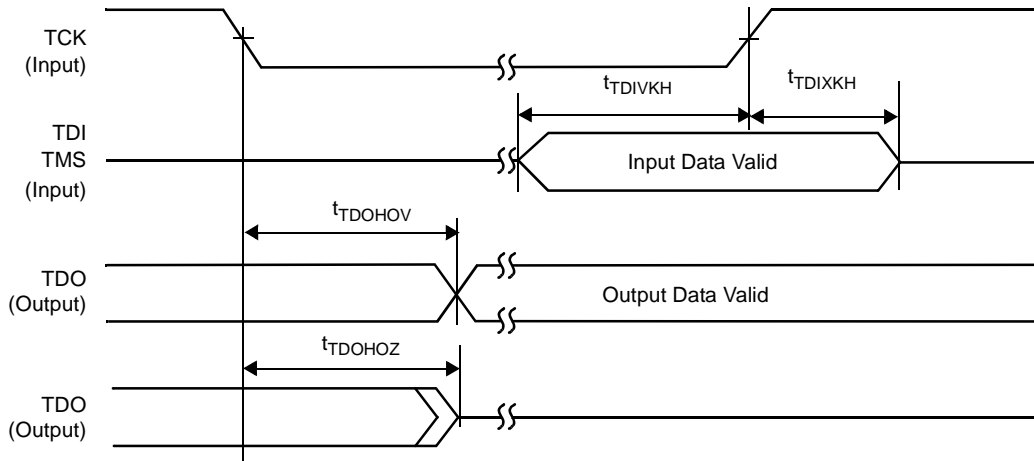


Figure 40. Test Access Port Timing

Figure 41 Shows the $\overline{\text{TRST}}$ timing diagram.



Figure 41. $\overline{\text{TRST}}$ Timing

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8144E device is designed into a system.

3.1 Start-up Sequencing Recommendations

3.1.1 Power-on Sequence

Use the following guidelines for power-on sequencing:

- There are no dependencies in power-on/power-off sequence between V_{DDM3} and V_{DD} supplies.
- There are no dependencies in power-on/power-off sequence between RapidIO supplies: V_{DDSCX} , V_{DDXP} , $V_{DDRIOPLL}$ and other MSC8144E supplies.
- V_{DDPLL} should be coupled with the V_{DD} power rail with extremely low impedance path.

External voltage applied to any input line must not exceed the related to this port I/O supply by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8144E device in the system during start-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4V/ns.

The following supplies should rise before any other supplies in any sequence

- V_{DD} and V_{DDPLL} coupled together
- V_{DDM3}

After the above supplies rise to 90% of their nominal value the following I/O supplies may rise in any sequence (see Figure 42):

- V_{DDGE1}
- V_{DDGE2}
- V_{DDIO}
- V_{DDDDR} and MV_{REF} coupled one to another. MV_{REF} should be either at same time or after V_{DDDDR} .
- V_{DDM3IO}
- V_{25M3}

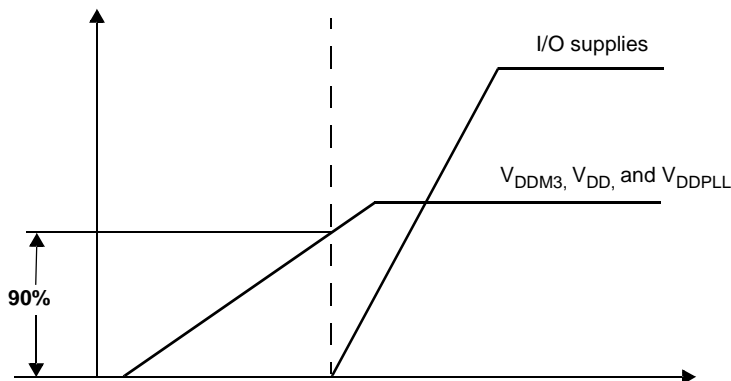


Figure 42. V_{DDM3} , V_{DDM3IO} and V_{25M3} Power-on Sequence

- Note:**
1. This recommended power sequencing is different from the MSC8122/MSC8126.
 2. If no pins that require V_{DDGE1} as a reference supply are used (see Table 1), V_{DDGE1} can be tied to GND.
 3. If no pins that require V_{DDGE2} as a reference supply are used (see Table 1), V_{DDGE2} can be tied to GND.
 4. If the DDR interface is not used, V_{DDDDR} and MV_{REF} can be tied to GND.
 5. If the M3 memory is not used, V_{DDM3} , V_{DDM3IO} , and V_{25M3} can be tied to GND.
 6. If the RapidIO interface is not used, V_{DDSX} , V_{DDXP} , and $V_{DDRIOPLL}$ can be tied to GND.

3.1.2 Start-Up Timing

Section 2.6.1 describes the start-up timing.

3.2 Power Supply Design Considerations

Each PLL supply must have an external RC filter for the V_{DDPLL} input. The filter is a 10 Ω resistor in series with two 2.2 μF , low ESL (<0.5 nH) and low ESR capacitors. All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately (see Figure 43). For optimal noise filtering, place the circuit as close as possible to its V_{DDPLL} inputs. These traces should be short and direct.

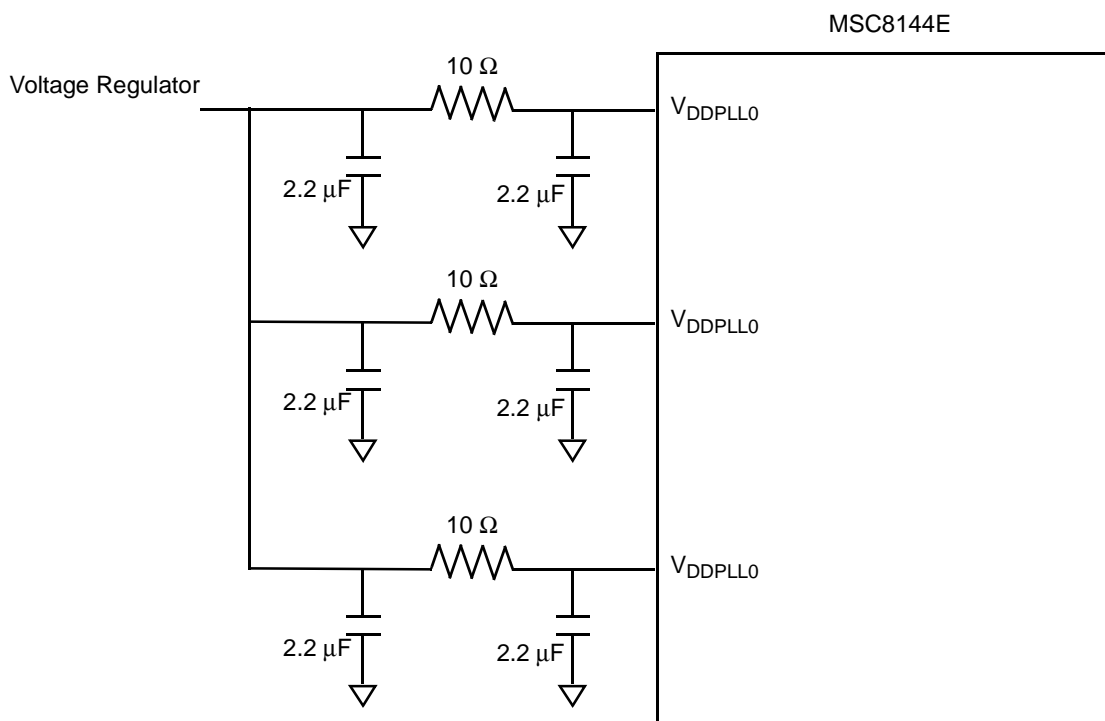


Figure 43. PLL Supplies

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

$$R_{term} = R_{im} - R_{buf}$$

where R_{im} = trace characteristic impedance

R_{buf} = clock buffer internal impedance.

Note: See *MSC8144 CLKIN and PCI_CLK_IN Board Layout* (AN3440) for an example layout.

3.4 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
2. V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor it is clearly indicated as “pull-up/pull-down”.

4. NC indicates “not connected” and means do not connect anything to the pin.
5. The phrase “in use” indicates a typical pin connection for the required function.

Note: Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.

3.4.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with DDR1 and DDR2 memory.

Note: For information about unused differential/non-differential pins in DDR1/DDR2 modes (that is, unused negative lines of strobes in DDR1), please refer to [Table 51](#).

3.4.1.1 DDR Interface Is Not Used

Table 51. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–31]	NC
MDQS[0–3]	NC
$\overline{\text{MDQS}}[0–3]$	NC
MA[0–15]	NC
MCK[0–2]	NC
$\overline{\text{MCK}}[0–2]$	NC
$\overline{\text{MCS}}[0–1]$	NC
MDM[0–3]	NC
MBA[0–2]	NC
$\overline{\text{MCAS}}$	NC
MCKE[0–1]	NC
MODT[0–1]	NC
MDIC[0–1]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[0–7]	NC
ECC_MDM	NC
ECC_MDQS	NC
$\overline{\text{ECC_MDQS}}$	NC
MV _{REF}	GND
V _{DDDDR}	GND
Note:	If the DDR controller is not used, disable the internal DDR clock by writing a 1 to the CLK11DIS bit in the System Clock Control Register (SCCR[CLK11DIS]). See Chapter 7, Clocks , in the <i>MSC8144E Reference Manual</i> for details.

3.4.1.2 16-Bit DDR Memory Only

Table 52 lists unused pin connection when using 16-bit DDR memory. The 16 most significant data lines are not used.

Table 52. Connectivity of DDR Related Pins When Using 16-bit DDR Memory Only

Signal Name	Pin connection
MDQ[0–15]	in use
MDQ[16–31]	pull-up to V _{DDDDR}
MDQS[0–1]	in use
MDQS[2–3]	pull-down to GND
$\overline{\text{MDQS}}[0–1]$	in use
$\overline{\text{MDQS}}[2–3]$	pull-up to V _{DDDDR}
MA[0–15]	in use
MCK[0–2]	in use
$\overline{\text{MCK}}[0–2]$	in use
$\overline{\text{MCS}}[0–1]$	in use
MDM[0–1]	in use
MDM[2–3]	NC
MBA[0–2]	in use
$\overline{\text{MCAS}}$	in use
MCKE[0–1]	in use
MODT[0–1]	in use
MDIC[0–1]	in use
$\overline{\text{MRAS}}$	in use
$\overline{\text{MWE}}$	in use
MV _{REF}	1/2*V _{DDDDR}
V _{DDDDR}	2.5 V or 1.8 V

3.4.1.3 ECC Unused Pin Connections

When the error code corrected mechanism is not used in any 32- or 16-bit DDR configuration, refer to Table 53 to determine the correct pin connections.

Table 53. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[0–7]	pull-up to V _{DDDDR}
ECC_MDM	NC
ECC_MDQS	pull-down to GND
$\overline{\text{ECC_MDQS}}$	pull-up to V _{DDDDR}

3.4.2 Serial RapidIO Interface Related Pins

3.4.2.1 Serial RapidIO interface Is Not Used

Table 54. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	GND
SRIO_IMP_CAL_TX	GND
$\overline{\text{SRIO_REF_CLK}}$	GND
SRIO_REF_CLK	GND
SRIO_RXD[0–3]	GND
$\overline{\text{SRIO_RXD[0–3]}}$	GND
$\overline{\text{SRIO_TXD[0–3]}}$	NC
SRIO_TXD[0–3]	NC
V _{DDRIOPLL}	GND
GND _{RIOPLL}	GND
GND _{SXP}	GND
GND _{SXC}	GND
V _{DDSXP}	GND
V _{DDSXC}	GND

3.4.2.2 Serial RapidIO Specific Lane Is Not Used

Table 55. Connectivity of Serial RapidIO Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	in use
SRIO_IMP_CAL_TX	in use
$\overline{\text{SRIO_REF_CLK}}$	in use
SRIO_REF_CLK	in use
SRIO_RXD _x	GND _{SXC}
$\overline{\text{SRIO_RXD}_x}$	GND _{SXC}
$\overline{\text{SRIO_TXD}_x}$	NC
SRIO_TXD _x	NC
V _{DDRIOPLL}	in use
GND _{RIOPLL}	in use
GND _{SXP}	GND _{SXP}
GND _{SXC}	GND _{SXC}
V _{DDSXP}	1.0 V
V _{DDSXC}	1.0 V

Note: The **x** indicates the lane number {0,1,2,3} for all unused lanes.

3.4.3 M3 Memory Related Pins

Table 56. Connectivity of M3 Related Pins When M3 Memory Is Not Used

Signal Name	Pin Connection
M3_RESET	NC
V _{25M3}	GND
V _{DDM3}	GND
V _{DDM3IO}	GND

3.4.4 Ethernet Related Pins

3.4.4.1 Ethernet Controller 1 (GE1) Related Pins

Note: Table 57 and Table 58 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.4.4.1.1 GE1 Interface Is Not Used

Table 57 assumes that the GE1 signals are not used for any purpose (including any multiplexed functions) and that V_{DDGE1} is tied to GND.

Table 57. Connectivity of GE1 Related Pins When the GE1 Interface Is Not Used

Signal Name	Pin Connection
GE1_COL	NC
GE1_CRS	NC
GE1_RD[0–4]	NC
GE1_RX_ER	NC
GE1_RX_CLK	NC
GE1_RX_DV	NC
GE1_SGMII_RX	GND _{SXC}
GE1_SGMII_RX	GND _{SXC}
GE1_SGMII_TX	NC
GE1_SGMII_TX	NC
GE1_TD[0–4]	NC
GE1_TX_CLK	NC
GE1_TX_EN	NC
GE1_TX_ER	NC

3.4.4.1.2 Subset of GE1 Pins Required

When only a subset of the whole GE1 interface is used, such as for RMII, the unused GE1 pins should be connected as described in Table 58. This table assumes that the unused GE1 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE1} is tied to either 2.5 V or 3.3 V.

Table 58. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE1_COL	GND
GE1_CRS	GND
GE1_RD[0-3]	GND
GE1_RX_ER	GND
GE1_RX_CLK	GND
GE1_RX_DV	GND
GE1_SGMII_RX	GND _{SXC}
$\overline{\text{GE1_SGMII_RX}}$	GND _{SXC}
$\overline{\text{GE1_SGMII_TX}}$	NC
GE1_SGMII_TX	NC
GE1_TD[0-3]	NC
GE1_TX_CLK	GND
GE1_TX_EN	NC
GE1_TX_ER	NC

3.4.4.2 Ethernet Controller 2 (GE2) Related Pins

Note: Table 59 through Table 61 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.4.4.2.1 GE2 interface Is Not Used

Table 59 assumes that the GE2 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE2} is tied to GND.

Table 59. Connectivity of GE2 Related Pins When the GE2 Interface Is Not Used

Signal Name	Pin Connection
GE2_RD[0-3]	NC
GE2_RX_CLK	NC
GE2_RX_DV	NC
GE2_RX_ER	NC
GE2_SGMII_RX	GND _{SXC}
$\overline{\text{GE2_SGMII_RX}}$	GND _{SXC}
$\overline{\text{GE2_SGMII_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	Nc

Table 59. Connectivity of GE2 Related Pins When the GE2 Interface Is Not Used (continued)

Signal Name	Pin Connection
GE2_TD[0–3]	Nc
GE2_TX_EN	NC

3.4.4.2.2 Subset of GE2 Pins Required

When only a subset of the whole GE2 interface is used, such as for RMII, the unused GE2 pins should be connected as described in [Table 60](#). The table assumes that the unused GE2 pins are not used for any purpose (including any multiplexed functions) and that V_{DDGE2} is tied to either 2.5 V or 3.3 V.

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE2_RD[0-3]	GND
GE2_RX_CLK	GND
GE2_RX_DV	GND
GE2_RX_ER	GND
GE2_SGMII_RX	GND _{SXC}
$\overline{\text{GE2_SGMII_RX}}$	GND _{SXC}
$\overline{\text{GE2_SGMII_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	NC
GE2_TD[0–3]	NC
GE2_TX_EN	NC

3.4.4.3 GE1 and GE2 Management Pins

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used (that is, V_{DDGE2} is connected to GND), [Table 61](#) lists the recommended management pin connections.

Table 61. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

3.4.5 UTOPIA/POS Related Pins

Table 62 lists the board connections of the UTOPIA/POS pins when the entire UTOPIA/POS interface is not used or subset of UTOPIA/POS interface is used. For multiplexing options that select a subset of the UTOPIA/POS interface, use the connections described in Table 62 for those signals that are not selected. Table 62 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 62. Connectivity of UTOPIA/POS Related Pins When UTOPIA/POS Interface Is Not Used

Signal Name	Pin Connection
UTP_IR	GND
UTP_RADDR[0–4]	V _{DDIO}
UTP_RCLAV_PDRPA	NC
UTP_RCLK	GND
UTP_RD[0–15]	GND
$\overline{\text{UTP_REN}}$	V _{DDIO}
UTP_RPRTY	GND
UTP_RSOC	GND
UTP_TADDR[0–4]	V _{DDIO}
UTP_TCLAV	NC
UTP_TCLK	GND
UTP_TD[0–15]	NC
$\overline{\text{UTP_TEN}}$	V _{DDIO}
UTP_TPRTY	NC
UTP_TSOC	NC
V _{DDIO}	3.3 V

3.4.6 TDM Interface Related Pins

Table 63 lists the board connections of the TDM pins when an entire specific TDM is not used. For multiplexing options that select a subset of a TDM interface, use the connections described in Table 63 for those signals that are not selected. Table 63 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 63. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM _x RCLK	GND
TDM _x RDAT	GND
TDM _x RSYN	GND
TDM _x TCLK	GND
TDMT _x DAT	GND
TDM _x TSYN	GND
V _{DDIO}	3.3 V
Notes: <ol style="list-style-type: none"> 1. $x = \{0, 1, 2, 3, 4, 5, 6, 7\}$ 2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See Chapter 20, TDM, in the <i>MSC8144E Reference Manual</i> for details. 	

3.4.7 PCI Related Pins

Table 64 lists the board connections of the pins when PCI is not used. Table 64 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 64. Connectivity of PCI Related Pins When PCI Is Not Used

Signal Name	Pin Connection
PCI_AD[0–31]	GND
PCI_CBE[0–3]	GND
PCI_CLK_IN	GND
PCI_DEVSEL	V _{DDIO}
PCI_FRAME	V _{DDIO}
PCI_GNT	V _{DDIO}
PCI_IDS	GND
PCI_IRDY	V _{DDIO}
PCI_PAR	GND
PCI_PERR	V _{DDIO}
PCI_REQ	NC
PCI_SERR	V _{DDIO}
PCI_STOP	V _{DDIO}
PCI_TRDY	V _{DDIO}
V _{DDIO}	3.3 V

3.4.8 Miscellaneous Pins

Table 65 lists the board connections for the pins if they are not required by the system design. Table 65 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 65. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[0–31]	GND
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
INT_OUT	NC
IRQ[0–15]	See the GPIO connectivity guidelines in this table.
NMI	V _{DDIO}
NMI_OUT	NC
RC[0–16]	GND
RC_LDF	NC
STOP_BS	GND

Table 65. Connectivity of Individual Pins When They Are Not Required (continued)

Signal Name	Pin Connection
TCK	GND
TDI	GND
TDO	NC
TMR[0–4]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	GND
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
V _{DDIO}	3.3 V
Note:	When using I/O multiplexing mode 5 or 6, tie the TDM7TSYN/PCI_AD4 signal (ball number AC9) to GND.

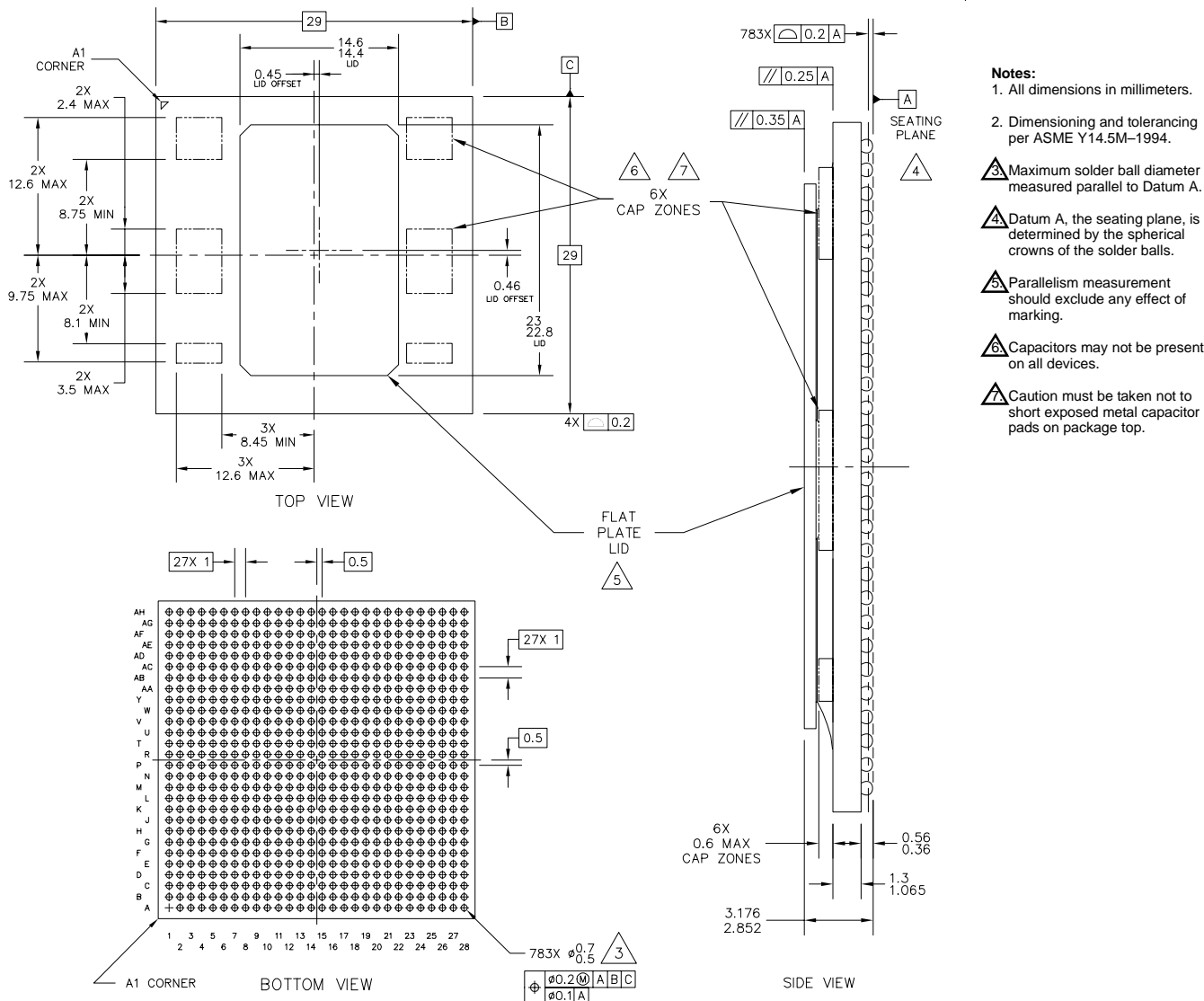
Note: For details on configuration, see the *MSC8144E Reference Manual*. For additional information, refer to the *MSC8144 Design Checklist (AN3202)*.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Spheres	Mask #	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number
MSC8144E	Flip Chip Plastic Ball Grid Array (FC-PBGA)	Lead-free	0M31H	1.0 V	0° to 90°C	800	MSC8144EVT800A
					0° to 105°C	800	MSC8144ESVT800A
					–40° to 105°C	800	MSC8144ETVT800A
					0° to 90°C	1000	MSC8144EVT1000A
					0° to 105°C	1000	MSC8144ESVT1000A
					–40° to 105°C	1000	MSC8144ETVT1000A
			1M31H	1.0 V	0° to 90°C	800	MSC8144EVT800B
					0° to 105°C	800	MSC8144ESVT800B
					–40° to 105°C	800	MSC8144ETVT800B
					0° to 90°C	1000	MSC8144EVT1000B
					0° to 105°C	1000	MSC8144ESVT1000B
					–40° to 105°C	1000	MSC8144ETVT1000B
Note:	See Table 3 for Core Voltage tolerance limits.						

5 Package Information



- Notes:**
1. All dimensions in millimeters.
 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder ball diameter measured parallel to Datum A.
 - Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
 - Parallelism measurement should exclude any effect of marking.
 - Capacitors may not be present on all devices.
 - Caution must be taken not to short exposed metal capacitor pads on package top.

CASE NO. 1842-04

Figure 44. MSC8144E Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

- *MSC8144E Technical Data Sheet (MSC8144E)*. Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8144E device.
- *MSC8144E Reference Manual (MSC8144ERM)*. Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8144E device.
- *SC3400 DSP Core Reference Manual*. Covers the SC3400 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 66 provides a revision history for this data sheet.

Table 66. Document Revision History

Revision	Date	Description
0	June. 2007	<ul style="list-style-type: none"> Initial public release.
1	Sep 2007	<ul style="list-style-type: none"> Updated M3 voltage range in Table 3. Changed note in Table 7 for PLL power supplies. DDR voltage designator changed from V_{DD} to V_{DDDDR} in Table 8, Table 10, Section 2.7.4.1, Section 2.7.4.2, and Figure 11. Changed range on I_{OZ} in Table 8 and Table 10. Deleted text before Table 13 and added note 2 to input pin capacitance. Deleted text before Table 14, added a 1 to the note, and added note 1 to input pin capacitance. Deleted Section 2.6.5 on page 32 and renumbered subsequent subsections. Deleted text before new Section 2.6.5.1. Added a 1 to the note in Table 15 and added note 1 to input pin capacitance. Deleted ac voltage rows from Table 16. Added note 1 to input pin capacitance. Changed output high and low voltage levels in Table 17 and Table 18. Deleted text before Table 19. Added clock skew ranges in percent in Table 21. Changed V_{REF} to MV_{REF} in Table 26. Changed V_{DD} to V_{DDIO} in Table 36 Updated note 2. Added note 4 to Table 42. Changed t_{DMSHOX} value. Changed V_{DD} to V_{DDGE} in Figure 27 and Figure 30. Changed the value of the data to clock out skew in Table 51. Changed EE pin timing in Table 55. Changed the head for the JTAG timing section, now Section 2.7.14. Updated JTAG timing for TCK cycle time, TCK high phase, and boundary scan input data hold time in Table 55. Added new Section 3.3 with guidelines for board layout for clock and timing signals. Renumbered subsequent sections.
2	Sep 2007	<ul style="list-style-type: none"> Changed leakage current values in Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, and Table 19 from -10 and $10 \mu\text{a}$ to -30 and $30 \mu\text{a}$. Change the minimum value of t_{MDDVKH} in Table 45 from 5 ns to 7 ns. Updated note 1 in Table 45.
3	Oct 2007	<ul style="list-style-type: none"> Corrected column numbering in Figure 3 and Figure 4. Updated SPI signal names in Table 1.
4	Oct 2007	<ul style="list-style-type: none"> Updated SPI signal names in Table 1.
5	Dec 2007	<ul style="list-style-type: none"> Changed minimum voltage level for V_{DDM3} to 1.213 (1.25 – 3%) in Table 3. Added POS to titles in Section 2.6.6. Added additional signals to titles in Section 2.6.8. Added high and low voltage ranges to Table 19. Added ATM and POS to headings in Section 2.7.11. Changed characteristics to generic input/output in Table 52, Figure 33, and Figure 34. Replaced Sections 2.7.13 and 2.7.14 with new Section 2.7.13. Renumbered subsequent sections, tables, and figures. Added POS to all UTOPIA references in Section 3.4.5.
6	Dec 2007	<ul style="list-style-type: none"> Changed GCR4 program value to 0x0004C130 in Note 7 in Table 51.
7	Mar 2008	<ul style="list-style-type: none"> Changed description of Table 16 in Section 2.7.2.
8	Apr 2008	<ul style="list-style-type: none"> Added ³ to the PLL supply voltage row in Table 2. Changed the first sentence in Section 3.4.8 to reflect that Table 70 indicates what to do with pins if they are “not” required by the design. Changed the Pin Connection for GPIO[0–31] to GND. Updated ordering information in Section 4. Multiple corrections of minor punctuation errors.

Table 66. Document Revision History (continued)

Revision	Date	Description
9	Aug 2008	<ul style="list-style-type: none"> Removed the comment about preliminary estimates before Table 4 and removed non-DDR rows in the table. Table 9 and Table 11 for DDR and DDR2 SDRAM capacitance removed and subsequent tables renumbered. Changed units for I_{OH} and I_{OL} to mA in Table 9. Removed signal low and high input current from Table 12. Added a note to Table 15 to exclude TDM and TMS. Removed reference to overshoot and undershoot and associated figure. Changed \overline{TRST} deassertion description in Section 3.1. Changed minimum clock frequency to 33 MHz and maximum clock frequency to 133 MHz in Table 16. Changed minimum input clock frequency to 33 MHz in Table 19. Changed the t_{DDKHAX} minimum value in Table 23 to 1.85 ns. Removed t_{REFFJ} and t_{REFCJ} from Table 24 because the specifications are not required or tested. Removed $t_{PCRSTCLK}$, $t_{PCRSTOFF}$, t_{PCRST}, and $t_{PCRHEFA}$ from Table 36 because the specifications are not required or tested. Removed t_{UAVKH} and t_{UAVXH} from Table 38 because the specifications are not required or tested. The parameters t_{MDCH}, t_{MDCR}, and t_{MDHF} were removed from Table 40 because the specifications are not required or tested. The parameters t_{MTXH}/t_{MTX}, t_{MTXR}, and t_{MTXF} were removed from Table 41 because the specifications are not required or tested. The parameters t_{MRXH}/t_{MRX}, t_{MRXR}, and t_{MRXF} were removed from Table 42 because the specifications are not required or tested. The parameters t_{RMXH}/t_{RMX}, t_{RMXR}, and t_{RMXF} were removed from Table 43 because the specifications are not required or tested. Changed the GTX_CLK125 reference clock duty cycle to 45%–55% in Table 45 and Table 46 and the parameters t_{RGT}, t_{RGTH}/t_{RGT} (1000Base-T), t_{RGTH}/t_{RGT} (10Base-T), t_{RGTR}, t_{RGTF}, t_{G12}, and t_{G125H}/t_{G125} were removed because the specifications are not required or tested. Changed t_{UEKHOX} to guaranteed by design in Table 47. Updated orderable part numbers in Section 4.
10	Aug 2008	<ul style="list-style-type: none"> Changed b8t to bit in the M3 memory description on the first page. Changed maximum input high voltage (V_{IH}) for SPI to 3.465 in the first row of Table 14. Changed packet processor to QUICC Engine Subsystem in the last row of Table 18.
11	Feb 2009	<ul style="list-style-type: none"> In Figure 31, for GTX_CLK, changed (at transmitter) to (at DSP) and for RX_CLK, changed (at PHY) to (at DSP). Updated package drawing to the latest revision, Case No. 1842-04 in Figure 44.
12	Jul 2009	<ul style="list-style-type: none"> Updated MV_{REF} equations and temperature ranges in Table 3. Updated orderable part numbers in Section 4.
13	Nov 2009	<ul style="list-style-type: none"> Updated Core and PLL input voltage tolerance in Table 3.
14	May 2010	<ul style="list-style-type: none"> Corrected typo in Table 23. Changed MCLK minimum time to 5 ns.

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