CY8CKIT-038

PSoC® 4200 Family Processor Module Kit Guide

Doc. # 001-85916 Rev. *A

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intnl): 408.943.2600
http://www.cypress.com

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Contents

Safety Information

Regulatory Compliance

The CY8CKIT-038 is intended for use as a development platform for hardware or software in a laboratory environment. The board is an open system design, which does not include a shielded enclosure. This may cause interference to other electrical or electronic devices in close proximity. In a domestic environment, this product may cause radio interference. In this case, take adequate prevention measures. Also, do not use the board near any medical equipment or RF devices.

Attaching additional wiring to this product or modifying the product operation from the factory default may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

The CY8CKIT-038, as shipped from the factory, has been verified to meet with requirements of CE as a Class A product.

The CY8CKIT-038 contains electrostatic discharge (ESD) sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused CY8CKIT-038 boards in the protective shipping package.

End-of-Life / Product Recycling

The end-of life for this kit is after five years from the date of manufacturing mentioned on the back of the box. Contact your nearest recycler for dispositioning the kit.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that you perform procedures only at an ESD workstation. If one is not available, use appropriate ESD protection by wearing an antistatic wrist strap attached to chassis ground (any unpainted metal surface) on your board when handling parts.

Handling Boards

CY8CKIT-038 boards are sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static free surface. Use a conductive foam pad if available. Do not slide board over any surface.

1. Introduction

Thank you for your interest in the CY8CKIT-038 PSoC® 4200 Family Processor Module Kit. This kit allows you to develop applications on various products such as the sensor-less e-bike, white goods, field oriented control (FOC) motor control, and home appliances. You can also design your own projects with PSoC Creator™, the integrated design environment (IDE) for PSoC devices.

The CY8CKIT-038 Processor Module is a PSoC 4200 family processor module designed for the CY8CKIT-001 DVK. PSoC 4200 is a family of programmable embedded system devices with an ARM Cortex-M0 CPU. It combines programmable analog, programmable interconnect, and user programmable digital logic with a high-performance ARM Cortex-M0 subsystem.

1.1 Kit Contents

This kit contains:

- CY8CKIT-038 processor module
- I2C character LCD
- Quick start guide
- Kit CD/DVD

You can purchase this kit and download the example projects at http:/www.cypress.com/go/CY8CKIT-038

Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help or visit www.cypress.com/support.

1.2 PSoC Creator

Cypress's PSoC Creator software is a state-of-the-art, easy-to-use software development IDE. It introduces a hardware and software co-design environment based on classical schematic entry and revolutionary embedded design methodology.

With PSoC Creator, you can:

- Create and share user-defined, custom peripherals using a hierarchical schematic design.
- Automatically place and route select components and integrate simple glue logic normally residing in discrete muxes.
- Trade-off hardware and software design considerations allowing you to focus on what matters and get to market faster.

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler tool chains, RTOS solutions, and production programmers to support PSoC devices.

For more information, visit the PSoC Creator web page.

1.3 Additional Learning Resources

Visit www.cypress.com/Products/Programmable System-on-Chip for additional learning resources in the form of datasheets, technical reference manual, and application notes.

- Beginner Resources: PSoC Creator Training
  - Getting Started With PSoC 4
- Learning from Peers: Cypress Developer Community Forums

1.4 Document Revision History

Table 1-1. Revision History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	05/10/2013	SRYP	Initial version of kit guide
*A	09/26/2013	SASH	Updated images for PSoC Creator 3.0

1.5 Documentation Conventions

Table 1-2. Document Conventions for Guides

Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes Cautions or unique functionality of the product.

2. Getting Started

This chapter describes how to install and configure the CY8CKIT-038 PSoC 4200 Family Processor Module kit software. Chapter 3 shows you how to program the kit, Chapter 4 documents the hardware features of the kit, and Chapter 5 explains the operation of the code examples. The Appendix section provides the schematics, PCB layout, and bill of materials (BOM) associated with the kit.

2.1 CD/DVD Installation

Follow these steps to install the CY8CKIT-038 PSoC 4200 Family Processor Module Kit software:

1. Insert the kit CD/DVD into your PC's CD/DVD drive. The CD/DVD is designed to auto-run. If auto-run does not execute, double click **AutoRun** on the root of the CD/DVD.
2. After the installation is complete, the kit contents are available at the following location:
   `<InstallDirectory>\PSoC 4200 Processor Module Kit\<version>`

2.2 Install Hardware

No hardware installation is required for this kit. The processor module is designed to be used in conjunction with the CY8CKIT-001.

2.3 Install Software

When installing the CY8CKIT-038 PSoC 4200 Family Processor Module Kit, the installer checks if your system has the required software. These include PSoC Creator, PSoC Programmer, Windows Installer, .NET, Acrobat Reader, and Keil complier. If these applications are not installed, the installer prompts you to download and install them.

The following software needs to be installed that are specified in the CD/DVD:

- PSoC Creator 3.0 or later
- PSoC Programmer 3.19.1 or later
  Note Select the **Typical** installation type for all installations.

Code examples are provided in the Firmware folder of the kit installer.

2.4 Uninstall Software

The software can be uninstalled using one of the following methods:

- Go to **Start** > **Control Panel** > **Programs** > **Uninstall Programs;** select the **Uninstall** tab for Windows.
- Go to **Start** > **All Programs** > **Cypress** > **Cypress Update Manager** > **Cypress Update Manager**; select the **Uninstall** button next to the software that needs to be uninstalled.

2.5 Verify Kit Version

To know the kit revision, look for the white sticker on the bottom left, on the reverse of the kit box. If the revision reads CY8CKIT-038 Rev **, then, you own the latest version.

3. Kit Operation

The CY8CKIT-038 PSoC 4200 Family Processor Module Kit should be mounted on the CY8CKIT-001 DVK. The serial wire debugger (SWD) interface is available for programming/debugging on the processor module board, as shown in the Figure 3-1.

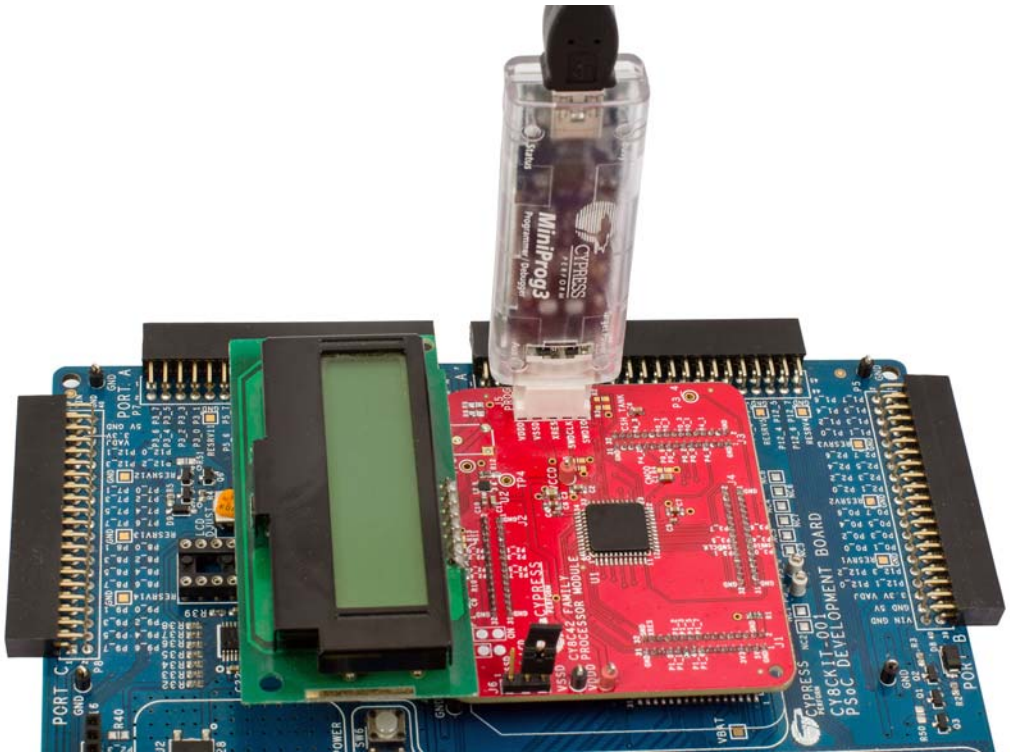
3.1 Programming CY8CKIT-038

This section provides details on how to program the PSoC 4200 family device by using the "VoltageDisplay_SAR_DAC" example project.

Follow this procedure to program a project onto the PSoC 4200 family device:

1. Connect the PSoC 4200 family processor module on the CY8CKIT-001 DVK.
2. Apply the power to the CY8CKIT-001 DVK using either the battery connections or a wall power unit using 12-V AC adapter.
3. Connect the MiniProg3 to the processor module on the 5-pin programming header J5, as shown in Figure 3-1; then, connect it to the host PC's USB high-speed port using a USB cable.

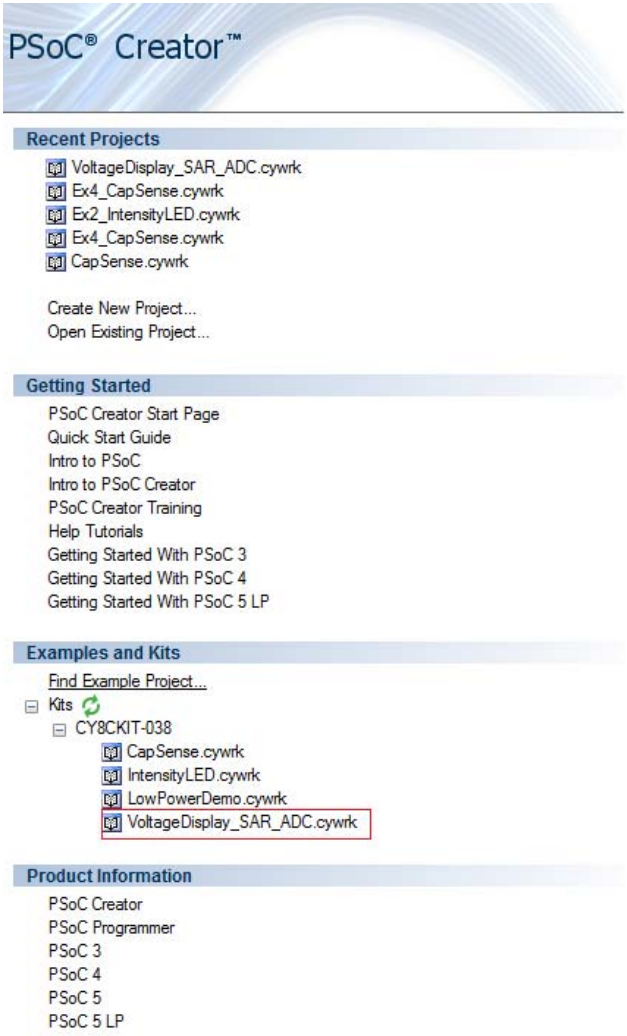
Figure 3-1. Connecting CY8CKIT-038 and MiniProg3 with CY8CKIT-001 DVK



Note Refer to CY8CKIT-001 PSoC Development Kit Board Guide for more details on connections.

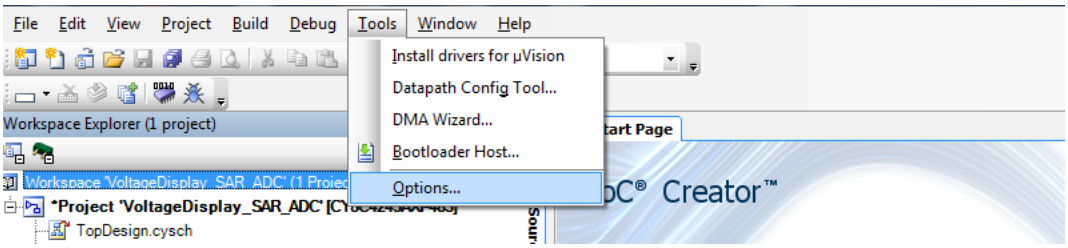
4. Open PSoC Creator. Click on the **VoltageDisplay_SAR_ADC** example project from the **Kits** folder present on the **Start Page**.

Figure 3-2. Kit Projects in the PSoC Creator Start Page



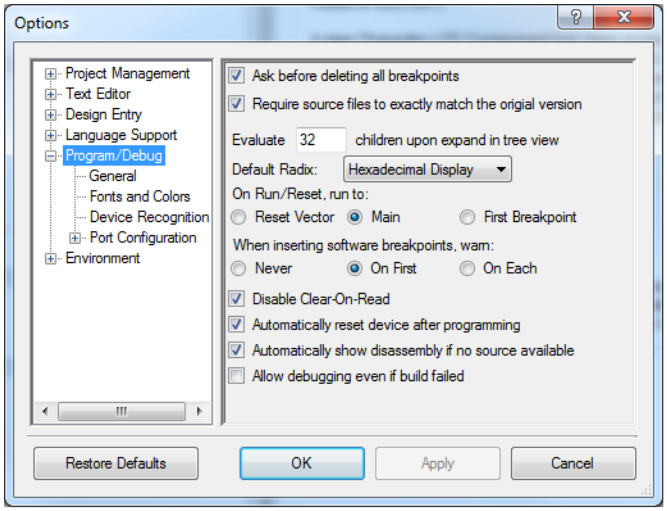
5. Create a folder in the desired location and click **OK.**
6. The project opens up in PSoC Creator and is saved in that folder.
7. Go to the **Tools** menu select **Options**.

Figure 3-3. Tools > Options



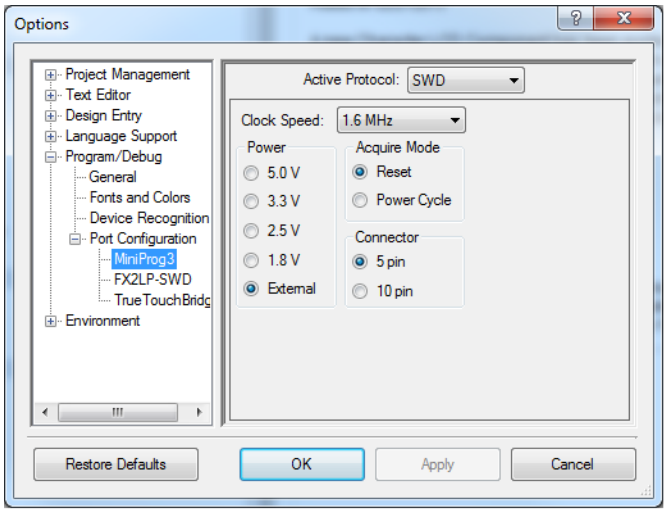
8. Go to **Program/Debug.**

Figure 3-4. Program/Debug Option



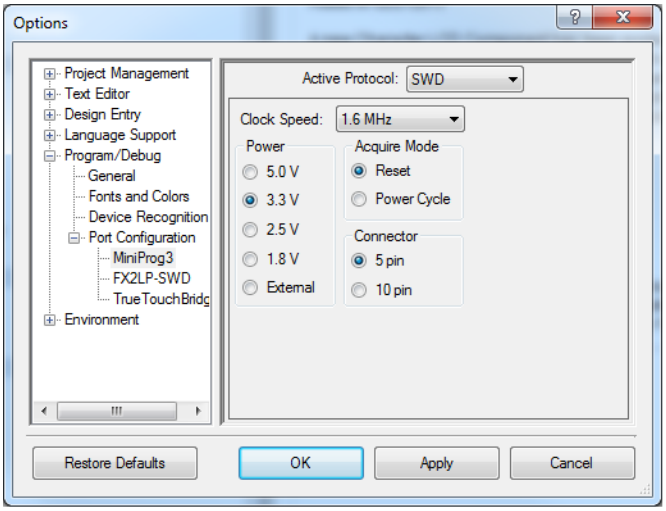
9. Select **Port Configuration** and click **MiniProg3**.

Figure 3-5. Select MiniProg3



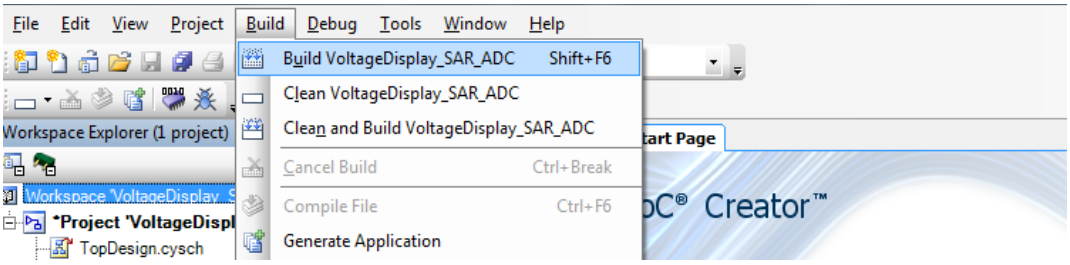
10. Configure **MiniProg3** using the following settings.

Figure 3-6. MiniProg3 Configurations



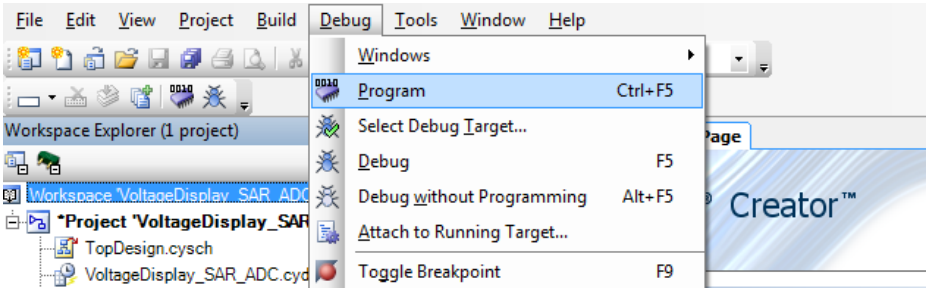
11. Build the project by selecting the **Build** option.

Figure 3-7. Build Option



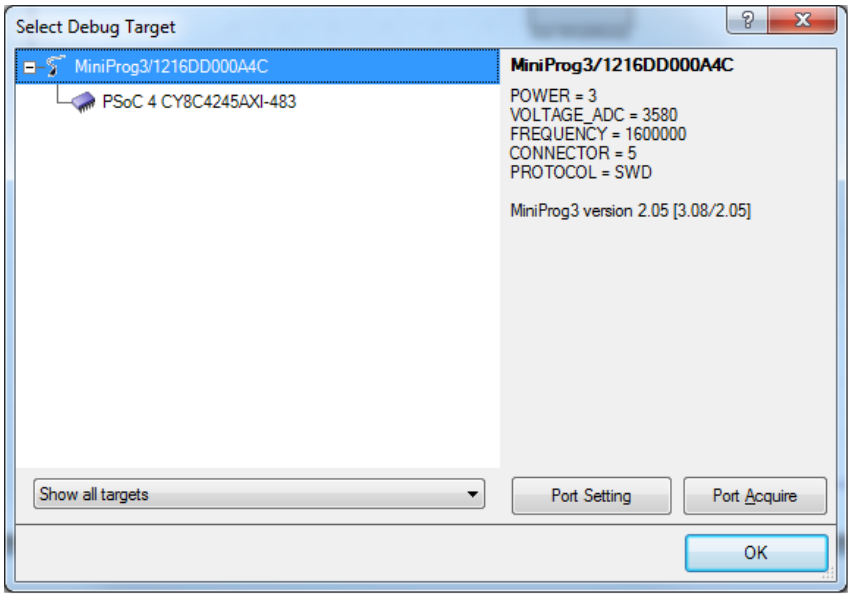
12. Click the **Program** icon.

Figure 3-8. Program Option



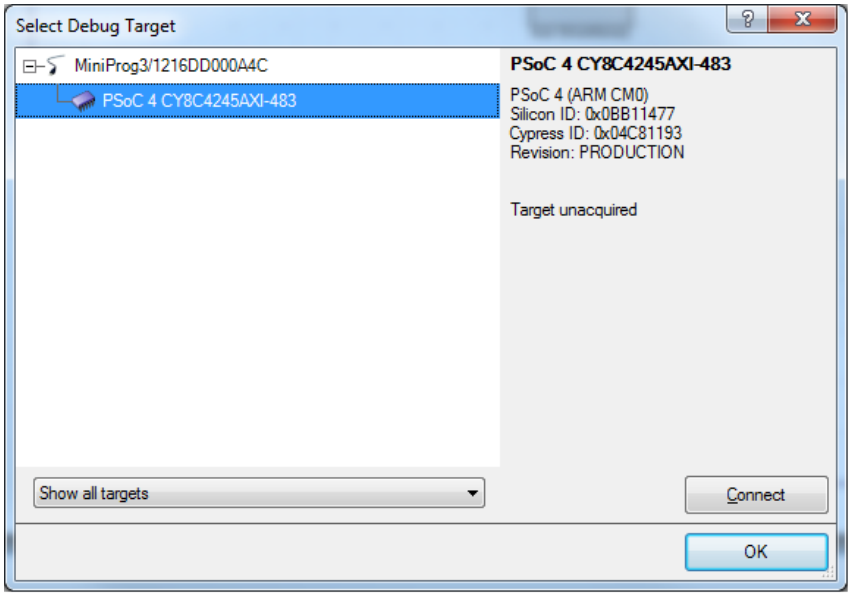
In some cases, when you click the **Program** tab, the following window pops up.

Figure 3-9. Select Debug Target Window



Click on **Port Acquire**. Click **Connect** and then select **OK** to program the device.

Figure 3-10. Program Device



13. After successful programming, a prompt message is displayed in the output window (see Figure 3-11).

Figure 3-11. Successful Programming Message in Output Window

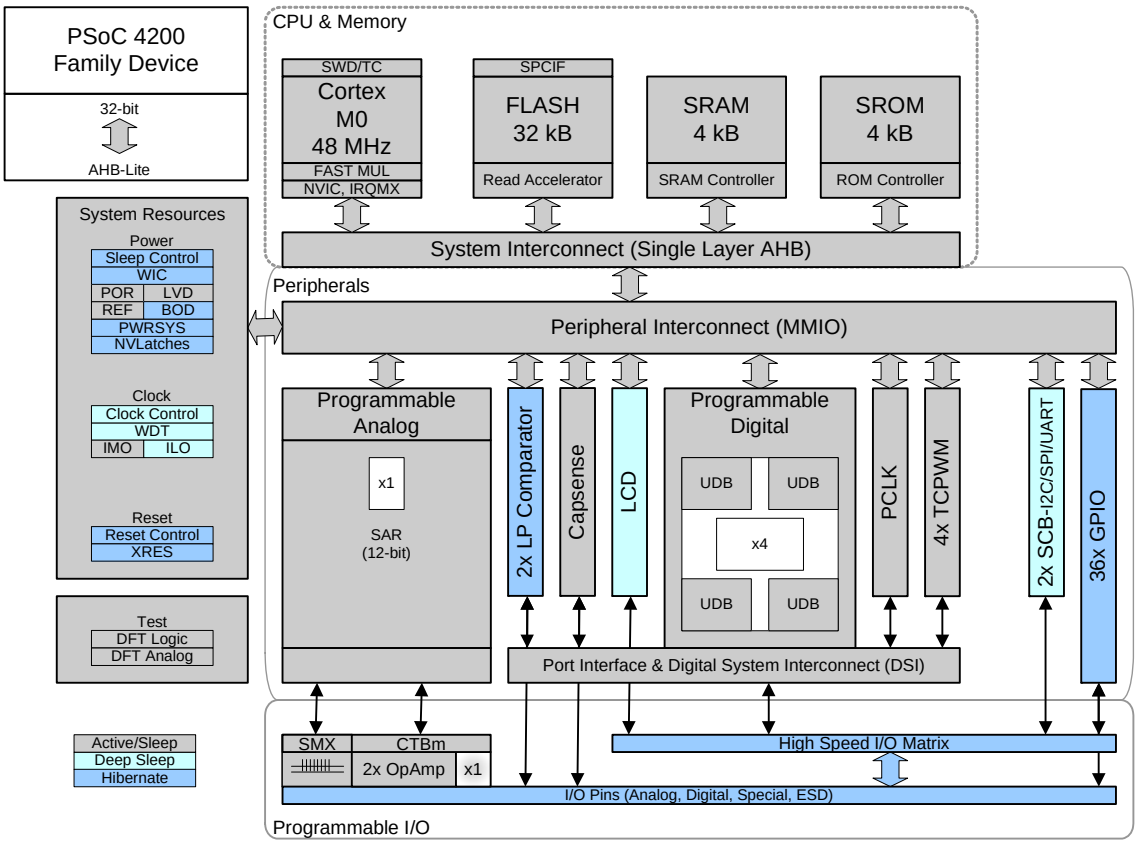
```
--------------- Build Succeeded: 04/02/2013 11:43:36 ---------------
Programming started for device: 'PSoC 4 CY8C4245AXI-483'.
Device ID Check
Erasing...
Programming of Flash Starting...
Protecting...
Verify Checksum...
Device 'PSoC 4 CY8C4245AXI-483' was successfully programmed at 04/02/2013 11:43:39.
```

Note Refer to Example Projects chapter on page 19 for more example projects.

4. Hardware

4.1 System Block Diagram

Figure 4-1. PSoC 4200 Family Block Diagram

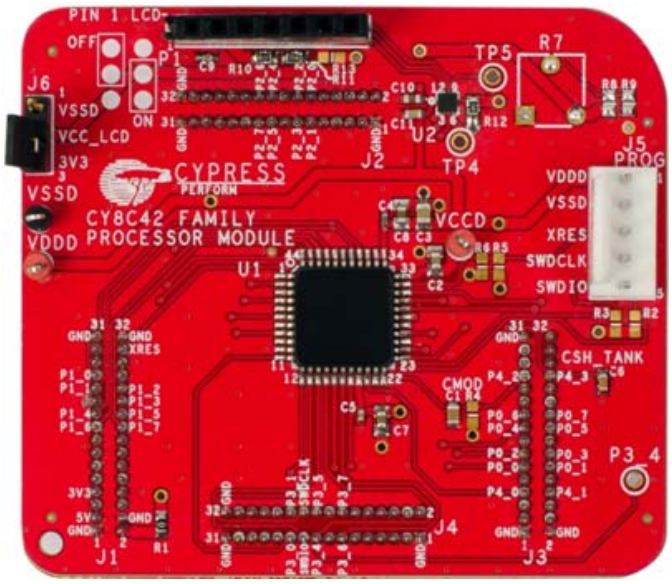


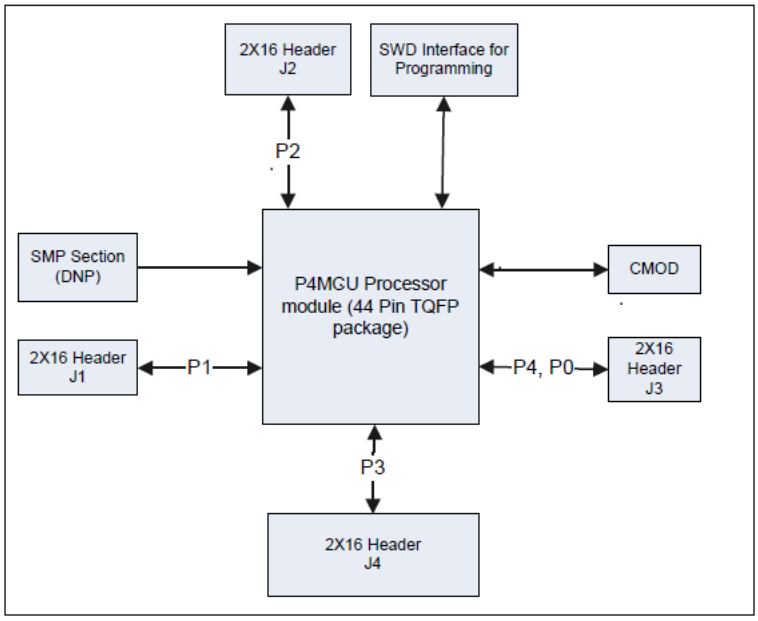
Features

- 48-MHz Cortex-M0 CPU (0.9 DMIPS/MHz)
- 32-KB flash and 4-KB SRAM
- Programmable logic: Four universal digital blocks
- Analog blocks: 12-bit 1-MSPS SAR ADC with sample and hold and a programmable sequencer, a continuous time block with two opamps with a comparator mode, a temperature sensor, and two low-power comparators
- Fixed-function digital blocks: Two combination UART/SPI/I2C (one function at a time) serial communication blocks (SCB). Four 16-bit counter/timer/PWMs with center-aligned capability

- Fixed-function special blocks: CSD CapSense block with shield driver for waterproofing and digital LCD drive on all pins
- Clocking: Trimmed IMO and ILO clock sources
- Deep Sleep, Hibernate, and Stop low-power modes

Figure 4-2. CY8CKIT-038 PSoC 4200 Family Processor Module Board





The CY8CKIT-038 PSoC 4200 family processor module board has the following four blocks:

- 44-Pin TQFP package PSoC 4200 family device
- Four 2 × 16 headers, which connect to the CY8CKIT-001 DVK main board
- CMOD circuitry for CapSense application
- Single-wire debug (SWD) connector

5. Example Projects

All code examples provided with this kit are for the PSoC 4 device, CY8C4245AXI-483. Make sure that you select this device when creating new projects using this processor module. Visit http://www.cypress.com/?id=4519 for more information about the PSoC 4200 device portfolio.

5.1 Project: VoltageDisplay_SAR_ADC

For all the projects, place jumper J12 on CY8CKIT-001 in the LCD power off position.

5.1.1 Project Description

This example project measures an analog voltage controlled by the potentiometer. The project uses the internal SAR ADC configured for a 12-bit operation; the ADC range is 0 to VDDA. The results are displayed on the I2C character LCD.

Figure 5-1. VoltageDisplay_SAR_ADC Schematic

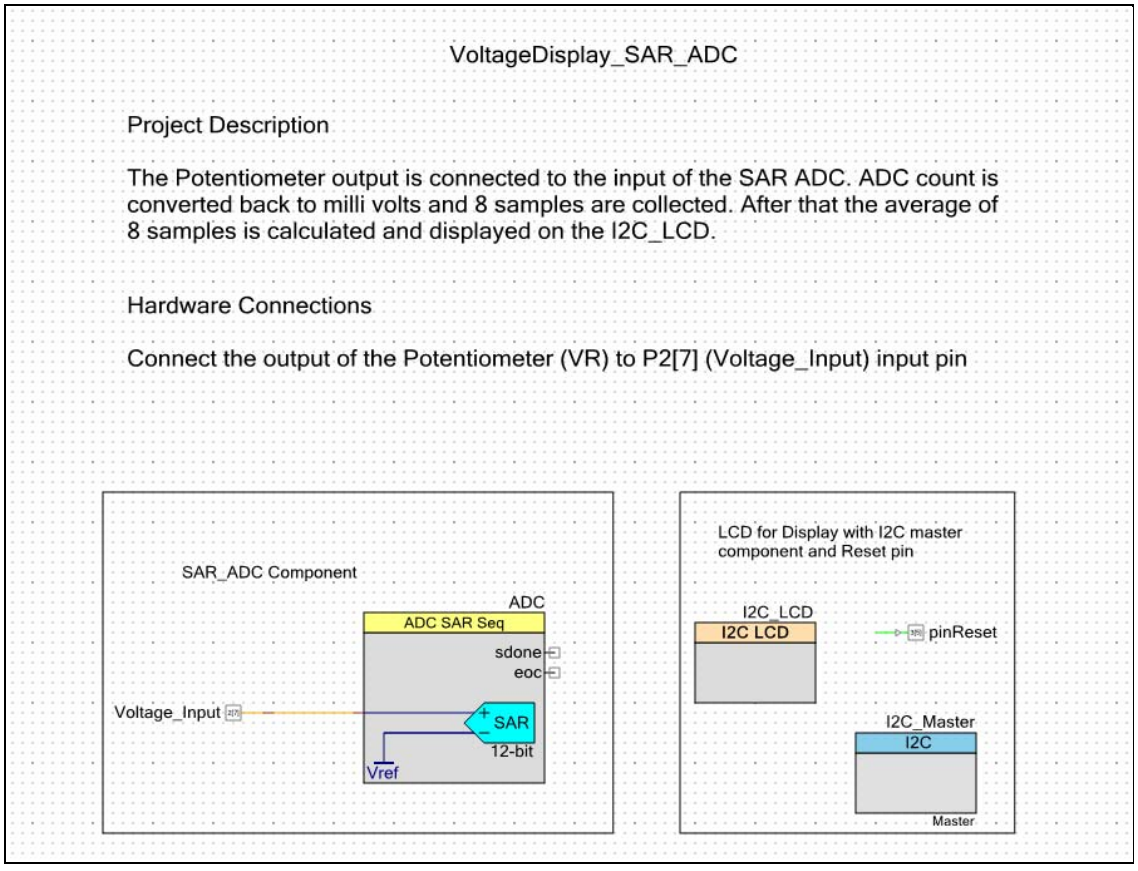
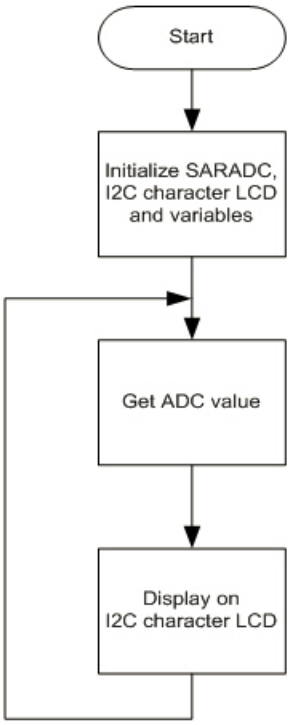


Figure 5-2. Project Flow Chart

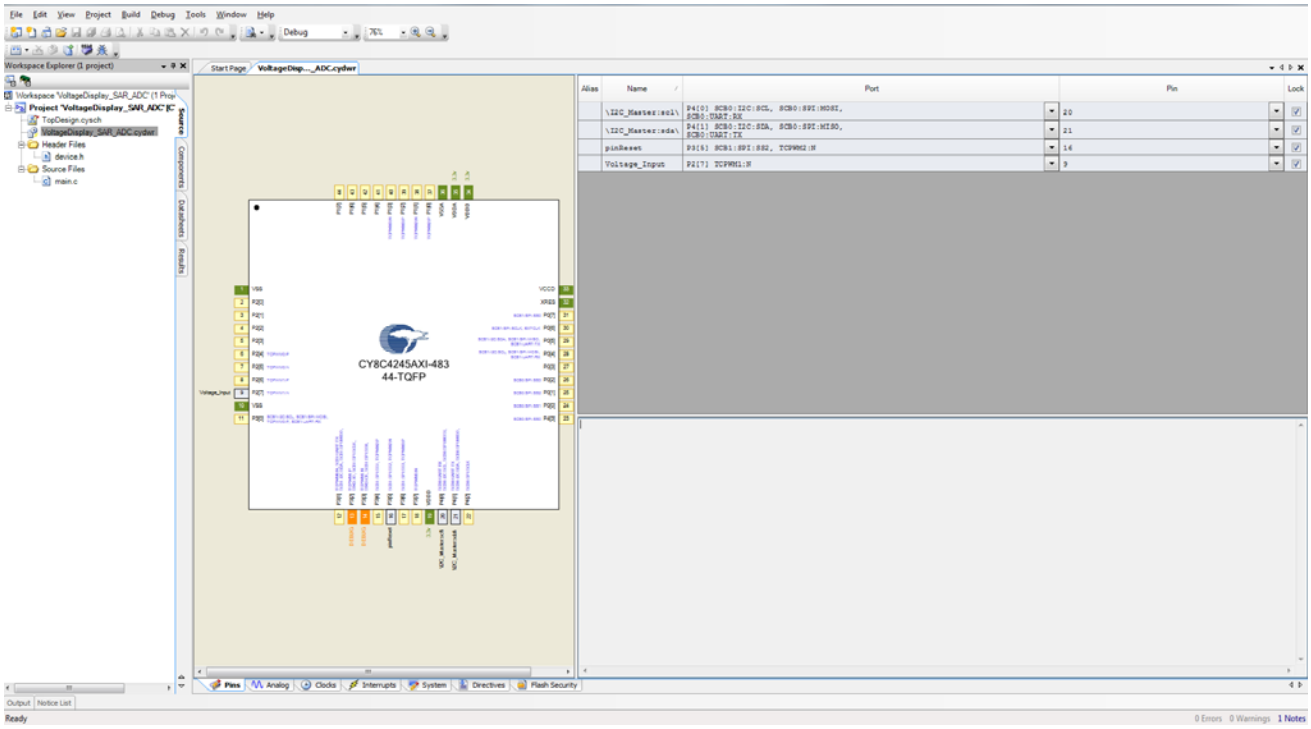


5.1.2 Hardware Connections

The I2C character LCD should be configured as shown in the following table.

Pin Name	Port Name
Reset	P3[5]
SCB_SCL	P4[0]
SCB_SDA	P4[1]

5.1.2.1 PSoC Creator Connections (VoltageDisplay_SAR_ADC.cydwr)



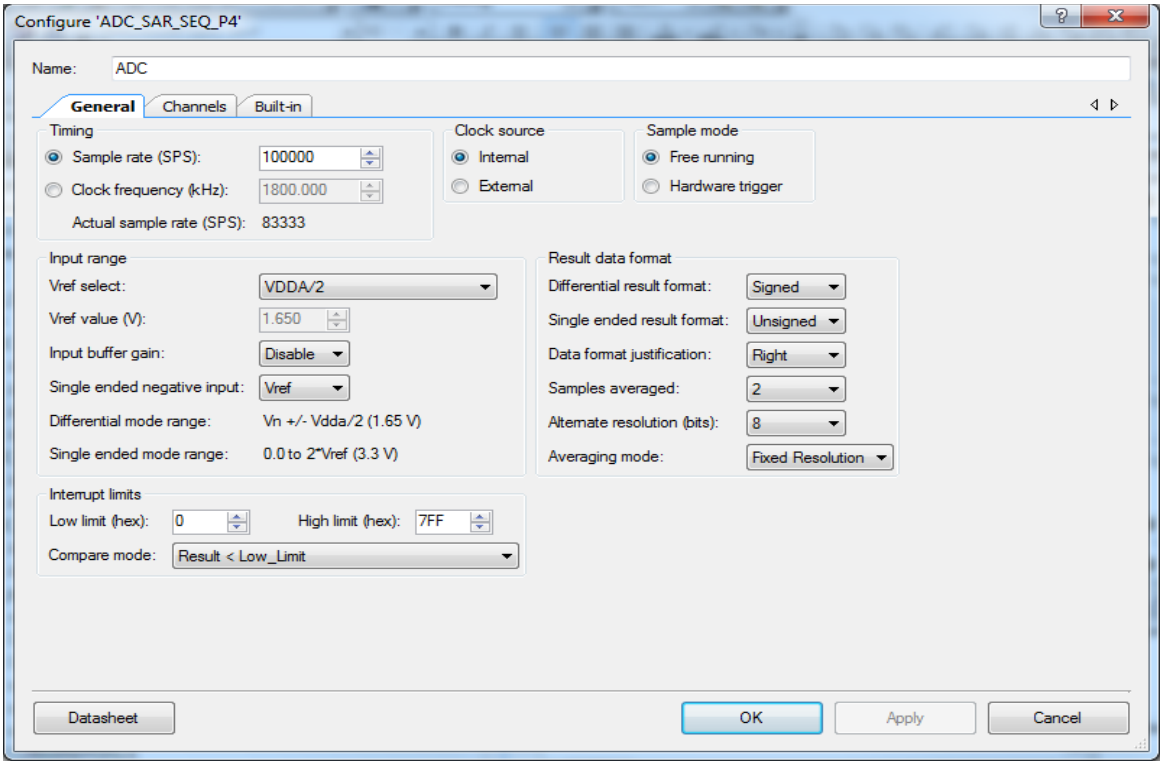
5.1.2.2 Physical Connections on CY8CKIT-001 DVK

Because it uses the potentiometer, the jumper VR_PWR (J11) should be in place. This connects the potentiometer to the VDDA. Connect the output of the VR pin to P2[7] (Voltage_Input) input pin, as shown in Figure 5-5 on page 23.

5.1.3 SAR ADC Configuration

To view or configure the SAR ADC component, double-click the component in the *TopDesign.cysch* file.

Figure 5-3. SAR ADC Configuration

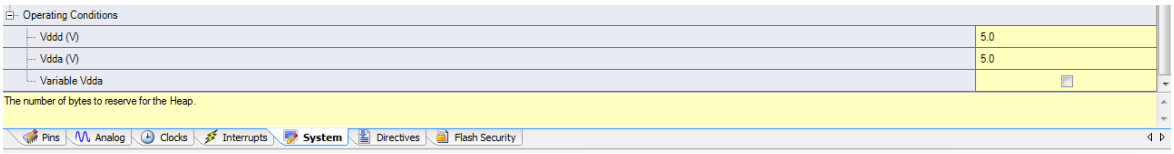


The SAR ADC is configured as follows:

- Free-running mode of operation is selected because the ADC scans only one channel continuously.
- Sample rate is set to 100,000 sps. The code waits for each sample, processes it, and displays the result on the LCD.
- Range is set to VSSA to 2*VREF (3.3 V) in single-ended mode because the potentiometer output is a single-ended signal that can go from 0 to VDDA.Therefore, at 12-bit resolution, the ADC resolves in steps of VDDA/2.
- Voltage reference should be set to VDDA/2 supply voltage when the input range is set to VSSA to VDDA. It is set to 1.65 V here, because by default the VDDA jumper setting on the board is set to 3.3 V.

When the VDDA jumper on the board is set to 5 V, set **Operating Conditions** in the **System** tab to 5 V as shown in Figure 5-4.

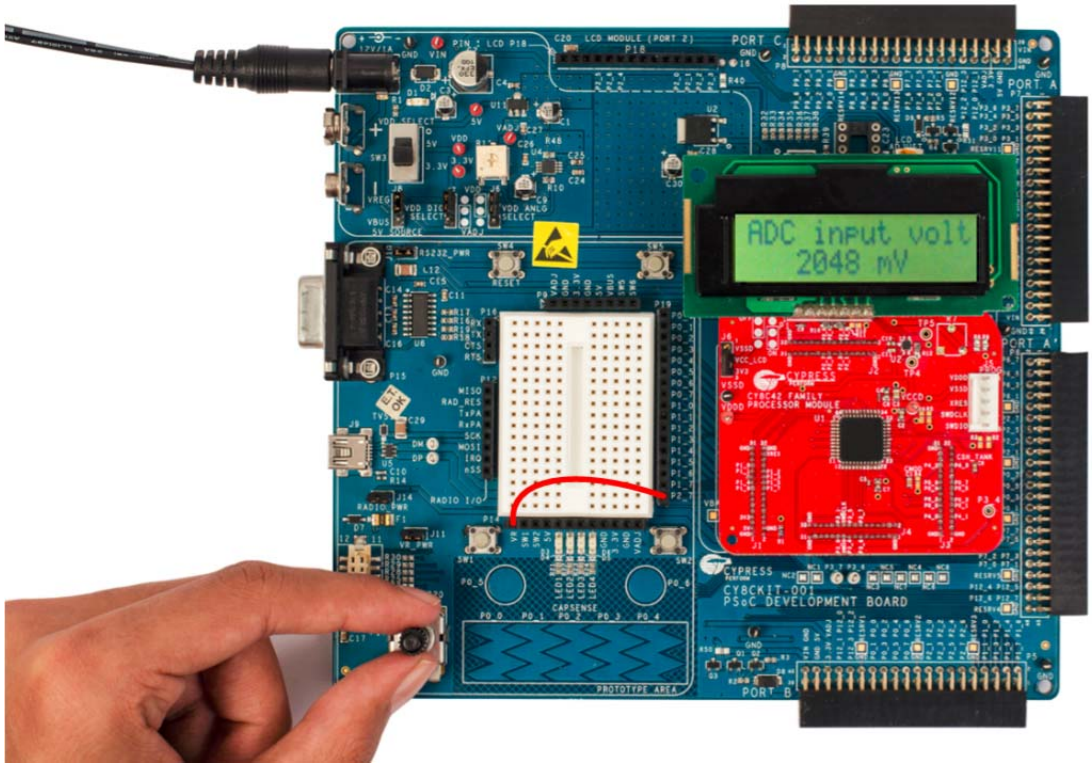
Figure 5-4. Operating Condition



5.1.4 Verify Output

Build and program the code example, and reset the device. The LCD shows the voltage reading corresponding to the voltage on the potentiometer. The following figure demonstrates the functionality. When you turn the potentiometer, the voltage value changes.

Figure 5-5. VoltageDisplay_SAR_ADC Project Demonstration



You can also verify the voltage on the potentiometer using a precision multimeter.

Note The potentiometer connects to a differential ADC, which works in the single-ended mode. This means the ADC input is measured against internal VSSA. Any offset in the measurement can be positive or negative. This can result in a small offset voltage even when the potentiometer is zero.

5.2 Project: IntensityLED

5.2.1 Project Description

This example code uses pulse-width modulators (PWM) to illuminate an LED. When the pulse width of the PWM varies, the LED brightness changes. By continuously varying the pulse width of the PWM, the example code makes an LED go from low brightness to a high brightness and back.

Figure 5-6. Intensity LED Schematic

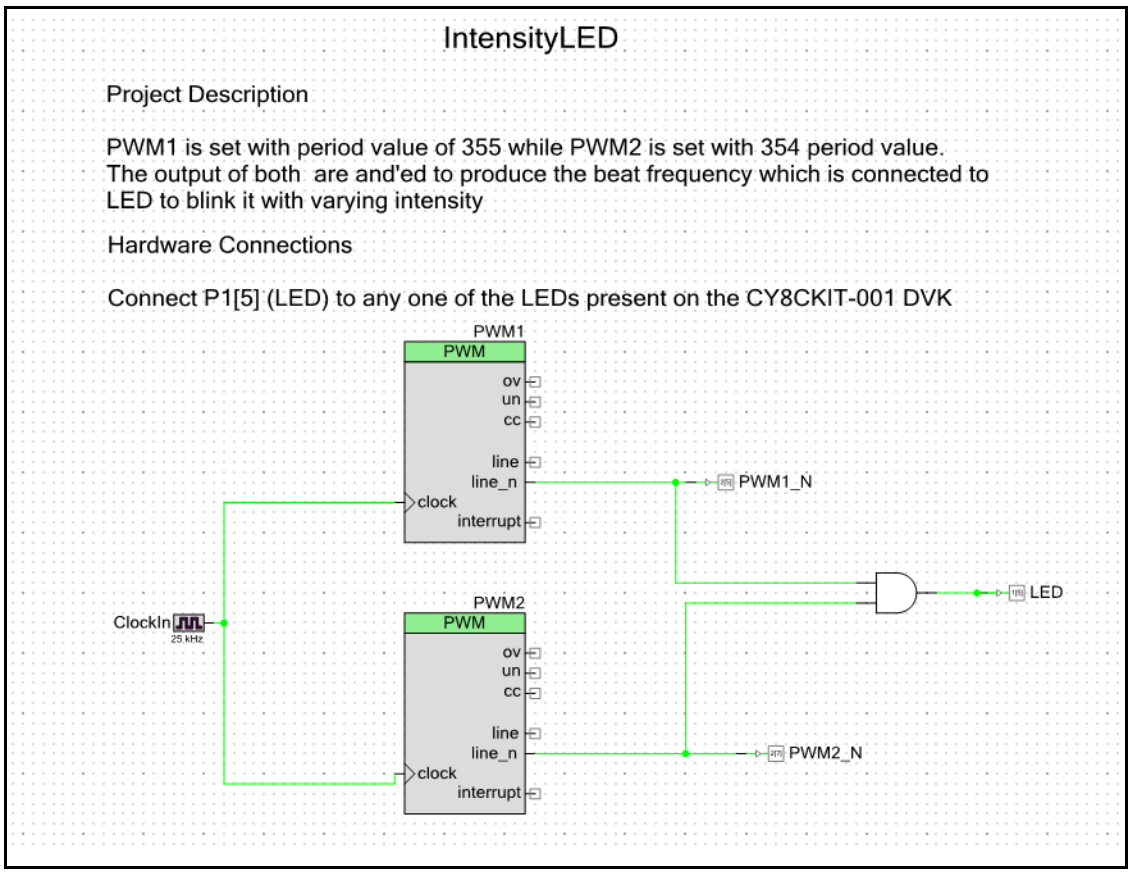
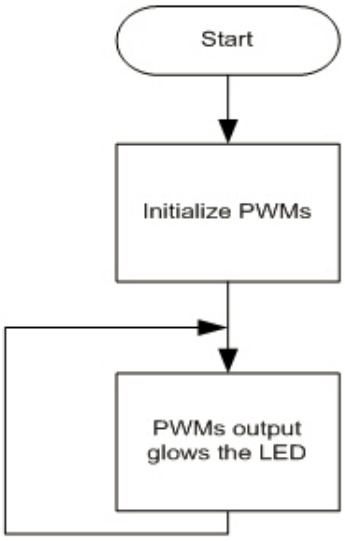
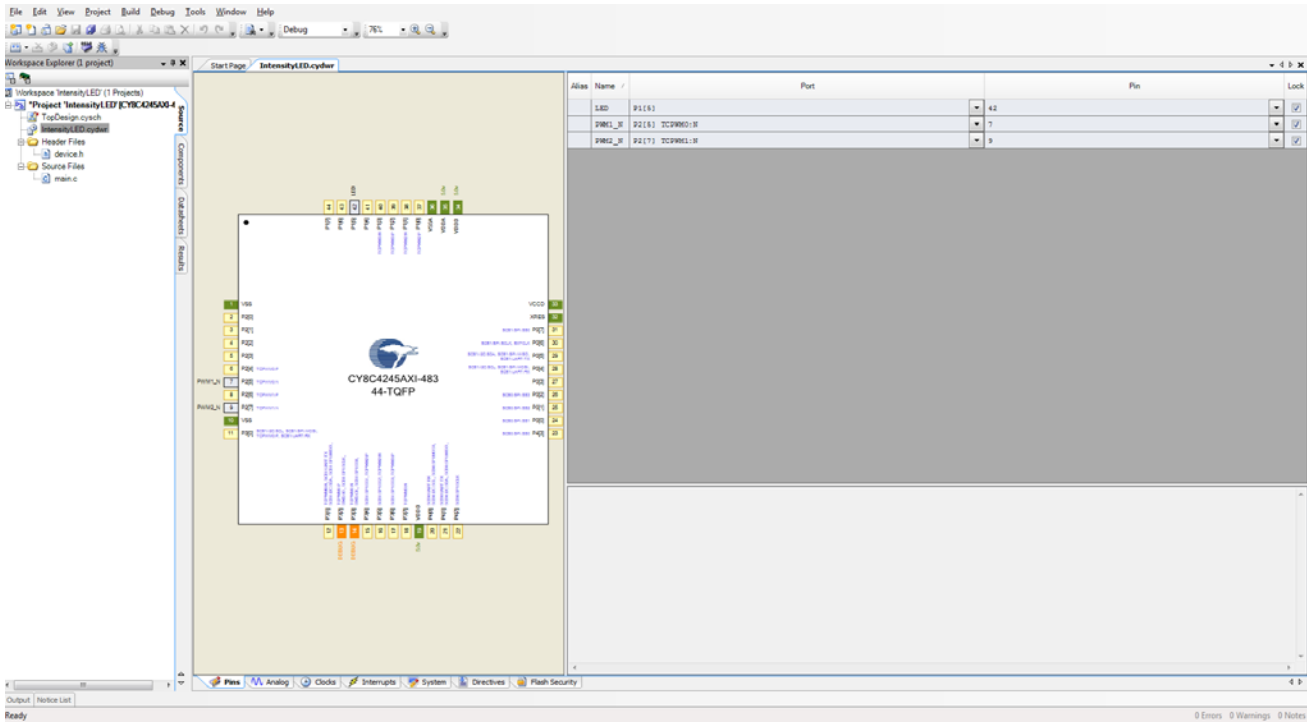


Figure 5-7. Project Flow Chart



5.2.2 Hardware Connections

5.2.2.1 PSoC Creator Connections (IntensityLED.cydwr)



5.2.2.2 Physical Connections on CY8CKIT-001 DVK

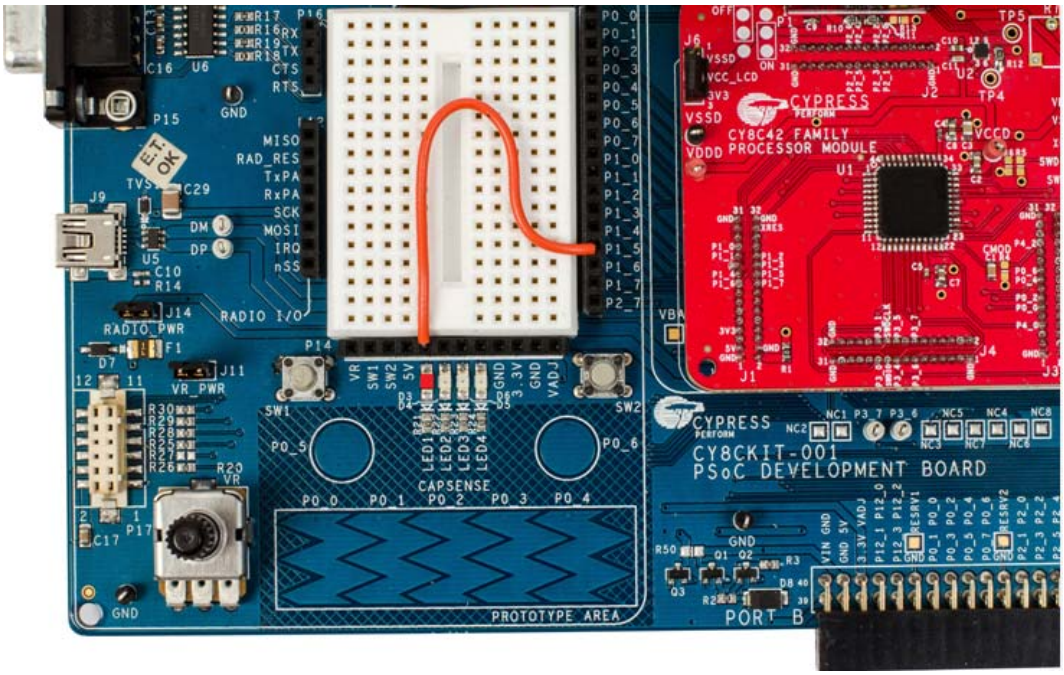
Connect the output pin P1[5] (LED) to any one of the LEDs present on the CY8CKIT-001 DVK, as shown in Figure 5-8.

5.2.3 Verify Output

When the example code is built and programmed into the device, reset the device by pressing the Reset button or power cycling the board. The project output is LED1 glowing with a brightness control that changes with time.

Note If the processor module is programmed with any other code example involving LCD display before programming the *IntensityLED.hex* file, the LCD continues to display the output of the previous project because the LCD component is used in the IntensityLED project. The LCD display is cleared by power cycling the board.

Figure 5-8. IntensityLED Project Demonstration



5.3 Project: LowPowerDemo

5.3.1 Project Description

This project demonstrates the low-power functionality of the PSoC 4200 family processor module. The project implements a firmware-based code, which continuously monitors a switch to put the system into sleep or wake-up mode.

Figure 5-9. LowPowerDemo Schematic

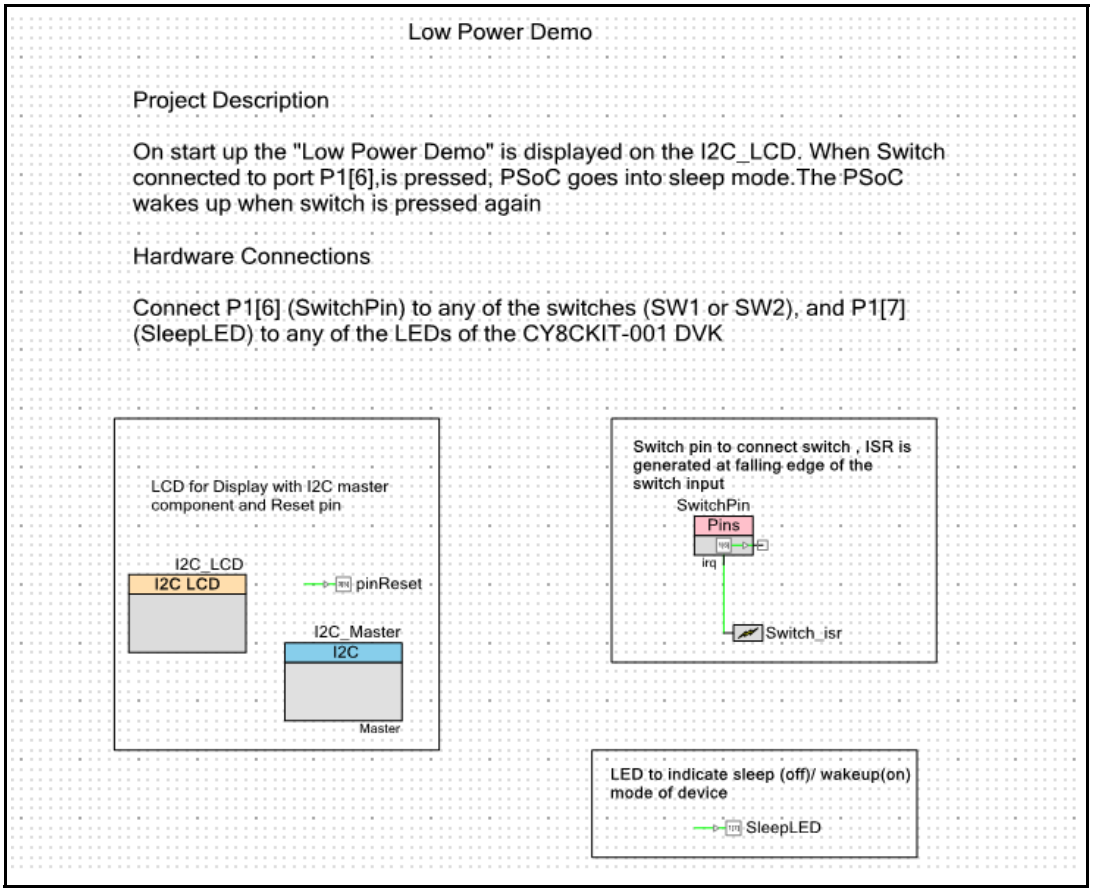
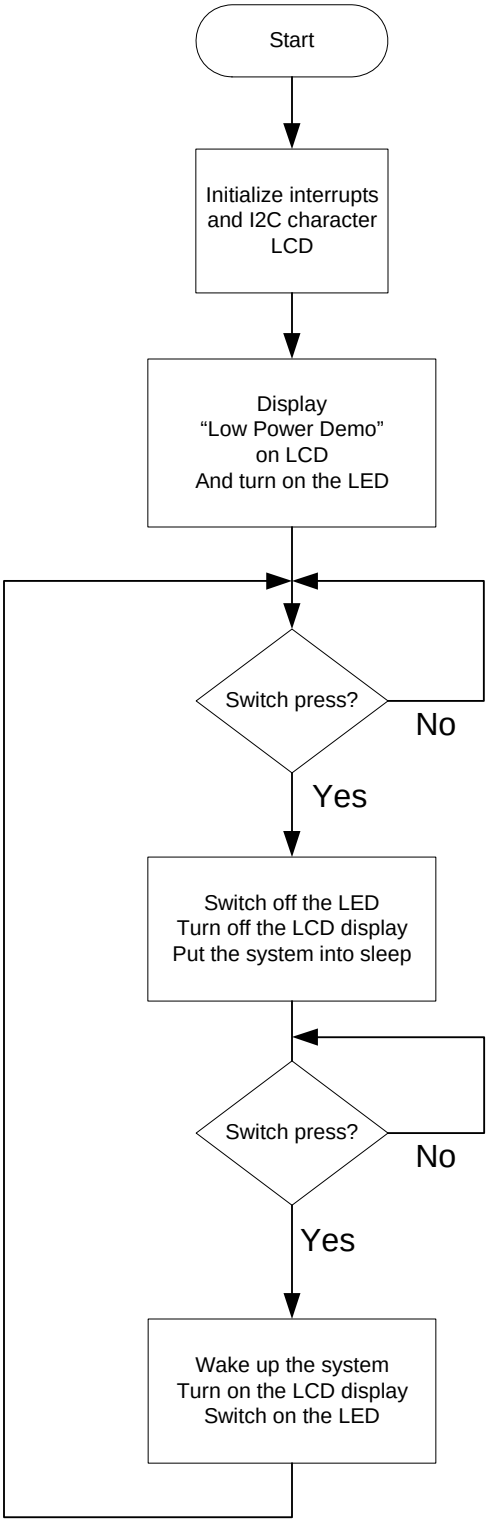


Figure 5-10. Project Flow Chart

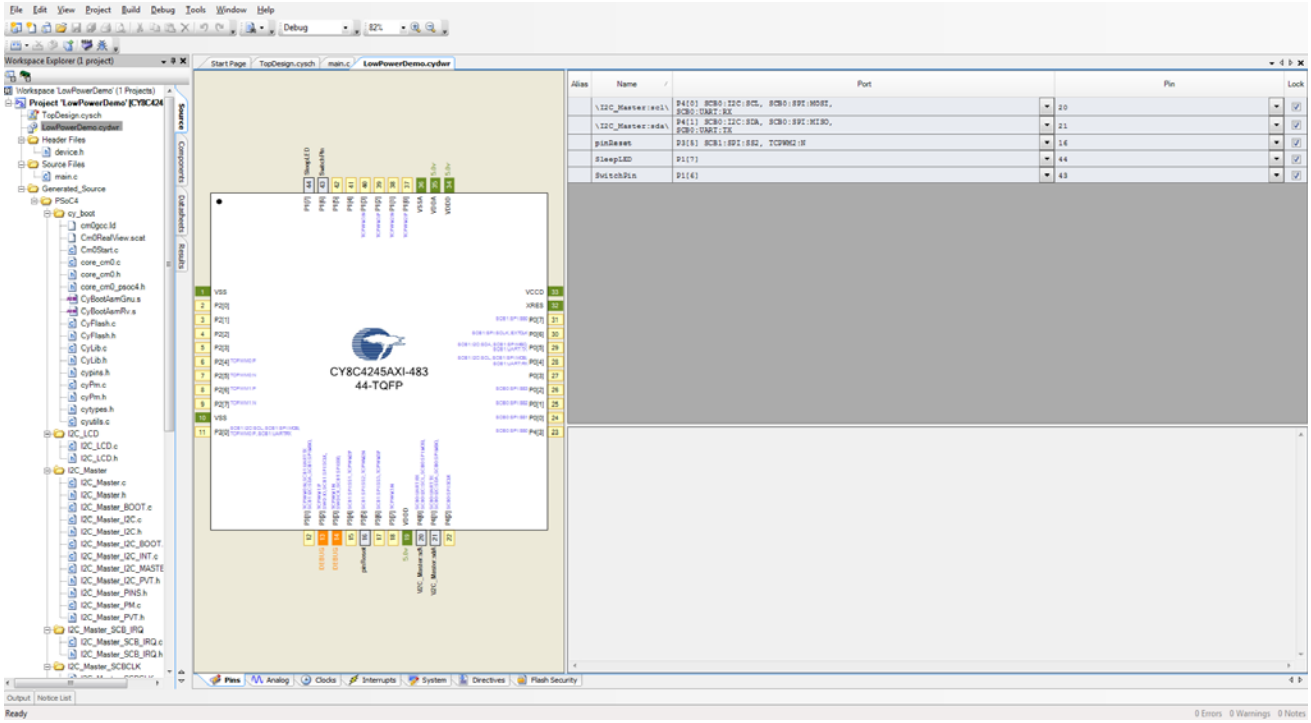


5.3.2 Hardware Connections

The I2C character LCD should be configured as shown in the following table.

Pin Name	Port Name
Reset	P3[5]
SCB_SCL	P4[0]
SCB_SDA	P4[1]

5.3.2.1 PSoC Creator Connections (LowPowerDemo.cydwr)



5.3.2.2 Physical Connections on CY8CKIT-001 DVK

Connect P1[6] (SwitchPin) to any of the switches (SW1 or SW2), and P1[7] (SleepLED) to any of the LEDs of the CY8CKIT-001 DVK, as shown in Figure 5-11 on page 30.

5.3.3 Verify Output

Build and program the code example, and reset the device.

- When powered or during normal operation, "Low Power Demo" is displayed on the LCD and the LED is in the ON state.
- When P1[6] (SwitchPin) is pressed, the LCD display turns off, LED turns off, and finally, the device goes to sleep.
- When P1[6] (SwitchPin) is pressed the second time, the device returns to Active mode and the LCD display and LED turn on.

Figure 5-11. LowPowerDemo Project Demonstration (Active Mode)

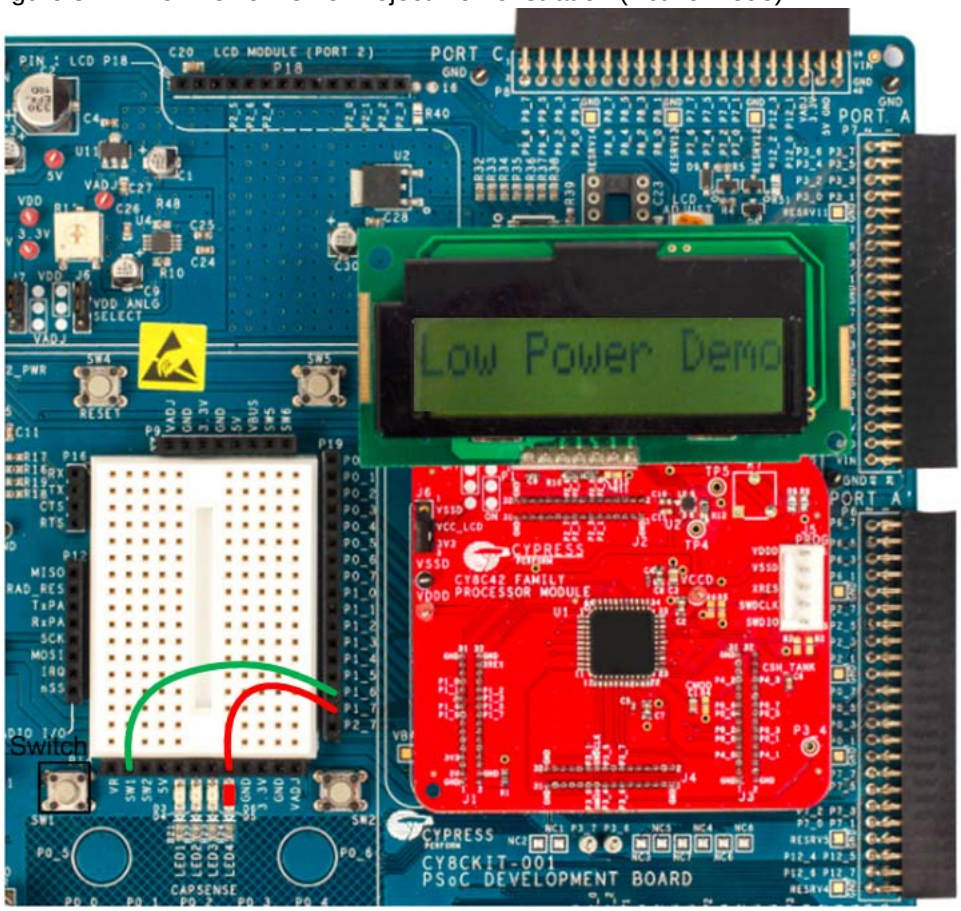
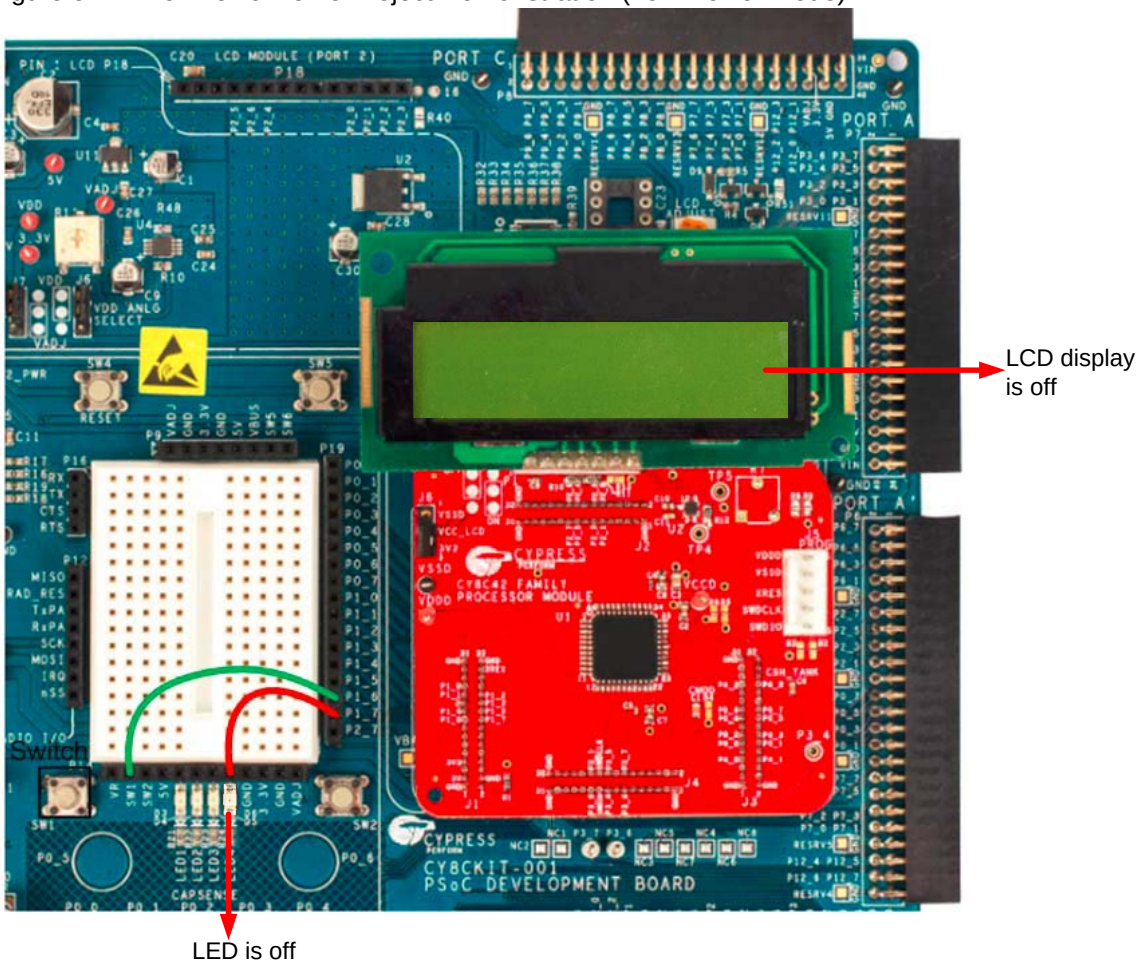


Figure 5-12. LowPowerDemo Project Demonstration (Low-Power Mode)



5.4 Project: CapSense

5.4.1 Project Description

This code example provides a platform to build CapSense-based projects using the PSoC 4200 family processor. The example uses two CapSense buttons and one five-element slider provided on the board. Each capacitive sensor on the board is scanned using the Cypress CSD algorithm. The buttons are pre-tuned in the example code to take care of factors such as board parasitic.

Figure 5-13. CapSense Schematic

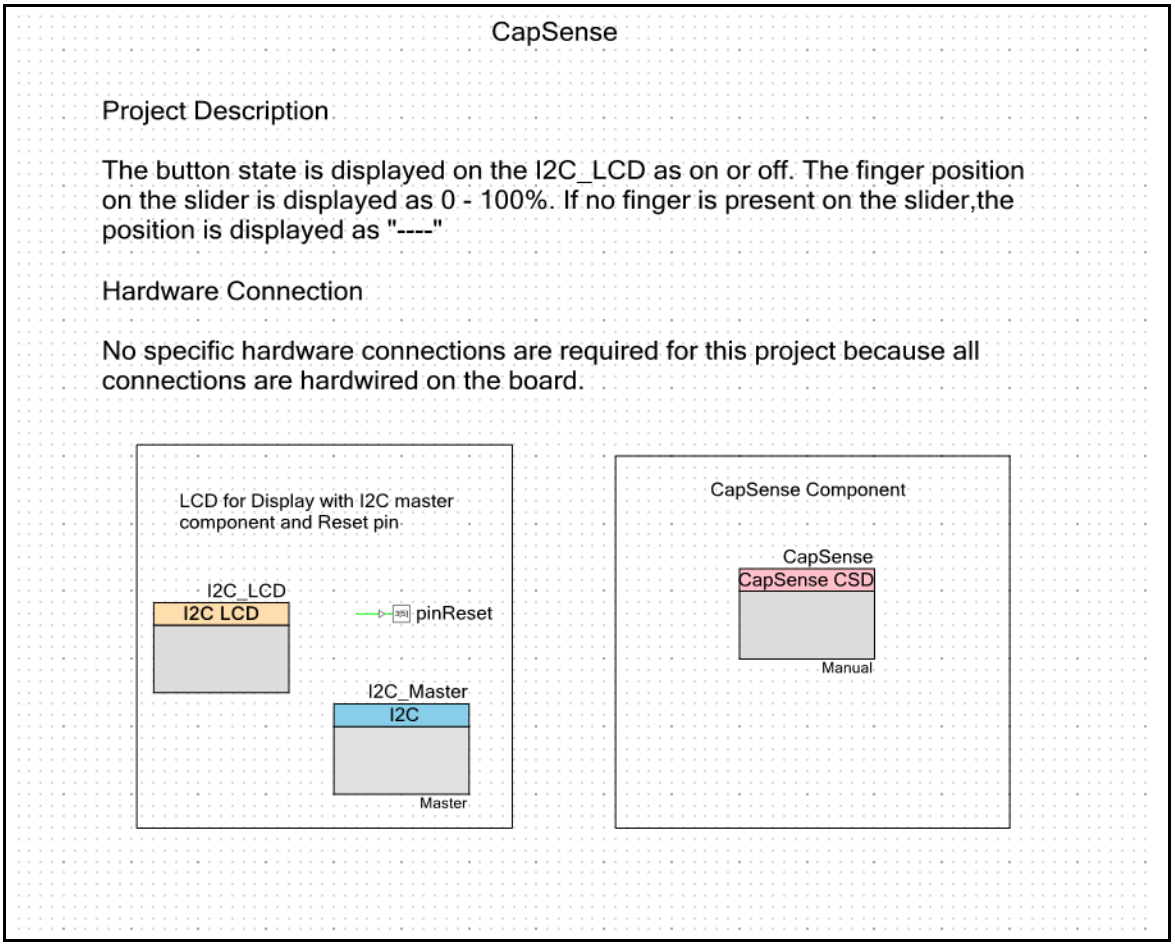
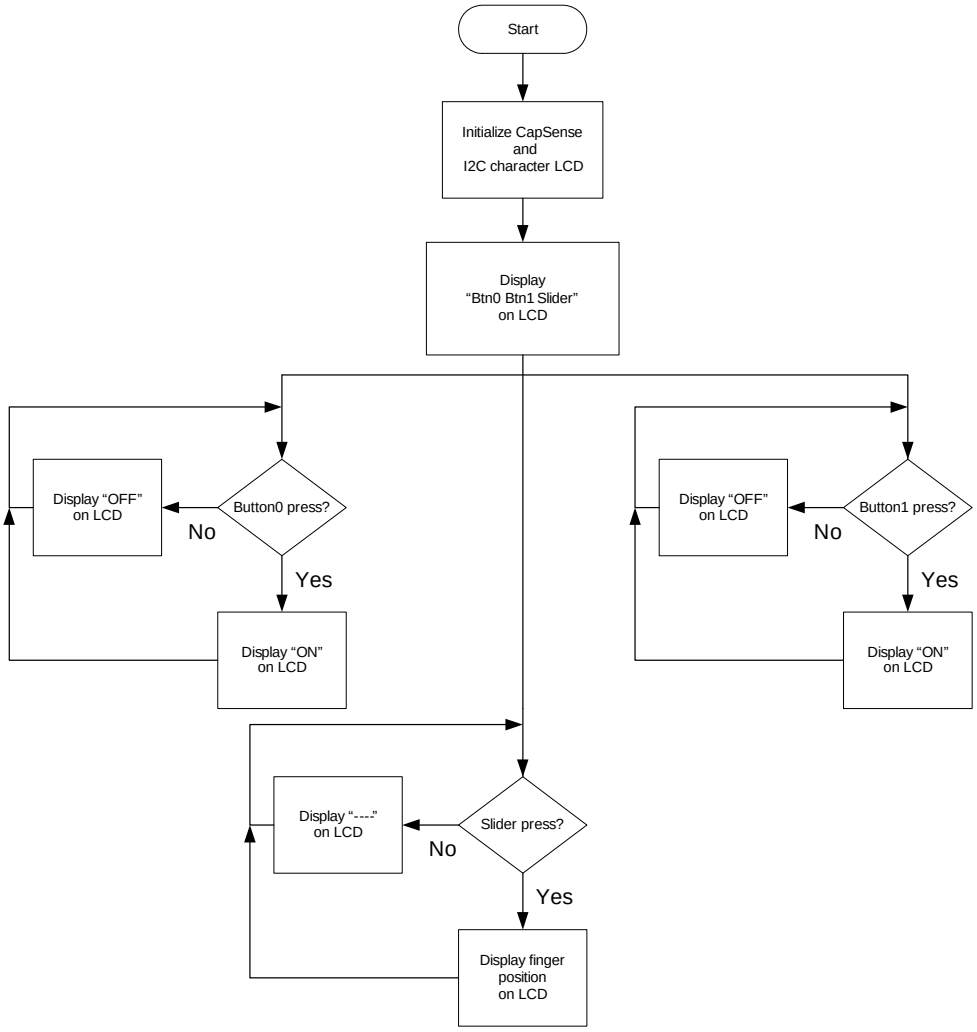


Figure 5-14. Project Flow Chart

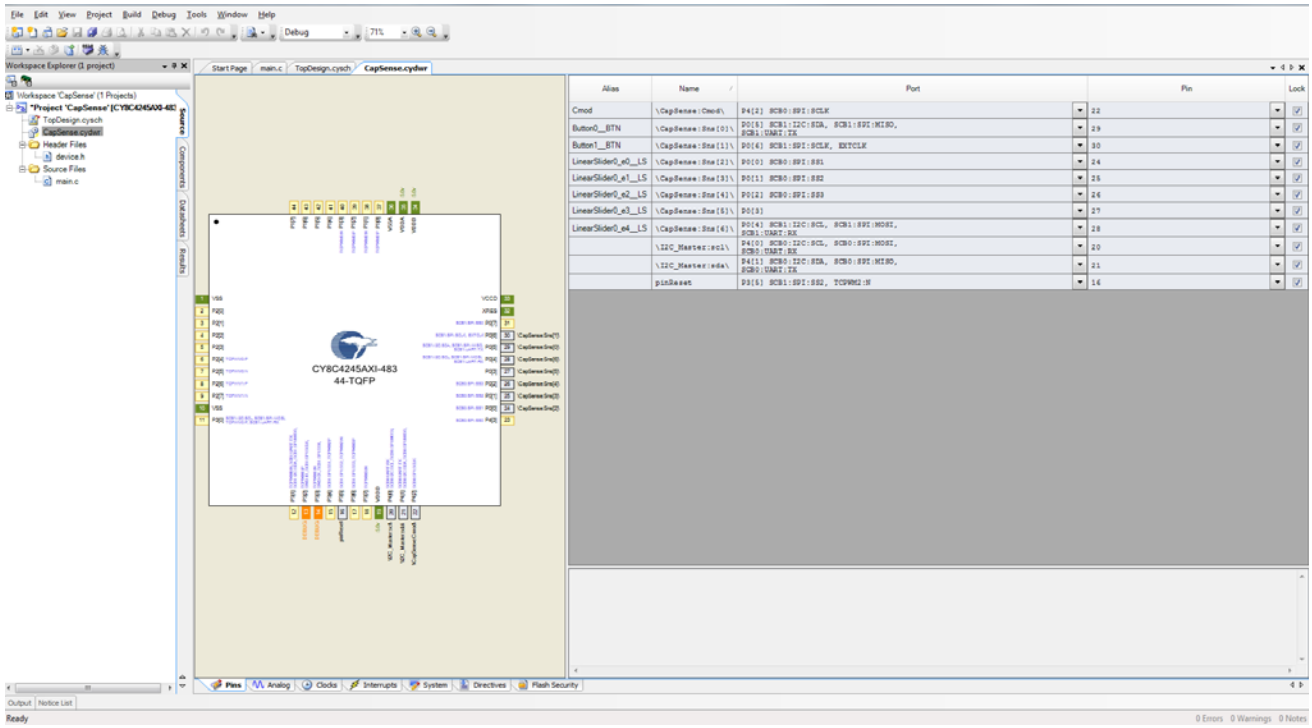


5.4.2 Hardware Connections

No specific hardware connections are required for this project because all connections are hard-wired on the board. The following table shows the I2C character LCD and CapSense configurations.

Pin Name	Port Name
Reset	P3[5]
SCB_SCL	P4[0]
SCB_SDA	P4[1]
Button0	P0[5]
Button1	P0[6]
Slider0	P0[0]
Slider1	P0[1]
Slider2	P0[2]
Slider3	P0[3]
Slider4	P0[4]

5.4.2.1 PSoC Creator Connections (CapSense.cydwr)

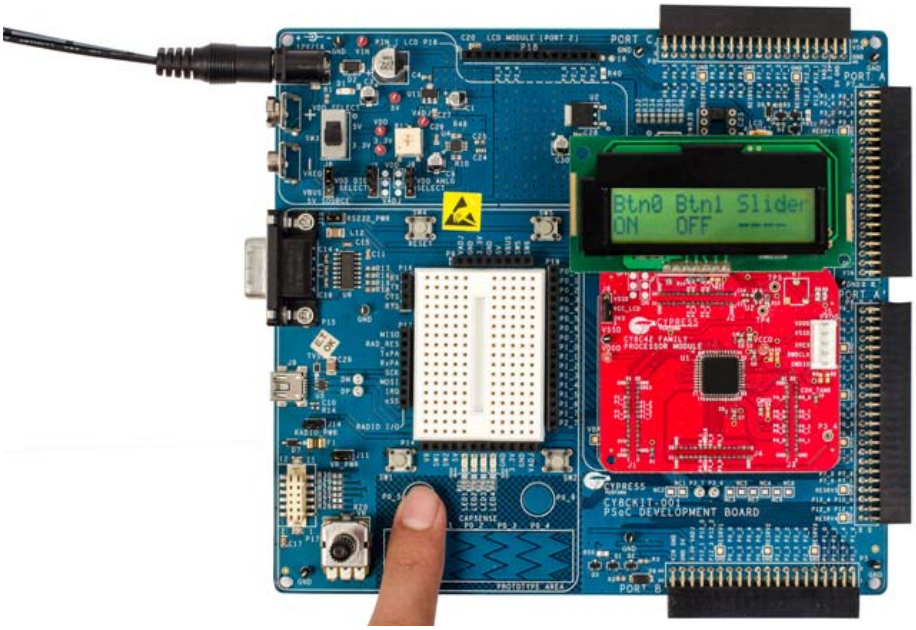


5.4.3 Verify Output

Build and program the code example, and reset the device. The LCD displays the status of the two buttons as ON or OFF. The LCD also shows the slider touch position as a percentage.

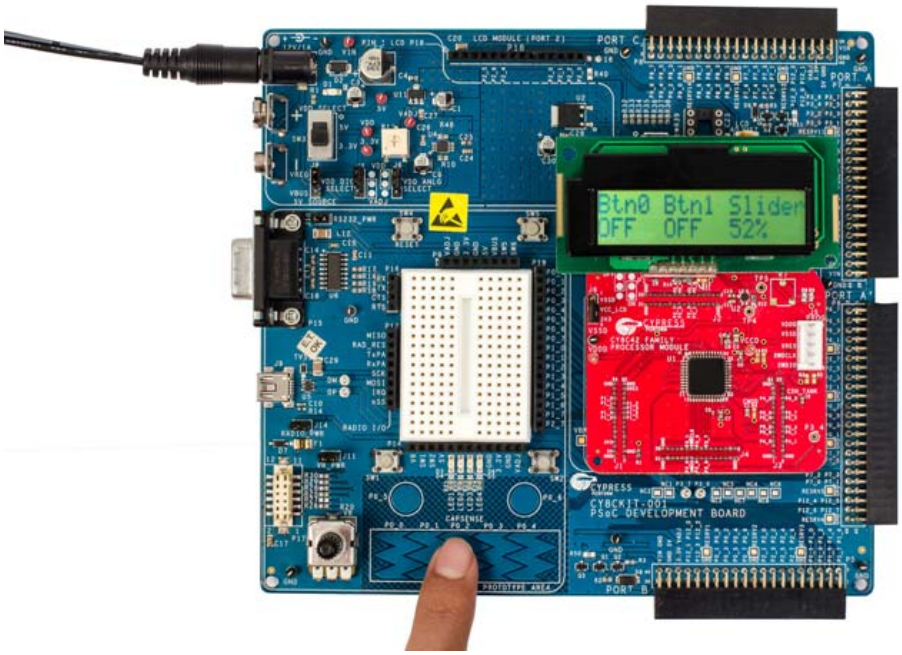
When you touch a button, the LCD displays ON; when you remove the finger from the button, the LCD displays OFF, as shown in Figure 5-15.

Figure 5-15. Capsense Button Demo



When the slider is touched, the corresponding finger position is displayed as a percentage on the LCD.

Figure 5-16. CapSense Slider Demo

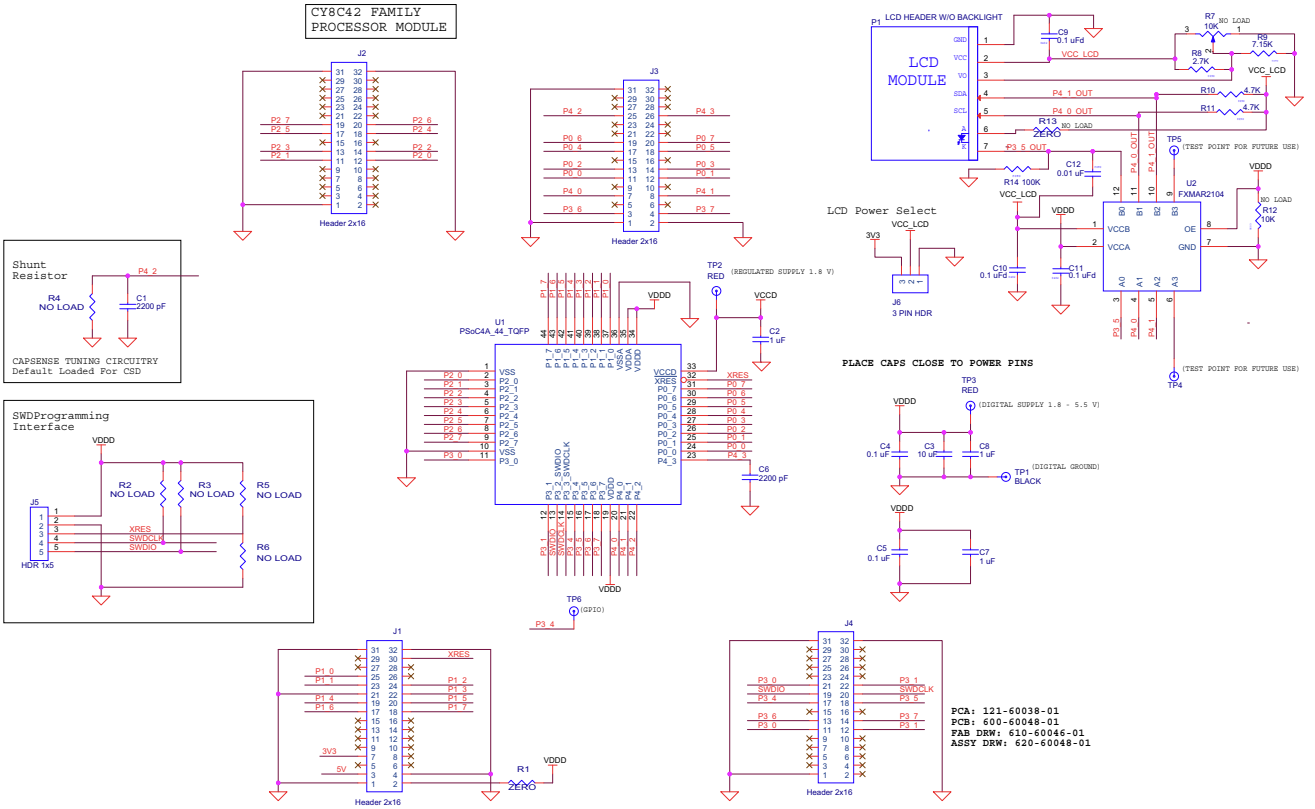


Note You can also use the character LCD provided with the CY8CKIT-001 DVK to implement your own designs using the PSoC 4200 Family Processor Module. Example projects using the character LCD are not provided with this kit.

To use the character LCD, move jumper J12 on CY8CKIT-001 to LCD power ON.

A. Appendix

A.1 Schematic



A.2 Bill of Materials (BOM)

Item	Qty	Reference	Value	Description	Manufacturer	Mfr Part Number
1	1	C3	10 uF	CAP CER 10 UF 16 V X5R 0805	Murata Electronics North America	GRM21BR61C106KE15L
2	3	C2,C7,C8	1uF	CAP CER 1UF 10 V 10% X5R 0805	Kemet	C0805C105K8PACTU
3	2	C1, C6	2200 pF	CAP CER 2200PF 50 V 5% C0G 0603	Murata	GRM1885C1H222JA01D
4	5	C4, C5, C9, C10, C11	0.1 uF	CAP .10 UF 10 V CERAMIC X5R 0402	Kemet	C0402C104K8PACTU
5	4	J1, J2, J3, J4	HDR 2x16	CONN MALE 32POS DL 050 TH SHRD GOLD	Centronic Precision Electronic Co.	HHLHS32GB1
6	1	J5	HDR 1x5	CONN HEADER 5POS 0.1 VERT KEYED	Molex	22-23-2051
7	1	J6	3 PIN HDR	CONN HEADR BRKWAY 100 03POS STR	TE Connectivity	9-146280-0-03
8	1	P1	LCD HEADER	CONN RECEPT 100 SNGL STR 7POS	3M	929850-01-07-RA
9	1	R1	ZERO	RES ZERO OHM 1/16W 0603 SMD	Panasonic - ECG	ERJ-3GEY0R00V
10	1	R8	2.7 K	RES 2.7K OHM 1/10W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ272V
11	1	R9	7.15 K	RES 7.15 K OHM 1/10W 1% 0603 SMD	Panasonic - ECG	ERJ-3EKF7151V
12	2	R10, R11	4.7 K	RES 4.7 K OHM 1/10W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ472V
13	5	TP2, TP3, TP4, TP5, TP6	RED	TEST POINT 43 HOLE 65 PLATED RED	Keystone Electronics	5000
14	1	TP1	BLACK	TEST POINT 43 HOLE 65 PLATED BLACK	Keystone Electronics	5001
15	1	U1	PSoC 4A	PSoC4A Mixed-Signal Array - 44-Pin TQFP	Cypress Semiconductor	PSoC4A
16	2			M2.5 x 1mm WASHER NYLON		
17	2			Self Thread Screws 2.5mm		
18	2			STANDOFF height 23mm		
19	1	U2	FXMAR2104	TRANSLATOR 4-BIT DUAL 12-UMLP	Fairchild Semiconductor	FXMAR2104UMX
20	1	R14	100 K	RES 100K OHM 1/10 W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ104X
21	1	C12	0.01 uF	CAP 10000PF 16 V CERAMIC 0402 SMD	Panasonic - ECG	ECJ-0EB1C103K
22	1			16X2 I2C 3.3 V LCD module	SUNLIKE	CON-1X7_2-54MM
No Load Components						
19	7	R2, R3, R4, R5, R6, R13, R12	NO LOAD	RES NO LOAD 0603 SMD	Panasonic - ECG	ERJ-3GEY0R00V
20	1	R7	10 K POT	Trimmer Resistors - Through Hole 3/8" round 10 Kohms 0.5 watt 20%	Bourns	3352T-1-103LF

A.3 Pin Assignment Table

Port	Pin	Pin Name	Description
Port 0	24	P0[0]	GPIO,LCD,CSD,SCB0,COMP
	25	P0[1]	GPIO,LCD,CSD,SCB0,COMP
	26	P0[2]	GPIO,LCD,CSD,SCB0,COMP
	27	P0[3]	GPIO,LCD,CSD,COMP
	28	P0[4]	GPIO,LCD,CSD,SCB1
	29	P0[5]	GPIO,LCD,CSD,SCB1
	30	P0[6]	GPIO,LCD,CSD,SCB1,EXT_CLK
	31	P0[7]	GPIO,LCD,CSD,SCB1,WAKEUP
Port 1	37	P1[0]	GPIO,LCD,CSD,CTB,PWM
	38	P1[1]	GPIO,LCD,CSD,CTB,PWM
	39	P1[2]	GPIO,LCD,CSD,CTB,PWM
	40	P1[3]	GPIO,LCD,CSD,CTB,PWM
	41	P1[4]	GPIO,LCD,CSD,CTB
	42	P1[5]	GPIO,LCD,CSD,CTB
	43	P1[6]	GPIO,LCD,CSD
	44	P1[7]	GPIO,LCD,CSD,EXT_REF
Port 2	2	P2[0]	GPIO,LCD,CSD,SARMUX
	3	P2[1]	GPIO,LCD,CSD,SARMUX
	4	P2[2]	GPIO,LCD,CSD,SARMUX
	5	P2[3]	GPIO,LCD,CSD,SARMUX
	6	P2[4]	GPIO,LCD,CSD,SARMUX,PWM
	7	P2[5]	GPIO,LCD,CSD,SARMUX,PWM
	8	P2[6]	GPIO,LCD,CSD,SARMUX,PWM
	9	P2[7]	GPIO,LCD,CSD,SARMUX,PWM
Port 3	11	P3[0]	GPIO,LCD,CSD,SCB1,PWM
	12	P3[1]	GPIO,LCD,CSD,SCB1,PWM
	13	P3[2]	GPIO,LCD,CSD,SCB1,PWM,SWD
	14	P3[3]	GPIO,LCD,CSD,SCB1,PWM,SWD
	15	P3[4]	GPIO,LCD,CSD,SCB1,PWM
	16	P3[5]	GPIO,LCD,CSD,SCB1,PWM
	17	P3[6]	GPIO,LCD,CSD,SCB1,PWM
	18	P3[7]	GPIO,LCD,CSD,PWM
Port 4	20	P4[0]	GPIO,LCD,CSD,SCB0
	21	P4[1]	GPIO,LCD,CSD,SCB0
	22	P4[2]	GPIO,LCD,CSD,SCB0
	23	P4[3]	GPIO,LCD,CSD,SCB0

Port	Pin	Pin Name	Description
Other	1	VSS	DIGITAL GROUND
	19	VDDD	DIGITAL SUPPLY (1.8-5.5 V)
	32	XRES	CHIP RESET (active low)
	33	VCCD	REGULATED SUPPLY (Connect TO 1 uF Cap or 1.8 V
	34	VDDD	DIGITAL SUPPLY (1.8-5.5 V)
	35	VDDA	ANALOG SUPPLY (1.8-5.5V)
	36	VSSA	ANALOG GROUND
	10	VSS	DIGITAL GROUND

A.4 Regulatory Compliance Information

CY8CKIT-038 has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations:

- EN 55022:2010 Class A - Emissions
- EN 55024:2010 Class A - Immunity