TLE42694-2

Low Dropout Fixed Voltage Regulator

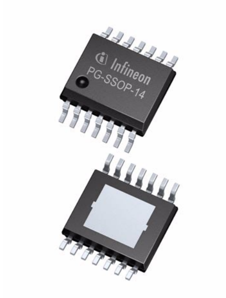
TLE42694-2EL

Data Sheet

Rev. 1.0, 2012-07-03

Automotive Power

1 Overview



PG-SSOP-14 exposed pad

Features

- Output Voltage 5 V ± 2%
- Ouput Current up to 150 mA
- Very Low Current Consumption
- Power-on and Undervoltage Reset with Programmable Delay Time
- Reset Low Down to V_Q = 1 V
- Adjustable Reset Threshold
- Very Low Dropout Voltage
- Output Current Limitation
- Reverse Polarity Protection
- Overtemperature Protection
- Suitable for Use in Automotive Electronics
- Wide Temperature Range -40 °C $\leq T_j \leq$ 150 °C
- Input Voltage Range from -42 V to 45 V
- Integrated Pull-Up Resistors at Logic Outputs
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE42694-2 is a monolithic integrated low dropout voltage regulator,
especially designed for automotive applications. An input voltage up to 45 V (with reverse polarity protection) is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 150 mA. Internal over-current and over-temperatuer features prevent damage of the part in over-load conditions. A reset signal is generated for an output voltage $V_{Q,rt}$ of typically 4.65 V. This threshold can be decreased by an external resistor divider. The power-on reset delay time can be programmed by the external delay capacitor. The reset output is internally connected to the output Q via a pull-up resistor.

Type	Package	Marking
TLE42694-2EL	PG-SSOP-14 exposed pad	426942E

2 Block Diagram

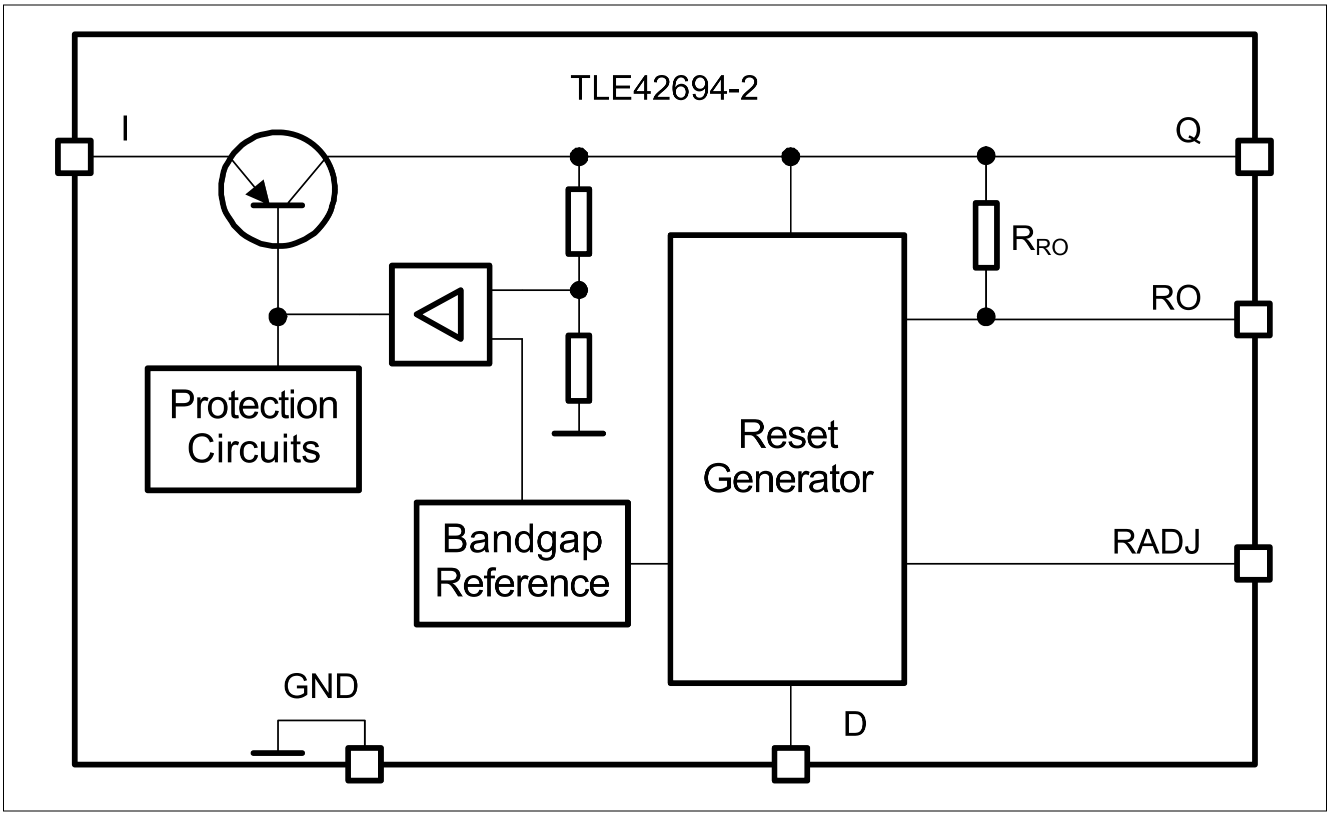


Figure 1 Block Diagram

2.1 Pin Assignment

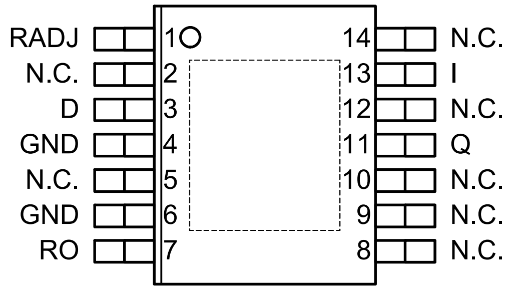


Figure 2 Pin Configuration (top view)

2.2 Pin Definitions and Functions

Table 1

Pin	Symbol	Function
1	RADJ	**Reset Threshold Adjust** connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2,5	n.c.	**not connected** No Internal Connection. Can be connected to I or GND (to improve heat dissipation).
3	D	**Reset Delay Timing** connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
4,6	GND	**Ground** all pins must be connected to GND
7	RO	**Reset Output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the reset function is not needed
8, 9, 10	n.c.	**not connected** No Internal Connection. Can be connected to I or GND (to improve heat dissipation).
11	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table **"Functional Range" on Page 6**
12	n.c.	**not connected** No Internal Connection. Can be connected to I or GND (to improve heat dissipation).
13	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended
14	n.c.	**not connected** No Internal Connection. Can be connected to I or GND (to improve heat dissipation).
Pad	-	**Exposed Pad** connect to heatsink area; connect to GND

3 General Product Characteristics

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

-40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Input						
3.1.1	Voltage	V_I	-40	45	V	–
Output, Reset Output, Reset Delay						
3.1.2	Voltage	V_Q, V_{RO}, V_D	-0.3	7	V	–
Reset Threshold						
3.1.3	Voltage	V_{RADJ}	-0.3	7	V	–
3.1.4	Current	I_{RADJ}	-10	10	mA	–
Temperature						
3.1.5	Junction Temperature	T_j	-40	150	°C	–
3.1.6	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
3.1.7	Human Body Model (HBM)[2)]	Voltage	-2	2	kV	–
3.1.8	Charged Device Model (CDM)[3)]	Voltage	-1	1	kV	–

1) not subject to production test, specified by design
2) ESD HBM Test according to AEC-Q100-002 - JESD22-A114 (1.5kOhm, 100pF)
3) ESD CDM Test according to ESDA ESD-STM5.3.1

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as outside normal operating range. Protections functions are not designed for continuous repetitive operation.

3.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
3.2.1	Input Voltage	V_I	5.5	45	V	–
3.2.2	Output Capacitor's Requirements for Stability	C_Q	10	–	µF	–[1]
		$ESR(C_Q)$	–	3	Ω	–[2]
3.2.3	Output Capacitor's Requirements for Stability	C_Q	4.7	–	µF	–[1]
		$ESR(C_Q)$	–	2.7	Ω	–[2]
3.2.4	Junction Temperature	T_j	-40	150	°C	–

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 40%
2) relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Value			Unit	Conditions
			Min.	Typ.	Max.		
TLE42694-2 (PG-SSOP-14 exposed pad)							
3.3.5	Junction to Soldering Point[1]	R_{thJSP}	–	10	–	K/W	measured to pin 5
3.3.6	Junction to Ambient[1]	R_{thJA}	–	47	–	K/W	[2]
3.3.7			–	145	–	K/W	Footprint only[3]
3.3.8			–	63	–	K/W	300mm^2 heatsink area on PCB[3]
3.3.9			–	53	–	K/W	600mm^2 heatsink area on PCB[3]

1) not subject to production test, specified by design
2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

4 Block Description and Electrical Characteristics

4.1 Voltage Regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table **"Functional Range" on Page 6** have to be maintained. For details see also the typical performance graph **"Output Capacitor Series Resistor ESR(CQ) versus Output Current IQ" on Page 10**. As the output capacitor also has to buffer load steps it should be sized according to the application's needs.

An input capacitor C_I is strongly recommended to compensate line influences. Connect the capacitors close to the component's terminals.

A protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. These safeguards contain an output current limitation, a reverse polarity protection as well as a thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above V_I = 22 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behaviour of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

The TLE42694-2 allows a negative supply voltage. In this fault condition, small currents are flowing into the IC, increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity conditions.

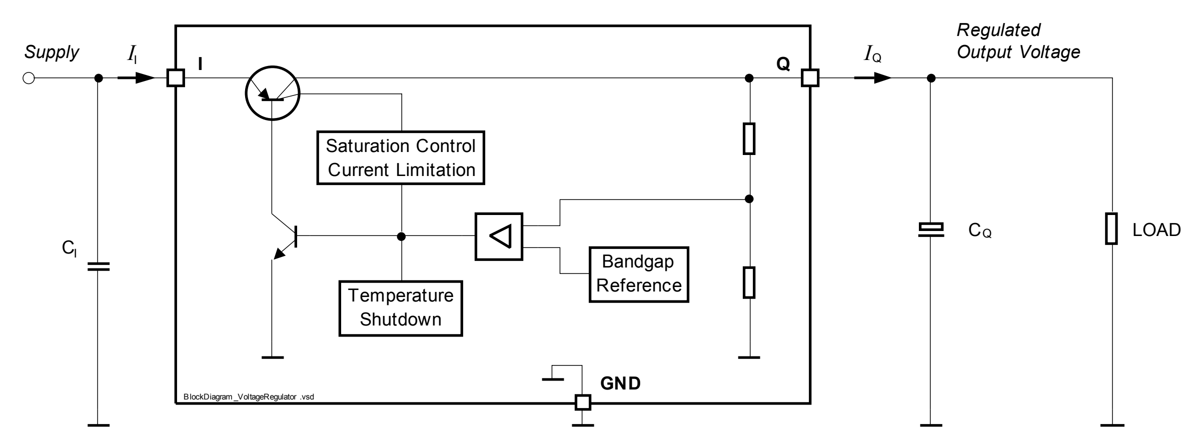


Figure 3 Voltage Regulator

Electrical Characteristics Voltage Regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

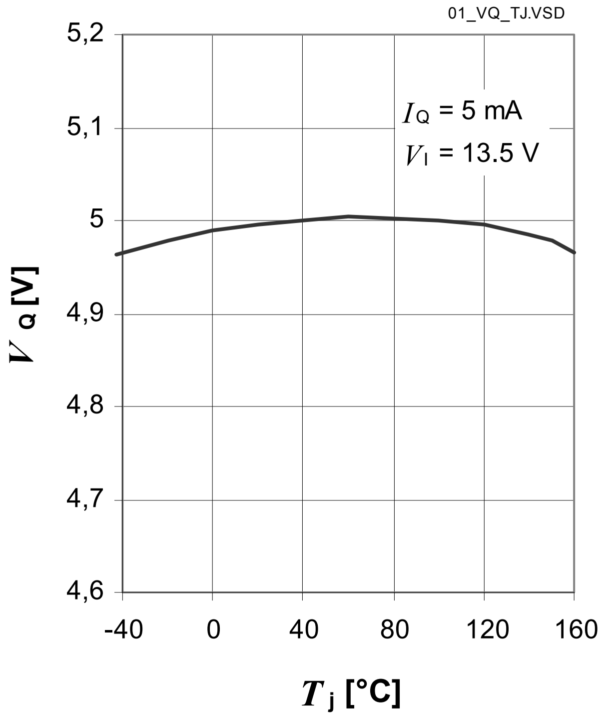
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.1.1	Output Voltage	V_Q	4.9	5.0	5.1	V	100 µA < I_Q < 100 mA 6 V < V_I < 18 V
4.1.2	Output Current Limitation	$I_{Q,max}$	150	200	500	mA	V_Q = 4.8V
4.1.3	Load Regulation steady-state	$\Delta V_{Q,load}$	-30	-15	–	mV	I_Q = 5 mA to 100 mA V_I = 6 V
4.1.4	Line Regulation steady-state	$\Delta V_{Q,line}$	–	10	40	mV	V_I = 6 V to 32 V I_Q = 5 mA
4.1.5	Dropout Voltage[1)] $V_{dr} = V_I - V_Q$	V_{dr}	–	200	330	mV	I_Q = 100 mA
4.1.6	Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing[2)]
4.1.7	Overtemperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	15	–	°C	T_j decreasing[2)]
4.1.8	Power Supply Ripple Rejection[2)]	$PSRR$	–	70	–	dB	f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp

1) measured when the output voltage V_Q has dropped 100mV from the nominal value obtained at V_I = 13.5V

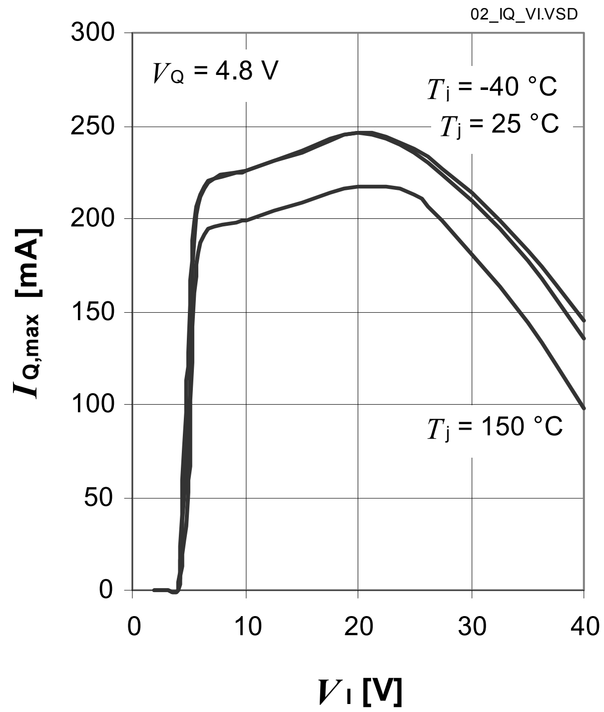
2) not subject to production test, specified by design

Typical Performance Characteristics Voltage Regulator

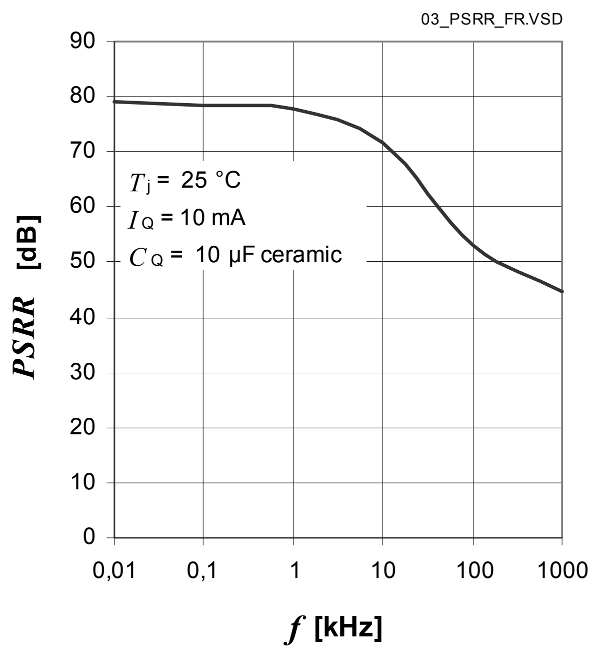
Output Voltage V_Q versus Junction Temperature T_j



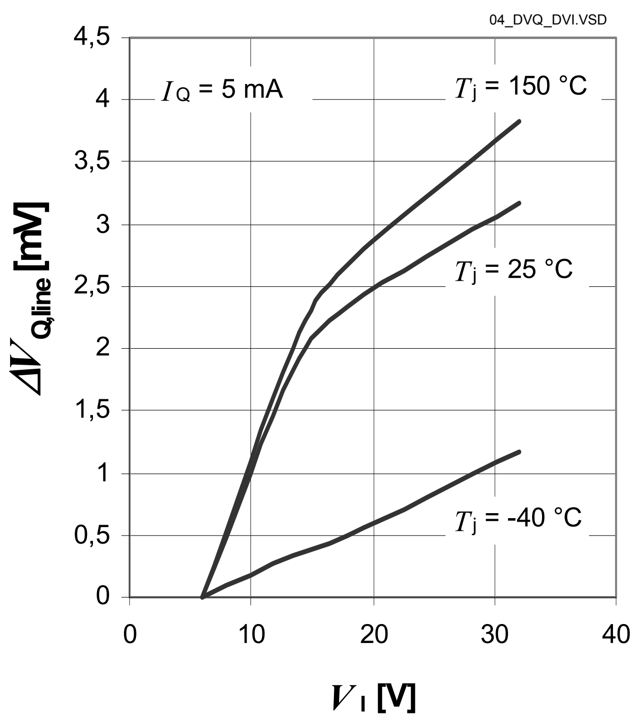
Output Current I_Q versus Input Voltage V_I



Power Supply Ripple Rejection $PSRR$ versus ripple frequency f_r

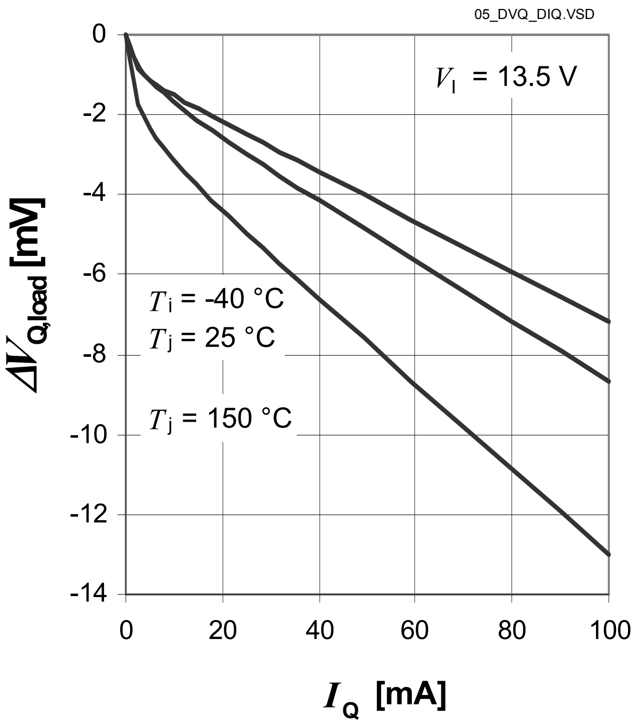


Line Regulation $\Delta V_{Q,line}$ versus Input Voltage Change ΔV_I

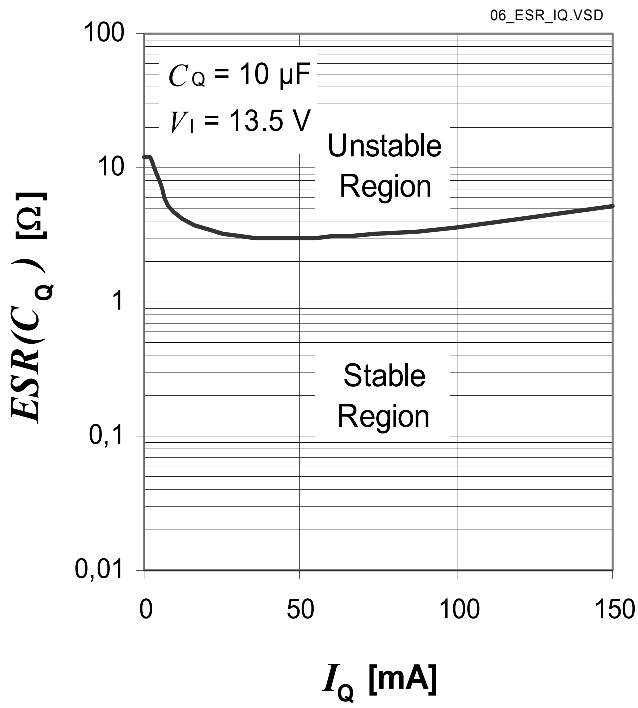


Typical Performance Characteristics Voltage Regulator

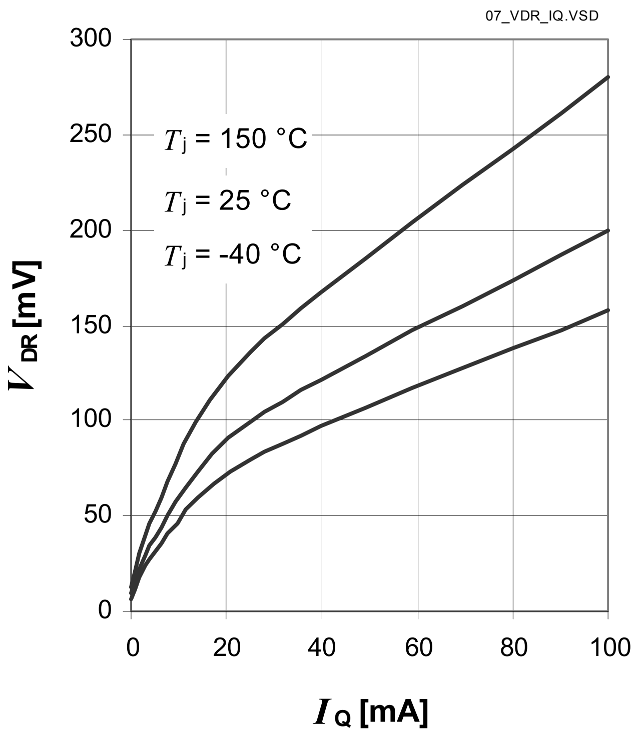
Load Regulation $\Delta V_{Q,load}$ versus Output Current Change ΔI_Q



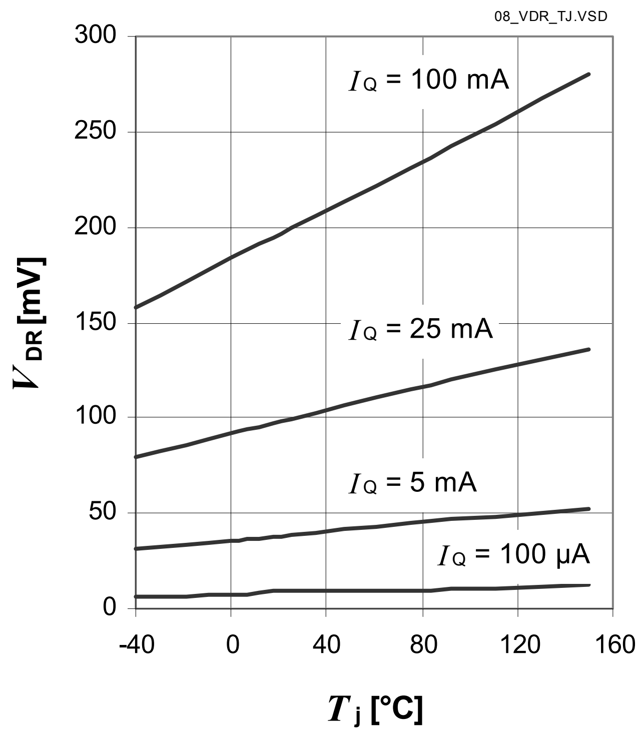
Output Capacitor Series Resistor $ESR(C_Q)$ versus Output Current I_Q



Dropout Voltage V_{dr} versus Output Current I_Q



Dropout Voltage V_{dr} versus Junction Temperature T_j



4.2 Current Consumption

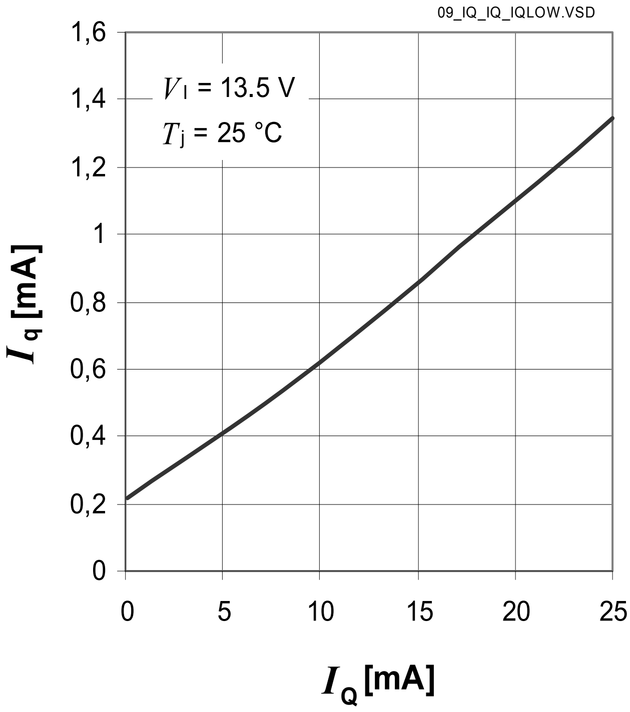
Electrical Characteristics Current Consumption

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, positive current flowing into pin
(unless otherwise specified)

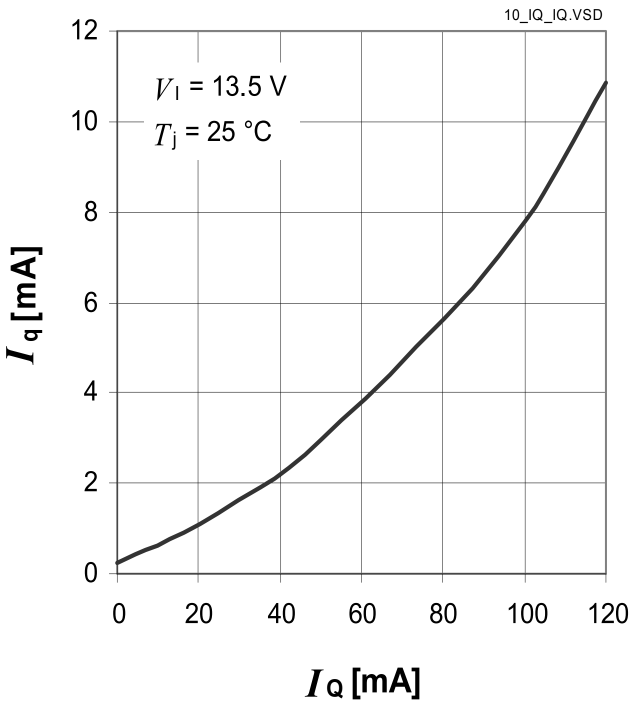
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.1	Current Consumption $I_q = I_I - I_Q$	I_q	–	210	280	µA	I_Q = 100 µA T_j = 25 °C
4.2.2			–	240	300	µA	I_Q = 100 µA T_j ≤ 85 °C
4.2.3			–	0.7	1	mA	I_Q = 10 mA
4.2.4			–	3.5	8	mA	I_Q = 50 mA

Typical Performance Characteristics Current Consumption

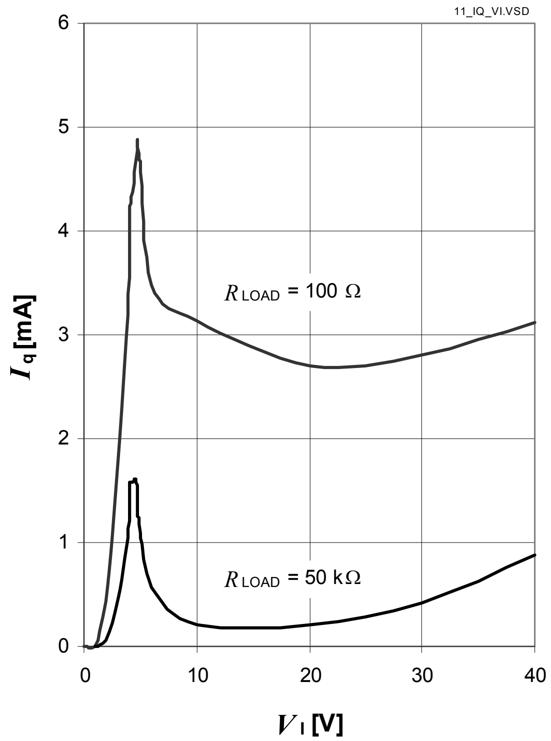
Current Consumption I_q versus Output Current I_Q (I_Q low)



Current Consumption I_q versus Output Current I_Q



Current Consumption I_q versus Input Voltage V_I



4.3 Reset Function

The reset function provides several features:

Output Undervoltage Reset:

An output undervoltage condition is indicated by setting the Reset Output RO to “low”. This signal might be used to reset a microcontroller during low supply voltage.

Power-On Reset Delay Time:

The power-on reset delay time t_{rd} allows a microcontoller and oscillator to start up. This delay time is the time frame from exceeding the reset switching threshold V_{RT} until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time t_{rd} is defined by an external delay capacitor C_D connected to pin D charged by the delay capacitor charge current $I_{D,ch}$ starting from V_D = 0 V.

If the application needs a power-on reset delay time t_{rd} different from the value given in **Item 4.3.9**, the delay capacitor’s value can be derived from the specified values in **Item 4.3.9** and the desired power-on delay time:

$$C_D = \frac{t_{rd,new}}{t_{rd}} \times 1{,}5\text{nF}$$

with

- C_D: capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- t_{rd}: power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor’s tolerance into consideration.

Reset Reaction Time:

The reset reaction time avoids that short undervoltage spikes trigger an unwanted reset “low” signal. The reset reaction rime t_{rr} considers the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor C_D (see typical performance graph for details). Hence, the total reset reaction time becomes:

$$t_{rr} = t_{rd,\,int} + t_{rr,\,d}$$

with

- t_{rr}: reset reaction time
- $t_{rr,int}$: internal reset reaction time
- $t_{rr,d}$: reset discharge

Optional Reset Output Pull-Up Resistor $R_{RO,ext}$:

The Reset Output RO is an open collector output with an integrated pull-up resistor. To improve the EMC behaviour of the component, an external pull-up resistor to the output V_Q can be added. In **Table “Electrical Characteristics Reset Function” on Page 16** a minimum value for the external resistor $R_{RO,ext}$ is given.

Reset Adjust Function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider (R_{ADJ1}, R_{ADJ2}) at pin RADJ. For selecting the default threshold connect pin RADJ to GND.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows:

$$V_{RT,\,new} = \frac{R_{ADJ,\,1} + R_{ADJ,\,2}}{R_{ADJ,\,2}} \times V_{RADJ,\,th}$$

with

- $V_{RT,new}$: the desired new reset switching threshold
- R_{ADJ1}, R_{ADJ2}: resistors of the external voltage divider
- $V_{RADJ,th}$: reset adjust switching threshold given in **Table "Electrical Characteristics Reset Function" on Page 16**

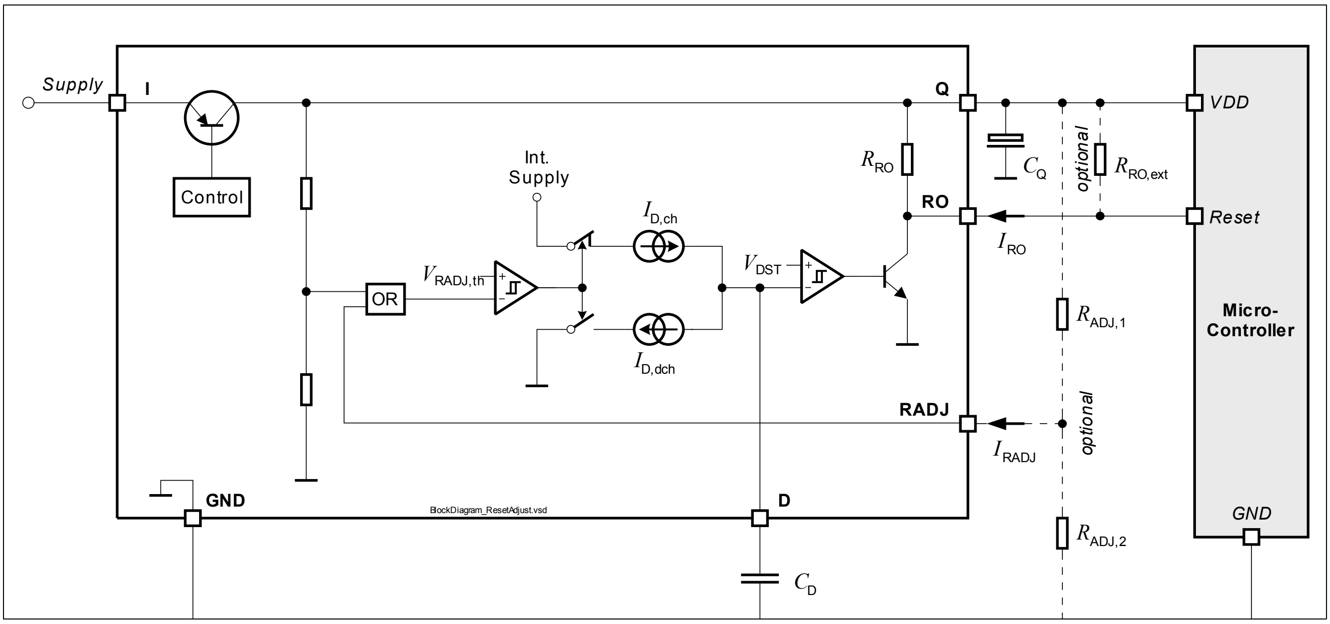


Figure 4 Block Diagram Reset Function

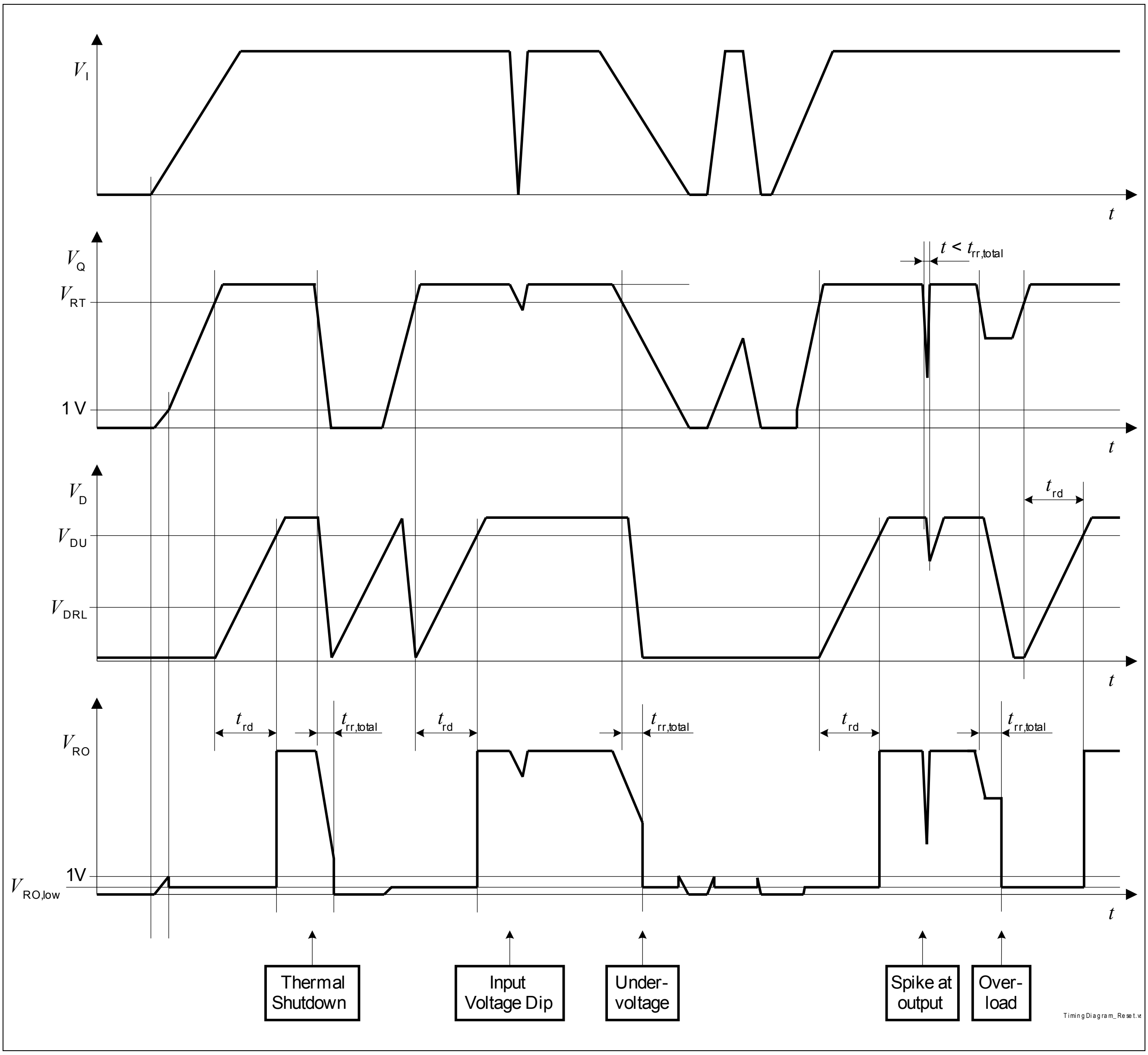


Figure 5 Timing Diagram Reset

Electrical Characteristics Reset Function

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

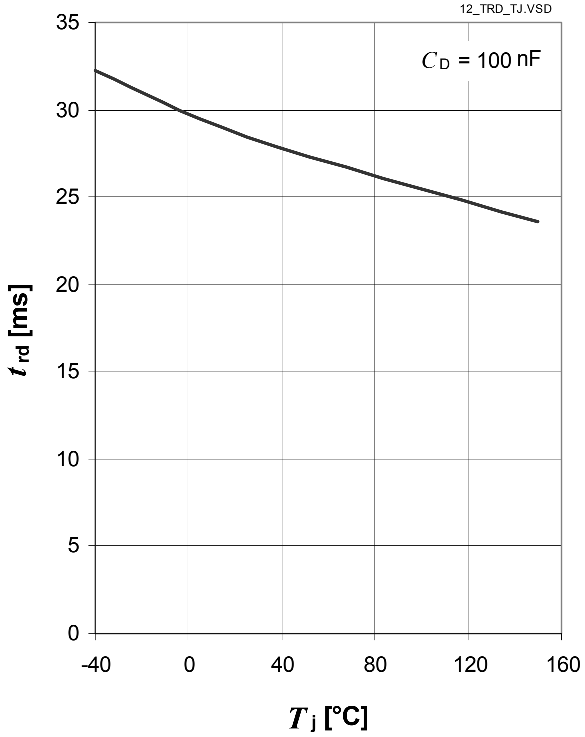
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Undervoltage Reset							
4.3.1	Default Output Undervoltage Reset Switching Thresholds	V_{RT}	4.5	4.65	4.8	V	V_Q decreasing
Output Undervoltage Reset Threshold Adjustment							
4.3.2	Reset Adjust Switching Threshold	$V_{RADJ,th}$	1.26	1.35	1.44	V	3.5 V ≤ V_Q < 5 V
4.3.3	Reset Adjustment Range[1]	$V_{RT,range}$	3.50	–	4.65	V	–
Reset Output RO							
4.3.4	Reset Output Low Voltage	$V_{RO,low}$	–	0.1	0.4	V	1 V ≤ V_Q ≤ V_{RT} no external $R_{RO,ext}$
4.3.5	Reset Output Internal Pull-Up Resistor to V_Q	R_{RO}	10	20	40	kΩ	–
4.3.6	Optional Reset Output External Pull-up Resistor to V_Q	$R_{RO,ext}$	20	–	–	kΩ	1 V ≤ V_Q ≤ V_{RT} ; V_{RO} ≤ 0.4 V
4.3.7	Optional Reset Output External Pull-up Resistor to V_Q	$R_{RO,ext}$	5	–	–	kΩ	2.5 V ≤ V_Q ≤ V_{RT} ; V_{RO} ≤ 0.4 V
Reset Delay Timing							
4.3.8	Delay Pin Output Voltage	V_D	–	–	5	V	–
4.3.9	Power On Reset Delay Time	t_{rd}	100	400	700	µs	C_D = 1.5 nF
4.3.10	Upper Delay Switching Threshold	V_{DU}	–	1.8	–	V	–
4.3.11	Lower Delay Switching Threshold	V_{DL}	–	0.45	–	V	–
4.3.12	Delay Capacitor Charge Current	$I_{D,ch}$	–	6.5	–	µA	V_D = 1 V
4.3.13	Delay Capacitor Reset Discharge Current	$I_{D,dch}$	–	70	–	mA	V_D = 1 V
4.3.14	Delay Capacitor Discharge Time	$t_{rr,d}$	–	30	100	ns	Calculated Value: $t_{rr,d} = C_D*(V_{DU} - V_{DL})/ I_{D,dch}$ C_D = 1.5 nF
4.3.15	Internal Reset Reaction Time	$t_{rr,int}$	–	3	7	µs	C_D = 0 nF [2]
4.3.16	Reset Reaction Time	$t_{rr,total}$	–	3	7.1	µs	Calculated Value: $t_{rr,total} = t_{rr,int} + t_{rr,d}$ C_D = 1.5 nF

1) V_{RT} is scaled linearly, in case the Reset Switching Threshold is modified

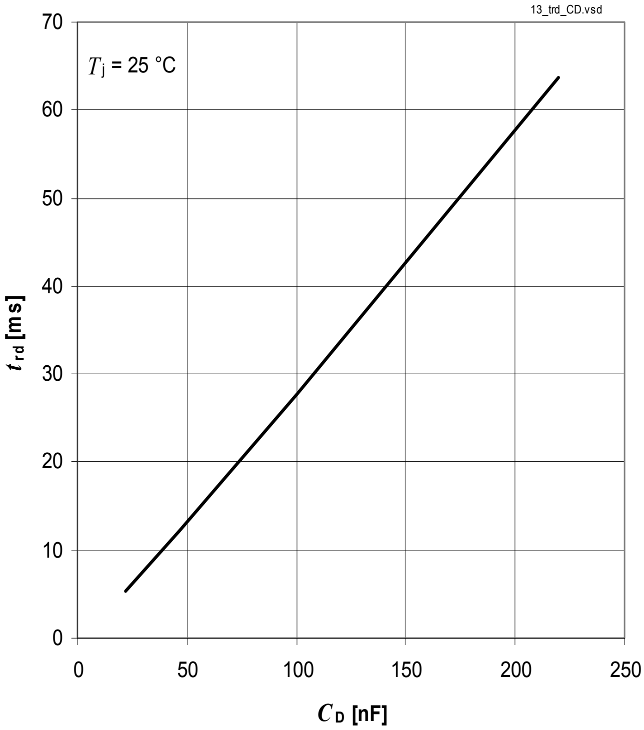
2) parameter not subject to production test; specified by design

Typical Performance Characteristics

Power On Reset Delay Time t_{rd} versus Junction Temperature T_j



Power On Reset Delay Time t_{rd} versus Capacitance C_D



5 Package Outlines

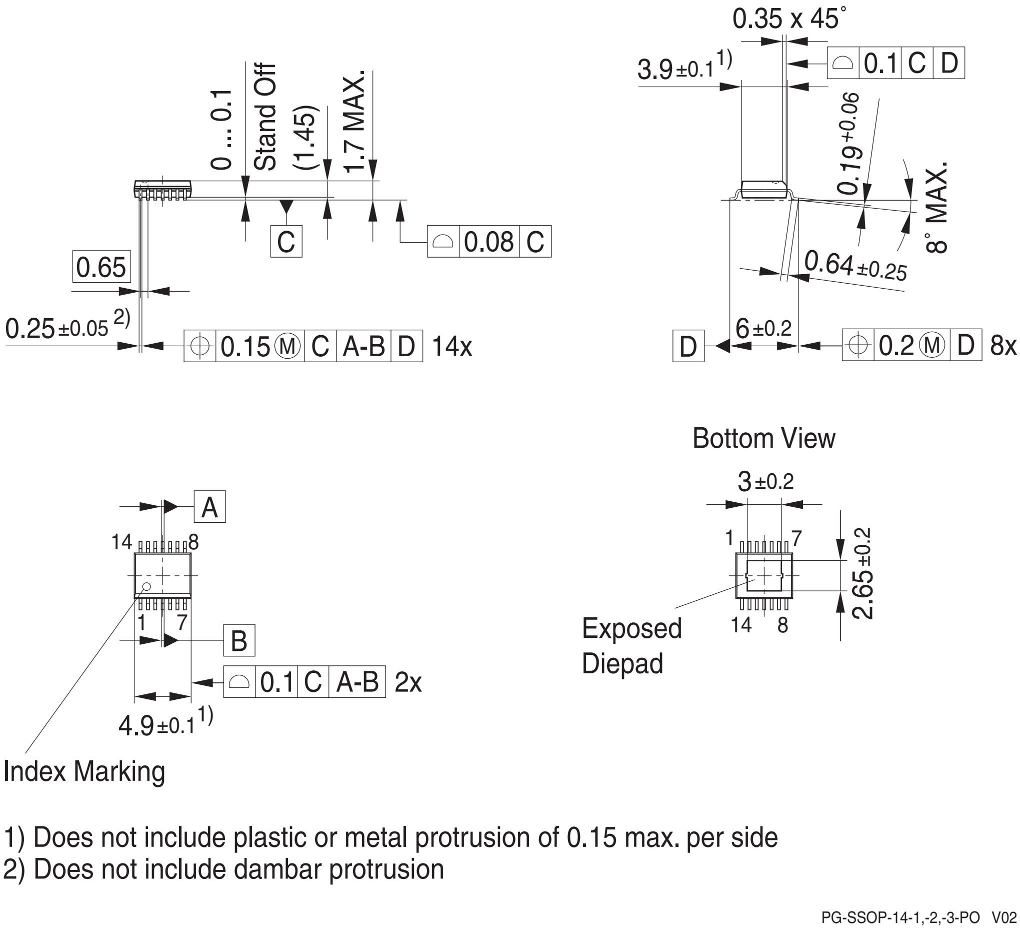


Figure 6 PG-SSOP-14 exposed pad

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/products**.

Dimensions in mm

6 Revision History

Revision	Date	Changes
1.0	2012-07-03	Initial Data sheet

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