Ordering number : ENA1935

LC87F2C64A

CMOS IC
64K-byte FROM and 2048-byte RAM integrated
8-bit 1-chip Microcontroller

ON Semiconductor®
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Overview

The LC87F2C64A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 64K-byte flash ROM (onboard programmable), 2048-byte RAM, an on-chip debugger, sophisticated 16-bit timer/counter (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a calendar function (RTC), High-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, two channels of UART interface (full duplex), four 12bit-PWMs, a 12/8-bit 16-channel AD converter, a system clock frequency divider, an internal reset function and a 28-source 10-vector interrupt feature.

Features

■Flash ROM
- On-board-programmable with wide range (3.0 to 5.5V) of voltage source
- Block-erasable in 128 byte units
- Writable in 2-byte units
- 65536 × 8 bits

■RAM
- 2048 × 9 bits

■Minimum Bus Cycle
- 83.3ns (12MHz at V_{DD}=3.0V to 5.5V)
- 250ns (4MHz at V_{DD}=2.4V to 5.5V)

Note: The bus cycle time here refers to the ROM read speed.

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■Minimum Instruction Cycle Time
- 250ns (12MHz at V_{DD}=3.0 to 5.5V)
- 750ns (4MHz at V_{DD}=2.4 to 5.5V)

■Temperature Range
- -30 to +70 degree Celsius

■Ports
- Normal withstand voltage I/O ports
  Ports I/O direction can be designated in 1-bit units — 71 (P0n, P1n, P2n, P30 to P34, P70 to P73, P8n, PAn, PBn, PCn, Pen, XT2, CF2)
- Normal withstand voltage input port (Oscillator) — 2 (XT1, CF1)
- Reset pin — 1 ($\overline{RES}$)
- Power pins — 6 ($V_{SS}1$ to $V_{SS}3$, $V_{DD}1$ to $V_{DD}3$)

■Timers
- Timer 0: 16-bit timer/counter with a capture register
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with a 8-bit capture register)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  Mode 3: 16-bit counter (with a 16-bit capture register)

- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)

- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)

- Base timer
  1) The clock is selectable from the sub-clock (32.768kHz crystal oscillation/slow RC oscillation), system clock, and prescaler output from timer 0.
  2) Interrupts are programmable in 5 different time schemes.

- Real time clock (RTC)
  1) Used with a base timer, it can be used as a century + year + month + day + hour + minute + second counter.
  2) Calendar counts up to December 31, 2799 with automatic leap-year calculation.

■High-speed Clock Counter
- Count clocks with a maximum clock rate of 24MHz (when main clock is 12MHz)
- Real-time output

■SIO
- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baud rate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
  4) HOLD/X'tal HOLD mode release function by receiving 1-byte (8-bit clock)

- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baud rates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 TCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART: 2 channels
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

■Remote Control Receiver Circuit
- Noise rejection function on P73/INT3/T0IN pin (noise rejection filter's time constant can be selected from 1, 32 or 128 tCYC.)

■AD Converter: 12 bits × 16 channels
- 12 bits/8 bits AD converter resolution selectable

■PWM: 4 channels
- Multi frequency 12-bit PWM

■Clock Output Function
- Output clock with a frequency 1/1, 1/2, 1/4, 1/8, 1/16, 1/32 or 1/64 of the source clock of the system clock.
- Output clock of the sub-clock.

■Buzzer Output
- 2kHz or 4kHz buzzer output can be generated using base timer.

■Watchdog Timer
- Watchdog timer can generate interrupt or system reset.
- Two types of watchdog timers are available:
  (1) External RC watchdog timer
  (2) Base timer watchdog timer
- Watchdog timer with base timer can select only one period (1, 2, 4 or 8s) by the user option.
  Once set the watchdog timer period and start the watchdog timer, the period is not changeable.

■Interrupts

- 28 sources, 10 vector addresses
  (1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  (2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/INT4/T0L
4	0001BH	H or L	INT3/INT5/Base timer0/ Base timer1/RTC
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive/UART2 receive
8	0003BH	H or L	SIO1/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, 5/SPI
10	0004BH	H or L	Port0/T4/T5/PWM0, 1

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

- IFLG (List of interrupt source flag function)
  (1) Shows a list of interrupt source flags that caused a branching to a particular vector address (shown in the table above).

■Subroutine Stack Levels

- 1024 levels (Stack is allocated in RAM)

■High-speed Multiplication/Division Instructions

- 16 bits×8 bits (5 tCYC execution time)
- 24 bits×16 bits (12 tCYC execution time)
- 16 bits÷8 bits (8 tCYC execution time)
- 24 bits÷16 bits (12 tCYC execution time)

■Oscillation Circuits

- On-chip fast RC oscillation circuit : For system clock
- On-chip slow RC oscillation circuit : For system clock
- CF oscillation circuit : For system clock, with built in Rf
- Crystal oscillation circuit : For low-speed system clock
- On-chip Frequency variable RC oscillation circuit : For system clock
  (1) Adjustable by ±4% (typical) step from selected center frequency
  (2) Frequency measurable by referencing input signal from XT1

■System Clock Divider Function

- Enables low power consumption operation
- The minimum instruction cycle selectable from 250ns, 500ns, 1.0µs, 2.0µs, 4.0µs, 8.0µs, 16.0µs, 32.0µs, and 64µs (at a main clock rate of 12MHz).

■Internal Reset Function

- Power-on reset (POR) function
  (1) POR reset is generated only at power-on.
  (2) The POR release level can be selected through option configuration.
- Low-voltage detection reset (LVD) function
  (1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  (2) The use/no-use of the LVD function and the low voltage threshold level can be selected through option configuration.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  (1) Oscillation is not halted automatically.
  (2) There are three ways of resetting the HALT mode.
    1) Setting the reset pin to the lower level
    2) System resetting by watchdog timer
    3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  (1) The CF, RC, crystal, and frequency variable RC oscillators automatically stop operation.
  (2) There are five ways of resetting the HOLD mode.
    1) Setting the reset pin to the lower level
    2) System resetting by watchdog timer
    3) Setting at least one of the INT0, INT1, INT2, INT3, INT4, INT5 pins to the specified level
    4) Having an interrupt source established at port 0
    5) Having an interrupt source established in SPI receiving 1-byte (8-bit clock)
- X''tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  (1) The CF, RC, and frequency variable RC oscillators automatically stop operation.
  (2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  (3) Power-save mode is available for even lower current consumption.
  (4) There are seven ways of resetting the X'tal HOLD mode.
    1) Setting the reset pin to the low level
    2) System resetting by watchdog timer
    3) Setting at least one of the INT0, INT1, INT2, INT3, INT4, INT5 pins to the specified level
    4) Having an interrupt source established at port0
    5) Having an interrupt source established in the base timer circuit
    6) Having an interrupt source established in the RTC
    7) Having an interrupt source established in SPI receiving 1-byte (8-bit clock)

■On-chip Debugging Function (flash ROM version)

- Supports software debugging with the test device installed on the target board.

■Data Security Function (flash ROM version)

- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: The data security function does not necessarily provide an absolute data security.

■Shipping form

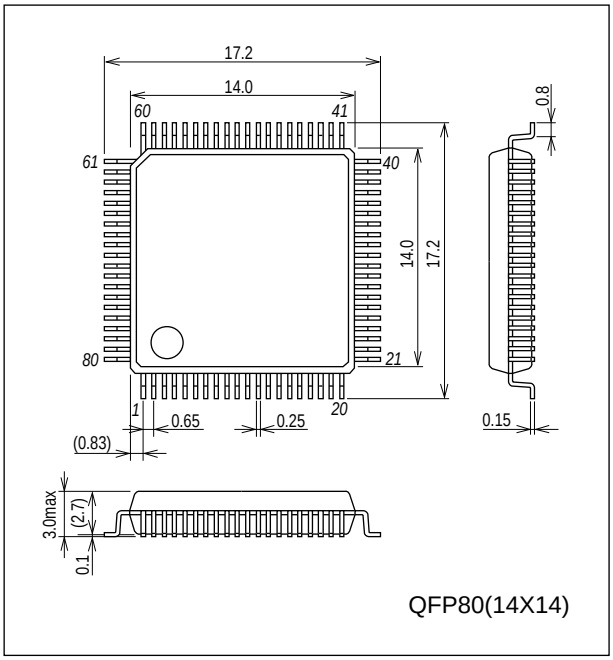
- QFP80 (14×14): Lead-free type
- TQFP80J (12×12): Lead-free type

■Development Tools

- On-chip-debugger: TCB87 TypeB + LC87F2C64A

Package Dimensions

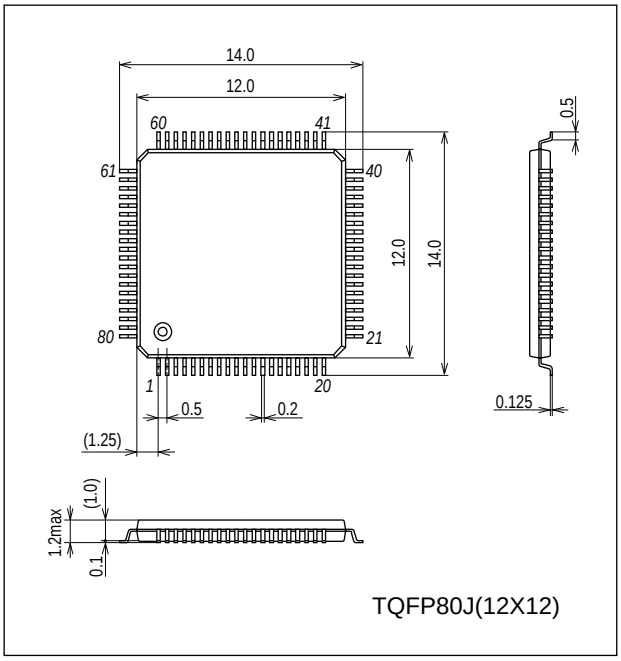
unit : mm (typ)
3255



QFP80(14X14)

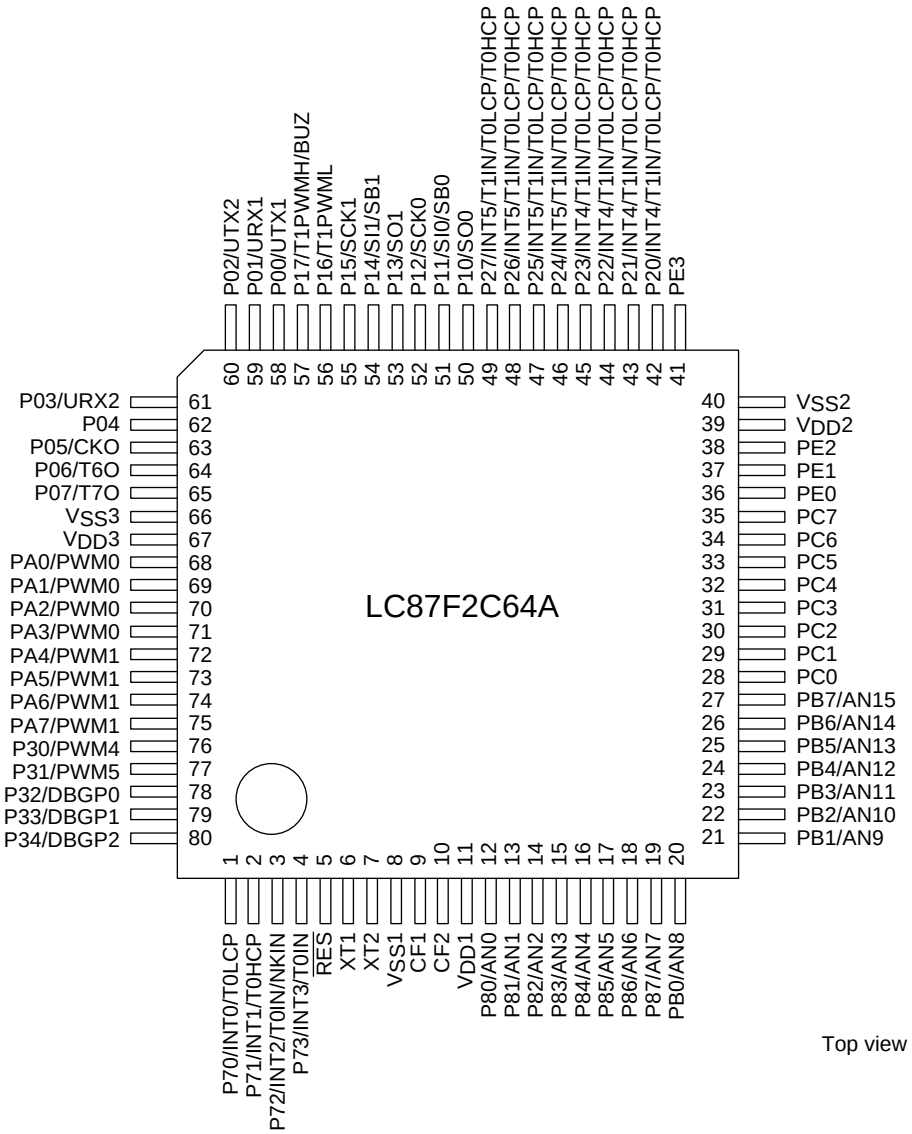
Package Dimensions

unit : mm (typ)
3290



TQFP80J(12X12)

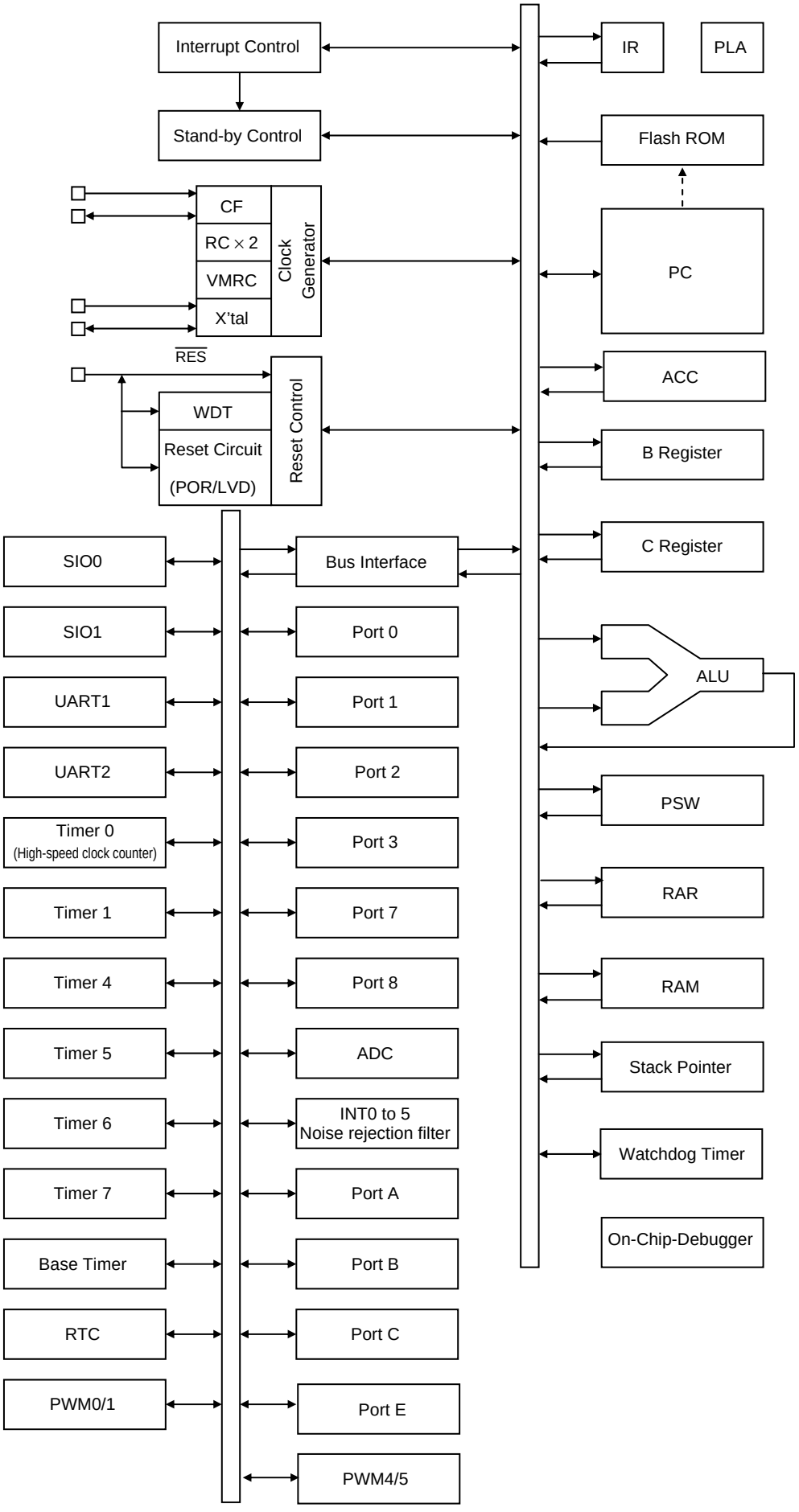
Pin Assignment



Top view

QFP80 (14×14) “Lead-free type”
TQFP80J (12×12) “Lead-free type”

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$ to $V_{SS}3$</td><td>-</td><td>- Power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$ to $V_{DD}3$</td><td>-</td><td>+ Power supply pin</td><td>No</td></tr>
<tr><td>V1</td><td>-</td><td>Open</td><td>No</td></tr>
<tr><td>VDC</td><td>-</td><td>Open</td><td>No</td></tr>
<tr><td>CUP1, CUP2</td><td>-</td><td>Open</td><td>No</td></tr>
<tr><td>PORT 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• HOLD release input
• Port 0 interrupt input
Other functions:
P00: UART1 transmit
P01: UART1 receive
P02: UART2 transmit
P03: UART2 receive
P05: System clock output
P06: Timer 6 toggle output
P07: Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>PORT 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
Other functions:
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: Timer 1PWML output
P17: Timer 1PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>PORT 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
Other functions:
P20 to P23: INT4 input/HOLD release input/timer 1 event input
/timer 0L capture input/timer 0H capture input
P24 to P27: INT5 input/HOLD release input/timer 1 event input
/timer 0L capture input/timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT5</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>PORT 3
P30 to P34</td><td>I/O</td><td>• 5-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
Other functions:
P30: PWM4 output
P31: PWM5 output
P32 (DBGP0) to P34 (DBGP2): On-chip-debugger port (Only on Flash version)</td><td>Yes</td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>PORT 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
Other functions:
P70: INT0 input/HOLD release input/timer 0L capture input
/watchdog timer output
P71: INT1 input/HOLD release input/timer 0H capture input
P72: INT2 input/HOLD release input/timer 0 event input
/timer 0L capture input/high speed clock counter input
P73: INT3 input (with noise filter)/ HOLD release input
/timer 0 event input/timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>No</td></tr>
<tr><td>PORT 8
P80 to P87</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
Other functions:
P80 to P87(AN0 to AN7): AD converter input</td><td>No</td></tr>
<tr><td>PORT A
PA0 to PA7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
Other functions:
PA0 to PA3: PWM0 output
PA4 to PA7: PWM1 output</td><td>Yes</td></tr>
<tr><td>PORT B
PB0 to PB7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
Other functions:
PB0 to PB7 (AN8 to AN15): AD converter input</td><td>Yes</td></tr>
<tr><td>PORT C
PC0 to PC7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.</td><td>Yes</td></tr>
<tr><td>PORT E
PE0 to PE3</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.</td><td>Yes</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input pin/Internal reset output pin</td><td>No</td></tr>
<tr><td>XT1</td><td>I</td><td>• Input for 32.768kHz crystal oscillation
Other functions:
• General purpose input port
*Connect to $V_{DD}1$ when the port is not used.</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• Output for 32.768kHz crystal oscillation
Other functions:
• General-purpose I/O port
*Must be set for oscillation mode and kept open if not to be used.</td><td>No</td></tr>
<tr><td>CF1</td><td>I</td><td>• Input for ceramic resonator
Other functions:
• General purpose input port
*Connect to $V_{DD}1$ when the port is not used.</td><td>No</td></tr>
<tr><td>CF2</td><td>I/O</td><td>• Output for ceramic resonator
Other functions:
• General-purpose I/O port
*Must be set for oscillation mode and kept open if not to be used.</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up/down resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected iIn Units of	Option Type	Output Type	Pull-Up Resistor
P00 to P07	1bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P10 to P17	1bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P34	1bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	Nch-open drain	No
PA0 to PA7	1bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PB0 to PC7	1bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PC0 to PC7	1bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PE0 to PE3	1bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
XT2	-	No	32.768kHz crystal oscillator output or Nch-open drain when selected as normal port	No
CF2	-	No	Ceramic resonator output or Nch-open drain when selected as normal port	No

User Option Table

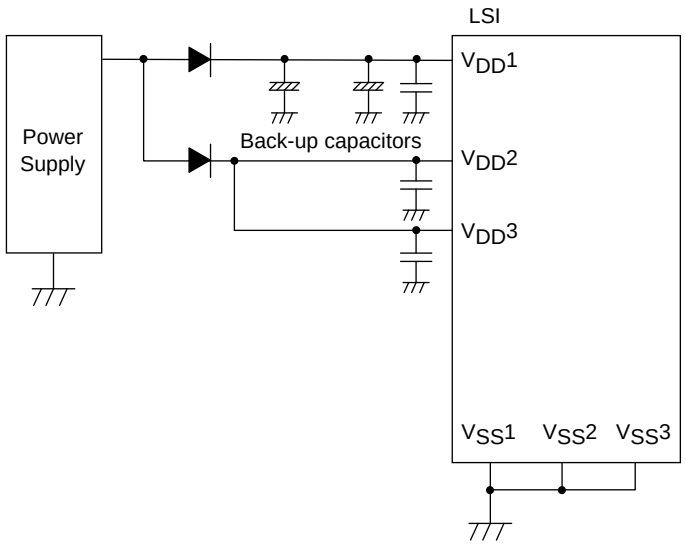
Option Name	Option to be Applied on	Mask-ROM Version*1	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	Yes	Yes	1 bit	CMOS
					Nch-open drain
	P10 to P17	Yes	Yes	1 bit	CMOS
					Nch-open drain
	P20 to P27	Yes	Yes	1 bit	CMOS
					Nch-open drain
	P30 to P34	Yes	Yes	1 bit	CMOS
					Nch-open drain
	PA0 to PA7	Yes	Yes	1 bit	CMOS
					Nch-open drain
	PB0 to PB7	Yes	Yes	1 bit	CMOS
					Nch-open drain
	PC0 to PC7	Yes	Yes	1 bit	CMOS
					Nch-open drain
	PE0 to PE3	Yes	Yes	1 bit	CMOS
					Nch-open drain
Program start address	-	No*2	Yes	-	0000H
					FE00H
Base timer Watchdog timer	Watchdog timer period	Yes	Yes	-	1s
					2s
					4s
					8s
Low-Voltage detect function	Detection level (Enable)	-	Yes	-	
	Power-on reset level (Disable)	-	Yes	-	

*1: The option selection cannot to be changed after the mask is created.
*2: Program start address for the mask-ROM version is 0000H.

*Note1: Connect the IC as shown below to minimize the noise input to the $V_{DD}1$. Be sure to electrically short the $V_{SS}1$, $V_{SS}2$ and $V_{SS}3$ pins.

*Note2: The internal memory is sustained by $V_{DD}1$. If none of $V_{DD}2$ and $V_{DD}3$ are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time. Make sure that the port outputs are held at the low level in the HOLD backup mode.

Example of power connection when power-save mode is used



Absolute Maximum Ratings at Ta=25°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	• $V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+6.5	V
Input voltage		VI	XT1, CF1, $\overline{RES}$			-0.3		V_{DD}+0.3	
Input/output voltage		VIO	Ports 0, 1, 2, 3, 7, 8, A, B, C, E, XT2, CF2			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3, A, B, C, E	• CMOS output select • Per 1 applicable pin		-10			mA
		IOPH(2)	P71, P72, P73	• Per 1 applicable pin		-5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3, A, B, C, E	• CMOS output select • Per 1 applicable pin		-7.5			
		IOMH(2)	P71, P72, P73	• Per 1 applicable pin		-3			
	Total output current	∑IOAH(1)	Port 0, P14 to P17	• Total of all applicable pins		-25			
		∑IOAH(2)	Port 3, A	• Total of all applicable pins		-25			
		∑IOAH(3)	Port 0, 3, A P14 to P17	• Total of all applicable pins		-45			
		∑IOAH(4)	Port 2 P10 to P13,PE3	• Total of all applicable pins		-25			
		∑IOAH(5)	Port B, C, PE0 to PE2	• Total of all applicable pins		-25			
		∑IOAH(6)	Port 2, B, C, E P10 to P13	• Total of all applicable pins		-45			
		∑IOAH(7)	P71, P72, P73	• Total of all applicable pins		-5			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 2, 3, A, B, C, E	• Per 1 applicable pin				20	
		IOPL(2)	Port 7, 8 XT2, CF2	• Per 1 applicable pin				10	
	Mean output current (Note 1-1)	IOML(1)	Ports 0, 1, 2, 3, A, B, C, E	• Per 1 applicable pin				15	
		IOML(2)	Port 7, 8 XT2, CF2	• Per 1 applicable pin				7.5	
	Total output current	∑IOAL(1)	Port 0, P14 to P17	• Total of all applicable pins				45	
		∑IOAL(2)	Port 3, A	• Total of all applicable pins				45	
		∑IOAL(3)	Port 0, 3, A P14 to P17	• Total of all applicable pins				80	
		∑IOAL(4)	Port 2 P10 to P13, PE3	• Total of all applicable pins				45	
		∑IOAL(5)	Port B, C, PE0 to PE2	• Total of all applicable pins				45	
		∑IOAL(6)	Port 2, B, C,E P10 to P13	• Total of all applicable pins				80	
		∑IOAL(7)	Port 7, XT2	• Total of all applicable pins				15	
		∑IOAL(8)	Port 8, CF2	• Total of all applicable pins				15	
		∑IOAL(9)	Port 7, 8, XT2, CF2	• Total of all applicable pins				20	
Power dissipation		Pd max(1)	QFP80	• Ta=-30 to +70°C • Package only				T.B.D	mW
				• Ta=-30 to +70°C • Package with thermal resistance board (Note 1-2)				T.B.D	
		Pd max(2)	TQFP80J	• Ta=-30 to +70°C • Package only				T.B.D	
				• Ta=-30 to +70°C • Package with thermal resistance board (Note 1-2)				T.B.D	
Operating ambient temperature		Topr				-30		+70	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6tmm, glass epoxy) is used.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta=-30 to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	• 0.245µs≤tCYC≤200µs		3.0		5.5	V
	$V_{DD}(2)$		• 0.735µs≤tCYC≤200µs		2.4		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	• RAM and register contents sustained in HOLD mode.		2.2		5.5	
High level input voltage	$V_{IH}(1)$	Ports 0, 1, 2, 3, 8, A, B, C, E, P71, P72, P73 P70 port input /interrupt side	• Output disabled	2.4 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(2)$	Port 70 watchdog timer side	• Output disabled	2.4 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(3)$	XT1, XT2, CF1, CF2, $\overline{RES}$		2.4 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 0, 1, 2, 3, 8, A, B, C, E, P71, P72, P73 P70 port input /interrupt side	• Output disabled	2.4 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
	$V_{IL}(2)$	Port 70 watchdog timer side	• Output disabled	2.4 to 5.5	V_{SS}		$0.8V_{DD}-1.0$	
	$V_{IL}(3)$	XT1, XT2, CF1, CF2, $\overline{RES}$		2.4 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-1)	tCYC (Note 2-2)			3.0 to 5.5	0.245		200	µs
				2.4 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio = 1/1 • External system clock duty = 50±5%	3.0 to 5.5	0.1		12	MHz
				2.4 to 5.5	0.1		4	
			• CF2 pin open • System clock frequency division ratio = 1/2 • External system clock duty = 50±5%	3.0 to 5.5	0.2		24	
				2.4 to 5.5	0.2		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	• 12MHz ceramic oscillation • See Fig. 1.	3.0 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	• 4MHz ceramic oscillation • See Fig. 1.	2.4 to 5.5		4		
	FmVMRC(1)		• Frequency variable RC source oscillation • VMRAJ2 to 0 = 4 • VMFAJ2 to 0 = 0 • VMSL4M = 0	3.0 to 5.5		10		
	FmVMRC(2)		• Frequency variable RC source oscillation • VMRAJ2 to 0 = 4 • VMFAJ2 to 0 = 0 • VMSL4M=1	2.4 to 5.5		4		
	FmRC		• Internal fast RC oscillation	2.4 to 5.5		500		kHz
	FsRC		• Internal slow RC oscillation	2.4 to 5.5		50		
	FsX'tal	XT1, XT2	• 32.768kHz crystal oscillation • See Fig. 2.	2.4 to 5.5		32.768		

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Table 1, 2 for the oscillation constants

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Frequency variable RC oscillation usable range	OpVMRC(1)		• VMSL4M=0	3.0 to 5.5	8	10	12	MHz
	OpVMRC(2)		• VMSL4M=1	2.4 to 5.5	3.5	4	4.5	
Frequency variable RC oscillation adjustment range	VmADJ(1)		• 1 step of VMRAJn (large range)	2.4 to 5.5	8	24	64	%
	VmADJ(2)		• 1 step of VMFAJn (small range)	2.4 to 5.5	1	4	8	

Electrical Characteristics at Ta=-30 to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 2, 3, 7, 8, A, B, C, E	• Output disabled • Pull-up resistor off • $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.4 to 5.5			1	µA
	I_{IH}(3)	$\overline{RES}$	• $V_{IN}=V_{DD}$	2.4 to 5.5			1	
	I_{IH}(4)	XT1, XT2 CF1, CF2	• Configured as input ports • $V_{IN}=V_{DD}$	2.4 to 5.5			1	
	I_{IH}(5)	CF1	• $V_{IN}=V_{DD}$	2.4 to 5.5			15	
Low level input current	I_{IL}(1)	Ports 0, 1, 2, 3, 7, 8, A, B, C, E	• Output disabled • Pull-up resistor off • $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.4 to 5.5	-1			
	I_{IL}(2)	$\overline{RES}$	• $V_{IN}=V_{SS}$	2.4 to 5.5	-1			
	I_{IL}(3)	XT1, XT2 CF1, CF2	• Configured as input ports • $V_{IN}=V_{SS}$	2.4 to 5.5	-1			
	I_{IL}(4)	CF1	• $V_{IN}=V_{SS}$	2.4 to 5.5	-15			
High level output voltage	V_{OH}(1)	Ports 0, 1, 2, 3, A, B, C	• I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)		• I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(3)		• I_{OH}=-0.2mA	2.4 to 5.5	V_{DD}-0.4			
	V_{OH}(4)	P71, P72, P73	• I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(5)		• I_{OH}=-0.2mA	2.4 to 5.5	V_{DD}-0.4			
	V_{OH}(6)	P30, P31, Port A (using as PWM)	• I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	V_{OH}(7)		• I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(8)		• I_{OH}=-1.0mA	2.4 to 5.5	V_{DD}-0.4			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 2, 3, A, B, C, E	• I_{OL}=10mA	4.5 to 5.5			1.5	
	V_{OL}(2)		• I_{OL}=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(3)		• I_{OL}=1.0mA	2.4 to 5.5			0.4	
	V_{OL}(4)	Port 7, 8 XT2, CF2	• I_{OL}=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(5)		• I_{OL}=1.0mA	2.4 to 5.5			0.4	
Pull-up resistance	Rpu	Ports 0, 1, 2, 3, 7, A, B, C, E	• $V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	40	70	kΩ
				2.4 to 4.5	25	70	150	
Hysteresis voltage	VHYS	Ports 0, 1, 2, 3, 7, A, $\overline{RES}$		2.4 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	• f=1MHz • Ta=25°C • For pins other than that under test: $V_{IN}=V_{SS}$	2.4 to 5.5		10		pF

Serial I/O Characteristics at Ta=-30 to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 6.	2.4 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.4 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	
Serial input	Data setup time		tsDI	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.4 to 5.5	0.03			µs
	Data hold time		thDI				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-3)	2.4 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: When using serial clock input under continuous data transmission/reception mode, the time from SI0RUN is set while serial clock is “H” to the first falling edge of serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 6.	2.4 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.4 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.4 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.4 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta=-30 to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70) INT1(P71) INT2(P72) INT3(P73) INT4(P20 to P23) INT5(P24 to P27)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.4 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.4 to 5.5	256			
	tPIH(5) tPIL(5)	NKIN(P72)	• High speed clock counter countable	2.4 to 5.5	1/12			
	tPIL(6)	$\overline{RES}$	• External reset input mode • Resetting is enabled	2.4 to 5.5	200			µs

AD Converter Characteristics at $V_{SS}1=V_{SS}2=V_{SS}3=0V$

<12bits AD Converter Mode / Ta=-30 to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87) AN8(PB0) to AN15(PB7)		3.0 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±16	LSB
Conversion time	tCAD		• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	µs
				3.0 to 5.5	64		115	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		• VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		• VAIN=V_{SS}	3.0 to 5.5	-1			

<8bits AD Converter Mode / Ta=-30 to +70°C>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN7(P87) AN8(PB0) to AN15(PB7)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	tCAD		• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	20		95	µs
				3.0 to 5.5	40		95	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		• VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		• VAIN=V_{SS}	3.0 to 5.5	-1			

Conversion time calculation formulas:
12bits AD Converter Mode : TCAD(Conversion time) = ((52/(AD division ratio))+2)×(1/3)×tCYC
8bits AD Converter Mode : TCAD(Conversion time) = ((32/(AD division ratio))+2)×(1/3)×tCYC

External oscillation (FmCF)	Operating supply voltage range (V_{DD})	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12bit AD	8bit AD
CF-12MHz	4.0V to 5.5V	1/1	250ns	1/8	34.8µs	21.5µs
	3.0V to 5.5V	1/1	250ns	1/16	69.5µs	42.8µs
CF-4MHz	3.0V to 5.5V	1/1	750ns	1/8	104.5µs	64.5µs

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Power-on Reset (POR) Characteristics at Ta=-30 to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
			Option selected voltage	min	typ	max	unit
POR release voltage	PORRL		• Select from option. (Note 7-1)	1.67V		1.67		V
				1.97V		1.97		
				2.07V		2.07		
				2.37V		2.37		
				2.57V		2.57		
				2.87V		2.87		
				3.86V		3.86		
				4.35V		4.35		
Detection voltage unknown state	POUKS		• See Fig. 8. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		• Power supply rise time from 0V to x V.				100	ms

Note7-1: The POR release level can be selected out of 7 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

Low Voltage Detection Reset (LVD) Characteristics at Ta=-30 to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
			Option selected voltage	min	typ	max	unit
LVD reset Voltage (Note 8-2)	LVDET		• Select from option. (Note 8-1) (Note 8-3) • See Fig. 9.	1.91V		1.91		V
				2.01V		2.01		
				2.31V		2.31		
				2.51V		2.51		
				2.81V		2.81		
				3.79V		3.79		
				4.28V		4.28		
LVD hysteresis width	LVHYS			1.91V		55		mV
				2.01V		55		
				2.31V		55		
				2.51V		55		
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unknown state	LVUKS		• See Fig. 9. (Note 8-4)			0.7	0.95	V
Low voltage detection minimum width (Reply sensitivity)	TLVDW		• LVDET-0.5V • See Fig. 10.		0.2			ms

Note8-1: The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.

Consumption Current Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Current consumption during normal operation (Note 9-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• FmCF=12MHz Ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped. • Internal RC oscillation stopped. • System clock: CF oscillation 12MHz • Divider : 1/1	4.5 to 5.5		8.4	22.1	mA
				3.0 to 3.6		4.9	12.1	
	IDDOP(2)		• FmCF=4MHz Ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped. • Internal RC oscillation stopped. • System clock: CF oscillation 4MHz • Divider : 1/1	4.5 to 5.5		3.5	10.0	
				2.4 to 3.6		2.8	6.3	
	IDDOP(3)		• FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • FmVMRC=10MHz Frequency variable RC oscillation • Internal RC oscillation stopped. • System clock: Frequency variable RC oscillation 10MHz • Divider :1/1	4.5 to 5.5		6.9	16.6	
				2.4 to 3.6		4.2	101	
	IDDOP(4)		• FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • FmVMRC=4MHz Frequency variable RC oscillation • Internal RC oscillation stopped. • System clock: Frequency variable RC oscillation 4MHz • Divider :1/1	4.5 to 5.5		2.8	8.5	
				2.4 to 3.6		2.5	5.4	
	IDDOP(5)		• FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped. • Internal RC oscillation=Fast RC oscillation • System clock: Fast RC oscillation • Divider :1/1	4.5 to 5.5		400	1000	µA
				2.4 to 3.6		300	600	
	IDDOP(6)		• FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped. • Internal RC oscillation stopped. • System clock: 32.768kHz • Divider :1/1	4.5 to 5.5		74	269.4	
				2.4 to 3.6		26.1	110.1	

Note 9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Current consumption during HALT mode (Note 9-1)	IDDHALT(1)	$V_{DD}1$ = $V_{DD}2$ = $V_{DD}3$	HALT mode • FmCF=12MHz Ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped. • Internal RC oscillation stopped. • System clock: CF oscillation 12MHz • Divider : 1/1	4.5 to 5.5		3.3	8.4	mA
				3.0 to 3.6		1.7	4.3	
	IDDHALT(2)		HALT mode • FmCF=4MHz Ceramic resonator oscillation • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped. • Internal RC oscillation stopped. • System clock: CF oscillation 4MHz • Divider : 1/1	4.5 to 5.5		0.3	4.1	
				2.4 to 3.6		0.1	1.8	
	IDDHALT(3)		HALT mode • FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • FmVMRC=10MHz Frequency variable RC oscillation • Internal RC oscillation stopped. • System clock: Frequency variable RC oscillation 10MHz • Divider :1/1	4.5 to 5.5		2.3	5.8	
				2.4 to 3.6		1.3	3.2	
	IDDHALT(4)		HALT mode • FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • FmVMRC=4MHz Frequency variable RC oscillation • Internal RC oscillation stopped. • System clock: Frequency variable RC oscillation 4MHz • Divider :1/1	4.5 to 5.5		1.0	2.5	
				2.4 to 3.6		0.5	1.3	
	IDDHALT(5)		HALT mode • FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped. • Internal RC oscillation=Fast RC oscillation • System clock: Fast RC oscillation • Divider :1/1	4.5 to 5.5		200	500	µA
				2.4 to 3.6		100	200	
	IDDHALT(6)		HALT mode • FmCF=0Hz (No oscillation) • FsX'tal=32.768kHz crystal oscillation • Frequency variable RC oscillation stopped. • Internal RC oscillation stopped. • System clock: 32.768kHz • Divider :1/1	4.5 to 5.5		57.2	230.9	
				2.4 to 3.6		13.6	83.2	

Note 9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Current consumption during HOLD mode (Note 9-1)	IDDHOLD(1)	$V_{DD}1$ = $V_{DD}2$ = $V_{DD}3$	HOLD mode • CF1=V_{DD} or open (when using external clock)	4.5 to 5.5		0.1	52	µA
				2.4 to 3.6		0.04	22	
Current consumption during Date/time clock HOLD mode (Note 9-1)	IDDHOLD(3)		Date/time clock HOLD mode • CF1=V_{DD} or open (when using external clock) • FmX'tal=32.768kHz crystal oscillation • Normal mode	4.5 to 5.5		49.9	213	
				2.4 to 3.6		9.6	73.4	
	IDDHOLD(4)		Date/time clock HOLD mode • CF1=V_{DD} or open (when using external clock) • FmX'tal=32.768kHz crystal oscillation • Power save mode	4.5 to 5.5		1.0	94.3	
				2.4 to 3.6		0.76	39.3	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1$ = $V_{SS}2$ = $V_{SS}3$ = 0V

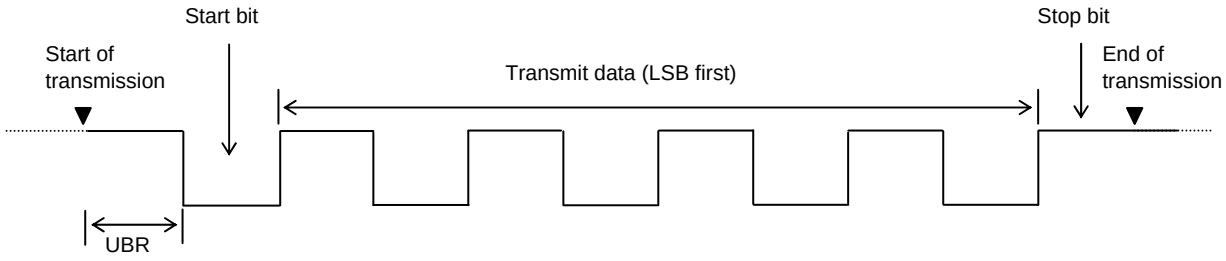
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW	$V_{DD}1$	• Current of the Flash module	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		• Erase time	3.0 to 5.5		20	30	ms
	tFW(2)		• Program time			40	60	µs

UART (Full Duplex) Operating Conditions at Ta = -30°C to +70°C, $V_{SS}1$ = $V_{SS}2$ = $V_{SS}3$ = 0V

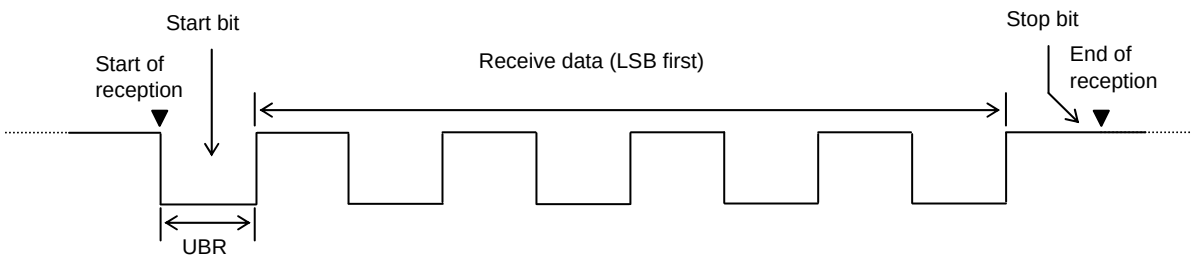
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	UTX1(P00), URX1(P01) UTX2(P02), URX2(P03)		2.4 to 5.5	16/3		8192/3	tCYC

Data length: 7, 8, and 9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (first transmit data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (first receive data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table1. Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]	[V]	typ [ms]	max [ms]	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table2. Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]	[V]	typ [s]	max [s]	
32.768kHz										

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

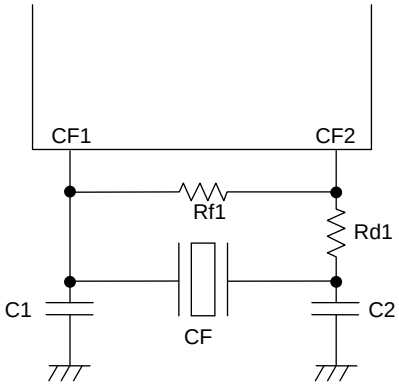


Figure 1 Ceramic Oscillation Circuit

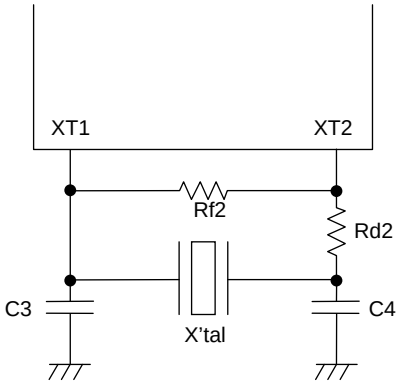


Figure 2 Crystal Oscillation Circuit

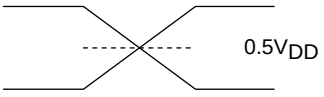
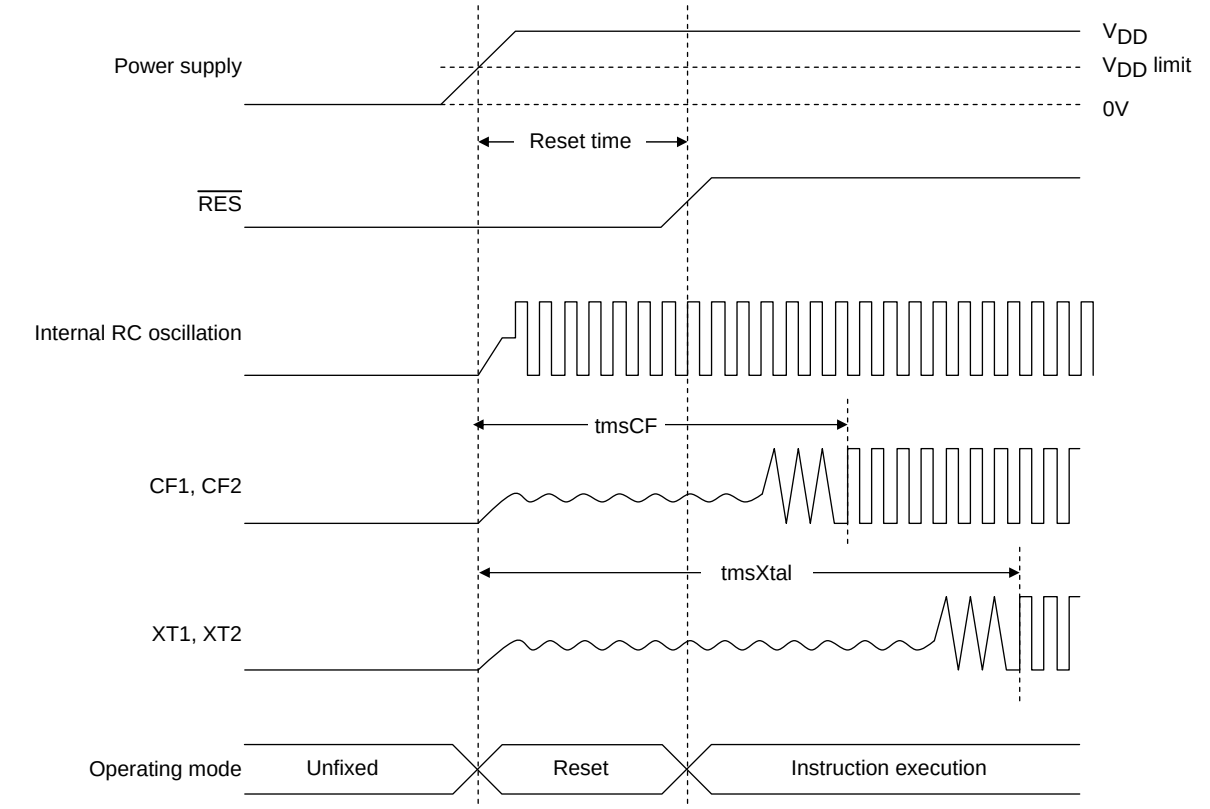
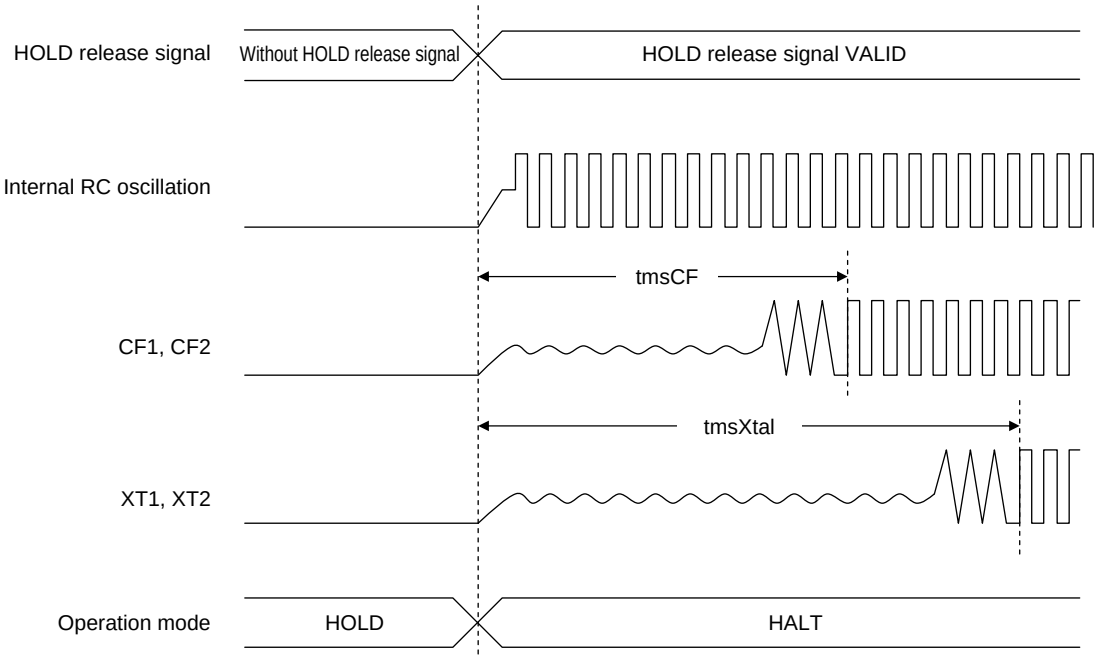


Figure 3 AC Timing Measurement Point

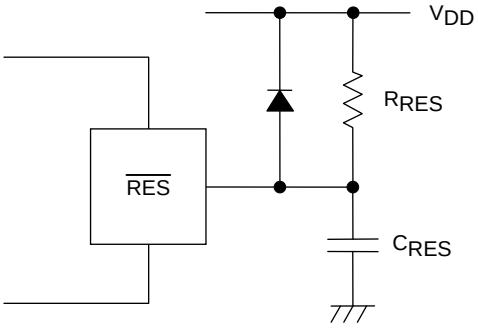


Reset Time and Oscillation Stable Time



HOLD Release Signal and Oscillation Stable Time

Figure 4 Oscillation Stabilization Times



Note:
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information.

Figure 5 Reset Circuit

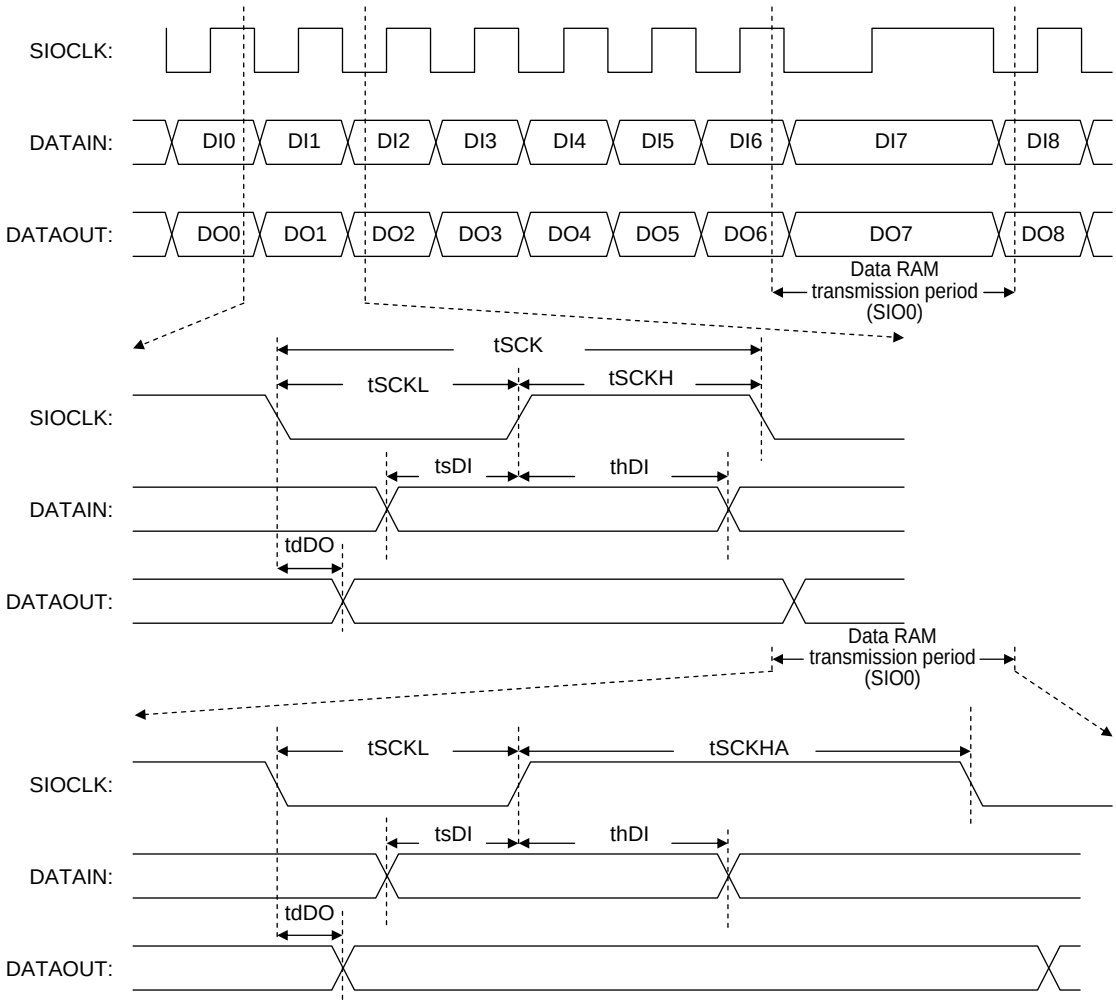


Figure 6 Serial I/O Output Waveforms

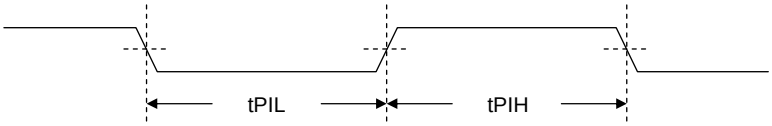


Figure 7 Pulse Input Timing Signal Waveform

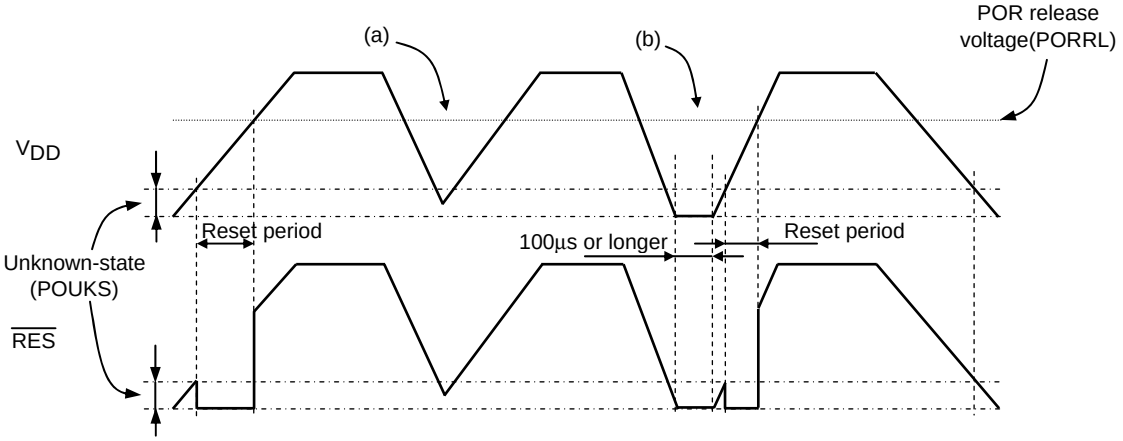


Figure 8 Waveform observed when only POR is used (LVD not used)
(RESET pin: Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

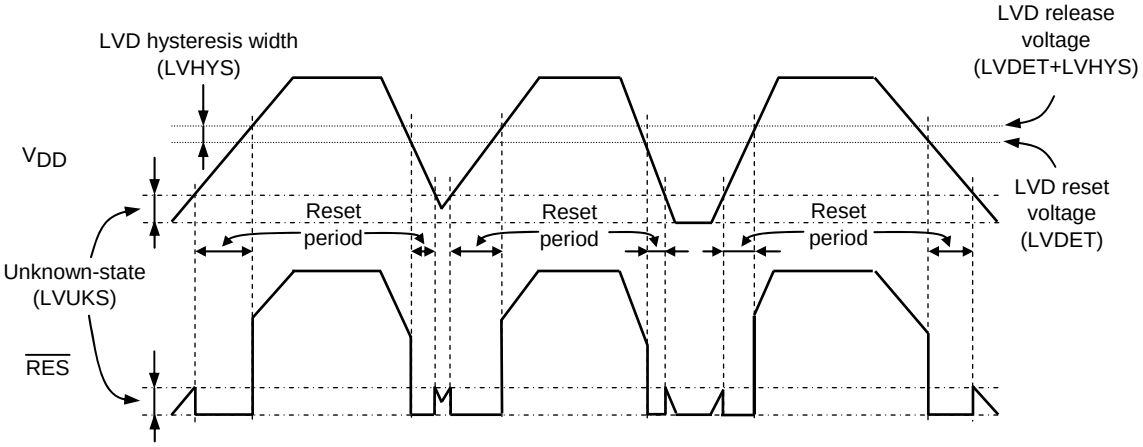


Figure 9 Waveform observed when both POR and LVD functions are used
(RESET pin: Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

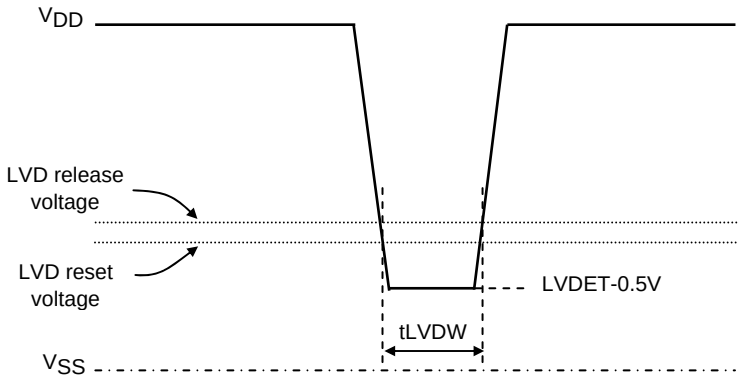


Figure 10 Low voltage detection minimum width
(Example of momentary power loss/Voltage variation waveform)