# AK4121A

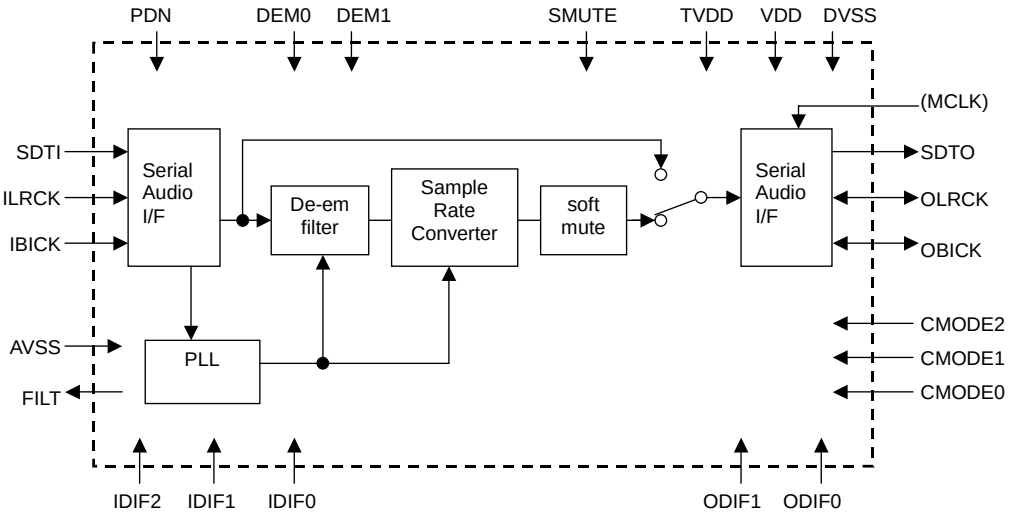
## Asynchronous Sample Rate Converter

## GENERAL DESCRIPTION

The AK4121A is a stereo asynchronous sample rate converter. The input sample rate ranges from 8kHz to 96kHz. The output sample rate is 32kHz, 44.1kHz, 48kHz or 96kHz. Since the internal PLL eliminates the need for a master clock in slave mode, the AK4121 simplifies the system design. Therefore, the AK4121A is suitable for applications requiring multiple sample rates, such as Car Audio, DVD recorders, and digital audio recording.

## FEATURES

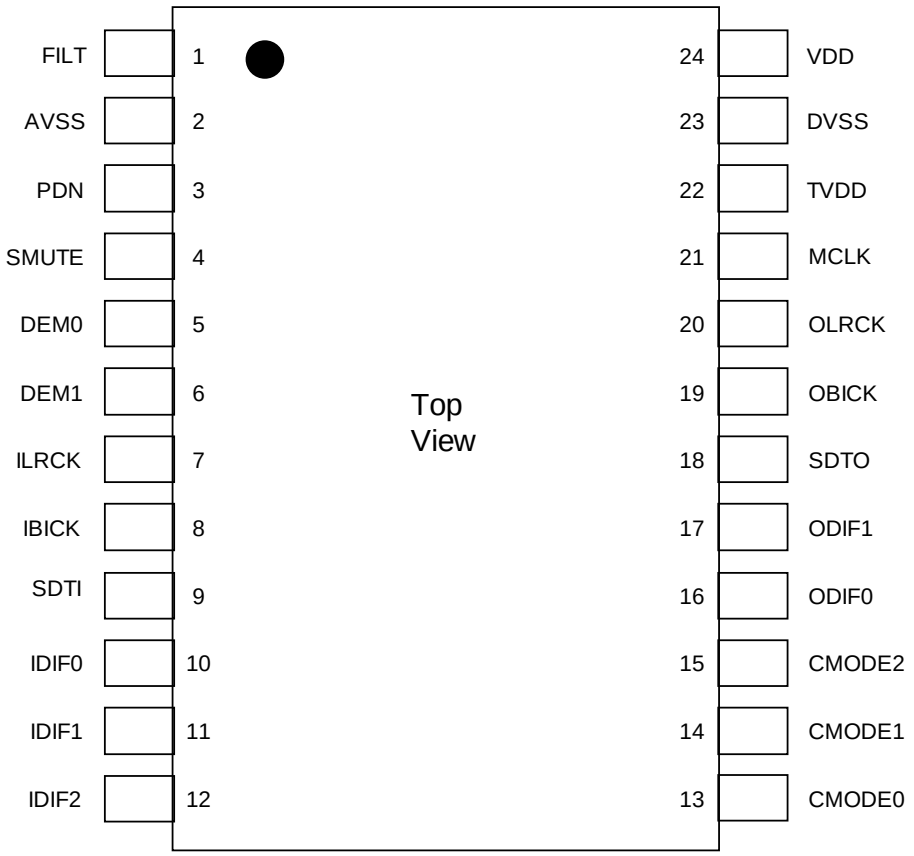
- **Stereo asynchronous sample rate converter**
- **Input sample rate range (FSI): 8kHz to 96kHz**
- **Output sample rate (FSO): 32kHz/44.1kHz/48kHz/96kHz**
- **Input to output Sample rate ratio: FSO/FSI = 0.33 to 6**
- **THD+N: –113dB**
- **I/F format: MSB justified, LSB justified (24/20/16bit) and $I^2S$**
- **Clock for Master mode: 256/384/512/768fso**
- **De-emphasis filter: 32kHz/44.1kHz/48kHz**
- **SRC Bypass mode**
- **Soft Mute function**
- **Power Supply: VDD: 3.0 to 3.6V, TVDD: 3.0 to 5.5V (for input tolerant)**
- **Ta: –40 to +85°C**



## ■ Ordering Guide

| | | |
|---|---|---|
| AK4121AVF | –40 ~ +85°C | 24pin VSOP (0.65mm pitch) |
| AKD4121A | Evaluation Board for AK4121A | |

## ■ Pin Layout




## ■ Difference between AK4121 and AK4121A

The AK4121A has a better performance than the AK4121 regarding of the tracking capability to the change of the input sampling frequency (FSI) which normally takes long settling time. Refer to "Tracking to the Input Sampling Frequency".

## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | FILT | O | Loop-Filter Pin for PLL |
| 2 | AVSS | I | Analog Ground Pin |
| 3 | PDN | I | Power-Down pin<br>When "L", the AK4121A is powered-down and reset. |
| 4 | SMUTE | I | Soft Mute Pin |
| 5 | DEM0 | I | De-emphasis Filter Control Pin #0 |
| 6 | DEM1 | I | De-emphasis Filter Control Pin #1 |
| 7 | ILRCK | I | L/R Clock Pin for Input |
| 8 | IBICK | I | Audio Serial Data Clock Pin for Input |
| 9 | SDTI | I | Audio Serial Data Input Pin |
| 10 | IDIF0 | I | Input Data Format pin #0 |
| 11 | IDIF1 | I | Input Data Format pin #1 |
| 12 | IDIF2 | I | Input Data Format pin #2 |
| 13 | CMODE0 | I | Clock Mode Select Pin #0 |
| 14 | CMODE1 | I | Clock Mode Select Pin #1 |
| 15 | CMODE2 | I | Clock Mode Select Pin #2 |
| 16 | ODIF0 | I | Output Data Format pin #0 |
| 17 | ODIF1 | I | Output Data Format pin #1 |
| 18 | SDTO | O | Audio Serial Data Output Pin |
| 19 | OBICK | I/O | Audio Serial Data Clock Pin for Output |
| 20 | OLRCK | I/O | L/R Clock Pin for Output |
| 21 | MCLK | I | Master Clock Pin for Output |
| 22 | TVDD | I | Input Buffer Power Supply Pin, 3.3V or 5V |
| 23 | DVSS | I | Digital Ground Pin |
| 24 | VDD | I | Power Supply Pin, 3.3V |

## ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS=0V; Note 1)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies: | Core | VDD | –0.3 | 4.6 | V |
| | Input Buffer | TVDD | –0.3 | 6.0 | V |
| | \|AVSS-DVSS\| (Note 1) | Δ GND | | 0.3 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Input Voltage | | VIN | –0.3 | TVDD+0.3 | V |
| Ambient Temperature (Power applied) | | Ta | –40 | 85 | °C |
| Storage Temperature | | Tstg | –65 | 150 | °C |

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS=0V; Note 2)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Power Supplies: Core | VDD | 3.0 | 3.3 | 3.6 | V |
| Input Buffer | TVDD | VDD | 5 | 5.5 | V |

Note 2. All voltages with respect to ground.

## SRC PERFORMANCE

(Ta=–40~85°C; VDD=3.0~3.6V; TVDD=3.0~5.5V; data=20bit; measurement bandwidth=20Hz~FSO/2; unless otherwise specified.)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Resolution | | | | 20 | Bits |
| Input Sample Rate | FSI | 8 | | 96 | kHz |
| Output Sample Rate | FSO | 32 | | 96 | kHz |
| Dynamic Range (Input= 1kHz, –60dBFS, Note 3) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | - | 114 | - | dB |
| FSO/FSI=48kHz/44.1kHz | | - | 114 | - | dB |
| FSO/FSI=32kHz/48kHz | | - | 114 | - | dB |
| FSO/FSI=96kHz/32kHz | | - | 115 | - | dB |
| Worst Case (FSO/FSI=48kHz/96kHz) | | 112 | - | - | dB |
| Dynamic Range (Input= 1kHz, –60dBFS, A-weighted, Note 3) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | - | 117 | - | dB |
| THD+N (Input= 1kHz, 0dBFS, Note 3) | | | | | |
| FSO/FSI=44.1kHz/48kHz | | - | –113 | - | dB |
| FSO/FSI=48kHz/44.1kHz | | - | –112 | - | dB |
| FSO/FSI=32kHz/48kHz | | - | –113 | - | dB |
| FSO/FSI=96kHz/32kHz | | - | –111 | - | dB |
| Worst Case (FSO/FSI=48kHz/8kHz) | | - | - | –103 | dB |
| Ratio between Input and Output Sample Rate (FSO/FSI, Note 4, Note 5) | FSO/FSI | 0.33 | | 6 | - |

Note 3. Measured by Rohde & Schwarz UPD04, Rejection Filter= wide, 8192point FFT.
Note 4. The “0.33” is the ratio of FSO/FSI when FSI is 96kHz and FSO is 32kHz
Note 5. The “6” is the ratio when FSI is 8kHz and FSO is 48kHz.

## DIGITAL FILTER

(Ta=–40~85°C; VDD=3.0~3.6V; TVDD=3.0~5.5V)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Passband –0.001dB | 0.985 ≤ FSO/FSI ≤ 6.000 | PB | 0 | | 0.4583FSI | kHz |
| | 0.905 ≤ FSO/FSI < 0.985 | PB | 0 | | 0.4167FSI | kHz |
| | 0.714 ≤ FSO/FSI < 0.905 | PB | 0 | | 0.3195FSI | kHz |
| | 0.656 ≤ FSO/FSI < 0.714 | PB | 0 | | 0.2852FSI | kHz |
| | 0.536 ≤ FSO/FSI < 0.656 | PB | 0 | | 0.2245FSI | kHz |
| | 0.492 ≤ FSO/FSI < 0.536 | PB | 0 | | 0.2003FSI | kHz |
| | 0.452 ≤ FSO/FSI < 0.492 | PB | 0 | | 0.1781FSI | kHz |
| | 0.333 ≤ FSO/FSI < 0.452 | PB | 0 | | 0.1092FSI | kHz |
| Stopband | 0.985 ≤ FSO/FSI ≤ 6.000 | SB | 0.5417FSI | | | kHz |
| | 0.905 ≤ FSO/FSI < 0.985 | SB | 0.5021FSI | | | kHz |
| | 0.714 ≤ FSO/FSI < 0.905 | SB | 0.3965FSI | | | kHz |
| | 0.656 ≤ FSO/FSI < 0.714 | SB | 0.3643FSI | | | kHz |
| | 0.536 ≤ FSO/FSI < 0.656 | SB | 0.2974FSI | | | kHz |
| | 0.492 ≤ FSO/FSI < 0.536 | SB | 0.2732FSI | | | kHz |
| | 0.452 ≤ FSO/FSI < 0.492 | SB | 0.2510FSI | | | kHz |
| | 0.333 ≤ FSO/FSI < 0.452 | SB | 0.1822FSI | | | kHz |
| Passband Ripple | | PR | | | ±0.01 | dB |
| Stopband Attenuation | | SA | 96 | | | dB |
| Group Delay | (Note 6) | GD | - | 57.5 | - | 1/fs |

Note 6. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.(at 20bit MSB justified, 16bit and 20bit LSB justified)

## DC CHARACTERISTICS

(Ta=–40~85°C; VDD=3.0~3.6V; TVDD=3.0~5.5V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Power Supply Current (VDD+TVDD) | | | | | |
| Normal operation: | | | | | |
| FSI=FSO=48kHz at Slave Mode: VDD=TVDD=3.3V | | | 10 | - | mA |
| FSI=FSO=96kHz at Master Mode: VDD=TVDD=3.3V | | | 20 | - | mA |
| : VDD=TVDD=3.6V | | | | 40 | mA |
| Power down: PDN = "L" (Note 7) | | | 10 | 100 | μA |
| High-Level Input Voltage | VIH | 0.7xVDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 0.3xVDD | V |
| High-Level Output Voltage (Iout=–400μA) | VOH | VDD-0.4 | - | - | V |
| Low-Level Output Voltage (Iout=400μA) | VOL | - | - | 0.4 | V |
| Input Leakage Current | Iin | - | - | ± 10 | μA |

Note 7. All digital inputs including clock pins are held DVSS.

## SWITCHING CHARACTERISTICS

(Ta=–40~85°C; VDD=3.0~3.6V; TVDD=3.0~5.5V; $C_L$=20pF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Master Clock Input (MCLK)** | | | | | | |
| Frequency | | fCLK | 8.192 | - | 36.864 | MHz |
| Duty Cycle | | dCLK | 40 | - | 60 | % |
| **L/R clock for Input data (ILRCK)** | | | | | | |
| Frequency | | fs | 8 | | 96 | kHz |
| Duty Cycle | | Duty | 48 | 50 | 52 | % |
| **L/R clock for Output data (OLRCK)** | | | | | | |
| Frequency | (Note 8) | fs | 32 | | 96 | kHz |
| Duty Cycle | Slave Mode | Duty | 48 | 50 | 52 | % |
| | Master Mode | Duty | | 50 | | % |
| **Audio Interface Timing** | | | | | | |
| **Input** | | | | | | |
| IBICK Period | | tBCK | 1/64fs | | | ns |
| IBICK Pulse Width Low | | tBCKL | 65 | | | ns |
| IBICK Pulse Width High | | tBCKH | 65 | | | ns |
| ILRCK Edge to IBICK "↑" | (Note 9) | | | | | |
| ILRCK Frequency = 8kHz ~ 32kHz | | tLRB | 1/256fs+45 | | 16/256fs | ns |
| ILRCK Frequency = 32kHz ~ 48kHz | | tLRB | 1/256fs+25 | | 16/256fs | ns |
| ILRCK Frequency = 48kHz ~ 96kHz | | tLRB | 1/256fs+15 | | 16/256fs | ns |
| BICK "↑" to ILRCK Edge | (Note 9) | tBLR | 30 | | | ns |
| SDTI Hold Time from IBICK "↑" | | tSDH | 30 | | | ns |
| SDTI Setup Time to IBICK "↑" | | tSDS | 30 | | | ns |
| **Output (Slave Mode)** | | | | | | |
| OBICK Period | | tBCK | 1/64fs | | | ns |
| OBICK Pulse Width Low | | tBCKL | 65 | | | ns |
| OBICK Pulse Width High | | tBCKH | 65 | | | ns |
| OLRCK Edge to OBICK "↑" | (Note 9) | tLRB | 30 | | | ns |
| OBICK "↑" to OLRCK Edge | (Note 9) | tBLR | 30 | | | ns |
| OLRCK to SDTO (MSB) | | tLRS | | | 30 | ns |
| OBICK "↓" to SDTO | | tBSD | | | 30 | ns |
| **Output (Master Mode)** | | | | | | |
| BICK Frequency | | fBCK | | 64fs | | Hz |
| BICK Duty | | dBCK | | 50 | | % |
| BICK "↓" to LRCK | | tMBLR | –20 | | 20 | ns |
| BICK "↓" to SDTO | | tBSD | –20 | | 30 | ns |
| **Power-down & Reset Timing** | | | | | | |
| PDN Pulse Width | (Note 10) | tPD | 150 | | | ns |

Note 8. Min is 8kHz when BYPASS="H".

Note 9. BICK rising edge must not occur at the same time as LRCK edge.

Note 10. The AK4121A must be reset by bringing PDN pin "H" to "L" upon power-up.

## ■ Timing Diagram

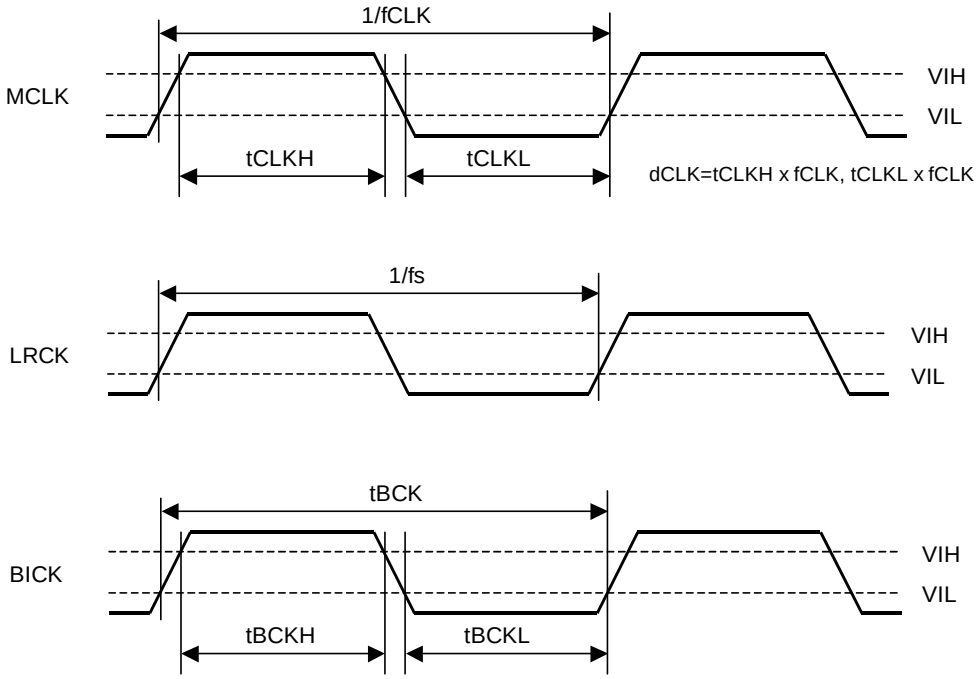



Figure 1. Clock Timing

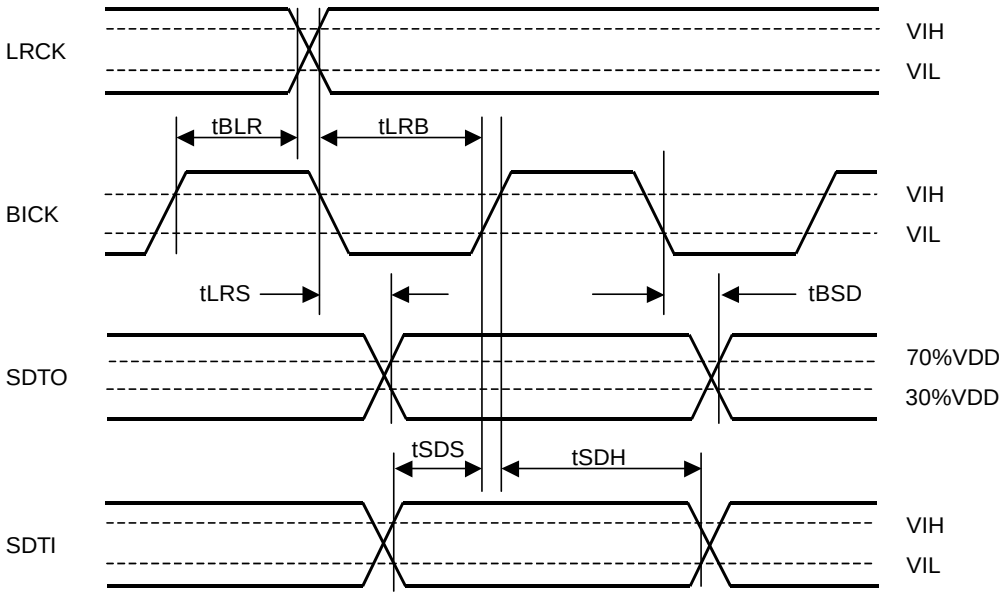



Figure 2. Audio Interface Timing at Slave Mode

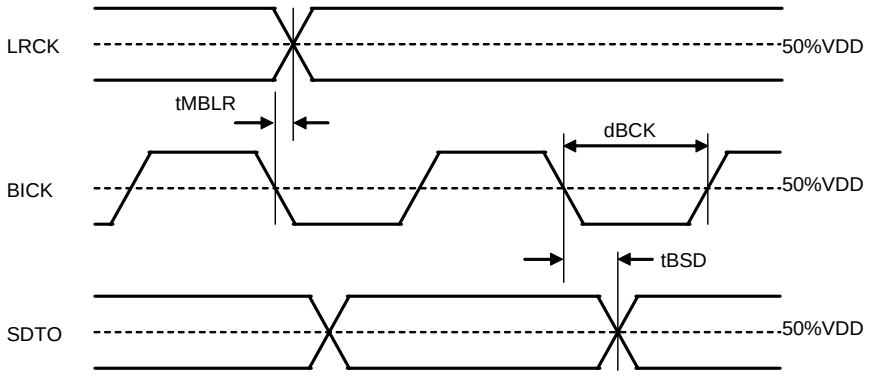



Figure 3. Audio Interface Timing at Master Mode

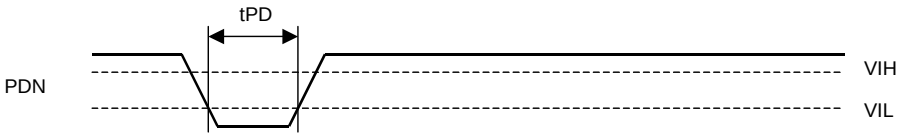



Figure 4. Power-down & Reset Timing

Note 11. BICK means IBICK and OBICK.
Note 12. LRCK means ILRCK and OLRCK.

# OPERATION OVERVIEW

## ■ System Clock

The input port works in slave mode only. The output port works in slave and master mode. An internal system clock is created by the internal PLL using ILRCK. The MCLK is not needed when the output port is in slave mode, and the MCLK pin should be connected to DVSS. The CMODE2-0 pins must be controlled when PDN pin ="L".

| Mode | CMODE2 | CMODE1 | CMODE0 | MCLK | Master/Slave (Output Port) |
|---|---|---|---|---|---|
| 0 | L | L | L | 256fso (fso~96kHz) | Master |
| 1 | L | L | H | 384fso (fso~96kHz) | Master |
| 2 | L | H | L | 512fso (fso~48kHz) | Master |
| 3 | L | H | H | 768fso (fso~48kHz) | Master |
| 4 | H | L | L | Not used. Set to DVSS | Slave |
| 5 | H | L | H | - | (Reserved) |
| 6 | H | H | L | - | (Reserved) |
| 7 | H | H | H | Not used. Set to DVSS | Master (BYPASS mode) |

Table 1. Master/Slave control

## ■ Audio Interface Format

The IDIF2-0 pins select the data mode for the input port. The ODIF1-0 pins select the data mode for the output port. In all modes the audio data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of OBICK. Select these modes when PDN pin="L". In BYPASS mode, both IBICK and OBICK are fixed to 64fs.

| Mode | IDIF2 | IDIF1 | IDIF0 | SDTI Format | IBICK (Slave) |
|---|---|---|---|---|---|
| 0 | L | L | L | 16bit LSB Justified | ≥32fs |
| 1 | L | L | H | 20bit LSB Justified | ≥40fs |
| 2 | L | H | L | 20bit MSB Justified | ≥40fs |
| 3 | L | H | H | 20/16bit $I^2S$ Compatible | ≥40fs or 32fs |
| 4 | H | L | L | 24bit LSB Justified | ≥48fs |

Table 2. Input Audio Data Formats

| Mode | ODIF1 | ODIF0 | SDTO Format | OBICK (Slave) | OBICK (Master) |
|---|---|---|---|---|---|
| 0 | L | L | 16bit LSB Justified | 64fs | 64fs |
| 1 | L | H | 20bit LSB Justified | 64fs | 64fs |
| 2 | H | L | 20/16bit MSB Justified (Note 13) | ≥40fs or 32fs | 64fs |
| 3 | H | H | 20/16bit $I^2S$ Compatible (Note 13) | ≥40fs or 32fs | 64fs |

Note 13. The 16bit output is available only when the OBICK = 32fs.

Table 3. Output Audio Data Formats

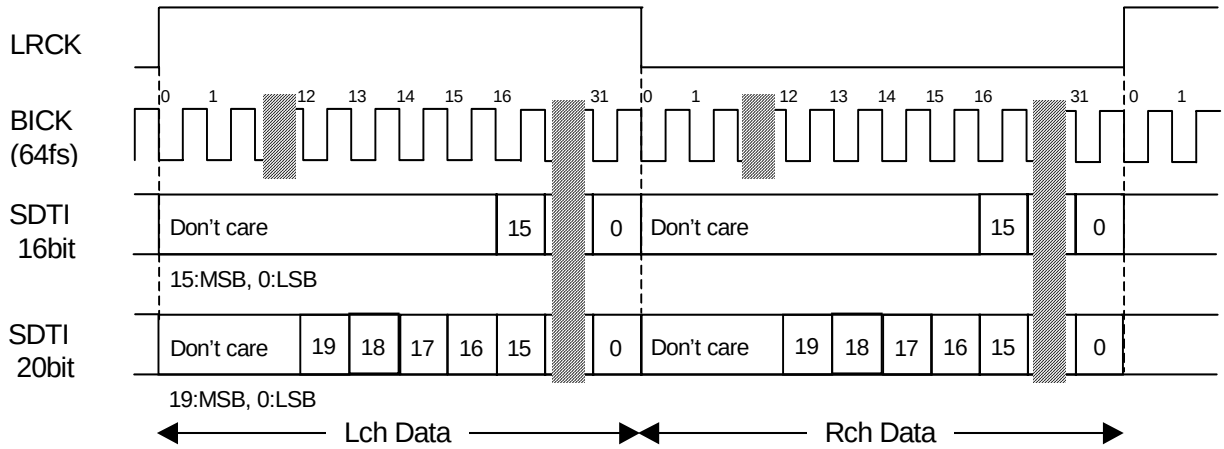



Figure 5. 16bit/20bit LSB justified Timing

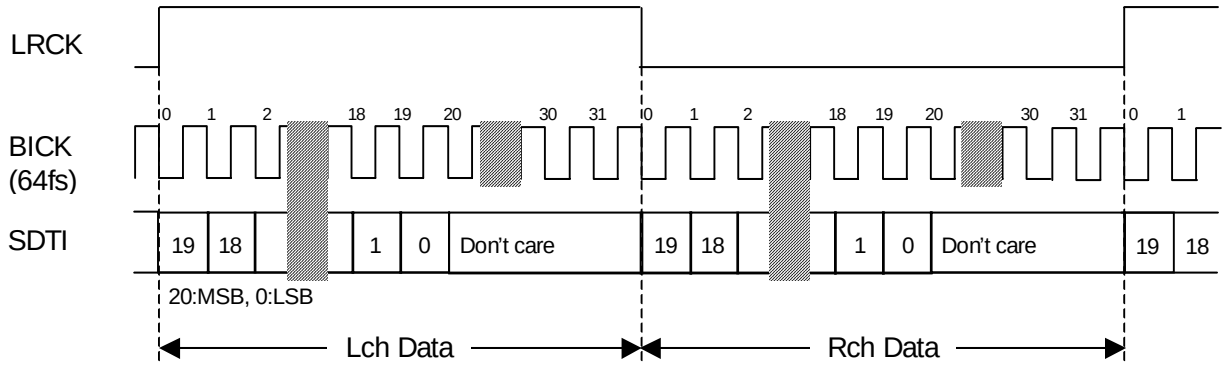



Figure 6. 20bit MSB justified Timing

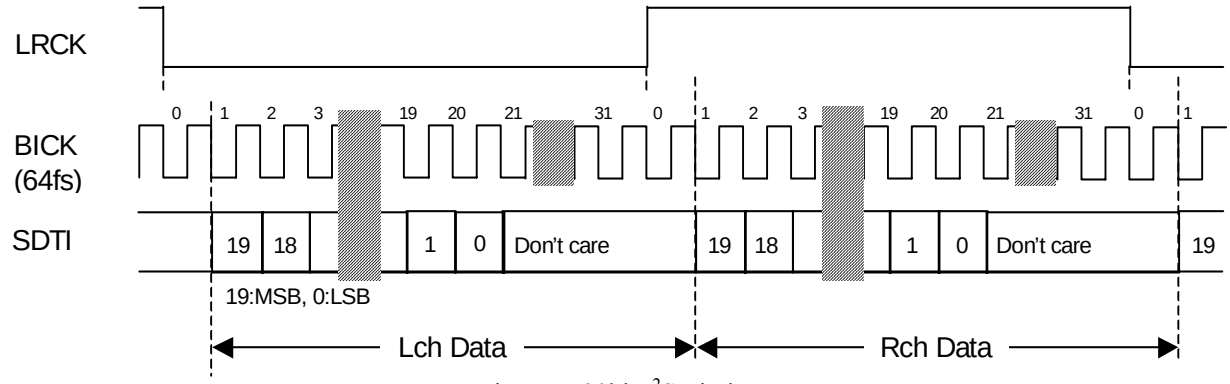
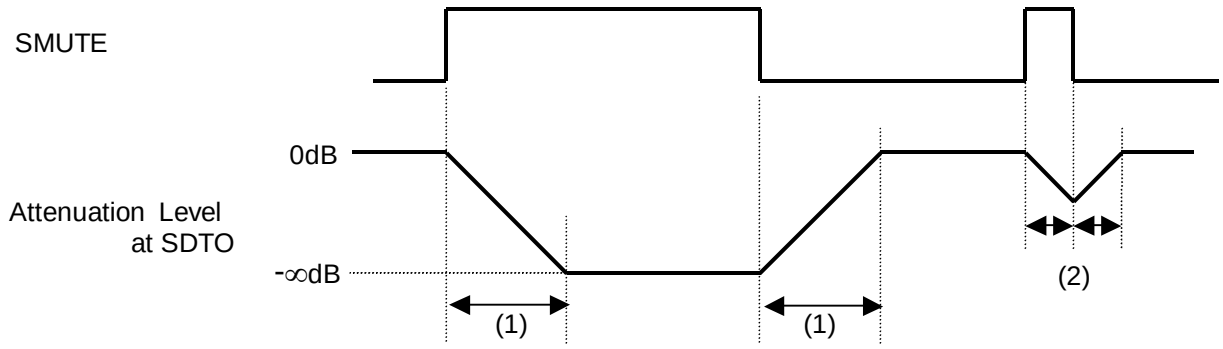



Figure 7. 20bit $I^2S$ Timing

## ■ Soft Mute Operation

When the SMUTE pin changes to "H", the output signal is attenuated from 0dB to −∞dB during 1024 OLRCK cycles. When the SMUTE pin returns to "L", the attenuation is cancelled and the output signal gradually changes to 0dB during 1024 OLRCK cycles. If the soft mute is cancelled before attenuating to −∞, the attenuation is discontinued and returns to 0dB by the same cycles. The soft mute is effective for changing the signal source.




Notes:

(1) Transition time. 1024 OLRCK cycles (1024/fso).

(2) If the soft mute is cancelled before attenuating to −∞ after starting the operation, the attenuation is discontinued and returned to 0dB by the same number of clock cycles.

Figure 8. Soft Mute

## ■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc=50/15μs) and is enabled or disabled with DEM0 and DEM1.

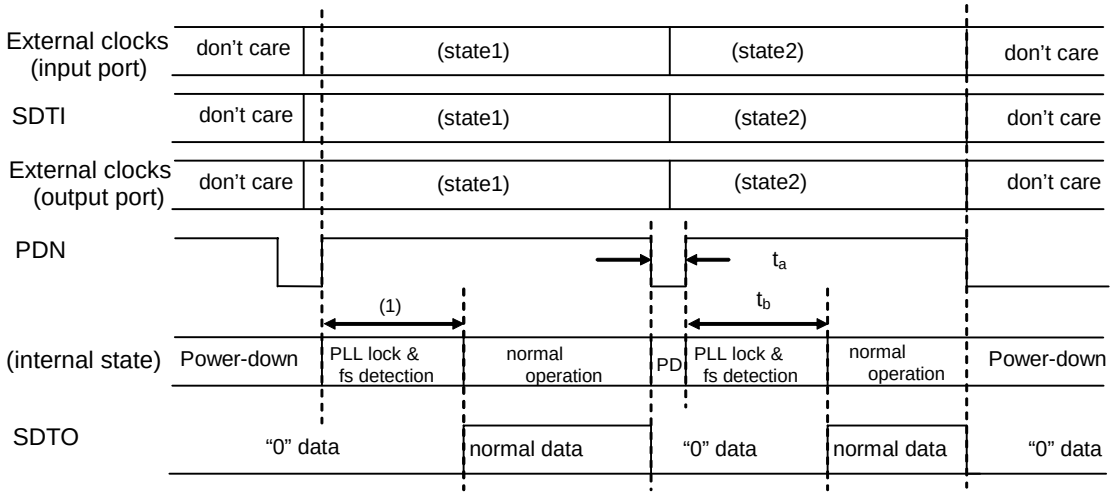
| Mode | DEM1 | DEM0 | De-emphasis filter |
|---|---|---|---|
| 0 | L | L | 44.1kHz |
| 1 | L | H | OFF |
| 2 | H | L | 48kHz |
| 3 | H | H | 32kHz |

Table 4. De-emphasis Filter Control

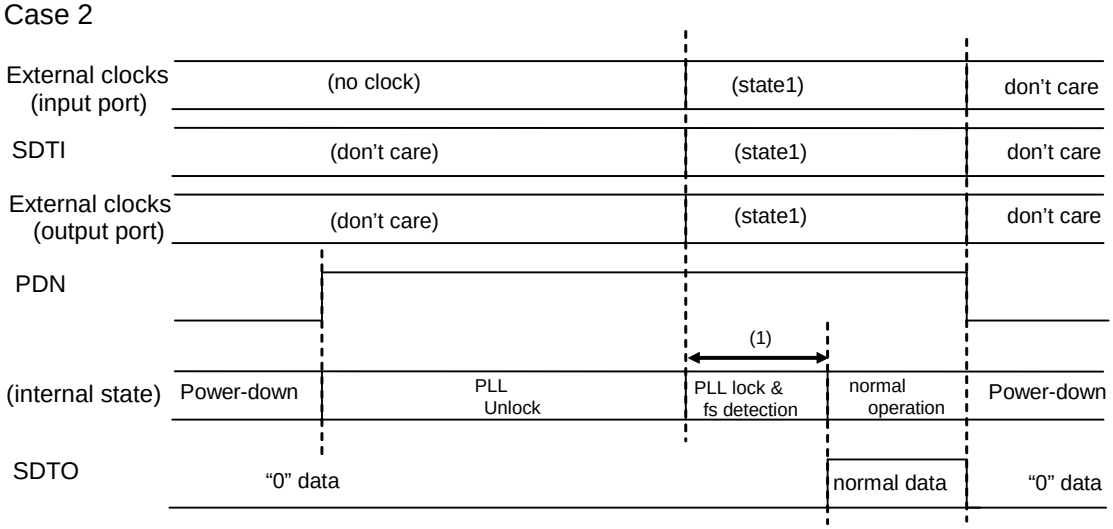
## ■ System Reset

Bringing the PDN pin="L" places the AK4121A in the power-down mode and initializes the digital filter. This reset should always be done after power-up. When the PDN pin = "L", the SDTO output is "L". Regarding the SDTO valid time, please refer to the Table 5. Until the output data becomes valid, the SDTO pin outputs "L".

Case 1




Case 2




Note:
(1) <100ms for recommended value 2, <200ms for recommended value 1. (Figure 11)

Figure 9. System Reset

| Reset time $t_a$ | Data valid time $t_b$ |
|---|---|
| ≤10ms | <100ms |
| 10ms< | <200ms |

Table 5. Reset time $t_a$ and Data valid time $t_b$.

## ■ Internal Reset Function for Clock Change

The AK4121A is reset automatically when the output clock is stopped. If the output clock is started again, normal data is output within 100ms.

## ■ Sequence of changing clocks

The recommended sequence for changing clocks is shown in Figure 10.

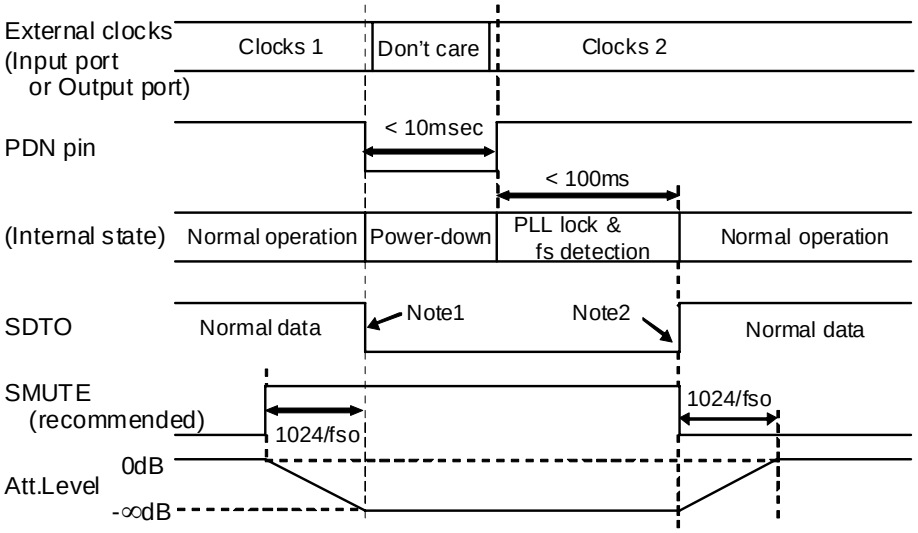



Figure 10. Sequence of changing clocks

Note 1. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to "0" from GD before the PDN pin changes to "L", which will cause the data on SDTO to remain "0".

Note 2. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to "0" for 1024/fso+100ms or more from the timing PDN pin changes to "H" while the SMUTE pin = "H".

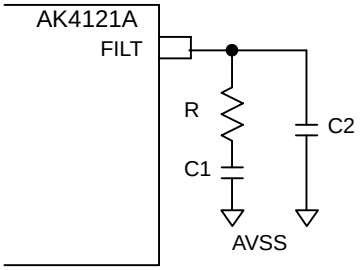
Note 3. When the PDN pin is not used for this clock change, a distorted signal may output for about 10ms ~ 100ms (typ) after changing clocks.

## ■ Grounding and Power Supply Decoupling

The AK4121A requires careful attention to power supply and grounding arrangements. VDD are usually supplied from the system's analog supply. **AVSS and DVSS of the AK4121A must be connected to the analog ground plane.** System analog ground and digital ground should be connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors especially a 0.1μF ceramic capacitor for high frequency noise should be placed as near to VDD as possible.

## ■ PLL Loop-Filter

The C1 (4.7μF) and R (560ohms) should be connected in series and attached between FILT pin and AVSS in parallel with C2 (1.0nF). A Care should be taken to ensure that noise on the FILT pin is minimized.



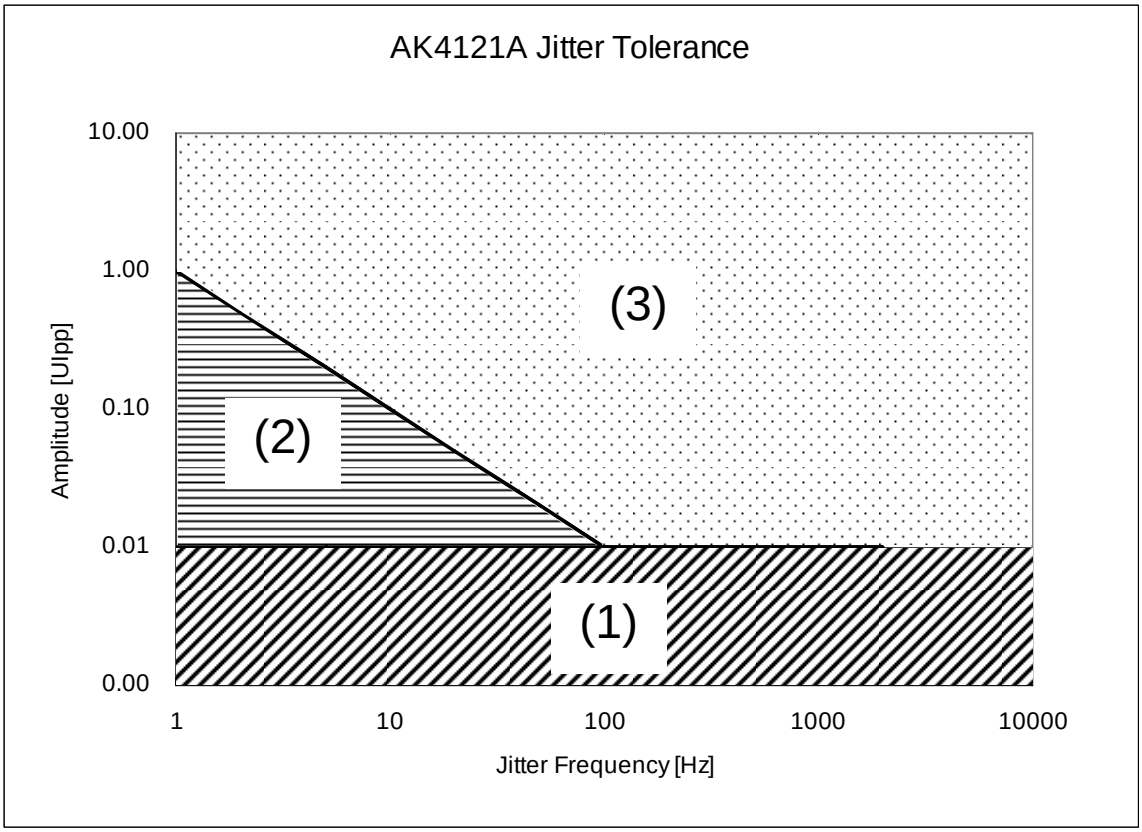

| Parameter | Recommended value 1 | Recommended value 2 |
|---|---|---|
| R | 560ohm +/–8% | 1.2kohm +/–8% |
| C1 | 4.7μF +/–40% | 2.2μF +/–40% |
| C2 | 1.0nF +/–40% | 2.2nF +/–40% |
| FSI range | 8k ~ 96kHz | 16k ~ 96kHz |

Note 14. Those recommended values include temperature dependence.

Figure 11. PLL Loop-Filter

## ■ Jitter Tolerance

Figure 12 shows the jitter tolerance to ILRCK. The jitter quantity is defined by the jitter frequency and the jitter amplitude shown in Figure 12. When the jitter amplitude is 0.01UIpp or less, the AK4121A operates normally regardless of the jitter frequency.




(1) Normal operation
(2) There is a possibility that the distortion degrades. (It may degrade up to about −50dB.)
(3) There is a possibility that the output data is lost.

Note 15. The jitter amplitude for 1UI (Unit Interval) is one cycle of ILRCK. When FSI = 48kHz, 1UI is 1/48kHz = 20.8μs.

Figure 12. Jitter Tolerance

## ■ Tracking to the Input Sampling Frequency

When the ILRCK is generated by an external PLL, it may take a time to settle after changing the input sampling frequency because the response of an external PLL to the frequency change is slow. In case of the AK4121, the output data becomes incorrect when the speed of the frequency change exceeds 0.14%/sec. The AK4121A operates normally up to 23%/sec speed and the output data becomes incorrect at the speed of the frequency change over 23%/sec.

## SYSTEM DESIGN

Figure 13 and Figure 14 illustrate typical system connection diagrams. The evaluation board [AKD4121A] demonstrates this application circuit, the optimum layout, and power supply arrangement and performance measurement results.

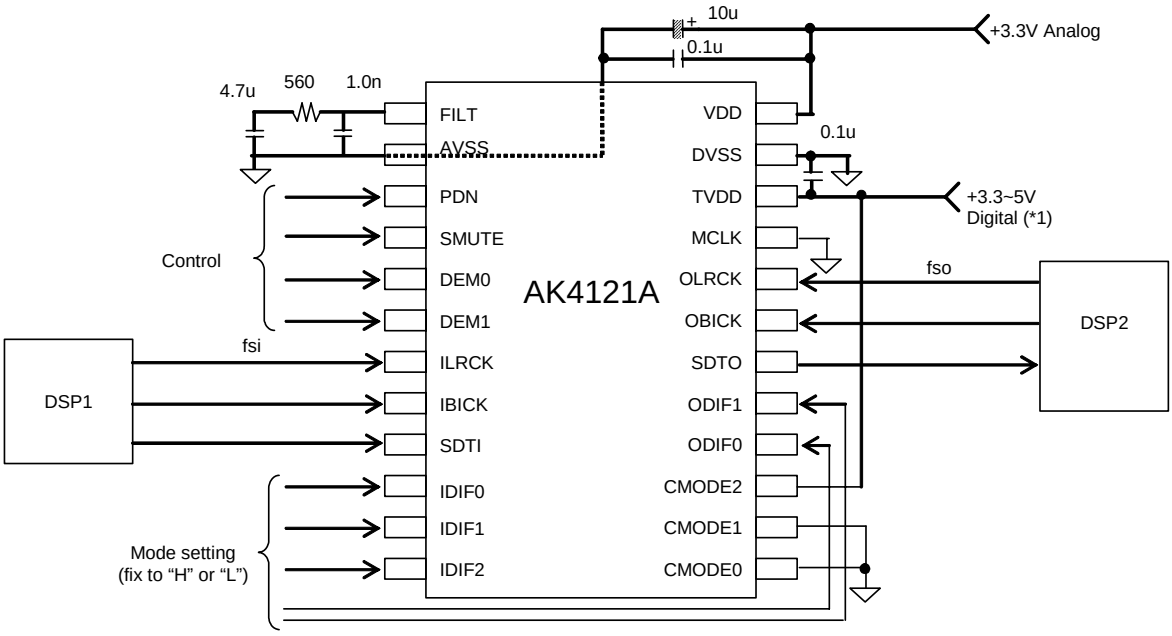



Figure 13. Example of a typical design (Slave Mode)

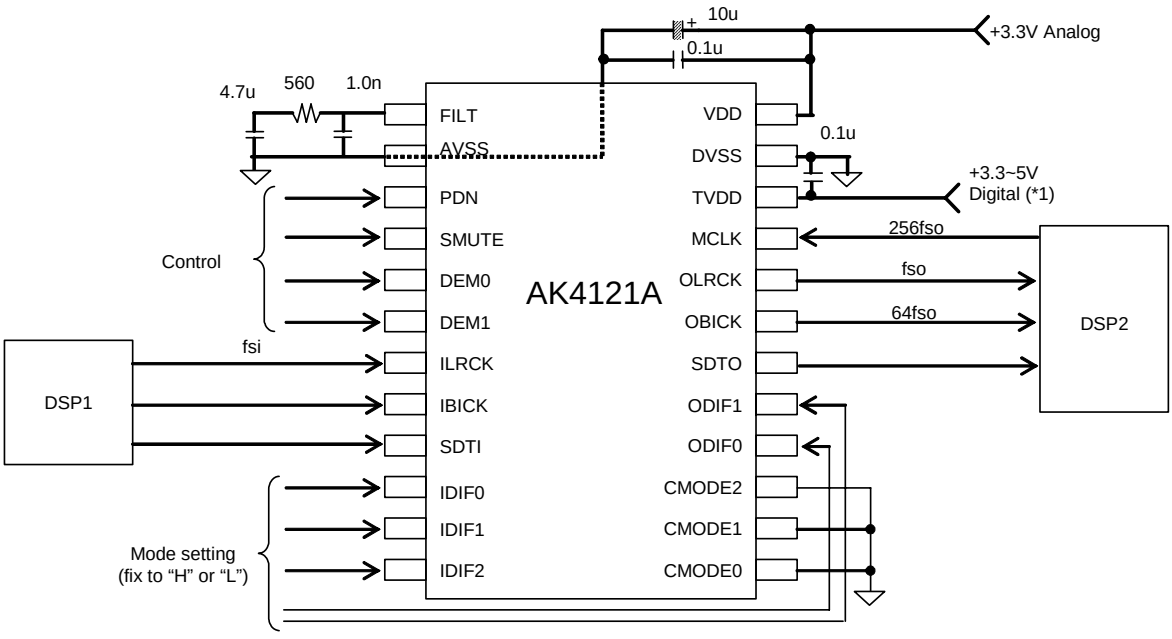
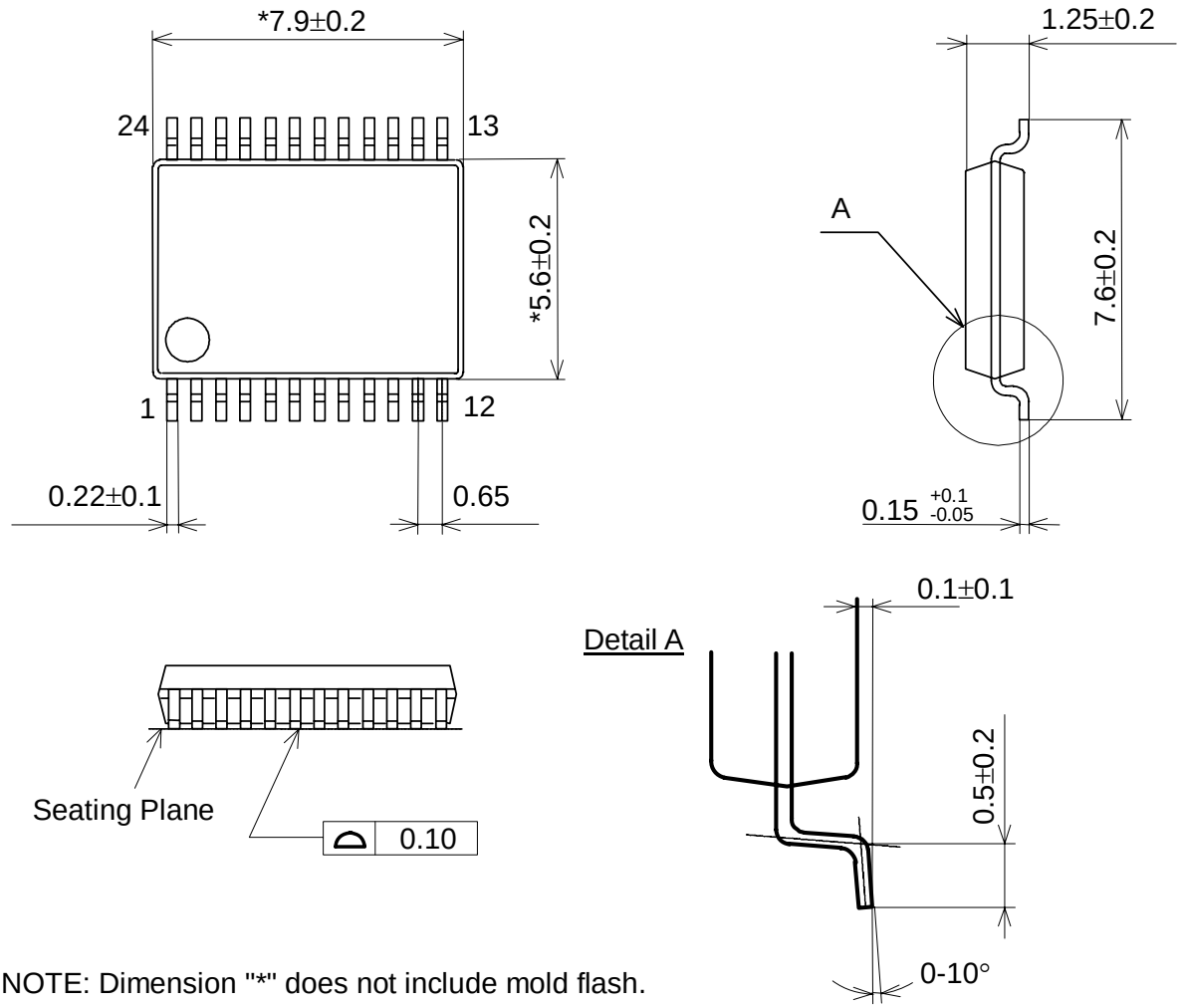



Figure 14. Example of a typical design (Master Mode; MCLK=256fso)

*1. TVDD should be the same as the maximum input voltage.

## PACKAGE

### 24pin VSOP (Unit: mm)

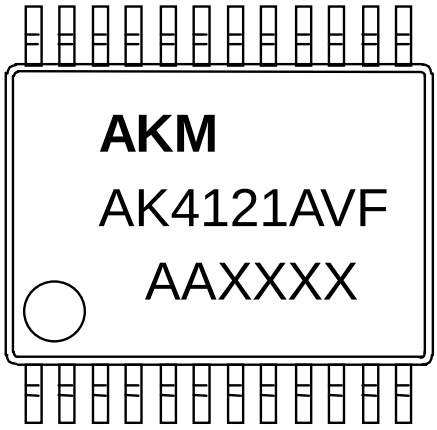



NOTE: Dimension "*" does not include mold flash.

**■ Package & Lead frame material**

| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder plate (Pb free) |

## MARKING




Contents of AAXXXX
AA: Lot#
XXXX: Date Code

## REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 04/09/01 | 00 | First Edition | | |
| 07/06/05 | 01 | Error Correct | 4 | SRC PERFORMANCE<br>Dynamic Range, Worst Case<br>FSO/FSI=32kHz/44.1kHz → 48kHz/96kHz |
| | | Description Change | 6 | SWITCHING CHARACTERISTICS<br>Audio Interface timing<br>ILRCK Edge to IBICK "↑" is changed to<br>ILRCK period (8kHz ~ 32kHz): 1/256fs+45<br>ILRCK period (32kHz ~ 48kHz): 1/256fs+25<br>ILRCK period (48kHz ~ 96kHz): 1/256fs+15 |
| 07/07/25 | 02 | Description Change | 13 | ■ Internal Reset Function for Clock Change<br>■ Sequence of Changing Clocks |
| 07/09/14 | 03 | Add Spec | 6 | Max values of ILRCK Edge to IBICK "↑" were added.<br>ILRCK Frequency =8kHz ~ 32kHz: 16/256fs<br>ILRCK Frequency =32kHz ~ 48kHz: 16/256fs<br>ILRCK Frequency =48kHz ~ 96kHz: 16/256fs |
| | | Error Correct | 6 | The Symbol of ILRCK Edge to IBICK "↑"<br>tBLR → tLRB<br>The Symbol of IBICK "↑" to ILRCK Edge<br>tLRB → tBLR |
| | | | | The Symbol of OLRCK Edge to OBICK "↑"<br>tBLR → tLRB<br>The Symbol of OBICK "↑" to OLRCK Edge<br>tLRB → tBLR |
| 08/03/05 | 04 | Description Addition | 9 | Note 13. was added. |
| 08/04/05 | 05 | Description Change | 5 | DC CHARACTERISTICS<br>Power Supply Current<br>(VDD+TVDD) description was added.<br>VDD =3.3V → VDD=TVDD=3.3V<br>VDD= 3.6V → VDD=TVDD=3.6V |
| 10/04/30 | 06 | Description Addition | 13 | ■ Sequence of changing clocks<br>Description is added in notes. |

**IMPORTANT NOTICE**

- These products and their specifications are subject to change without notice.
  When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei Microdevices Corporation (AKM) or authorized distributors as to current status of the products.
- Descriptions of external circuits, application circuits, software and other related information contained in this document are provided only to illustrate the operation and application examples of the semiconductor products. You are fully responsible for the incorporation of these external circuits, application circuits, software and other related information in the design of your equipments. AKM assumes no responsibility for any losses incurred by you or third parties arising from the use of these information herein. AKM assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of such information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components$_{Note1)}$ in any safety, life support, or other hazard related device or system$_{Note2)}$, and AKM assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKM. As used here:
  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKM products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.