**Freescale Semiconductor**
Data Sheet: Technical Data

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MCF51QU128

# MCF51QU128

## Supports the MCF51QU128VLH, MCF51QU128VHS, MCF51QU64VLF, MCF51QU64VHS, MCF51QU32VHS, MCF51QU32VFM

### Features

- Operating characteristics
  - Voltage range: 1.71 V to 3.6 V
  - Flash write voltage range: 1.71 V to 3.6 V
  - Temperature range (ambient): -40°C to 105°C
- Core
  - Up to 50 MHz V1 ColdFire CPU
  - Dhrystone 2.1 performance: 1.10 DMIPS per MHz when executing from internal RAM, 0.99 DMIPS per MHz when executing from flash memory
- System
  - DMA controller with four programmable channels
  - Integrated ColdFire DEBUG_Rev_B+ interface with single-wire BDM connection
- Power management
  - 10 low power modes to provide power optimization based on application requirements
  - Low-leakage wakeup unit (LLWU)
  - Voltage regulator (VREG)
- Clocks
  - Crystal oscillators (two, each with range options): 1 kHz to 32 kHz (low), 1 MHz to 8 MHz (medium), 8 MHz to 32 MHz (high)
  - Multipurpose clock generator (MCG)
- Memories and memory interfaces
  - Flash memory, FlexNVM, FlexRAM, and RAM
  - Serial programming interface (EzPort)
  - Mini-FlexBus external bus interface
- Security and integrity
  - Hardware CRC module to support fast cyclic redundancy checks
  - 128-bit unique identification (ID) number per chip
- Analog
  - 12-bit SAR ADC
  - 12-bit DAC
  - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference (VREF)
- Timers
  - Programmable delay block (PDB)
  - Motor control/general purpose/PWM timers (FTM)
  - 16-bit low-power timers (LPTMRs)
  - 16-bit modulo timer (MTIM)
  - Carrier modulator transmitter (CMT)
- Communication interfaces
  - UARTs with Smart Card support and FIFO
  - SPI modules, one with FIFO
  - Inter-Integrated Circuit (I2C) modules
- Human-machine interface
  - Up to 48 EGPIO pins
  - Up to 16 rapid general purpose I/O (RGPIO) pins
  - Low-power hardware touch sensor interface (TSI)
  - Interrupt request pin (IRQ)

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device:

1. Go to http://www.freescale.com.
2. Perform a part number search for the following partial device numbers: PCF51QU and MCF51QU.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q CCCC DD MMM T PP

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| CCCC | Core code | CF51 = ColdFire V1 |
| DD | Device number | JF, JU, QF, QH, QM, QU |

*Table continues on the next page...*

| Field | Description | Values |
|---|---|---|
| MMM | Memory size (program flash memory)[1] | • 32 = 32 KB<br>• 64 = 64 KB<br>• 128 = 128 KB |
| T | Temperature range, ambient (°C) | V = –40 to 105 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• HS = 44 Laminate QFN (5 mm x 5 mm)<br>• LF = 48 LQFP (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm) |

1. All parts also have FlexNVM, FlexRAM, and RAM.

## 2.4 Example

This is an example part number:

MCF51QU128VLH

# 3 Terminology and guidelines

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/ pulldown current | 10 | 130 | µA |

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

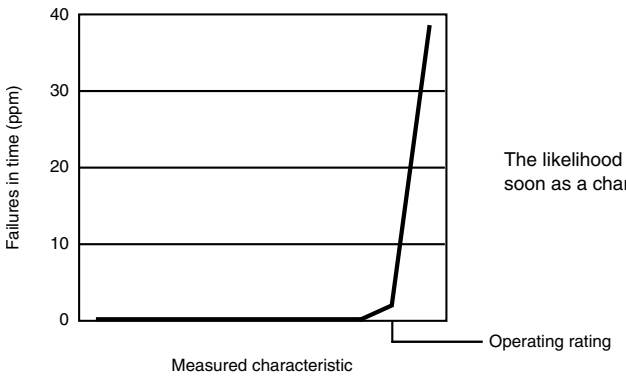
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

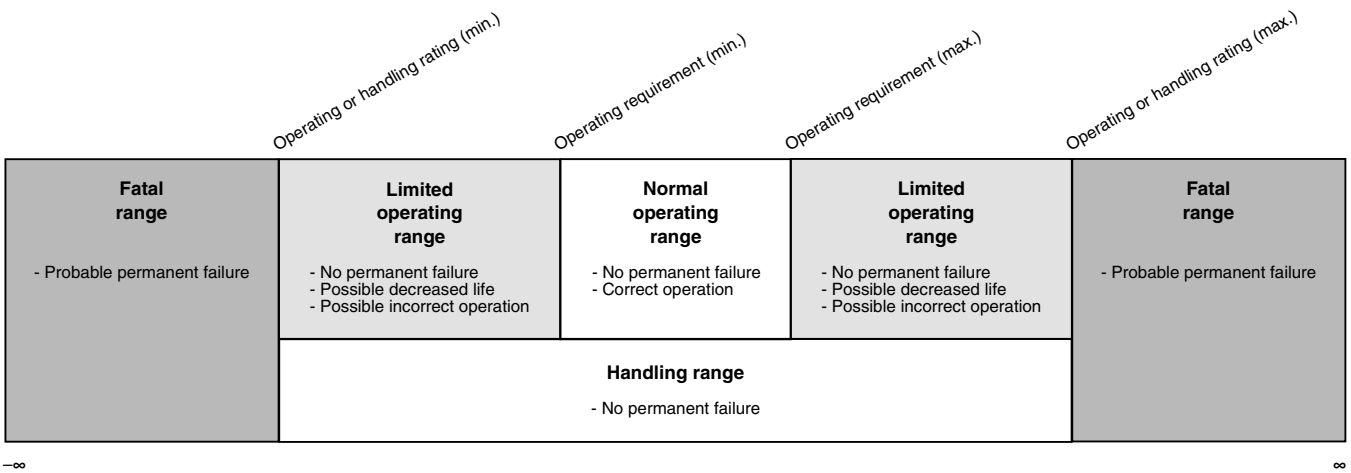
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 3.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 3.6 Relationship between ratings and operating requirements




## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

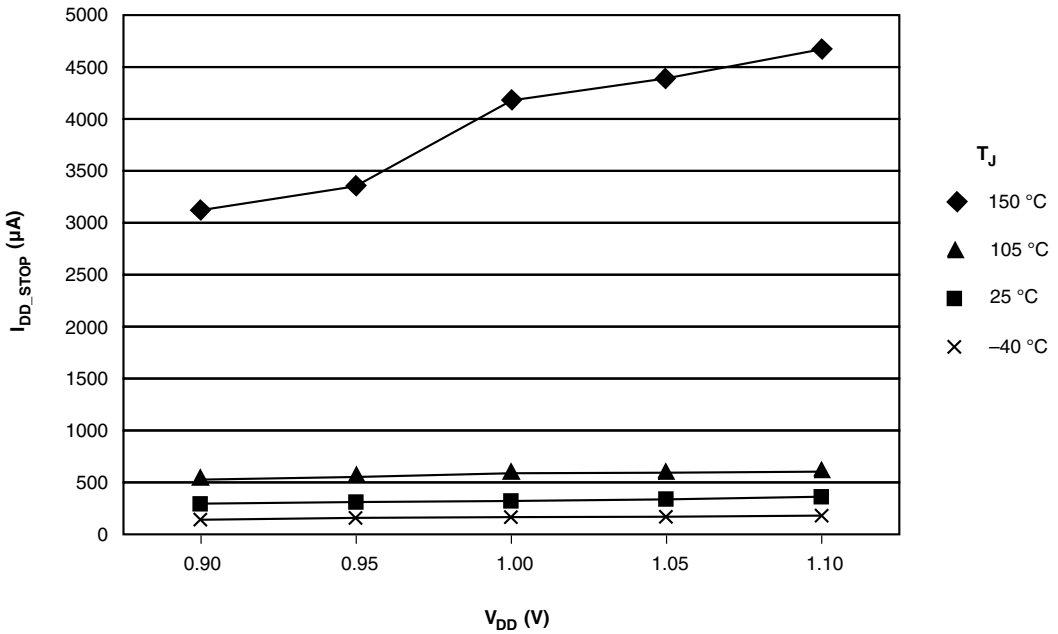
### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




# 4 Ratings

## 4.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |
| | Solder temperature, leaded | — | 245 | | |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 120 | mA |
| $V_{DIO}$ | Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL) | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{AIO}$ | Analog, $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| VREGIN | Regulator input | –0.3 | 6.0 | V |

# 5 General

## 5.1 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

# 5.2 Nonswitching electrical specifications

## 5.2.1 Voltage and Current Operating Requirements

**Table 1. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} – V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{SS} – V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{IH}$ | Input high voltage | | | | 1 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0.7 × $V_{DD}$ | — | V | |
| | • 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | 0.75 × $V_{DD}$ | — | V | |
| $V_{IL}$ | Input low voltage | | | | 2 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | — | 0.35 × $V_{DD}$ | V | |
| | • 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | — | 0.3 × $V_{DD}$ | V | |
| $I_{IC}$ | DC injection current — single pin | | | | 3 |
| | • $V_{IN}$ > $V_{DD}$ | 0 | 2 | mA | |
| | • $V_{IN}$ < $V_{SS}$ | 0 | –0.2 | mA | |
| | DC injection current — total MCU limit, includes sum of all stressed pins | | | | 3 |
| | • $V_{IN}$ > $V_{DD}$ | 0 | 25 | mA | |
| | • $V_{IN}$ < $V_{SS}$ | 0 | –5 | mA | |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | |

1. The device always interprets an input as a 1 when the input is greater than or equal to $V_{IH}$ (min.) and less than or equal to $V_{IH}$ (max.), regardless of whether input hysteresis is turned on.
2. The device always interprets an input as a 0 when the input is less than or equal to $V_{IL}$ (max.) and greater than or equal to $V_{IL}$ (min.), regardless of whether input hysteresis is turned on.
3. All functional non-supply pins are internally clamped to VSS and VDD. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values. Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current (VIn > VDD) is greater than IDD, the injection current may flow out of VDD and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

## 5.2.2 LVD and POR operating requirements

**Table 2. LVD and POR operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±80 | — | mV | |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±60 | — | mV | |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| $t_{LPO}$ | Internal low power oscillator period<br>factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising thresholds are falling threshold + hysteresis voltage

## 5.2.3 Voltage and current operating behaviors

**Table 3. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = - 9 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -3 mA | $V_{DD}$ – 0.5 | — | V | |
| | Output high voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -2 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -0.6 mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 9 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 3 mA | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 2 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 0.6 mA | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) | | | | |
| | • @ full temperature range | — | 1.0 | µA | 1 |
| | • @ 25 °C | — | 0.1 | µA | |
| $I_{OZ}$ | Hi-Z (off-state) leakage current (per pin) | — | 1 | µA | |
| $I_{OZ}$ | Total Hi-Z (off-state) leakage current (all input pins) | — | 4 | µA | |
| $R_{PU}$ | Internal pullup resistors | 22 | 50 | kΩ | 2 |
| $R_{PD}$ | Internal pulldown resistors | 22 | 50 | kΩ | 3 |

1. Tested by ganged leakage method
2. Measured at Vinput = $V_{SS}$
3. Measured at Vinput = $V_{DD}$

## 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$ and VLLSx-RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock (and flash and Mini-FlexBus clocks) = 25 MHz

**Table 4. Power mode transition operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | — | 300 | µs | 1 |
| | • VLLS1 → RUN | — | 150 | µs | 1, 2 |
| | • VLLS2 → RUN | — | 75 | µs | 1, 2 |
| | • VLLS3 → RUN | — | 75 | µs | 1, 2 |
| | • LLS → RUN | — | 6.5 | µs | 2 |
| | • VLPS → RUN | — | 4.6 | µs | 2 |
| | • STOP → RUN | — | 4.6 | µs | 2 |

1. Normal boot (FTFL_FOPT[LPBOOT] is 1)
2. The wakeup time includes the execution time for a small amount of firmware used to produce a GPIO clear event. Wakeup time is measured from the falling edge of the external wakeup event to the falling edge of a GPIO clear performed by software.

## 5.2.5 Power consumption operating behaviors

**Table 5. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from RAM | | | | | 2 |
| | • @ 1.8 V | — | 13 | — | mA | |
| | • @ 3.0 V | — | 13 | 16 | mA | |
| $I_{DD_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from flash memory with page buffering disabled | | | | | 2 |
| | • @ 1.8 V | — | 14.3 | — | mA | |
| | • @ 3.0 V | — | 14.5 | 17.9 | mA | |

*Table continues on the next page...*

## Table 5. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD_RUN}$ | Run mode current — all peripheral clocks enabled, code executing from RAM, exercising flash memory<br>• @ 1.8 V<br>• @ 3.0 V | <br><br>—<br>— | <br><br>20<br>20 | <br><br>23.5<br>25 | <br><br>mA<br>mA | 3 |
| $I_{DD_WAIT}$ | Wait mode current at 3.0 V — all peripheral clocks disabled | — | 5.8 | 6.8 | mA | 4 |
| $I_{DD_STOP}$ | Stop mode current at 3.0 V<br>• @ –40 to 25 °C<br>• @ 105 °C | <br>—<br>— | <br>0.34<br>0.90 | <br>0.41<br>1.8 | <br>mA<br>mA | |
| $I_{DD_VLPR}$ | Very low-power run mode current at 3.0 V — all peripheral clocks disabled | — | 0.63 | 1.32 | mA | 5 |
| $I_{DD_VLPR}$ | Very low-power run mode current at 3.0 V — all peripheral clocks enabled | — | 0.78 | 1.46 | mA | 6 |
| $I_{DD_VLPW}$ | Very low-power wait mode current at 3.0 V | — | 0.15 | 0.62 | mA | 7 |
| $I_{DD_VLPS}$ | Very low-power stop mode current at 3.0 V<br>• @ –40 to 25 °C<br>• @ 105 °C | <br>—<br>— | <br>19<br>145 | <br>45<br>312 | µA | 8 |
| $I_{DD_LLS}$ | Low leakage stop mode current at 3.0 V<br>• @ –40 to 25 °C<br>• @ 105 °C | <br>—<br>— | <br>3.0<br>53.3 | <br>4.8<br>157 | <br>µA<br>µA | 8,9,10 |
| $I_{DD_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V<br>• @ –40 to 25 °C<br>• @ 105 °C | <br>—<br>— | <br>1.8<br>39.2 | <br>3.3<br>115 | <br>µA<br>µA | 8,9,10 |
| $I_{DD_VLLS2}$ | Very low-leakage stop mode 2 current at 3.0 V<br>• @ –40 to 25 °C<br>• @ 105 °C | <br>—<br>— | <br>1.6<br>22.2 | <br>2.8<br>65 | <br>µA<br>µA | 8,9 |
| $I_{DD_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V<br>• @ –40 to 25 °C<br>• @ 105 °C | <br>—<br>— | <br>1.4<br>17.6 | <br>2.6<br>50 | <br>µA<br>µA | 8,9 |
| $I_{DD_RTC}$ | Average current adder for real-time clock function<br>• @ –40 to 25 °C | <br>— | <br>0.7 | <br>— | <br>µA | 11 |

1. The analog supply current is the sum of the active current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode.

5. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash memory.
6. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash memory.
7. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled.
8. OSC clocks disabled.
9. All pads disabled.
10. Data reflects devices with 32 KB of RAM. For devices with 16 KB of RAM, power consumption is reduced by 500 nA. For devices with 8 KB of RAM, power consumption is reduced by 750 nA.
11. RTC function current includes LPTMR with OSC enabled with 32.768 kHz crystal at 3.0 V

#### 5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode, except for 50 MHz core (FEI mode)
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL
- For the ALLON curve, all peripheral clocks are enabled, but peripherals are not in active operation
- Voltage Regulator disabled
- No GPIOs toggled
- Code execution from flash memory with cache enabled

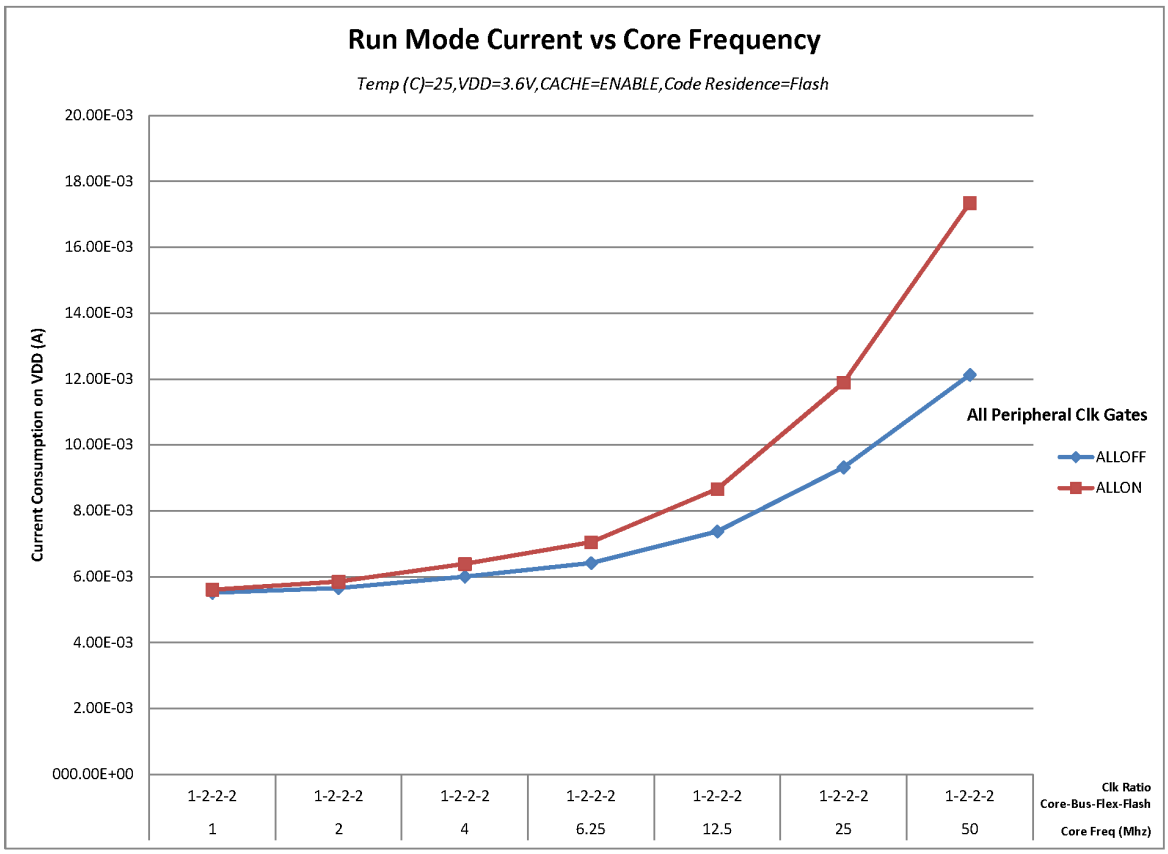



**Figure 1. Run mode supply current vs. core frequency**

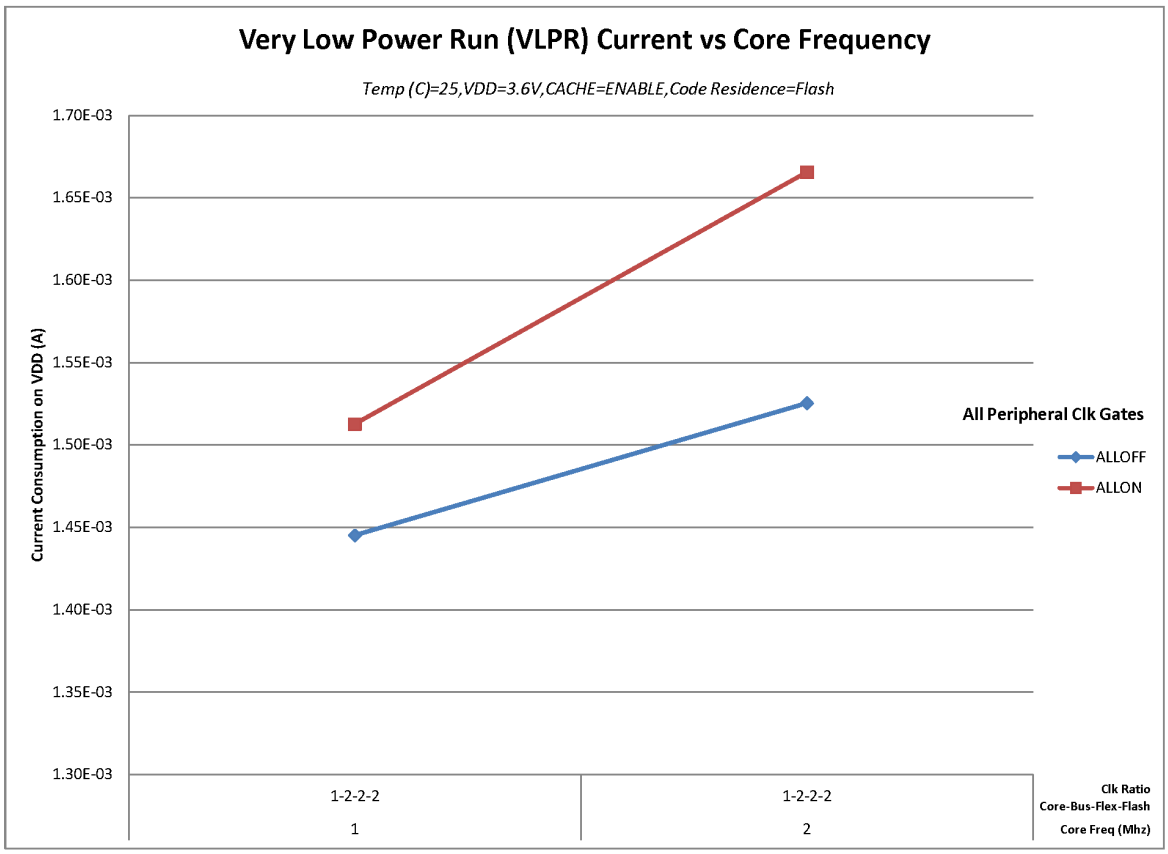



**Figure 2. VLPR mode supply current vs. core frequency**

## 5.2.6 EMC radiated emissions operating behaviors

**Table 6. EMC radiated emissions operating behaviors**

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{RE1}$ | Radiated emissions voltage, band 1 | 0.15–50 | 20 | dBµV | 1, 2 |
| $V_{RE2}$ | Radiated emissions voltage, band 2 | 50–150 | 19 | | |
| $V_{RE3}$ | Radiated emissions voltage, band 3 | 150–500 | 17 | | |
| $V_{RE4}$ | Radiated emissions voltage, band 4 | 500–1000 | 16 | | |
| $V_{RE_IEC}$ | IEC level | 0.15–1000 | L | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

2. $V_{DD}$ = 3 V, $T_A$ = 25 °C, $f_{OSC}$ = 32 kHz (crystal), $f_{BUS}$ = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

### 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to http://www.freescale.com.
2. Perform a keyword search for "EMC design."

### 5.2.8 Capacitance attributes

**Table 7. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN_D}$ | Input capacitance: digital pins | — | 7 | pF |

## 5.3 Switching electrical specifications

**Table 8. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Normal run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 50 | MHz | |
| $f_{BUS}$ | Bus clock | — | 25 | MHz | |
| FB_CLK | Mini-FlexBus clock | — | 25 | MHz | 1 |
| $f_{LPTMR}$ | LPTMR clock | — | 25 | MHz | |
| VLPR mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 2 | MHz | |
| $f_{BUS}$ | Bus clock | — | 1 | MHz | |
| FB_CLK | Mini-FlexBus clock | — | 1 | MHz | 1 |
| $f_{LPTMR}$ | LPTMR clock[2] | — | 25 | MHz | |

1. When the Mini-FlexBus is enabled, its clock frequency is always the same as the bus clock frequency.
2. A maximum frequency of 25 MHz for the LPTMR in VLPR mode is possible when the LPTMR is configured for pulse counting mode and is driven externally via the LPTMR_ALT1, LPTMR_ALT2, or LPTMR_ALT3 pin.

### 5.3.1 General Switching Specifications

These general purpose specifications apply to all signals configured for EGPIO, MTIM, CMT, PDB, IRQ, and $I^2C$ signals. The conditions are 50 pf load, $V_{DD}$ = 1.71 V to 3.6 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

**Table 9. EGPIO General Control Timing**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| G1 | Bus clock from CLK_OUT pin high to GPIO output valid | — | 32 | ns |
| G2 | Bus clock from CLK_OUT pin high to GPIO output invalid (output hold) | 1 | — | ns |
| G3 | GPIO input valid to bus clock high | 28 | — | ns |
| G4 | Bus clock from CLK_OUT pin high to GPIO input invalid | — | 4 | ns |
| | GPIO pin interrupt pulse width (digital glitch filter disabled)<br>Synchronous path[1] | 1.5 | — | Bus clock cycles |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled)<br>Asynchronous path[2] | 100 | — | ns |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled)<br>Asynchronous path[2] | 50 | — | ns |
| | External reset pulse width (digital glitch filter disabled) | 100 | — | ns |
| | Mode select (MS) hold time after reset deassertion | 2 | — | Bus clock cycles |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

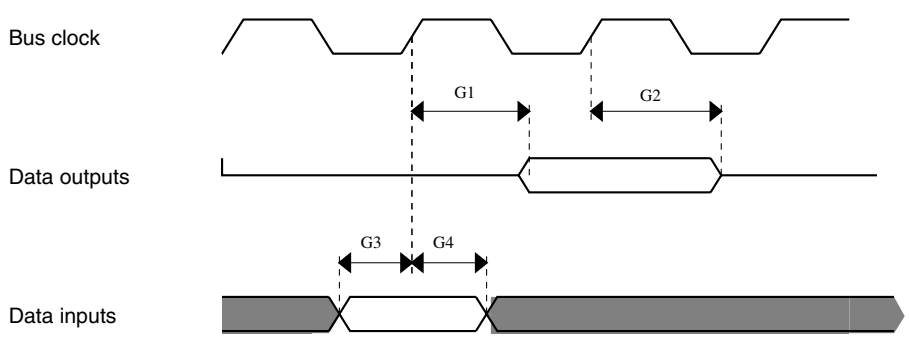



**Figure 3. EGPIO timing diagram**

The following general purpose specifications apply to all signals configured for RGPIO, FTM, and UART. The conditions are 25 pf load, $V_{DD}$ = 3.6 V to 1.71 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

**Table 10. RGPIO General Control Timing**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| R1 | CPUCLK from CLK_OUT pin high to GPIO output valid | — | 16 | ns |
| R2 | CPUCLK from CLK_OUT pin high to GPIO output invalid (output hold) | 1 | — | ns |
| R3 | GPIO input valid to bus clock high | 17 | — | ns |
| R4 | CPUCLK from CLK_OUT pin high to GPIO input invalid | — | 2 | ns |

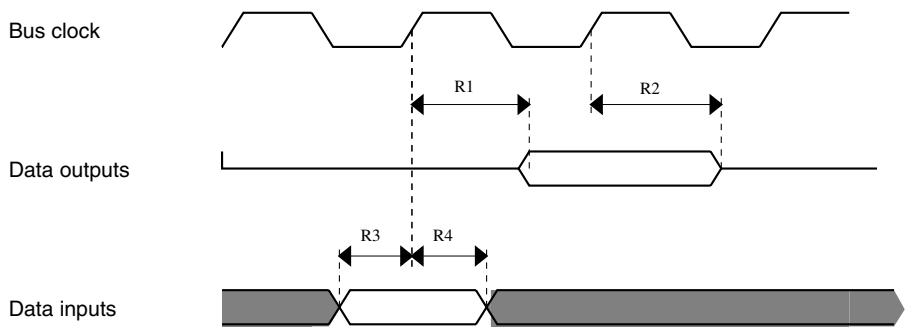



**Figure 4. RGPIO timing diagram**

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

**Table 11. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 115 | °C |
| $T_A$ | Ambient temperature | –40 | 105 | °C |

### 5.4.2 Thermal attributes

| Board type | Symbol | Description | 64 LQFP | 48 LQFP | 44 Laminate QFN | 32 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 73 | 79 | 108 | 98 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 54 | 55 | 69 | 33 | °C/W | 1 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 61 | 66 | 91 | 81 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 48 | 48 | 63 | 28 | °C/W | 1 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 37 | 34 | 44 | 13 | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 20 | 20 | 31 | 2.2 | °C/W | 3 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 5.0 | 4.0 | 6.0 | 6.0 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*.

# 6 Peripheral operating requirements and behaviors

## 6.1 Core modules

### 6.1.1 Debug specifications

**Table 12. Background debug mode (BDM) timing**

| Number | Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | $t_{MSSU}$ | BKGD/MS setup time after issuing background debug force reset to enter user mode or BDM | 500 | — | ns |
| 2 | $t_{MSH}$ | BKGD/MS hold time after issuing background debug force reset to enter user mode or BDM[1] | 100 | — | µs |

1. To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of $t_{MSH}$ after $V_{DD}$ rises above $V_{LVD}$.

# 6.2 System modules

## 6.2.1 VREG electrical specifications

**Table 13. VREG electrical specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| VREGIN | Input supply voltage | 2.7 | — | 5.5 | V | |
| $I_{DDon}$ | Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V | — | 120 | 186 | µA | |
| $I_{DDstby}$ | Quiescent current — Standby mode, load current equal zero | — | 1.1 | 1.54 | µA | |
| $I_{DDoff}$ | Quiescent current — Shutdown mode<br>• VREGIN = 5.0 V and temperature=25C<br>• Across operating voltage and temperature | <br>—<br>— | <br>650<br>— | <br>—<br>4 | <br>nA<br>µA | |
| $I_{LOADrun}$ | Maximum load current — Run mode | — | — | 120 | mA | |
| $I_{LOADstby}$ | Maximum load current — Standby mode | — | — | 1 | mA | |
| $V_{Reg33out}$ | Regulator output voltage — Input supply (VREGIN) > 3.6 V<br>• Run mode<br>• Standby mode | <br>3<br>2.1 | <br>3.3<br>2.8 | <br>3.6<br>3.6 | <br>V<br>V | |
| $V_{Reg33out}$ | Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode | 2.1 | — | 3.6 | V | 2 |
| $C_{OUT}$ | External output capacitor | 1.76 | 2.2 | 8.16 | µF | |
| ESR | External output capacitor equivalent series resistance | 1 | — | 100 | mΩ | |
| $I_{LIM}$ | Short circuit current | — | 290 | — | mA | |

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to $I_{Load}$.

# 6.3 Clock modules

## 6.3.1 MCG specifications

**Table 14. MCG specifications**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only | | — | ± 0.2 | ± 0.5 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | | — | ± 10 | — | $\%f_{dco}$ | 1 |
| $\Delta f_{dco_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | | — | ± 1.0 | ± 4.5 | $\%f_{dco}$ | 1 |
| $f_{intf_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | | — | 3.3 | 4 | MHz | |
| $f_{intf_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints_t}$ | — | — | kHz | |
| $f_{loc_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00) 640 × $f_{fll_ref}$ | 20 | 20.97 | 25 | MHz | 2, 3 |
| | | Mid range (DRS=01) 1280 × $f_{fll_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) 1920 × $f_{fll_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) 2560 × $f_{fll_ref}$ | 80 | 83.89 | 100 | MHz | |

*Table continues on the next page...*

## Table 14. MCG specifications (continued)

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{dco_t_DMX32}$ | DCO output frequency | Low range (DRS=00)<br>732 × $f_{fll_ref}$ | — | 23.99 | — | MHz | 4, 5 |
| | | Mid range (DRS=01)<br>1464 × $f_{fll_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10)<br>2197 × $f_{fll_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11)<br>2929 × $f_{fll_ref}$ | — | 95.98 | — | MHz | |
| $J_{cyc_fll}$ | FLL period jitter<br>• $f_{VCO}$ = 48 MHz<br>• $f_{VCO}$ = 98 MHz | | —<br>— | 180<br>150 | —<br>— | ps | |
| $t_{fll_acquire}$ | FLL target frequency acquisition time | | — | — | 1 | ms | 6 |
| PLL | | | | | | | |
| $f_{vco}$ | VCO operating frequency | | 48.0 | — | 100 | MHz | |
| $I_{pll}$ | PLL operating current<br>• PLL @ 96 MHz ($f_{osc_hi_1}$ = 8 MHz, $f_{pll_ref}$ = 2 MHz, VDIV multiplier = 48) | | — | 1060 | — | µA | 7 |
| $I_{pll}$ | PLL operating current<br>• PLL @ 48 MHz ($f_{osc_hi_1}$ = 8 MHz, $f_{pll_ref}$ = 2 MHz, VDIV multiplier = 24) | | — | 600 | — | µA | 7 |
| $f_{pll_ref}$ | PLL reference frequency range | | 2.0 | — | 4.0 | MHz | |
| $J_{cyc_pll}$ | PLL period jitter (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | | —<br>— | 120<br>50 | —<br>— | ps<br>ps | 8 |
| $J_{acc_pll}$ | PLL accumulated jitter over 1µs (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | | —<br>— | 1350<br>600 | —<br>— | ps<br>ps | 8 |
| $D_{lock}$ | Lock entry frequency tolerance | | ± 1.49 | — | ± 2.98 | % | |
| $D_{unl}$ | Lock exit frequency tolerance | | ± 4.47 | — | ± 5.97 | % | |
| $t_{pll_lock}$ | Lock detector detection time | | — | — | $150 \times 10^{-6}$ + 1075(1/$f_{pll_ref}$) | s | 9 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco_t}$) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.

6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC electrical specifications

**Table 15. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 1 MHz | — | 200 | — | µA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 1 MHz | — | 300 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |

*Table continues on the next page...*

## Table 15. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | | | | | |
| | • 1 MHz resonator | — | 6.6 | — | kΩ | |
| | • 2 MHz resonator | — | 3.3 | — | kΩ | |
| | • 4 MHz resonator | — | 0 | — | kΩ | |
| | • 8 MHz resonator | — | 0 | — | kΩ | |
| | • 16 MHz resonator | — | 0 | — | kΩ | |
| | • 20 MHz resonator | — | 0 | — | kΩ | |
| | • 32 MHz resonator | — | 0 | — | kΩ | |
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$,$C_y$ can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

#### 6.3.2.2 Oscillator frequency specifications

**Table 16. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc_lo}$ | Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc_hi_1}$ | Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01) | 1 | — | 8 | MHz | |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| $t_{dc_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash (FTFL) electrical specifications

This section describes the electrical characteristics of the FTFL module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 17. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk32k}$ | Erase Block high-voltage time for 32 KB | — | 52 | 452 | ms | 1 |
| $t_{hversblk128k}$ | Erase Block high-voltage time for 128 KB | — | 208 | 1808 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

### 6.4.1.2 Flash timing specifications — commands

**Table 18. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Read 1s Block execution time | | | | | |
| $t_{rd1blk32k}$ | • 32 KB data flash | — | — | 0.5 | ms | |
| $t_{rd1blk128k}$ | • 128 KB program flash | — | — | 1.7 | ms | |
| $t_{rd1sec1k}$ | Read 1s Section execution time (data flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | |
| | Erase Flash Block execution time | | | | | 2 |
| $t_{ersblk32k}$ | • 32 KB data flash | — | 55 | 465 | ms | |
| $t_{ersblk128k}$ | • 128 KB program flash | — | 220 | 1850 | ms | |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| | Program Section execution time | | | | | |
| $t_{pgmsec512}$ | • 512 B flash | — | 4.7 | — | ms | |
| $t_{pgmsec1k}$ | • 1 KB flash | — | 9.3 | — | ms | |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 1.8 | ms | |
| $t_{rdonce}$ | Read Once execution time | — | — | 25 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | µs | |
| $t_{ersall}$ | Erase All Blocks execution time | — | 275 | 2350 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |
| | Program Partition for EEPROM execution time | | | | | |
| $t_{pgmpart32k}$ | • 32 KB FlexNVM | — | 70 | — | ms | |

*Table continues on the next page...*

**Table 18. Flash command timing specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Set FlexRAM Function execution time: | | | | | |
| $t_{setramff}$ | • Control Code 0xFF | — | 50 | — | µs | |
| $t_{setram8k}$ | • 8 KB EEPROM backup | — | 0.3 | 0.5 | ms | |
| $t_{setram32k}$ | • 32 KB EEPROM backup | — | 0.7 | 1.0 | ms | |
| | Byte-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr8bers}$ | Byte-write to erased FlexRAM location execution time | — | 175 | 260 | µs | 3 |
| | Byte-write to FlexRAM execution time: | | | | | |
| $t_{eewr8b8k}$ | • 8 KB EEPROM backup | — | 340 | 1700 | µs | |
| $t_{eewr8b16k}$ | • 16 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr8b32k}$ | • 32 KB EEPROM backup | — | 475 | 2000 | µs | |
| | Word-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr16bers}$ | Word-write to erased FlexRAM location execution time | — | 175 | 260 | µs | |
| | Word-write to FlexRAM execution time: | | | | | |
| $t_{eewr16b8k}$ | • 8 KB EEPROM backup | — | 340 | 1700 | µs | |
| $t_{eewr16b16k}$ | • 16 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr16b32k}$ | • 32 KB EEPROM backup | — | 475 | 2000 | µs | |
| | Longword-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr32bers}$ | Longword-write to erased FlexRAM location execution time | — | 360 | 540 | µs | |
| | Longword-write to FlexRAM execution time: | | | | | |
| $t_{eewr32b8k}$ | • 8 KB EEPROM backup | — | 545 | 1950 | µs | |
| $t_{eewr32b16k}$ | • 16 KB EEPROM backup | — | 630 | 2050 | µs | |
| $t_{eewr32b32k}$ | • 32 KB EEPROM backup | — | 810 | 2250 | µs | |

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

### 6.4.1.3 Flash (FTFL) current and power specfications

**Table 19. Flash (FTFL) current and power specfications**

| Symbol | Description | Typ. | Unit |
|---|---|---|---|
| $I_{DD_PGM}$ | Worst case programming current in program flash | 10 | mA |

### 6.4.1.4 Reliability specifications

**Table 20. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Program Flash | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | 2 |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 10 | 100 | — | years | 2 |
| $t_{nvmretp100}$ | Data retention after up to 100 cycles | 15 | 100 | — | years | 2 |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 35 K | — | cycles | 3 |
| | Data Flash | | | | | |
| $t_{nvmretd10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | 2 |
| $t_{nvmretd1k}$ | Data retention after up to 1 K cycles | 10 | 100 | — | years | 2 |
| $t_{nvmretd100}$ | Data retention after up to 100 cycles | 15 | 100 | — | years | 2 |
| $n_{nvmcycd}$ | Cycling endurance | 10 K | 35 K | — | cycles | 3 |
| | FlexRAM as EEPROM | | | | | |
| $t_{nvmretee100}$ | Data retention up to 100% of write endurance | 5 | 50 | — | years | 2 |
| $t_{nvmretee10}$ | Data retention up to 10% of write endurance | 10 | 100 | — | years | 2 |
| $t_{nvmretee1}$ | Data retention up to 1% of write endurance | 15 | 100 | — | years | 2 |
| | Write endurance | | | | | 4 |
| $n_{nvmwree16}$ | • EEPROM backup to FlexRAM ratio = 16 | 35 K | 175 K | — | writes | |
| $n_{nvmwree128}$ | • EEPROM backup to FlexRAM ratio = 128 | 315 K | 1.6 M | — | writes | |
| $n_{nvmwree512}$ | • EEPROM backup to FlexRAM ratio = 512 | 1.27 M | 6.4 M | — | writes | |
| $n_{nvmwree4k}$ | • EEPROM backup to FlexRAM ratio = 4096 | 10 M | 50 M | — | writes | |
| $n_{nvmwree8k}$ | • EEPROM backup to FlexRAM ratio = 8192 | 20 M | 100 M | — | writes | |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology.
2. Data retention is based on $T_{javg}$ = 55°C (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at -40°C ≤ $T_j$ ≤ 125°C.
4. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

### 6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFL to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write_efficiency} \times n_{\text{nvmcycd}}$$

where

- Writes_FlexRAM — minimum number of writes to each FlexRAM location
- EEPROM — allocated FlexNVM based on DEPART; entered with Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance

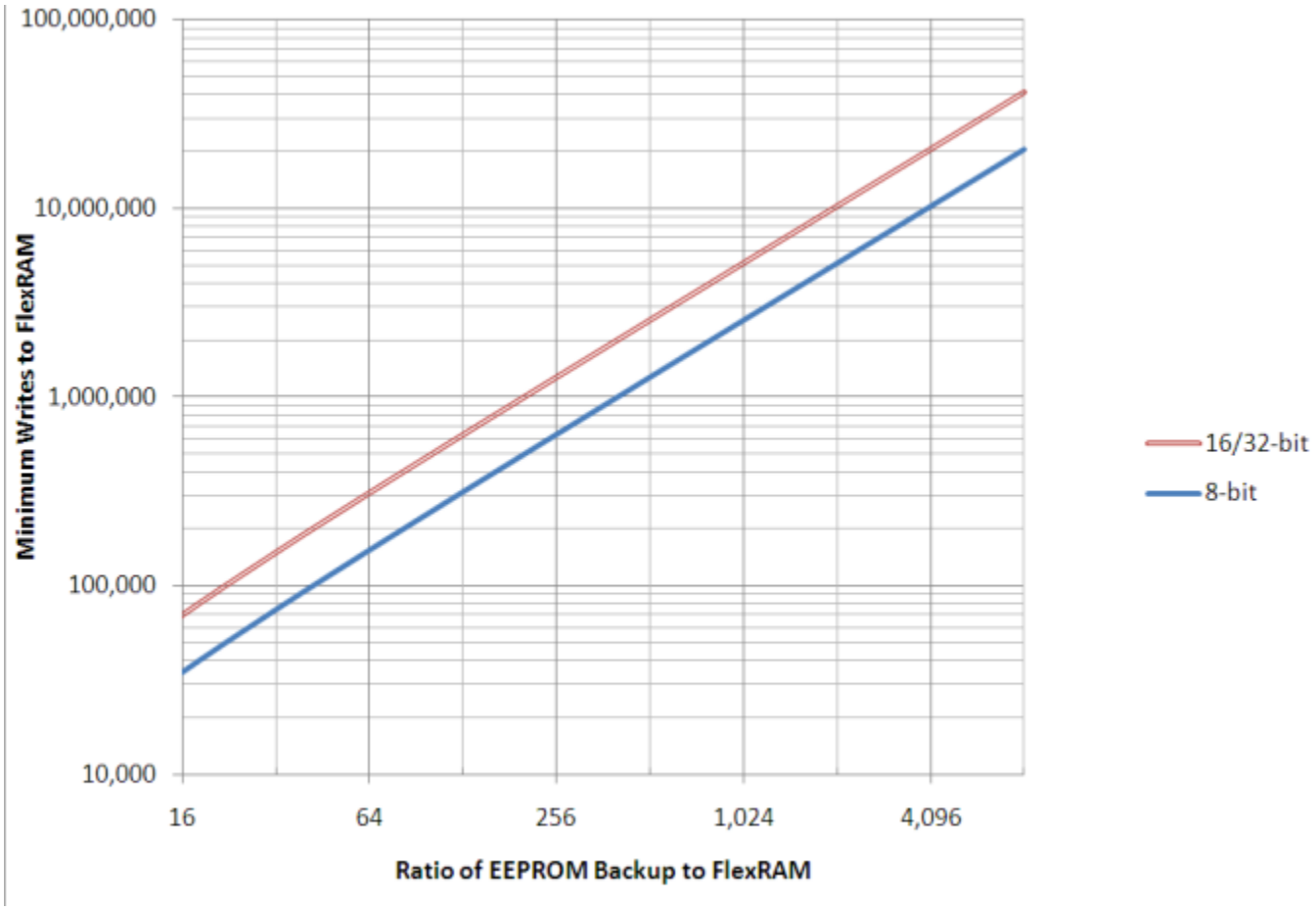



**Figure 5. EEPROM backup writes to FlexRAM**

## 6.4.2 EzPort Switching Specifications

All timing is shown with respect to a maximum pin load of 50 pF and input signal transitions of 3 ns.

**Table 21. EzPort switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| EP1 | EZP_CK frequency of operation (all commands except READ) | — | $f_{SYS}/2$ | MHz |
| EP1a | EZP_CK frequency of operation (READ command) | — | $f_{SYS}/8$ | MHz |
| EP2 | $\overline{\text{EZP_CS}}$ negation to next $\overline{\text{EZP_CS}}$ assertion | 2 x $t_{EZP_CK}$ | — | ns |
| EP3 | $\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup) | 15 | — | ns |
| EP4 | EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold) | 0.0 | — | ns |
| EP5 | EZP_D input valid to EZP_CK high (setup) | 15 | — | ns |

*Table continues on the next page...*

**Table 21. EzPort switching specifications (continued)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| EP6 | EZP_CK high to EZP_D input invalid (hold) | 0.0 | — | ns |
| EP7 | EZP_CK low to EZP_Q output valid (setup) | — | 25 | ns |
| EP8 | EZP_CK low to EZP_Q output invalid (hold) | 0.0 | — | ns |
| EP9 | $\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state | — | 12 | ns |

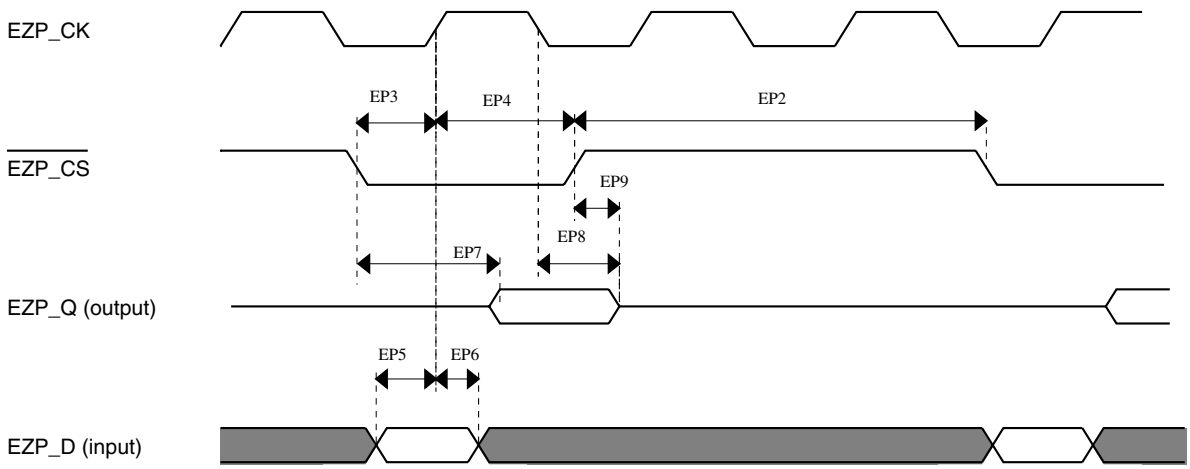



**Figure 6. EzPort Timing Diagram**

## 6.4.3 Mini-Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

**Table 22. Flexbus switching specifications**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | 25 | MHz | |
| FB1 | Clock period | 40 | — | ns | |

*Table continues on the next page...*

**Table 22. Flexbus switching specifications (continued)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| FB2 | Address, data, and control output valid | — | 20 | ns | 1 |
| FB3 | Address, data, and control output hold | 1 | — | ns | 1 |
| FB4 | Data and $\overline{\text{FB_TA}}$ input setup | 20 | — | ns | 2 |
| FB5 | Data and $\overline{\text{FB_TA}}$ input hold | 10 | — | ns | 2 |

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_CS}}n$, $\overline{\text{FB_OE}}$, FB_R/$\overline{\text{W}}$, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all FB_AD[31:0].

## Note

The following diagrams refer to signal names that may not be included on your particular device. Ignore these extraneous signals.

Also, ignore the AA=0 portions of the diagrams because this setting is not supported in the Mini-FlexBus.

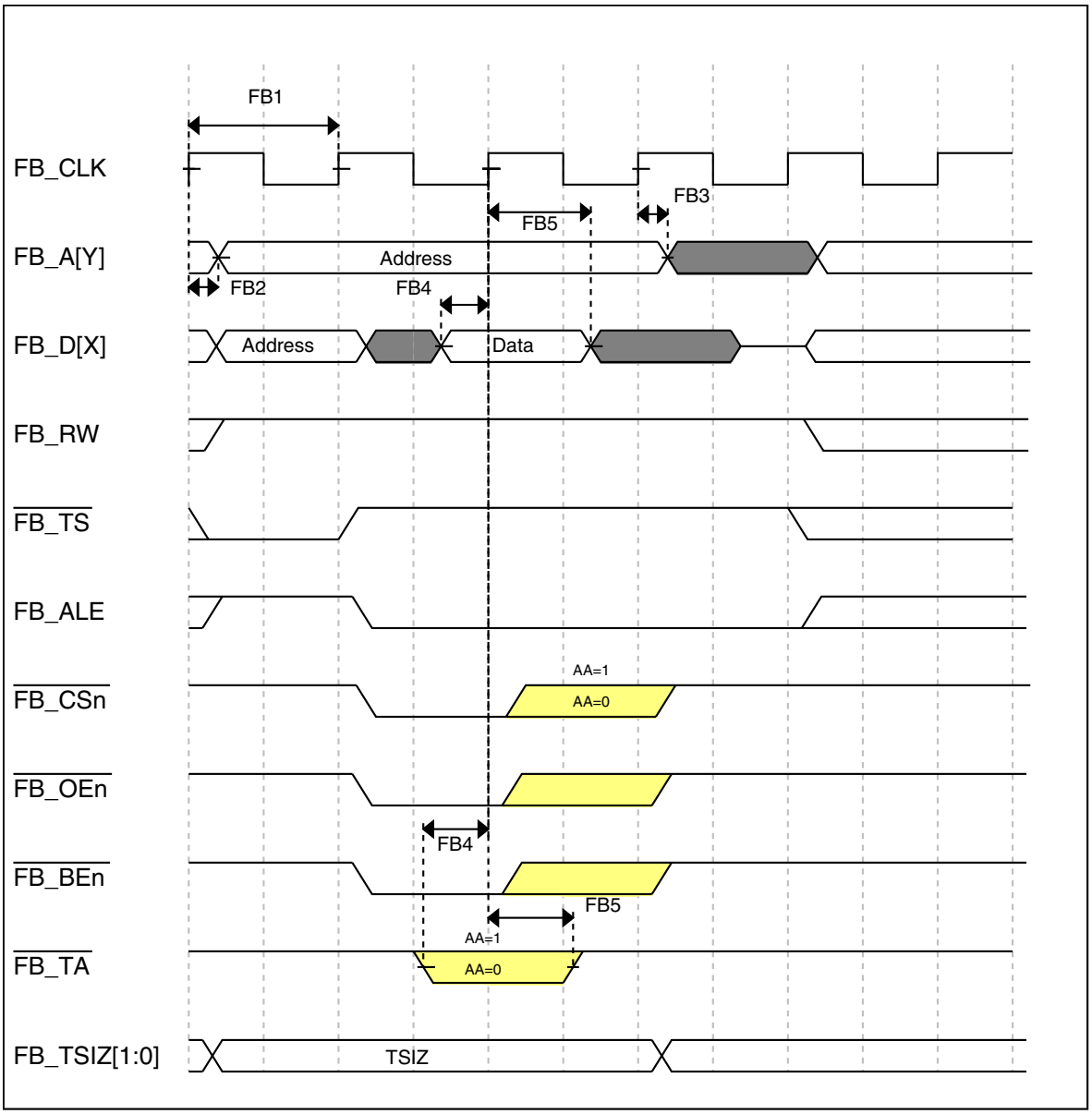



**Figure 7. Mini-FlexBus read timing diagram**

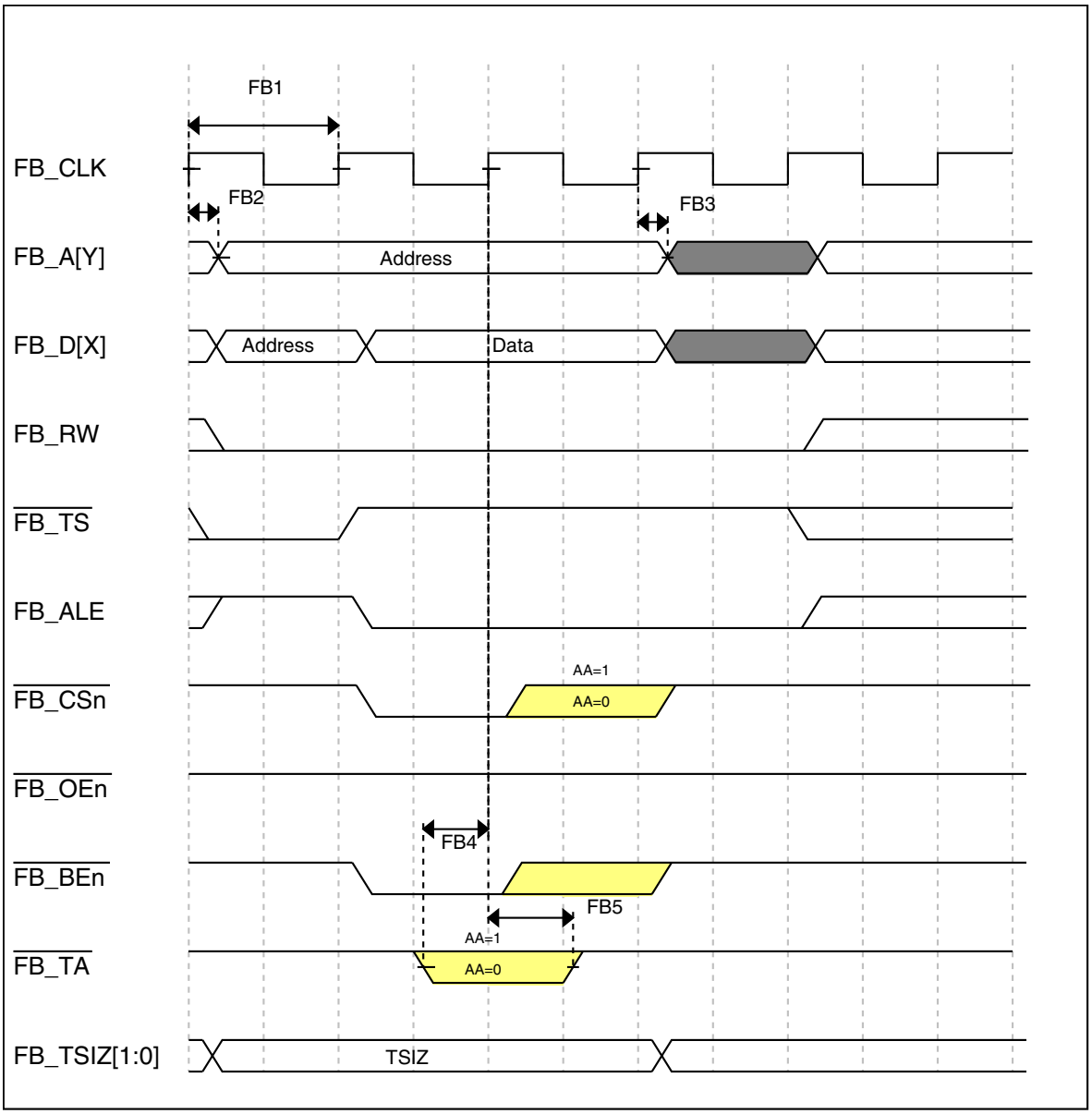



**Figure 8. Mini-FlexBus write timing diagram**

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

# 6.6 Analog

## 6.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

### 6.6.1.1 12-bit ADC operating conditions

**Table 23. 12-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$-$V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS}$-$V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | Reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| $C_{ADIN}$ | Input capacitance | • 8/10/12 bit modes | —<br>— | 4 | 5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 12 bit modes<br>$f_{ADCK}$ < 4MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 12 bit modes | 1.0 | — | 18.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 12 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 5 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The $R_{AS}$/$C_{AS}$ time constant should be kept to <1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.

5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

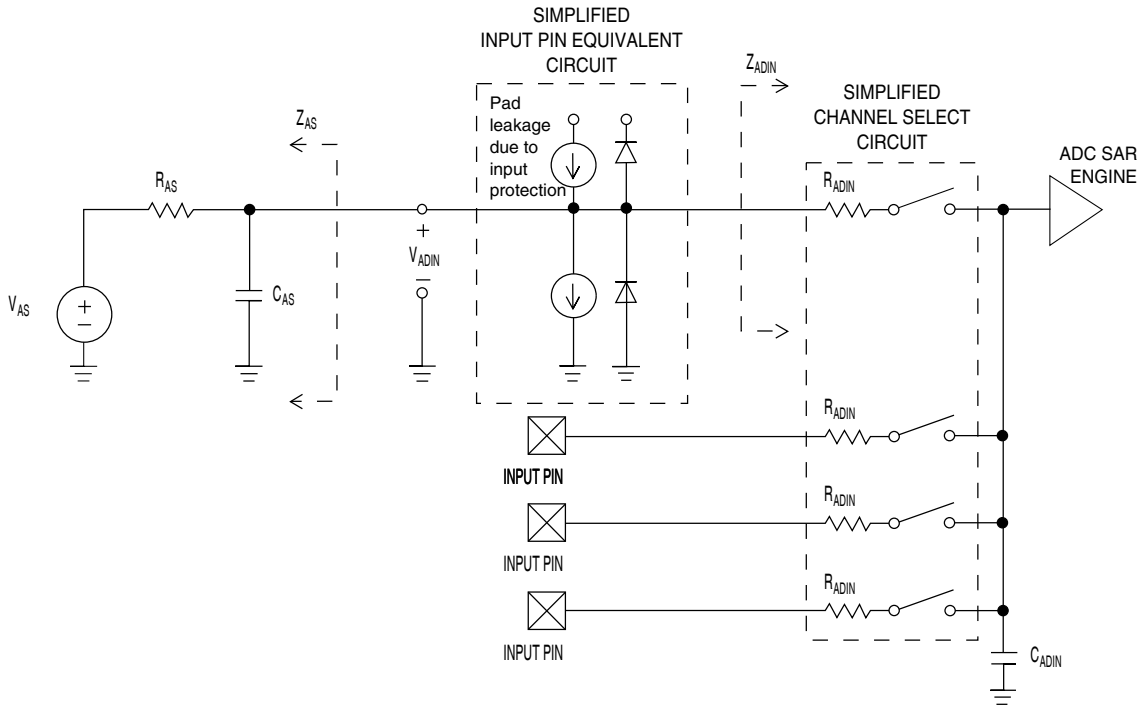



**Figure 9. ADC input impedance equivalency diagram**

### 6.6.1.2 12-bit ADC electrical characteristics

**Table 24. 12-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$)**

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA_ADC}$ | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| $f_{ADACK}$ | ADC asynchronous clock source | • ADLPC=1, ADHSC=0<br>• ADLPC=1, ADHSC=1<br>• ADLPC=0, ADHSC=0<br>• ADLPC=0, ADHSC=1 | 1.2<br>3.0<br>2.4<br>4.4 | 2.4<br>4.0<br>5.2<br>6.2 | 3.9<br>7.3<br>6.1<br>9.5 | MHz<br>MHz<br>MHz<br>MHz | $t_{ADACK}$ = 1/ $f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12 bit modes<br>• <12 bit modes | —<br>— | ±4<br>±1.4 | ±6.8<br>±2.1 | LSB[4] | 5 |
| DNL | Differential non-linearity | • 12 bit modes<br>• <12 bit modes | —<br>— | ±0.7<br>±0.2 | -1.1 to +1.9<br>-0.3 to 0.5 | LSB[4] | 5 |
| INL | Integral non-linearity | • 12 bit modes<br>• <12 bit modes | —<br>— | ±1.0<br>±0.5 | -2.7 to +1.9<br>-0.7 to +0.5 | LSB[4] | 5 |

*Table continues on the next page...*

**Table 24. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)**

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $E_{FS}$ | Full-scale error | • 12 bit modes<br>• <12 bit modes | —<br>— | -4<br>-1.4 | -5.4<br>-1.8 | LSB[4] | $V_{ADIN} = V_{DDA}$<br>5 |
| $E_Q$ | Quantization error | • 12 bit modes | — | — | ±0.5 | LSB[4] | |
| $E_{IL}$ | Input leakage error | | $I_{In} \times R_{AS}$ | | | mV | $I_{In}$ = leakage current<br>(refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | –40°C to 105°C | — | 1.715 | — | mV/°C | |
| $V_{TEMP25}$ | Temp sensor voltage | 25°C | — | 719 | — | mV | |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)

## 6.6.2 CMP and 6-bit DAC electrical specifications

**Table 25. Comparator and 6-bit DAC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ – 0.3 | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |

*Table continues on the next page...*

## Table 25. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD}$ – 0.5 | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | µA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}$-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

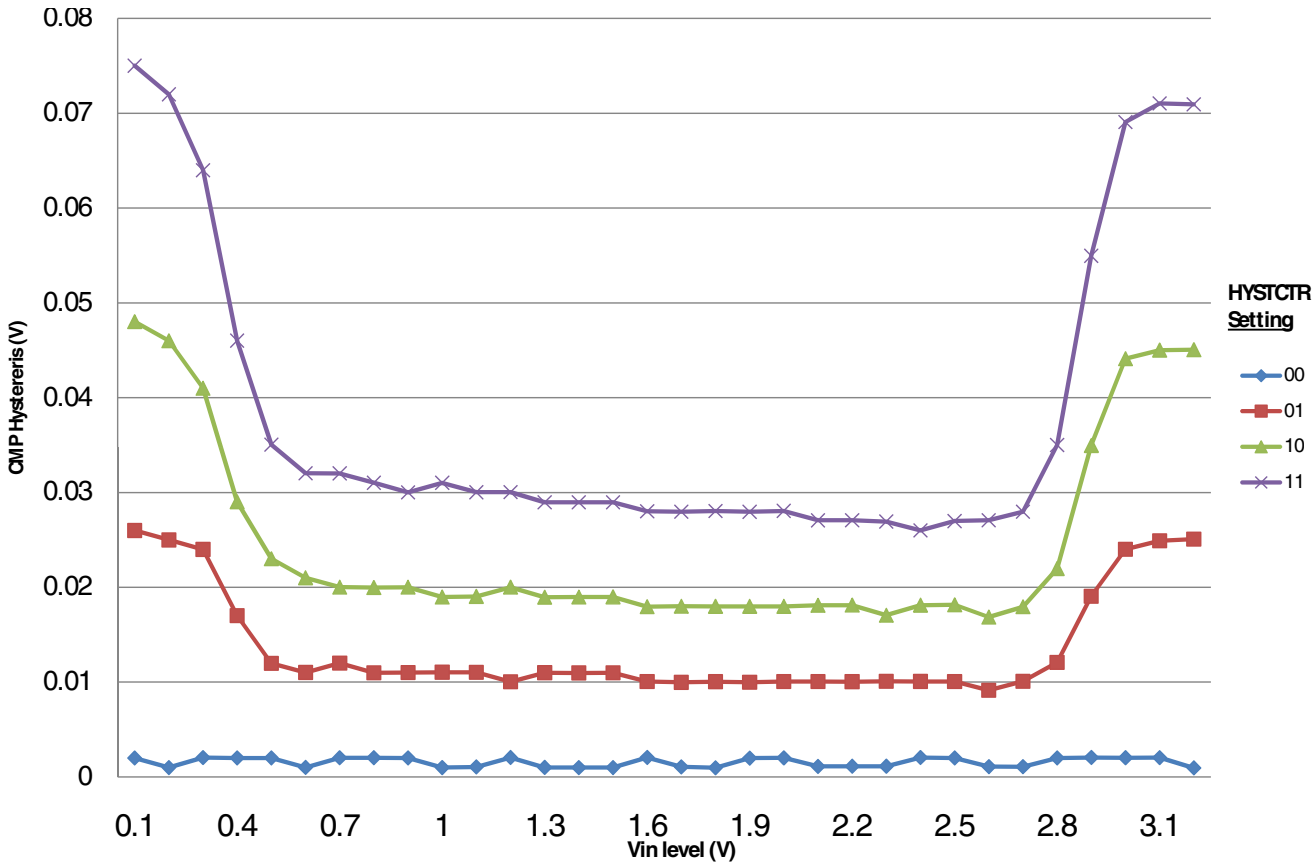



**Figure 10. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)**

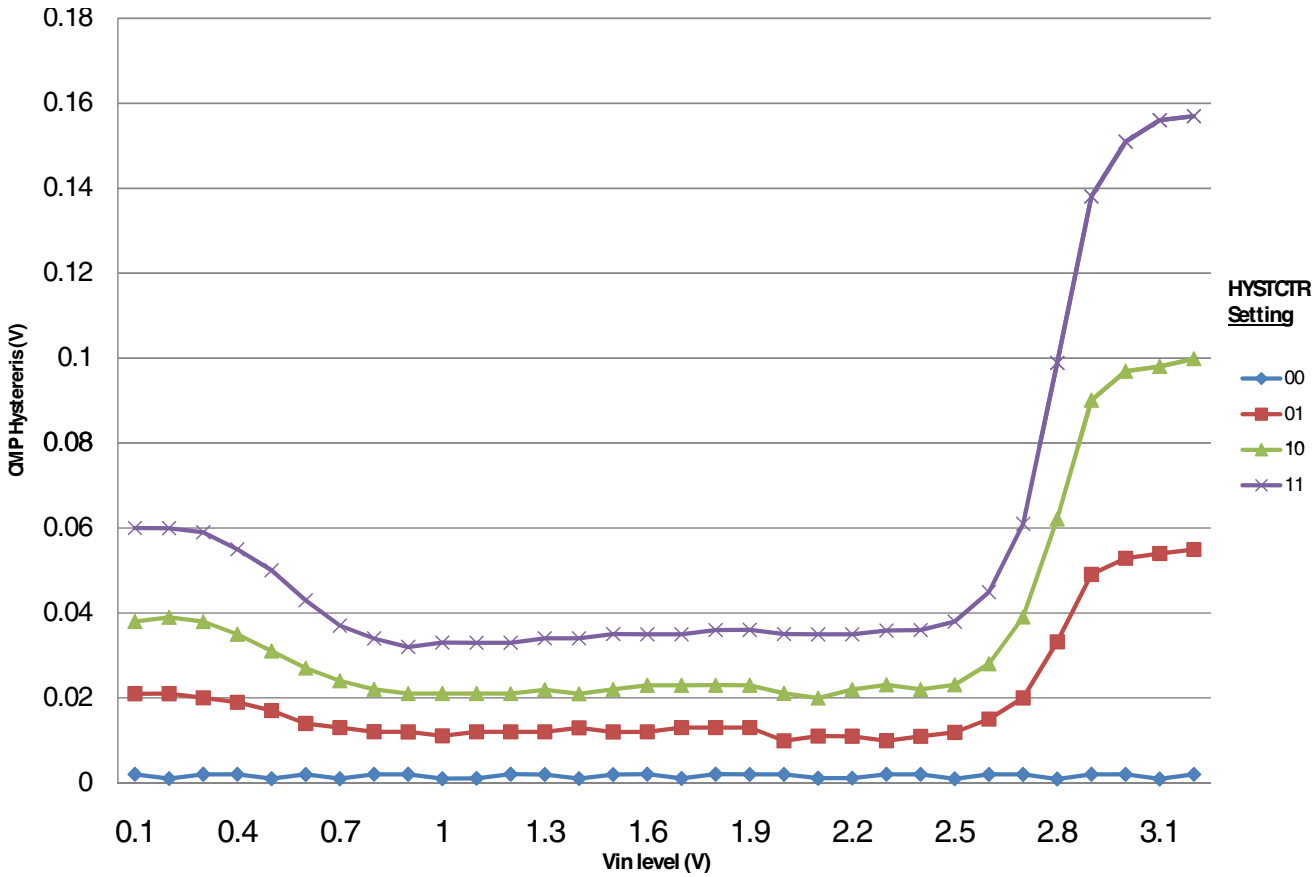



**Figure 11. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)**

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

**Table 26. 12-bit DAC operating requirements**

| Symbol | Desciption | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DACR}$ | Reference voltage | 1.13 | 3.6 | V | 1 |
| $T_A$ | Temperature | –40 | 105 | °C | |
| $C_L$ | Output load capacitance | — | 100 | pF | 2 |
| $I_L$ | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

### 6.6.3.2 12-bit DAC operating behaviors

**Table 27. 12-bit DAC operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA_DACLP}$ | Supply current — low-power mode | — | — | 450 | µA | |
| $I_{DDA_DACHP}$ | Supply current — high-speed mode | — | — | 1000 | µA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | µs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | µs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | µs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ –100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA}$ > = 2.4 V | 60 | | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | µV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance load = 3 kΩ | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h<br>• High power ($SP_{HP}$)<br>• Low power ($SP_{LP}$) | <br>1.2<br>0.05 | <br>1.7<br>0.12 | <br>—<br>— | V/µs | |
| CT | Channel to channel cross talk | — | — | -80 | dB | |
| BW | 3dB bandwidth<br>• High power ($SP_{HP}$)<br>• Low power ($SP_{LP}$) | <br>550<br>40 | <br>—<br>— | <br>—<br>— | kHz | |

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to $V_{DACR}$–100 mV
3. The DNL is measured for 0+100 mV to $V_{DACR}$–100 mV
4. The DNL is measured for 0+100mV to $V_{DACR}$–100 mV with $V_{DDA}$ > 2.4V

5. Calculated by a best fit curve from $V_{SS}$+100 mV to $V_{DACR}$–100 mV
6. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C

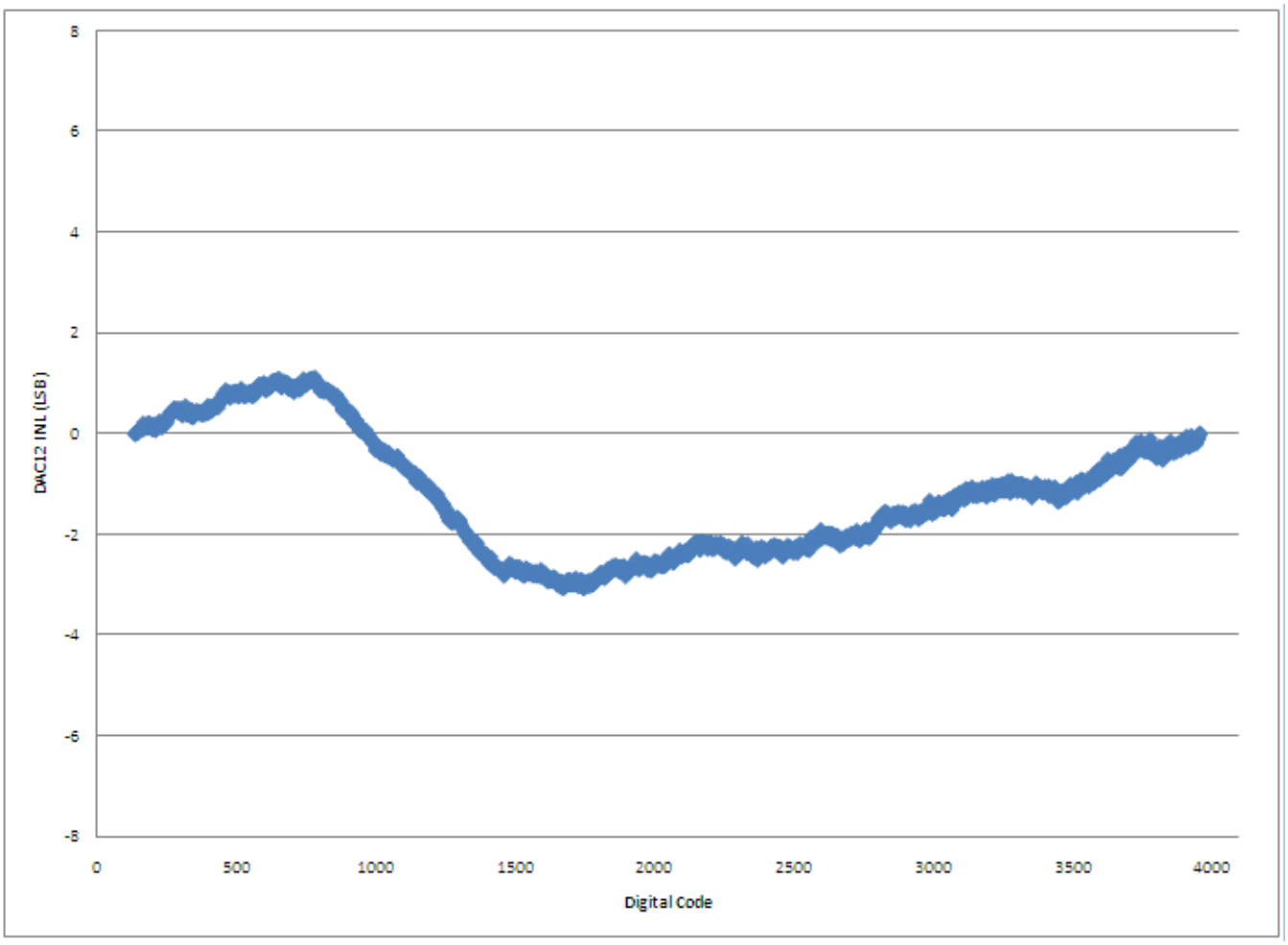



**Figure 12. Typical INL error vs. digital code**

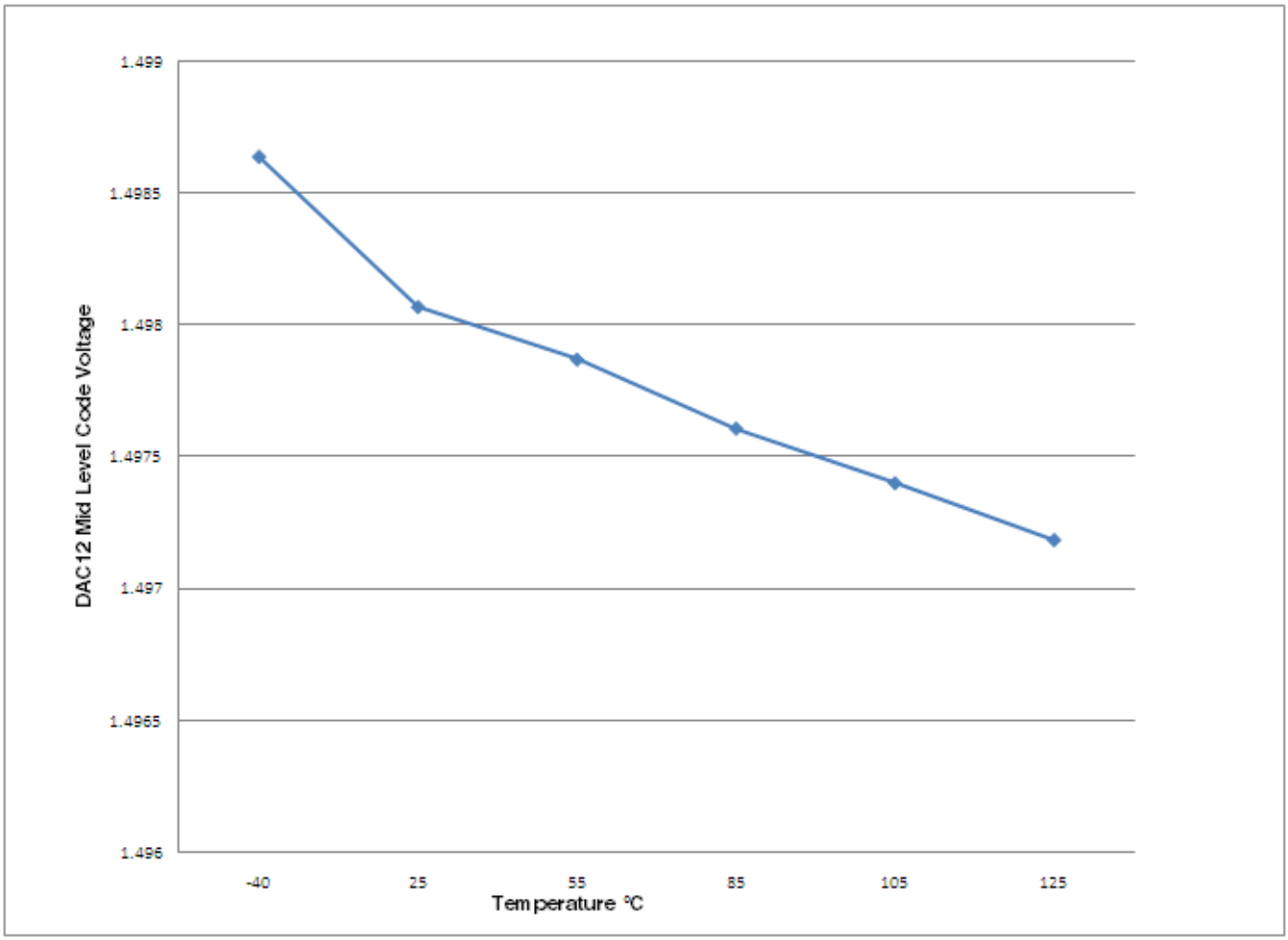



**Figure 13. Offset at half scale vs. temperature**

## 6.6.4 Voltage reference electrical specifications

**Table 28. VREF full-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | |
| $T_A$ | Temperature | –40 | 105 | °C | |
| $C_L$ | Output load capacitance | 100 | | nF | 1 |

1. $C_L$ must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

### Table 29. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{out}$ | Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C | 1.1965 | 1.2 | 1.2027 | V | |
| $V_{out}$ | Voltage reference output with— factory trim | 1.1584 | — | 1.2376 | V | |
| $V_{out}$ | Voltage reference output — user trim | 1.198 | — | 1.202 | V | |
| $V_{step}$ | Voltage reference trim step | — | 0.5 | — | mV | |
| $V_{tdrift}$ | Temperature drift (Vmax -Vmin across the full temperature range) | — | — | 80 | mV | |
| $I_{bg}$ | Bandgap only (MODE_LV = 00) current | — | — | 80 | µA | |
| $I_{tr}$ | Tight-regulation buffer (MODE_LV =10) current | — | — | 1.1 | mA | |
| $\Delta V_{LOAD}$ | Load regulation (MODE_LV = 10)<br>• current = + 1.0 mA<br>• current = - 1.0 mA | <br>—<br>— | <br>2<br>5 | <br>—<br>— | mV | 1 |
| $T_{stup}$ | Buffer startup time | — | — | 100 | µs | |
| $V_{vdrift}$ | Voltage drift (Vmax -Vmin across the full voltage range) (MODE_LV = 10, REGEN = 1) | — | 2 | — | mV | |

1. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

### Table 30. VREF limited-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_A$ | Temperature | 0 | 50 | °C | |

### Table 31. VREF limited-range operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{out}$ | Voltage reference output with factory trim | 1.173 | 1.225 | V | |

## 6.7 Timers

See General Switching Specifications.

# 6.8 Communication interfaces

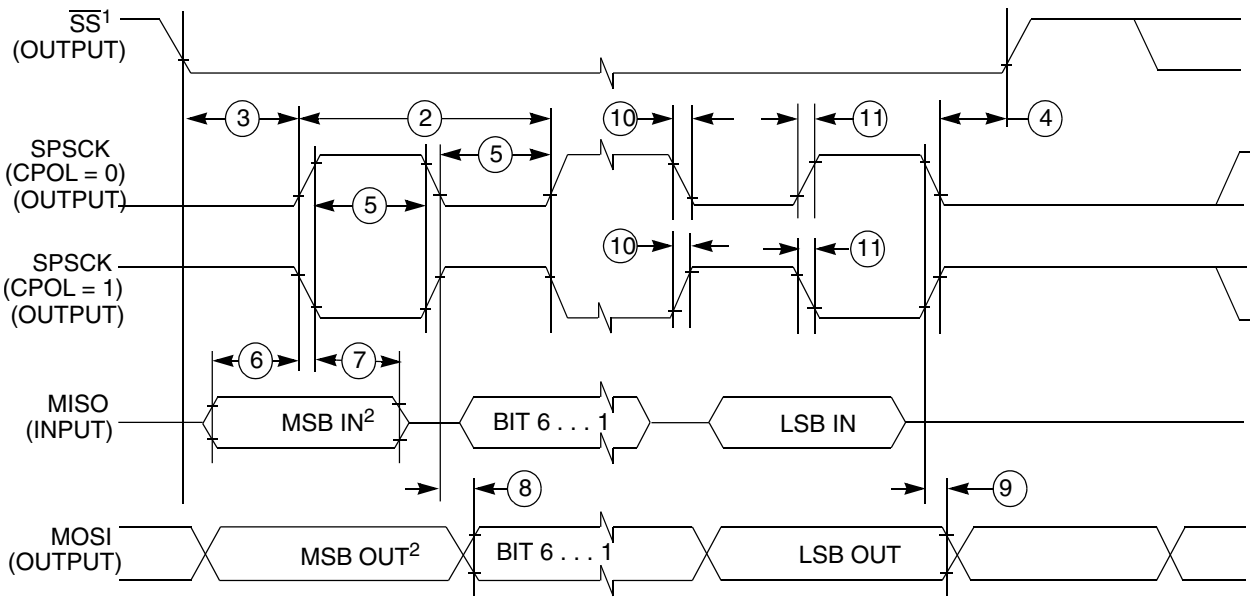
## 6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% $V_{DD}$ and 70% $V_{DD}$, unless noted, as well as input signal transitions of 3 ns and a 50 pF maximum load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

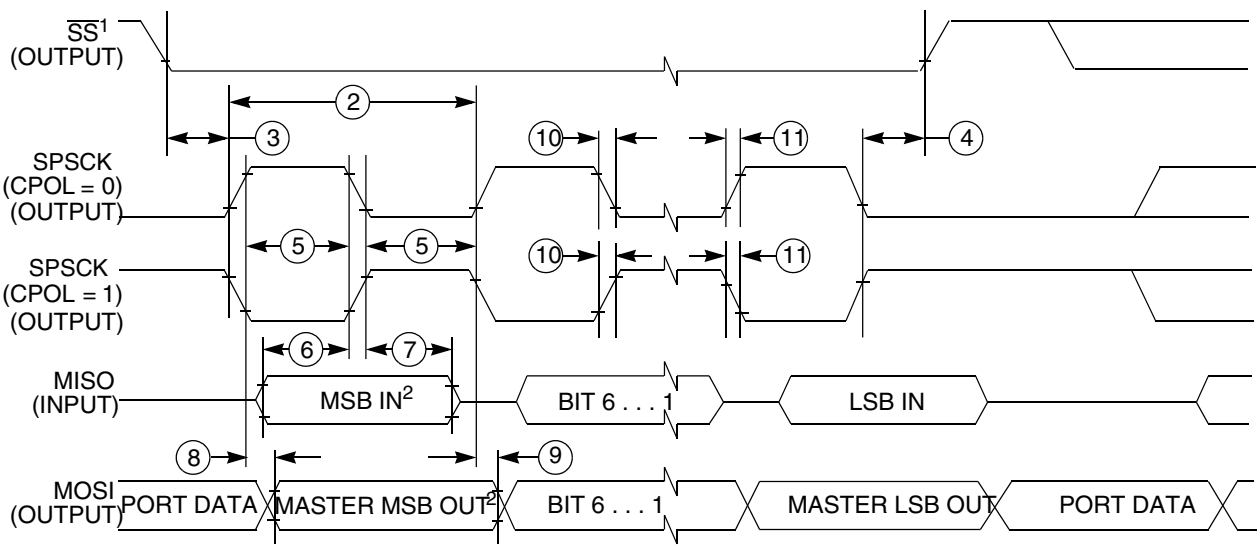
**Table 32. SPI master mode timing**

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{BUS}/2048$ | $f_{BUS}/2$ | Hz | $f_{BUS}$ is the bus clock as defined in Table 8. |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{BUS}$ | 2048 x $t_{BUS}$ | ns | $t_{BUS}$ = 1/ $f_{BUS}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{BUS}$ - 30 | 1024 x $t_{BUS}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 21 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_{v}$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{BUS}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |




1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA=0)**




1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 15. SPI master mode timing (CPHA=1)**

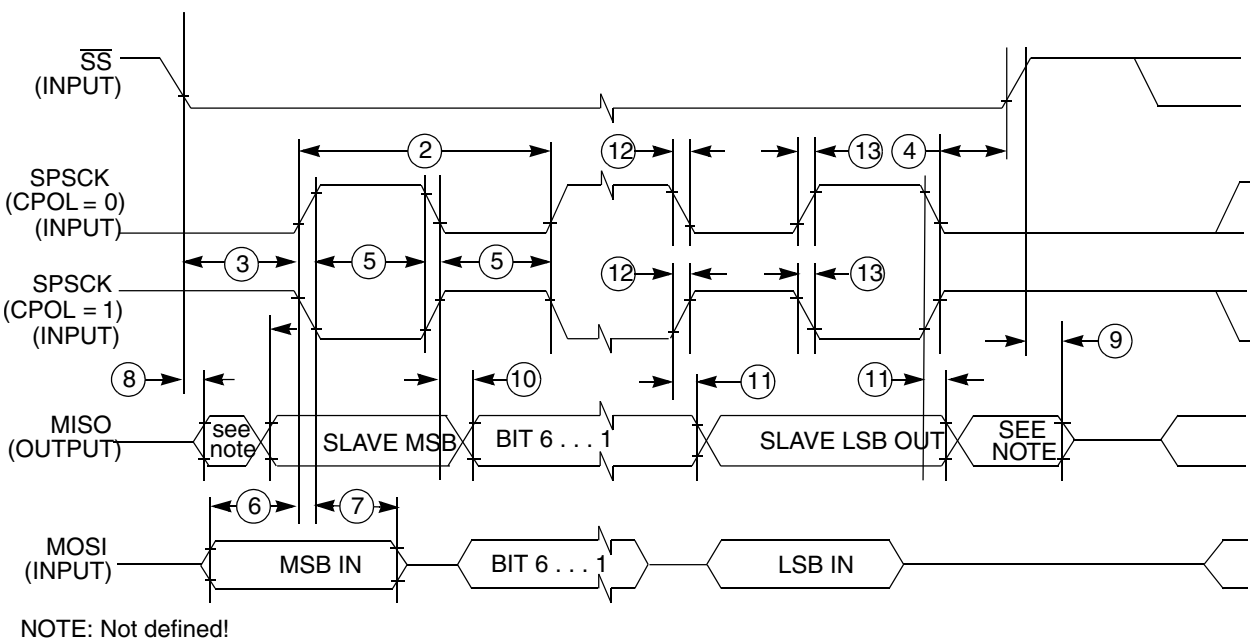
**Table 33. SPI slave mode timing**

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{BUS}/4$ | Hz | $f_{BUS}$ is the bus clock as defined in Table 8. |

*Table continues on the next page...*

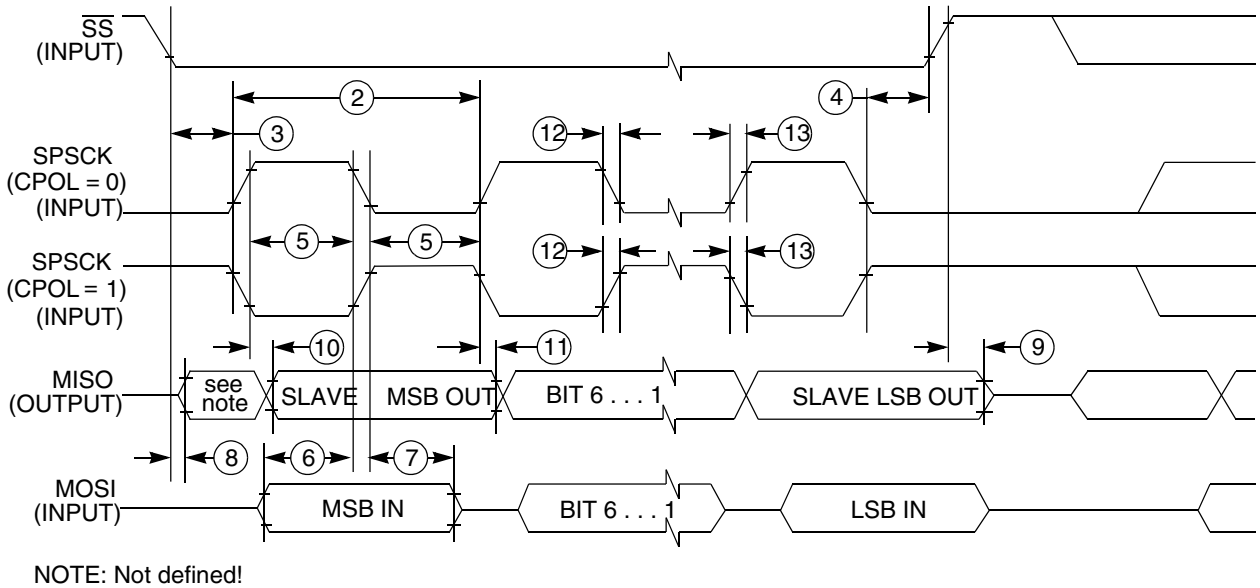
## Table 33. SPI slave mode timing (continued)

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{BUS}$ | — | ns | $t_{BUS}$ = 1/ $f_{BUS}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{BUS}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{BUS}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{BUS}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 19.5 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{BUS}$ | ns | Time to data active from high-impedanc e state |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{BUS}$ | ns | Hold time to high-impedanc e state |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 27 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{BUS}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |




NOTE: Not defined!

**Figure 16. SPI slave mode timing (CPHA=0)**




NOTE: Not defined!

**Figure 17. SPI slave mode timing (CPHA=1)**

# 6.9 Human-machine interfaces (HMI)

## 6.9.1 TSI electrical specifications

**Table 34. TSI electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DDTSI}$ | Operating voltage | 1.71 | — | 3.6 | V | |
| $C_{ELE}$ | Target electrode capacitance range | 1 | 20 | 500 | pF | 1 |
| $f_{REFmax}$ | Reference oscillator frequency | — | 5.5 | 14 | MHz | 2 |
| $f_{ELEmax}$ | Electrode oscillator frequency | — | 0.5 | 4.0 | MHz | 3 |
| $C_{REF}$ | Internal reference capacitor | 0.5 | 1 | 1.2 | pF | |
| $V_{DELTA}$ | Oscillator delta voltage | 100 | 600 | 760 | mV | 4 |
| $I_{REF}$ | Reference oscillator current source base current<br>• 1uA setting (REFCHRG=0)<br>• 32uA setting (REFCHRG=31) | —<br>— | 1.133<br>36 | 1.5<br>50 | µA | 3 , 5 |
| $I_{ELE}$ | Electrode oscillator current source base current<br>• 1uA setting (EXTCHRG=0)<br>• 32uA setting (EXTCHRG=31) | —<br>— | 1.133<br>36 | 1.5<br>50 | µA | 3 , 6 |
| Pres5 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | % | 7 |
| Pres20 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | % | 8 |
| Pres100 | Electrode capacitance measurement precision | — | 8.3333 | 38400 | % | 9 |
| MaxSens | Maximum sensitivity | 0.003 | 12.5 | — | fF/count | 10 |

*Table continues on the next page...*

**Table 34. TSI electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Res | Resolution | — | — | 16 | bits | |
| $T_{Con20}$ | Response time @ 20 pF | 8 | 15 | 25 | µs | 11 |
| $I_{TSI_RUN}$ | Current added in run mode | — | 55 | — | µA | |
| $I_{TSI_LP}$ | Low power mode current adder | — | 1.3 | 2.5 | µA | 12 |

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. CAPTRM=7, DELVOL=7, and fixed external capacitance of 20 pF.
3. CAPTRM=0, DELVOL=2, and fixed external capacitance of 20 pF.
4. CAPTRM=0, EXTCHRG=9, and fixed external capacitance of 20 pF.
5. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
6. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
7. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
8. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
10. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to ($C_{ref}$ * $I_{ext}$)/( $I_{ref}$ * PS * NSCN). Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: Iext = 5 µA, EXTCHRG = 4, PS = 128, NSCN = 2, $I_{ref}$ = 16 µA, REFCHRG = 15, $C_{ref}$ = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: $I_{ext}$ = 1 µA, EXTCHRG = 0, PS = 128, NSCN = 32, $I_{ref}$ = 32 µA, REFCHRG = 31, $C_{ref}$= 0.5 pF
11. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, DELVOL = 2, EXTCHRG = 15.
12. CAPTRM=7, DELVOL=2, REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 32-pin QFN | 98ARE10566D |
| 44-pin Laminate QFN | 98ASA00239D |
| 48-pin LQFP | 98ASH00962A |
| 64-pin LQFP | 98ASS23234W |

# 8 Pinout

## 8.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Mux Control module is responsible for selecting which ALT functionality is available on each pin.

**NOTE**

- On PTB0, EZP_MS_b is active only during reset. Refer to the detailed boot description.
- PTC1 is open drain.

| 64-pin | 48-pin | 44-pin | 32-pin | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | — | — | — | VDD | VDD | | | | | | | | |
| 2 | — | — | — | VSS | VSS | | | | | | | | |
| 3 | — | — | — | Disabled | Disabled | PTC6 | UART0_TX | I2C0_SCL | RGPIO6 | SPI1_MOSI | FBa_AD11 | | |
| 4 | — | — | — | Disabled | Disabled | PTC7 | UART0_RX | I2C0_SDA | RGPIO7 | SPI1_MISO | FBa_AD12 | | |
| 5 | 1 | — | — | Disabled | Disabled | PTD0 | UART0_CTS_b | I2C1_SDA | RGPIO8 | SPI1_SCLK | FBa_AD13 | | |
| 6 | 2 | — | — | Disabled | Disabled | PTD1 | UART0_RTS_b | I2C1_SCL | RGPIO9 | SPI1_SS | FBa_AD14 | | |
| 7 | 3 | 1 | 1 | Disabled | Disabled | PTA0 | | I2C2_SCL | FTM1_CH0 | SPI0_SS | FBa_AD15 | | |
| 8 | 4 | 2 | 2 | Disabled | Disabled | PTA1 | | I2C2_SDA | FTM1_CH1 | | FBa_AD16 | | |
| 9 | 5 | 3 | 3 | Disabled | Disabled | PTA2 | UART1_TX | | FTM1_CH2 | SPI1_SS | | | |
| 10 | 6 | 4 | 4 | Disabled | Disabled | PTA3 | UART1_RX | | FTM1_CH3 | SPI1_SCLK | | | EZP_CLK |
| 11 | 7 | 5 | 5 | ADC0_SE2 | ADC0_SE2 | PTA4 | UART1_CTS_b | I2C2_SCL | FTM1_CH4 | SPI1_MISO | | | EZP_DI |
| 12 | 8 | 6 | 6 | ADC0_SE3 | ADC0_SE3 | PTA5 | UART1_RTS_b | I2C2_SDA | FTM1_CH5 | SPI1_MOSI | CLKOUT | | EZP_DO |
| 13 | 9 | 7 | 7 | VDDA | VDDA | | | | | | | | |
| 14 | 10 | 8 | — | VREFH | VREFH | | | | | | | | |
| 15 | 11 | 9 | — | VREF_OUT | VREF_OUT | | | | | | | | |
| 16 | 12 | 10 | — | VREFL | VREFL | | | | | | | | |
| 17 | 13 | 11 | 8 | VSSA | VSSA | | | | | | | | |
| 18 | 14 | 12 | 9 | DAC0_OUT | DAC0_OUT | | | | | | | | |
| 19 | 15 | 13 | 10 | ADC0_SE0 | ADC0_SE0 | | | | | | | | |
| 20 | 16 | 14 | 11 | ADC0_SE1 | ADC0_SE1 | | | | | | | | |
| 21 | 17 | 15 | 12 | VREGIN | VREGIN | | | | | | | | |
| 22 | 18 | 16 | 13 | VOUT33 | VOUT33 | | | | | | | | |
| 23 | 19 | 17 | 14 | VSS | VSS | | | | | | | | |

| 64-pin | 48-pin | 44-pin | 32-pin | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 24 | 20 | 18 | — | VDD | VDD | | | | | | | | |
| 25 | 21 | 19 | 15 | ADC0_SE8/ TSI0_CH0 | ADC0_SE8/ TSI0_CH0 | PTA6 | | LPTMR_ALT1 | FTM_FLT1 | FBa_D7 | FBa_AD17 | | |
| 26 | — | — | — | ADC0_SE9/ TSI0_CH1 | ADC0_SE9/ TSI0_CH1 | PTD2 | FTM0_QD_PHA | RGPIO10 | FTM0_CH0 | | | | |
| 27 | 22 | 20 | — | ADC0_SE10/TSI0_CH2 | ADC0_SE10/TSI0_CH2 | PTD3 | FTM0_QD_PHB | RGPIO11 | FTM0_CH1 | FBa_D6 | FBa_AD0 | | |
| 28 | — | — | — | ADC0_SE11/TSI0_CH3 | ADC0_SE11/TSI0_CH3 | PTD4 | | RGPIO12 | | | FBa_D7 | | |
| 29 | — | — | — | ADC0_SE12/TSI0_CH4 | ADC0_SE12/TSI0_CH4 | PTD5 | | RGPIO13 | | | FBa_D6 | | |
| 30 | 23 | 21 | 16 | ADC0_SE13/TSI0_CH5 | ADC0_SE13/TSI0_CH5 | PTA7 | UART0_TX | | FTM0_QD_PHA | | FBa_D5 | | |
| 31 | 24 | 22 | — | ADC0_SE14/TSI0_CH6 | ADC0_SE14/TSI0_CH6 | PTD6 | UART0_RX | RGPIO14 | | | FBa_D4 | | |
| 32 | — | — | — | ADC0_SE15/TSI0_CH7 | ADC0_SE15/TSI0_CH7 | PTD7 | UART0_CTS_b | I2C3_SCL | RGPIO15 | | FBa_D3 | | |
| 33 | — | — | — | TSI0_CH8 | TSI0_CH8 | PTE0 | UART0_RTS_b | I2C3_SDA | | | FBa_D2 | | |
| 34 | — | — | — | TSI0_CH9 | TSI0_CH9 | PTE1 | SPI0_SS | | FTM_FLT0 | | FBa_D1 | | |
| 35 | 25 | 23 | 17 | IRQ/ EZP_MS_b | Disabled | PTB0 | | I2C0_SCL | | IRQ/ EZP_MS_b | | | EZP_CS_b |
| 36 | 26 | 24 | 18 | TSI0_CH10 | TSI0_CH10 | PTB1 | SPI0_SCLK | I2C0_SDA | FTM_FLT2 | LPTMR_ALT2 | FTM0_QD_PHB | FB_CLKOUT | |
| 37 | — | — | — | TSI0_CH11 | TSI0_CH11 | PTE2 | | I2C3_SCL | | | FBa_D0 | | |
| 38 | — | — | — | ADC0_SE16/ TSI0_CH12 | ADC0_SE16/ TSI0_CH12 | PTE3 | SPI0_MOSI | I2C3_SDA | | | FBa_OE_b | | |
| 39 | 27 | 25 | 19 | ADC0_SE17/ TSI0_CH13 | ADC0_SE17/ TSI0_CH13 | PTB2 | SPI0_MISO | | | | FBa_CS0_b | | |
| 40 | 28 | 26 | 20 | ADC0_SE18/ TSI0_CH14 | ADC0_SE18/ TSI0_CH14 | PTB3 | SPI0_MOSI | | | FBa_CS1_b | FBa_ALE | | |
| 41 | 29 | — | — | ADC0_SE19/ TSI0_CH15 | ADC0_SE19/ TSI0_CH15 | PTE4 | UART0_RTS_b | LPTMR_ALT3 | SPI1_SS | | FBa_AD1 | | |
| 42 | 30 | — | — | ADC0_SE20 | ADC0_SE20 | PTE5 | UART0_CTS_b | I2C1_SCL | SPI1_SCLK | | FBa_AD2 | | |
| 43 | — | — | — | ADC0_SE21 | ADC0_SE21 | PTE6 | UART0_RX | I2C1_SDA | SPI1_MISO | | FBa_AD3 | | |
| 44 | 31 | 27 | — | ADC0_SE22 | ADC0_SE22 | PTE7 | UART0_TX | PDB0_EXTRG | SPI1_MOSI | FBa_RW_b | FBa_AD4 | | |
| 45 | 32 | 28 | 21 | BKGD/MS | Disabled | PTB4 | BKGD/MS | | | | | | |
| 46 | 33 | 29 | 22 | XTAL2 | XTAL2 | PTB5 | | | | | | | |
| 47 | 34 | 30 | 23 | EXTAL2 | EXTAL2 | PTB6 | | | | | | | |
| 48 | 35 | 31 | 24 | VDD | VDD | | | | | | | | |

| 64-pin | 48-pin | 44-pin | 32-pin | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 49 | 36 | 32 | 25 | VSS | VSS | | | | | | | | |
| 50 | 37 | 33 | 26 | EXTAL1 | EXTAL1 | PTB7 | | I2C1_SDA | TMR_CLKIN1 | | | | |
| 51 | 38 | 34 | 27 | XTAL1 | XTAL1 | PTC0 | | I2C1_SCL | TMR_CLKIN0 | RGPIO0 | | | |
| 52 | 39 | 35 | 28 | RESET_b | Disabled | PTC1 | RESET_b | | | | | | |
| 53 | — | — | — | CMP0_IN0 | CMP0_IN0 | PTF0 | SPI0_SS | | | | FBa_AD5 | | |
| 54 | — | — | — | Disabled | Disabled | PTF1 | SPI0_SCLK | | | CMP0_OUT | FBa_AD6 | | |
| 55 | — | — | — | CMP0_IN1 | CMP0_IN1 | PTF2 | SPI0_MISO | | | | FBa_AD7 | | |
| 56 | 40 | 36 | — | CMP0_IN2 | CMP0_IN2 | PTF3 | SPI0_MOSI | | | RGPIO1 | FBa_AD8 | | |
| 57 | 41 | 37 | 29 | CMP0_IN3 | CMP0_IN3 | PTC2 | UART1_RTS_b | SPI1_SS | | RGPIO2 | FBa_AD18 | | |
| 58 | 42 | 38 | — | Disabled | Disabled | PTF4 | UART1_CTS_b | SPI1_SCLK | | FBa_D3 | FBa_AD19 | | |
| 59 | 43 | 39 | — | Disabled | Disabled | PTF5 | UART1_RX | SPI1_MISO | | FBa_D2 | FBa_RW_b | | |
| 60 | 44 | 40 | — | Disabled | Disabled | PTF6 | UART1_TX | SPI1_MOSI | | FBa_D1 | FBa_AD9 | | |
| 61 | 45 | 41 | — | Disabled | Disabled | PTF7 | UART0_RTS_b | | SPI0_SS | FBa_D0 | FBa_AD10 | | |
| 62 | 46 | 42 | 30 | Disabled | Disabled | PTC3 | UART0_CTS_b | RGPIO3 | SPI0_SCLK | CLKOUT | | | |
| 63 | 47 | 43 | 31 | Disabled | Disabled | PTC4 | UART0_RX | RGPIO4 | SPI0_MISO | PDB0_EXTRG | | | |
| 64 | 48 | 44 | 32 | Disabled | Disabled | PTC5 | UART0_TX | RGPIO5 | SPI0_MOSI | CMT_IRO | | | |

## 8.2 Pinout diagrams

The following diagrams show pinouts for the 64-pin, 48-pin, 44-pin, and 32-pin packages. These diagrams are representations for ease of reference. See the package drawings for mechanical details.

For each pin, the diagrams show the default function or (when disabled is the default) the ALT1 signal for a GPIO function. However, many signals may be multiplexed onto a single pin.

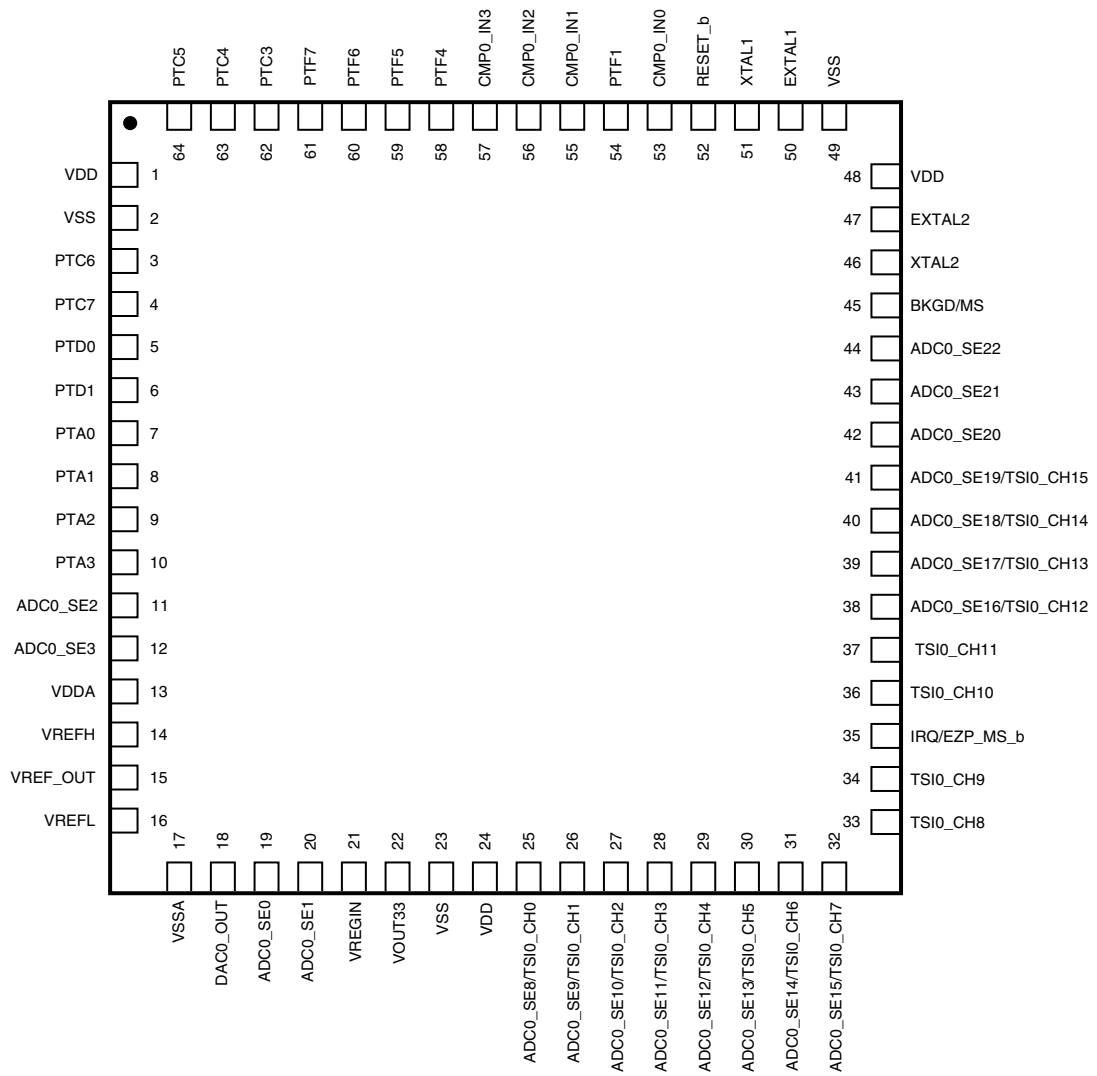



**Figure 18. 64-pin LQFP**

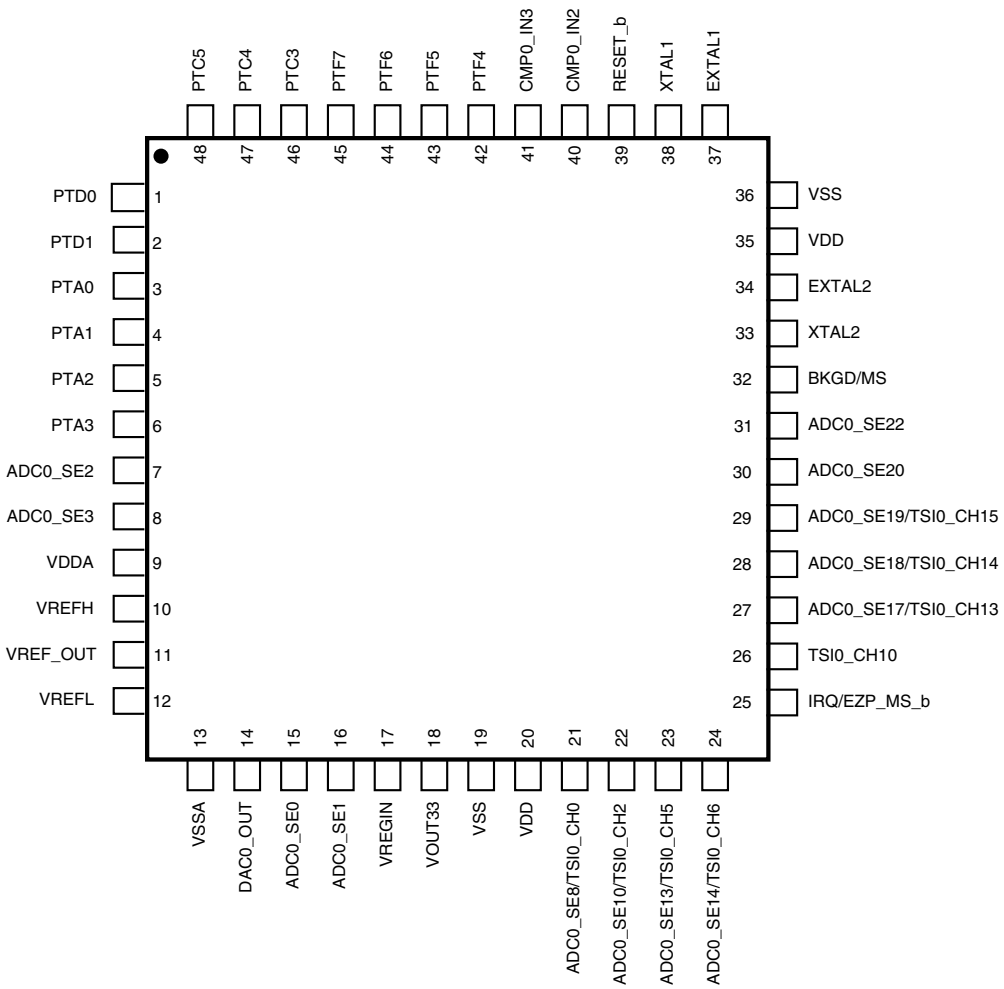



**Figure 19. 48-pin LQFP**

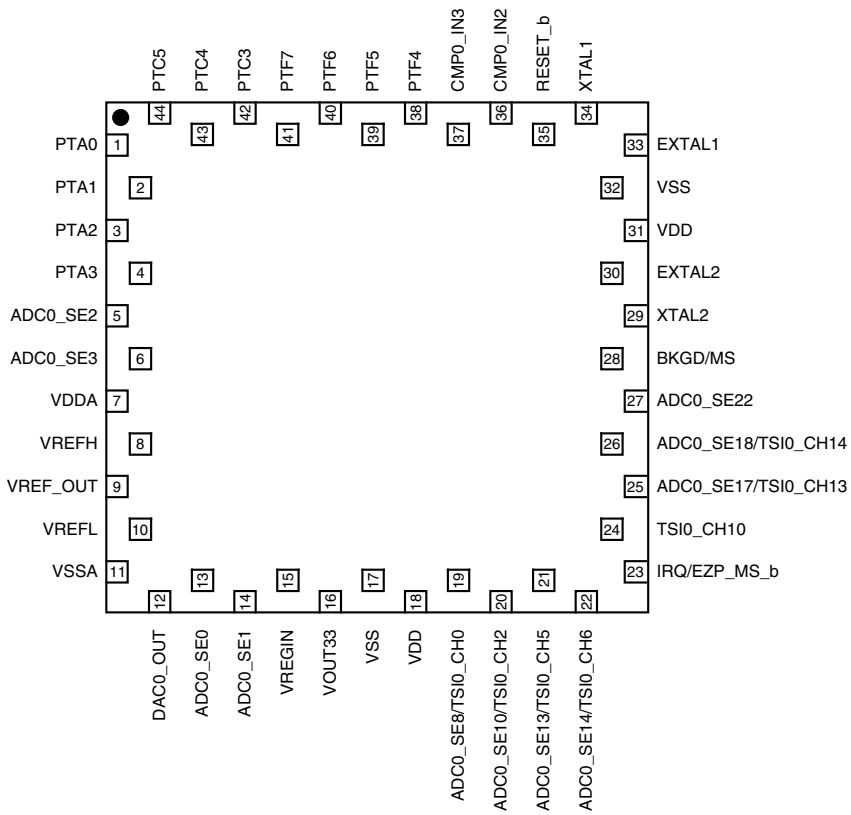



**Figure 20. 44-pin Laminate QFN**

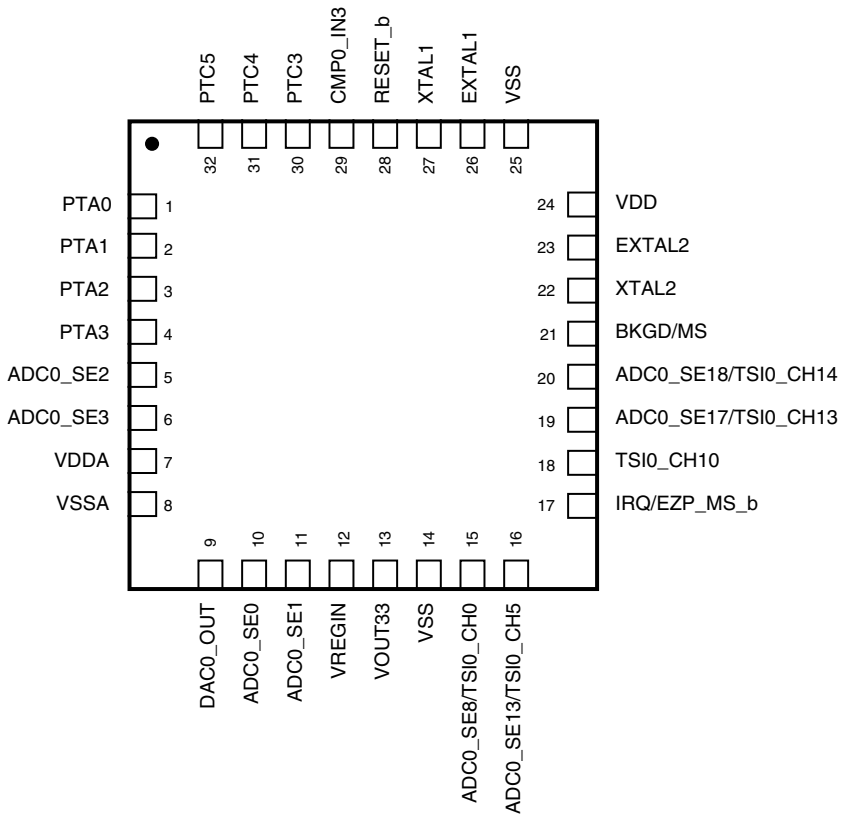



**Figure 21. 32-pin QFN**

## 8.3 Module-by-module signals

**NOTE**

- On PTB0, EZP_MS_b is active only during reset. Refer to the detailed boot description.
- PTC1 is open drain.

**Table 35. Module signals by GPIO port and pin**

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| Power and ground | | | | | |
| 1 | | | | | VDD |
| 24 | 20 | 18 | | | VDD |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 48 | 35 | 31 | 24 | | VDD |
| 2 | | | | | VSS |
| 23 | 19 | 17 | 14 | | VSS |
| 49 | 36 | 32 | 25 | | VSS |
| System | | | | | |
| 45 | 32 | 28 | 21 | PTB4 | BKGD/MS |
| 12 | 8 | 6 | 6 | PTA5 | CLKOUT |
| 62 | 46 | 42 | 30 | PTC3 | CLKOUT |
| 10 | 6 | 4 | 4 | PTA3 | EZP_CLK |
| 11 | 7 | 5 | 5 | PTA4 | EZP_DI |
| 12 | 8 | 6 | 6 | PTA5 | EZP_DO |
| 35 | 25 | 23 | 17 | PTB0 | IRQ/EZP_MS_b, EZP_CS_b |
| 52 | 39 | 35 | 28 | PTC1 | RESET_b |
| OSC | | | | | |
| 50 | 37 | 33 | 26 | PTB7 | EXTAL1 |
| 47 | 34 | 30 | 23 | PTB6 | EXTAL2 |
| 51 | 38 | 34 | 27 | PTC0 | XTAL1 |
| 46 | 33 | 29 | 22 | PTB5 | XTAL2 |
| LLWU | | | | | |
| 4 | | | | PTC7 | LLWU_P0 |
| 6 | 2 | | | PTD1 | LLWU_P1 |
| 12 | 8 | 6 | 6 | PTA5 | LLWU_P2 |
| 30 | 23 | 21 | 16 | PTA7 | LLWU_P3 |
| 32 | | | | PTD7 | LLWU_P4 |
| 35 | 25 | 23 | 17 | PTB0 | LLWU_P5 |
| 36 | 26 | 24 | 18 | PTB1 | LLWU_P6 |
| 39 | 27 | 25 | 19 | PTB2 | LLWU_P7 |
| 44 | 31 | 27 | | PTE7 | LLWU_P8 |
| 45 | 32 | 28 | 21 | PTB4 | LLWU_P9 |
| 55 | | | | PTF2 | LLWU_P10 |
| 56 | 40 | 36 | | PTF3 | LLWU_P11 |
| 57 | 41 | 37 | 29 | PTC2 | LLWU_P12 |
| 59 | 43 | 39 | | PTF5 | LLWU_P13 |
| 62 | 46 | 42 | 30 | PTC3 | LLWU_P14 |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 63 | 47 | 43 | 31 | PTC4 | LLWU_P15 |
| RGPIO | | | | | |
| 51 | 38 | 34 | 27 | PTC0 | RGPIO0 |
| 56 | 40 | 36 | | PTF3 | RGPIO1 |
| 57 | 41 | 37 | 29 | PTC2 | RGPIO2 |
| 62 | 46 | 42 | 30 | PTC3 | RGPIO3 |
| 63 | 47 | 43 | 31 | PTC4 | RGPIO4 |
| 64 | 48 | 44 | 32 | PTC5 | RGPIO5 |
| 3 | | | | PTC6 | RGPIO6 |
| 4 | | | | PTC7 | RGPIO7 |
| 5 | 1 | | | PTD0 | RGPIO8 |
| 6 | 2 | | | PTD1 | RGPIO9 |
| 26 | | | | PTD2 | RGPIO10 |
| 27 | 22 | 20 | | PTD3 | RGPIO11 |
| 28 | | | | PTD4 | RGPIO12 |
| 29 | | | | PTD5 | RGPIO13 |
| 31 | 24 | 22 | | PTD6 | RGPIO14 |
| 32 | | | | PTD7 | RGPIO15 |
| LPTMR | | | | | |
| 25 | 21 | 19 | 15 | PTA6 | LPTMR_ALT1 |
| 36 | 26 | 24 | 18 | PTB1 | LPTMR_ALT2 |
| 41 | 29 | | | PTE4 | LPTMR_ALT3 |
| LPTMR-TOD | | | | | |
| 50 | 37 | 33 | 26 | PTB7 | EXTAL1 |
| 47 | 34 | 30 | 23 | PTB6 | EXTAL2 |
| 25 | 21 | 19 | 15 | PTA6 | LPTMR_ALT1 |
| 36 | 26 | 24 | 18 | PTB1 | LPTMR_ALT2 |
| 41 | 29 | | | PTE4 | LPTMR_ALT3 |
| 51 | 38 | 34 | 27 | PTC0 | XTAL1 |
| 46 | 33 | 29 | 22 | PTB5 | XTAL2 |
| PTA | | | | | |
| 7 | 3 | 1 | 1 | PTA0 | PTA0 |
| 8 | 4 | 2 | 2 | PTA1 | PTA1 |
| 9 | 5 | 3 | 3 | PTA2 | PTA2 |
| 10 | 6 | 4 | 4 | PTA3 | PTA3 |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 11 | 7 | 5 | 5 | PTA4 | PTA4 |
| 12 | 8 | 6 | 6 | PTA5 | PTA5 |
| 25 | 21 | 19 | 15 | PTA6 | PTA6 |
| 30 | 23 | 21 | 16 | PTA7 | PTA7 |
| PTB | | | | | |
| 35 | 25 | 23 | 17 | PTB0 | PTB0 |
| 36 | 26 | 24 | 18 | PTB1 | PTB1 |
| 39 | 27 | 25 | 19 | PTB2 | PTB2 |
| 40 | 28 | 26 | 20 | PTB3 | PTB3 |
| 45 | 32 | 28 | 21 | PTB4 | PTB4 |
| 46 | 33 | 29 | 22 | PTB5 | PTB5 |
| 47 | 34 | 30 | 23 | PTB6 | PTB6 |
| 50 | 37 | 33 | 26 | PTB7 | PTB7 |
| PTC | | | | | |
| 51 | 38 | 34 | 27 | PTC0 | PTC0 |
| 52 | 39 | 35 | 28 | PTC1 | PTC1 |
| 57 | 41 | 37 | 29 | PTC2 | PTC2 |
| 62 | 46 | 42 | 30 | PTC3 | PTC3 |
| 63 | 47 | 43 | 31 | PTC4 | PTC4 |
| 64 | 48 | 44 | 32 | PTC5 | PTC5 |
| 3 | | | | PTC6 | PTC6 |
| 4 | | | | PTC7 | PTC7 |
| PTD | | | | | |
| 5 | 1 | | | PTD0 | PTD0 |
| 6 | 2 | | | PTD1 | PTD1 |
| 26 | | | | PTD2 | PTD2 |
| 27 | 22 | 20 | | PTD3 | PTD3 |
| 28 | | | | PTD4 | PTD4 |
| 29 | | | | PTD5 | PTD5 |
| 31 | 24 | 22 | | PTD6 | PTD6 |
| 32 | | | | PTD7 | PTD7 |
| PTE | | | | | |
| 33 | | | | PTE0 | PTE0 |
| 34 | | | | PTE1 | PTE1 |
| 38 | | | | PTE3 | PTE2 |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 39 | 27 | 25 | 19 | PTB2 | PTE3 |
| 41 | 29 | | | PTE4 | PTE4 |
| 42 | 30 | | | PTE5 | PTE5 |
| 43 | | | | PTE6 | PTE6 |
| 44 | 31 | 27 | | PTE7 | PTE7 |
| PTF | | | | | |
| 53 | | | | PTF0 | PTF0 |
| 54 | | | | PTF1 | PTF1 |
| 55 | | | | PTF2 | PTF2 |
| 56 | 40 | 36 | | PTF3 | PTF3 |
| 58 | 42 | 38 | | PTF4 | PTF4 |
| 59 | 43 | 39 | | PTF5 | PTF5 |
| 60 | 44 | 40 | | PTF6 | PTF6 |
| 61 | 45 | 41 | | PTF7 | PTF7 |
| 5 V VREG | | | | | |
| 22 | 18 | 16 | 13 | | VOUT33 |
| 21 | 17 | 15 | 12 | | VREGIN |
| ADC0 | | | | | |
| 11 | 7 | 5 | 5 | PTA4 | ADC0_SE2 |
| 12 | 8 | 6 | 6 | PTA5 | ADC0_SE3 |
| 25 | 21 | 19 | 15 | PTA6 | ADC0_SE8 |
| 26 | | | | PTD2 | ADC0_SE9 |
| 27 | 22 | 20 | | PTD3 | ADC0_SE10 |
| 28 | | | | PTD4 | ADC0_SE11 |
| 29 | | | | PTD5 | ADC0_SE12 |
| 30 | 23 | 21 | 16 | PTA7 | ADC0_SE13 |
| 31 | 24 | 22 | | PTD6 | ADC0_SE14 |
| 32 | | | | PTD7 | ADC0_SE15 |
| 38 | | | | PTE3 | ADC0_SE16 |
| 39 | 27 | 25 | 19 | PTB2 | ADC0_SE17 |
| 40 | 28 | 26 | 20 | PTB3 | ADC0_SE18 |
| 41 | 29 | | | PTE4 | ADC0_SE19 |
| 42 | 30 | | | PTE5 | ADC0_SE20 |
| 43 | | | | PTE6 | ADC0_SE21 |
| 44 | 31 | 27 | | PTE7 | ADC0_SE22 |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 13 | 9 | 7 | 7 | | VDDA |
| 14 | 10 | 8 | | | VREFH |
| 16 | 12 | 10 | | | VREFL |
| 17 | 13 | 11 | 8 | | VSSA |
| DAC0 | | | | | |
| 18 | 14 | 12 | 9 | | DAC0_OUT |
| VREF | | | | | |
| 15 | 11 | 9 | | | VREF_OUT |
| CMP0 | | | | | |
| 53 | | | | PTF0 | CMP0_IN0 |
| 55 | | | | PTF2 | CMP0_IN1 |
| 56 | 40 | 36 | | PTF3 | CMP0_IN2 |
| 57 | 41 | 37 | 29 | PTC2 | CMP0_IN3 |
| 54 | | | | PTF1 | CMP0_OUT |
| CMT | | | | | |
| 64 | 48 | 44 | 32 | PTC5 | CMT_IRO |
| TSI0 | | | | | |
| 25 | 21 | 19 | 15 | PTA6 | TSI0_CH0 |
| 26 | | | | PTD2 | TSI0_CH1 |
| 27 | 22 | 20 | | PTD3 | TSI0_CH2 |
| 28 | | | | PTD4 | TSI0_CH3 |
| 29 | | | | PTD5 | TSI0_CH4 |
| 30 | 23 | 21 | 16 | PTA7 | TSI0_CH5 |
| 31 | 24 | 22 | | PTD6 | TSI0_CH6 |
| 32 | | | | PTD7 | TSI0_CH7 |
| 33 | | | | PTE0 | TSI0_CH8 |
| 34 | | | | PTE1 | TSI0_CH9 |
| 36 | 26 | 24 | 18 | PTB1 | TSI0_CH10 |
| 37 | | | | PTE2 | TSI0_CH11 |
| 38 | | | | PTE3 | TSI0_CH12 |
| 39 | 27 | 25 | 19 | PTB2 | TSI0_CH13 |
| 40 | 28 | 26 | 20 | PTB3 | TSI0_CH14 |
| 41 | 29 | | | PTE4 | TSI0_CH15 |
| PDB0 | | | | | |
| 44 | 31 | 27 | | PTE7 | PDB0_EXTRG |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 63 | 47 | 43 | 31 | PTC4 | PDB0_EXTRG |
| FTM0 | | | | | |
| 34 | | | | PTE1 | FTM_FLT0 |
| 25 | 21 | 19 | 15 | PTA6 | FTM_FLT1 |
| 36 | 26 | 24 | 18 | PTB1 | FTM_FLT2 / FTM0_QD_PHB |
| 26 | | | | PTD2 | FTM0_CH0/ FTM0_QD_PHA |
| 27 | 22 | 20 | | PTD3 | FTM0_CH1 / FTM0_QD_PHB |
| 30 | 23 | 21 | 16 | PTA7 | FTM0_QD_PHA |
| 51 | 38 | 34 | 27 | PTC0 | TMR_CLKIN0 |
| 50 | 37 | 33 | 26 | PTB7 | TMR_CLKIN1 |
| FTM1 | | | | | |
| 34 | | | | PTE1 | FTM_FLT0 |
| 25 | 21 | 19 | 15 | PTA6 | FTM_FLT1 |
| 36 | 26 | 24 | 18 | PTB1 | FTM_FLT2 |
| 7 | 3 | 1 | 1 | PTA0 | FTM1_CH0 |
| 8 | 4 | 2 | 2 | PTA1 | FTM1_CH1 |
| 9 | 5 | 3 | 3 | PTA2 | FTM1_CH2 |
| 10 | 6 | 4 | 4 | PTA3 | FTM1_CH3 |
| 11 | 7 | 5 | 5 | PTA4 | FTM1_CH4 |
| 12 | 8 | 6 | 6 | PTA5 | FTM1_CH5 |
| 51 | 38 | 34 | 27 | PTC0 | TMR_CLKIN0 |
| 50 | 37 | 33 | 26 | PTB7 | TMR_CLKIN1 |
| MTIM | | | | | |
| 51 | 38 | 34 | 27 | PTC0 | TMR_CLKIN0 |
| 50 | 37 | 33 | 26 | PTB7 | TMR_CLKIN1 |
| Mini-FlexBus | | | | | |
| 36 | 26 | 24 | 18 | PTB1 | FB_CLKOUT |
| 27 | 22 | 20 | | PTD3 | FBa_AD0 |
| 41 | 29 | | | PTE4 | FBa_AD1 |
| 42 | 30 | | | PTE5 | FBa_AD2 |
| 43 | | | | PTE6 | FBa_AD3 |
| 44 | 31 | 27 | | PTE7 | FBa_AD4 |
| 53 | | | | PTF0 | FBa_AD5 |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 54 | | | | PTF1 | FBa_AD6 |
| 55 | | | | PTF2 | FBa_AD7 |
| 56 | 40 | 36 | | PTF3 | FBa_AD8 |
| 60 | 44 | 40 | | PTF6 | FBa_AD9 |
| 61 | 45 | 41 | | PTF7 | FBa_AD10 |
| 3 | | | | PTC6 | FBa_AD11 |
| 4 | | | | PTC7 | FBa_AD12 |
| 5 | 1 | | | PTD0 | FBa_AD13 |
| 6 | 2 | | | PTD1 | FBa_AD14 |
| 7 | 3 | 1 | 1 | PTA0 | FBa_AD15 |
| 8 | 4 | 2 | 2 | PTA1 | FBa_AD16 |
| 25 | 21 | 19 | 15 | PTA6 | FBa_AD17 |
| 57 | 41 | 37 | 29 | PTC2 | FBa_AD18 |
| 58 | 42 | 38 | | PTF4 | FBa_AD19 |
| 40 | 28 | 26 | 20 | PTB3 | FBa_ALE |
| 39 | 27 | 25 | 19 | PTB2 | FBa_CS0_b |
| 37 | | | | PTE2 | FBa_D0 |
| 34 | | | | PTE1 | FBa_D1 |
| 33 | | | | PTE0 | FBa_D2 |
| 32 | | | | PTD7 | FBa_D3 |
| 31 | 24 | 22 | | PTD6 | FBa_D4 |
| 30 | 23 | 21 | 16 | PTA7 | FBa_D5 |
| 29 | | | | PTD5 | FBa_D6 |
| 28 | | | | PTD4 | FBa_D7 |
| 38 | | | | PTE3 | FBa_OE_b |
| 59 | 43 | 39 | | PTF5 | FBa_RW_b |
| DATA_BUS | | | | | |
| 8 | 4 | 2 | 2 | PTA1 | FBa_AD16 |
| 39 | 27 | 25 | 19 | PTB2 | FBa_CS0_b |
| 61 | 45 | 41 | | PTF7 | FBa_D0 |
| 60 | 44 | 40 | | PTF6 | FBa_D1 |
| 59 | 43 | 39 | | PTF5 | FBa_D2 |
| 58 | 42 | 38 | | PTF4 | FBa_D3 |
| 31 | 24 | 22 | | PTD6 | FBa_D4 |
| 30 | 23 | 21 | 16 | PTA7 | FBa_D5 |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 27 | 22 | 20 | | PTD3 | FBa_D6 |
| 25 | 21 | 19 | 15 | PTA6 | FBa_D7 |
| 44 | 31 | 27 | | PTE7 | FBa_RW_b |
| I2C0 and I2C1 | | | | | |
| 3 | | | | PTC6 | I2C0_SCL |
| 35 | 25 | 23 | 17 | PTB0 | I2C0_SCL |
| 4 | | | | PTC7 | I2C0_SDA |
| 36 | 26 | 24 | 18 | PTB1 | I2C0_SDA |
| 6 | 2 | | | PTD1 | I2C1_SCL |
| 42 | 30 | | | PTE5 | I2C1_SCL |
| 51 | 38 | 34 | 27 | PTC0 | I2C1_SCL |
| 5 | 1 | | | PTD0 | I2C1_SDA |
| 43 | | | | PTE6 | I2C1_SDA |
| 50 | 37 | 33 | 26 | PTB7 | I2C1_SDA |
| I2C2 and I2C3 | | | | | |
| 7 | 3 | 1 | 1 | PTA0 | I2C2_SCL |
| 11 | 7 | 5 | 5 | PTA4 | I2C2_SCL |
| 8 | 4 | 2 | 2 | PTA1 | I2C2_SDA |
| 12 | 8 | 6 | 6 | PTA5 | I2C2_SDA |
| 32 | | | | PTD7 | I2C3_SCL |
| 37 | | | | PTE2 | I2C3_SCL |
| 33 | | | | PTE0 | I2C3_SDA |
| 38 | | | | PTE3 | I2C3_SDA |
| SPI0 | | | | | |
| 39 | 27 | 25 | 19 | PTB2 | SPI0_MISO |
| 55 | | | | PTF2 | SPI0_MISO |
| 63 | 47 | 43 | 31 | PTC4 | SPI0_MISO |
| 38 | | | | PTE3 | SPI0_MOSI |
| 40 | 28 | 26 | 20 | PTB3 | SPI0_MOSI |
| 56 | 40 | 36 | | PTF3 | SPI0_MOSI |
| 64 | 48 | 44 | 32 | PTC5 | SPI0_MOSI |
| 36 | 26 | 24 | 18 | PTB1 | SPI0_SCLK |
| 54 | | | | PTF1 | SPI0_SCLK |
| 62 | 46 | 42 | 30 | PTC3 | SPI0_SCLK |
| 7 | 3 | 1 | 1 | PTA0 | SPI0_SS |

*Table continues on the next page...*

## Table 35. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 34 | | | | PTE1 | SPI0_SS |
| 53 | | | | PTF0 | SPI0_SS |
| 61 | 45 | 41 | | PTF7 | SPI0_SS |
| SPI1 | | | | | |
| 4 | | | | PTC7 | SPI1_MISO |
| 11 | 7 | 5 | 5 | PTA4 | SPI1_MISO |
| 43 | | | | PTE6 | SPI1_MISO |
| 59 | 43 | 39 | | PTF5 | SPI1_MISO |
| 3 | | | | PTC6 | SPI1_MOSI |
| 12 | 8 | 6 | 6 | PTA5 | SPI1_MOSI |
| 44 | 31 | 27 | | PTE7 | SPI1_MOSI |
| 60 | 44 | 40 | | PTF6 | SPI1_MOSI |
| 5 | 1 | | | PTD0 | SPI1_SCLK |
| 10 | 6 | 4 | 4 | PTA3 | SPI1_SCLK |
| 42 | 30 | | | PTE5 | SPI1_SCLK |
| 58 | 42 | 38 | | PTF4 | SPI1_SCLK |
| 6 | 2 | | | PTD1 | SPI1_SS |
| 9 | 5 | 3 | 3 | PTA2 | SPI1_SS |
| 41 | 29 | | | PTE4 | SPI1_SS |
| 57 | 41 | 37 | 29 | PTC2 | SPI1_SS |
| UART0 | | | | | |
| 5 | 1 | | | PTD0 | UART0_CTS_b |
| 32 | | | | PTD7 | UART0_CTS_b |
| 42 | 30 | | | PTE5 | UART0_CTS_b |
| 62 | 46 | 42 | 30 | PTC3 | UART0_CTS_b |
| 6 | 2 | | | PTD1 | UART0_RTS_b |
| 33 | | | | PTE0 | UART0_RTS_b |
| 41 | 29 | | | PTE4 | UART0_RTS_b |
| 61 | 45 | 41 | | PTF7 | UART0_RTS_b |
| 4 | | | | PTC7 | UART0_RX |
| 31 | 24 | 22 | | PTD6 | UART0_RX |
| 43 | | | | PTE6 | UART0_RX |
| 63 | 47 | 43 | 31 | PTC4 | UART0_RX |
| 3 | | | | PTC6 | UART0_TX |
| 30 | 23 | 21 | 16 | PTA7 | UART0_TX |

*Table continues on the next page...*

**Table 35. Module signals by GPIO port and pin (continued)**

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 44 | 31 | 27 | | PTE7 | UART0_TX |
| 64 | 48 | 44 | 32 | PTC5 | UART0_TX |
| UART1 | | | | | |
| 11 | 7 | 5 | 5 | PTA4 | UART1_CTS_b |
| 58 | 42 | 38 | | PTF4 | UART1_CTS_b |
| 12 | 8 | 6 | 6 | PTA5 | UART1_RTS_b |
| 57 | 41 | 37 | 29 | PTC2 | UART1_RTS_b |
| 10 | 6 | 4 | 4 | PTA3 | UART1_RX |
| 59 | 43 | 39 | | PTF5 | UART1_RX |
| 9 | 5 | 3 | 3 | PTA2 | UART1_TX |
| 60 | 44 | 40 | | PTF6 | UART1_TX |

# 9 Revision History

The following table summarizes content changes since the previous release of this document.

**Table 36. Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 4 | 01/2012 | Thermal operating requirements: Changed maximum $T_J$ value from 125°C to 115°C |

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