3A and 4A Compact Synchronous Buck Regulators

ISL78233, ISL78234

The ISL78233, ISL78234 are highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver 3A (ISL78233), or 4A (ISL78234) of continuous output current from a 2.7V to 5.5V input supply. The devices use current mode control architecture to deliver a very low duty cycle operation at high frequency with fast transient response and excellent loop stability.

The ISL78233, ISL78234 integrate a very low ON-resistance P-channel (35mΩ) high-side FET and N-channel (11mΩ) low-side FET to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 200mV dropout voltage at 4A output current. The operation frequency of the Pulse Width Modulator (PWM) is adjustable from 500kHz to 4MHz. The default switching frequency of 2MHz is set by connecting the FS pin high.

The ISL78233, ISL78234 can be configured for discontinuous or forced continuous operation at light load. Forced continuous operation reduces noise and RF interference, while discontinuous mode provides higher efficiency by reducing switching losses at light loads.

Fault protection is provided by internal hiccup mode current limiting during short-circuit and overcurrent conditions. Other protection, such as overvoltage and over-temperature are also integrated into the device. A power-good output voltage monitor indicates when the output is in regulation.

The ISL78233, ISL78234 offers a 1ms Power-Good (PG) timer at power-up. When in shutdown, the ISL78233, ISL78234 discharges the output capacitor through an internal soft-stop switch. Other features include internal fixed or adjustable soft-start and internal/external compensation.

The ISL78233, ISL78234 is available in a 3mmx3mm 16 Ld Thin Quad Flat Pb-free (TQFN) package and in a 5mmx5mm 16 Ld Wettable Flank Quad Flat No-Lead (WFQFN) package with an exposed pad for improved thermal performance. The ISL78233, ISL78234 are rated to operate across the temperature range of -40°C to +125°C.

Features

- 2.7V to 5.5V input voltage range
- Very low ON-resistance FETs - P-channel 35mΩ and N-Channel 11mΩ typical values
- High efficiency synchronous buck regulator with up to 95% efficiency
- -1.2%/1% reference accuracy over temperature/load/line
- Complete BOM with as few as 3 external parts
- Internal soft-start - 1ms or adjustable
- Soft-stop output discharge during disable
- Adjustable frequency from 500kHz to 4MHz - default at 2MHz
- External synchronization up to 4MHz
- Over-temperature, overcurrent, overvoltage and negative overcurrent protection
- Shared common device pinout allows simplified output power upgrades over time
- Tiny 3mmx3mm TQFN package
- AEC-Q100 qualified

Applications

- DC/DC POL modules
- µC/µP, FPGA and DSP power
- Video processor/SOC power
- Li-ion battery powered devices
- Automotive infotainment power

Related Literature

- UG015, “ISL7823xEVAL1Z Evaluation Board User Guide”
- ISL78235 datasheet.
- UG062, “ISL7823xEVAL2Z Evaluation Board User Guide”

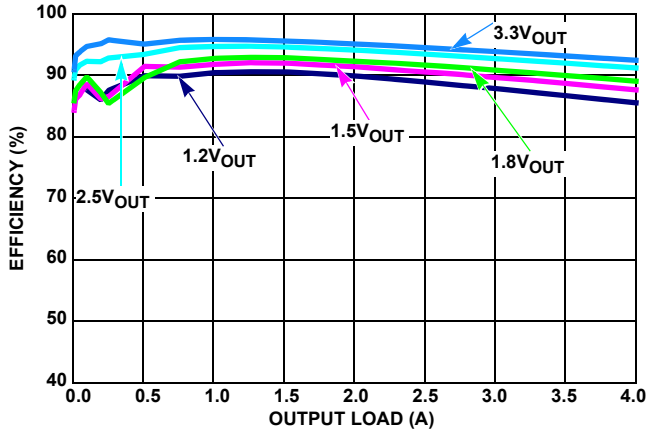
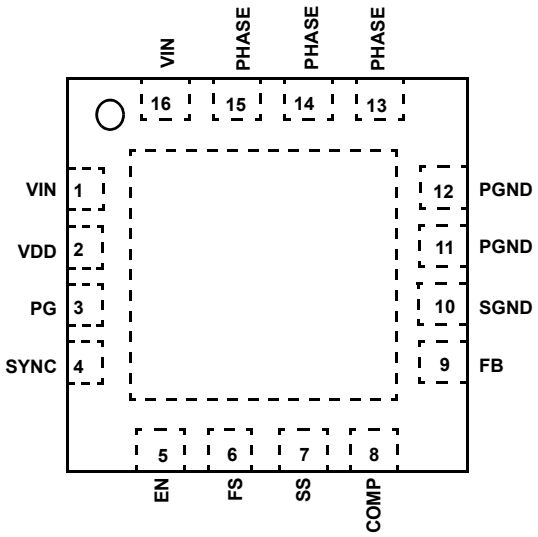


FIGURE 1. EFFICIENCY vs LOAD (2MHz $5V_{IN}$ PFM, T_A = +25°C)

Pin Configuration

ISL78233, ISL78234
(16 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 16	VIN	Input supply voltage. Place a minimum of two 22µF ceramic capacitors from VIN to PGND as close as possible to the IC for decoupling.
2	VDD	Input supply voltage for logic. Connect to VIN pin.
3	PG	Power-good is an open-drain output. Use a 10kΩ to 100kΩ pull-up resistor connected between VIN and PG. At power-up or EN HI, PG rising edge is delayed by 1ms upon output reached within regulation.
4	SYNC	Mode Selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. Connect to an external function generator for synchronization with the positive edge trigger. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case of SYNC pin float.
5	EN	Regulator enable pin. Enable the output when driven to high. Shutdown the chip and discharge output capacitor when driven to low.
6	FS	This pin sets the oscillator switching frequency, using a resistor, RFS, from the FS pin to GND. The frequency of operation may be programmed between 500kHz to 4MHz. The default frequency is 2MHz if FS is connected to VIN.
7	SS	SS is used to adjust the soft-start time. Set to SGND for internal 1ms rise time. Connect a capacitor from SS to SGND to adjust the soft-start time. Do not use more than 33nF per IC.
8, 9	COMP, FB	The feedback network of the regulator, FB, is the negative input to the transconductance error amplifier. COMP is the output of the amplifier if COMP not tied to VDD. Otherwise, COMP is disconnected through a MOSFET for internal compensation. Must connect COMP to VDD in internal compensation mode. The output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. There is an internal compensation to meet a typical application. Additional external networks across COMP and SGND might be required to improve the loop compensation of the amplifier operation. In addition, the regulator power-good and undervoltage protection circuitry use FB to monitor the regulator output voltage.
10	SGND	Signal ground
11, 12	PGND	Power ground
13, 14, 15	PHASE	Switching node connections. Connect to one terminal of the inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See "Functional Block Diagram" on page 5 for more detail.
Exposed Pad	-	The exposed pad must be connected to the SGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to SGND plane for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	OUTPUT VOLTAGE (V)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL78233ARZ	8233	Adjustable	-40 to +125	16 Ld 3x3 TQFN	L16.3x3D
ISL78233AARZ	78233A ARZ	Adjustable	-40 to +125	16 Ld 5x5mm WFQFN	L16.5x5D
ISL78234ARZ	8234	Adjustable	-40 to +125	16 Ld 3x3 TQFN	L16.3x3D
ISL78234AARZ	78234A ARZ	Adjustable	-40 to +125	16 Ld 5x5mm WFQFN	L16.5x5D
ISL78233EVAL1Z	3x3mm TQFN Evaluation Board				
ISL78234EVAL1Z	3x3mm TQFN Evaluation Board				
ISL78233EVAL2Z	5x5mm WFQFN Evaluation Board				
ISL78234EVAL2Z	5x5mm WFQFN Evaluation Board				

NOTES:

1. Add “-T” suffix for 6k unit or “-T7A” suffix for 250 unit tape and reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78233, ISL78234 For more information on MSL please see techbrief TB363.

TABLE 1. KEY DIFFERENCE BETWEEN FAMILY OF PARTS

PART NUMBER	I_{OUT} MAX (A)
ISL78233	3
ISL78234	4
ISL78235	5

Typical Application Diagram

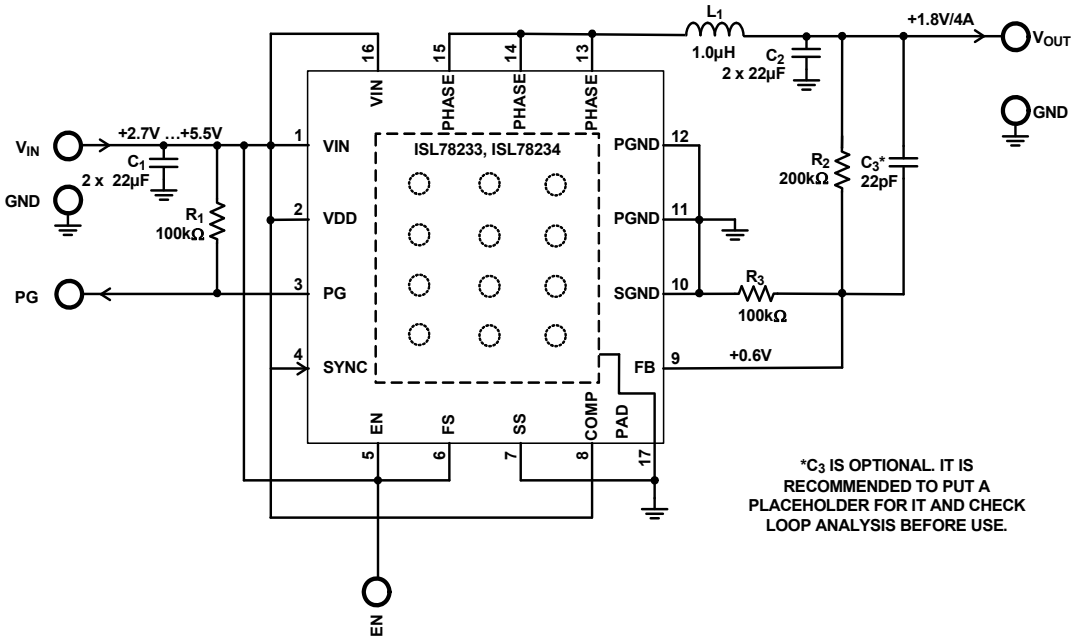


FIGURE 2. TYPICAL APPLICATION DIAGRAM

TABLE 2. COMPONENT SELECTION TABLE

V_{OUT}	1.2V	1.5V	1.8V	2.5V	3.3V	3.6V
C_1	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF
C_2	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF
C_3	22pF	22pF	22pF	22pF	22pF	22pF
L_1	0.33-0.68µH	0.33-0.68µH	0.33-0.68µH	0.47-0.78µH	0.47-0.78µH	0.47-0.78µH
R_2	100kΩ	150kΩ	200kΩ	316kΩ	450kΩ	500kΩ
R_3	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ

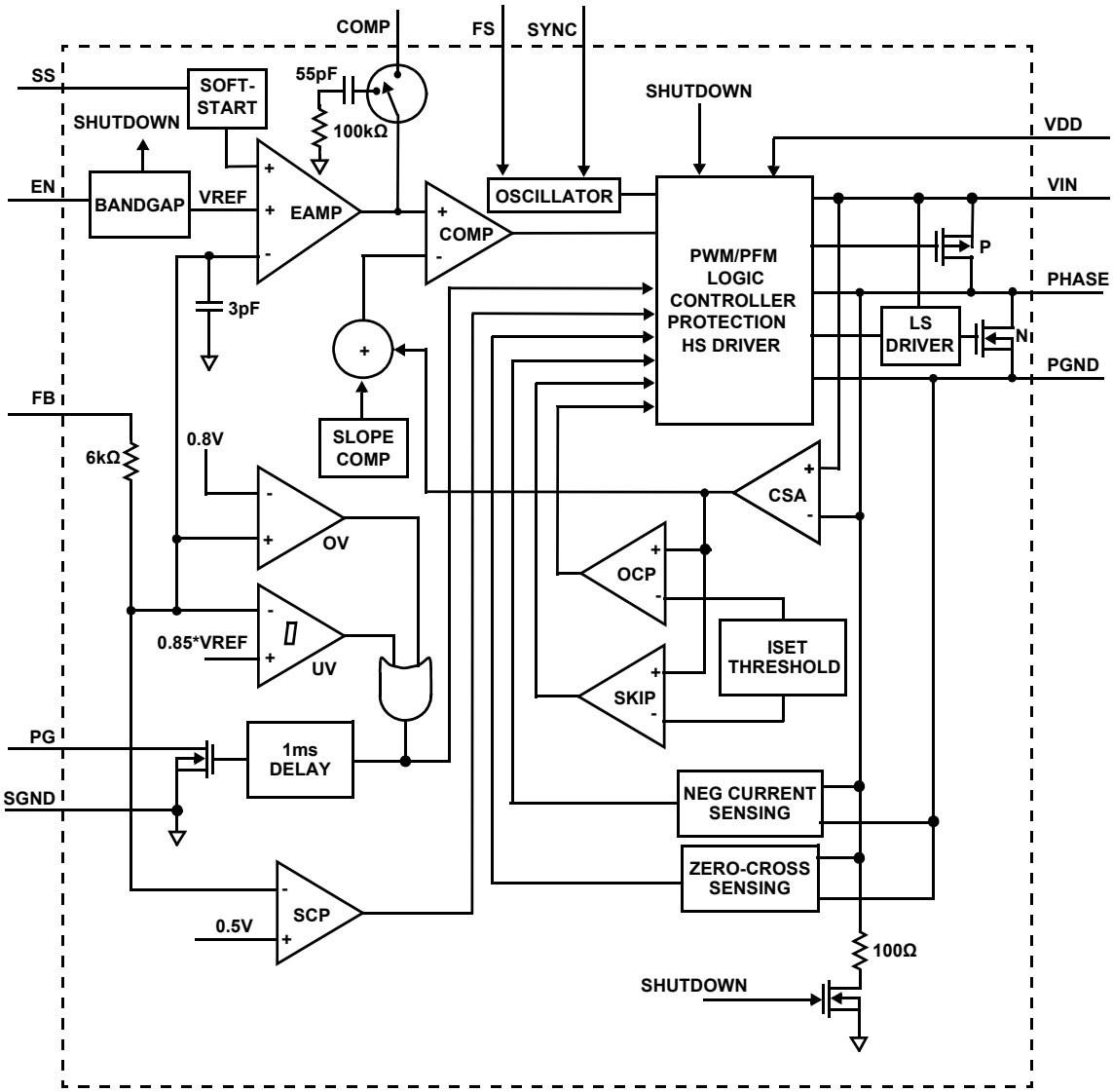


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings (Reference to GND)

VIN . . . . . -0.3V to 5.8V (DC) or 7V (20ms)
EN, FS, PG, SYNC, VFB . . . . . -0.3V to VIN + 0.3V
PHASE . . . . . -1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
COMP, SS . . . . . -0.3V to 2.7V
ESD Rating
Human Body Model (Tested per AEC-Q100-002) 5kV
Machine Model (Tested per AEC-Q100-003) 300V
Charge Device Model (Tested per AEC-Q100-011) 2kV
Latch-Up (Tested per AEC-Q100-004, Class II, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TQFN Package (Notes 4, 5)	43	3.5
16 Ld WFQFN Package (Notes 4, 5)	33	3.5

Operating Junction Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range . . . . . 2.7V to 5.5V
Load Current Range
(ISL78233) . . . . . 0A to 3A
(ISL78234) . . . . . 0A to 4A
Ambient Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the specification limits are measured at the following conditions: T_A = -40°C to +125°C, V_{IN} = 3.6V, EN = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT SUPPLY						
VIN Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load		2.5	**2.7**	V
		Falling, no load	**2.2**	2.45		V
Quiescent Supply Current	I_{VIN}	SYNC = GND, no load at the output		45		µA
		SYNC = GND, no load at the output and no switches switching		45	**60**	µA
		SYNC = V_{IN}, FS = 2MHz, no load at the output		19	**25**	mA
Shutdown Supply Current	I_{SD}	SYNC = GND, V_{IN} = 5.5V, EN = low		3.8	**10**	µA
OUTPUT REGULATION						
Reference Voltage	V_{REF}		**0.593**	0.600	**0.606**	V
VFB Bias Current	I_{VFB}	VFB = 0.75V		0.1		µA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.7V)		0.2		%/V
Soft-Start Ramp Time Cycle		SS = SGND		1		ms
Soft-Start Charging Current	I_{SS}	V_{SS} = 0.1V	**1.7**	2.1	**2.5**	µA
OVERCURRENT PROTECTION						
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Current Limit	I_{PLIMIT}	ISL78234, T_A = +25°C	5.4	6.7	8.1	A
		ISL78234, T_A = -40°C to +125°C	**5.2**		**9**	A
		ISL78233, T_A = +25°C	3.9	4.9	6	A
		ISL78233, T_A = -40°C to +125°C	**3.7**		**6.6**	A

Electrical Specifications Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the specification limits are measured at the following conditions: T_A = -40°C to +125°C, V_{IN} = 3.6V, EN = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Peak Skip Limit	I_{SKIP}	ISL78234, T_A = +25°C	0.9	1.1	1.35	A
		ISL78234, T_A = -40°C to +125°C	**0.84**		**1.5**	A
		ISL78233, T_A = +25°C	0.7	0.9	1.2	A
		ISL78233, T_A = -40°C to +125°C	**0.6**		**1.3**	A
Zero Cross Threshold			**-275**		**375**	mA
Negative Current Limit	I_{NLIMIT}	T_A = +25°C	-5.1	-2.8	-1.3	A
		T_A = -40°C to +125°C	**-6.0**		**-0.6**	A
COMPENSATION						
Error Amplifier Transconductance		COMP = VDD, Internal compensation		125		µA/V
		External compensation		130		µA/V
Transresistance	RT	4A application	**0.145**	0.2	**0.25**	Ω
PHASE						
P-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA	**26**	35	**50**	mΩ
		V_{IN} = 2.7V, I_O = 200mA	**38**	52	**78**	mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA	**5**	11	**20**	mΩ
		V_{IN} = 2.7V, I_O = 200mA	**8**	15	**31**	mΩ
PHASE Maximum Duty Cycle				100		%
PHASE Minimum On-Time		SYNC = High			**100**	ns
OSCILLATOR						
Nominal Switching Frequency	f_{SW}	FS = VIN	**1700**	2000	**2350**	kHz
		FS with RS = 402kΩ		**420**		kHz
		FS with RS = 42.2kΩ		4200		kHz
SYNC Logic LOW to HIGH Transition Range			**0.67**	0.75	**0.84**	V
SYNC Hysteresis				0.17		V
SYNC Logic Input Leakage Current		V_{IN} = 3.6V		3.7	**5**	µA
PG						
Output Low Voltage		IPG = 1mA			**0.3**	V
Delay Time (Rising Edge)		Time from V_{OUT} reached regulation	**0.5**	1	**2**	ms
PG Pin Leakage Current		PG = V_{IN}		0.01	**0.1**	µA
OVP PG Rising Threshold				0.80		V
UVP PG Rising Threshold			**80**	86	**90**	%
UVP PG Hysteresis				5.5		%
PGOOD Delay Time (Falling Edge)				6.5		µs
EN						
Logic Input Low					**0.4**	V
Logic Input High			**0.9**			V
EN Logic Input Leakage Current		Pulled up to 3.6V		0.1	**1**	µA
Thermal Shutdown		Temperature Rising		150		°C
Thermal Shutdown Hysteresis		Temperature Falling		25		°C

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A.

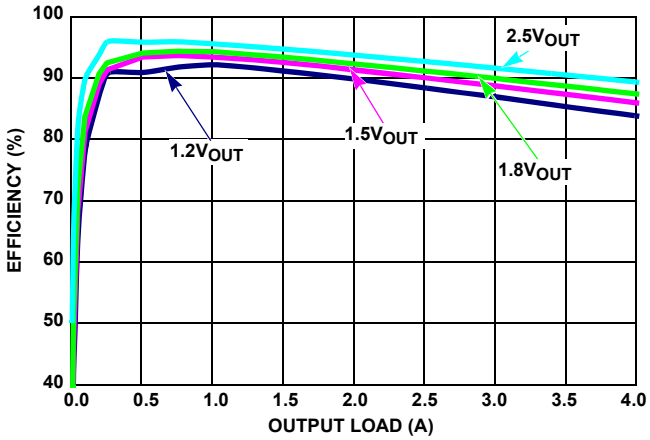


FIGURE 4. EFFICIENCY vs LOAD (2MHz, 3.3V_{IN} PWM)

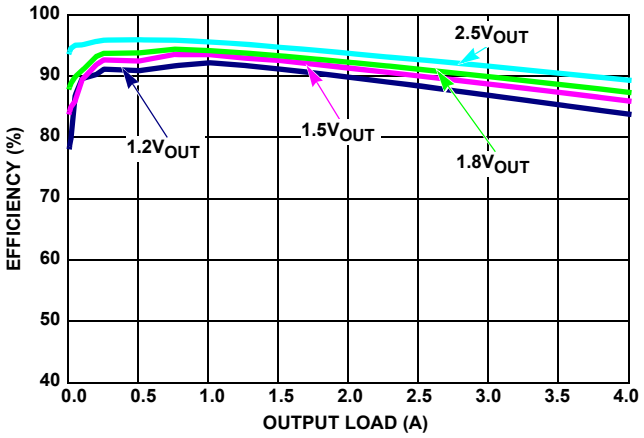


FIGURE 5. EFFICIENCY vs LOAD (2MHz, 3.3V_{IN} PFM)

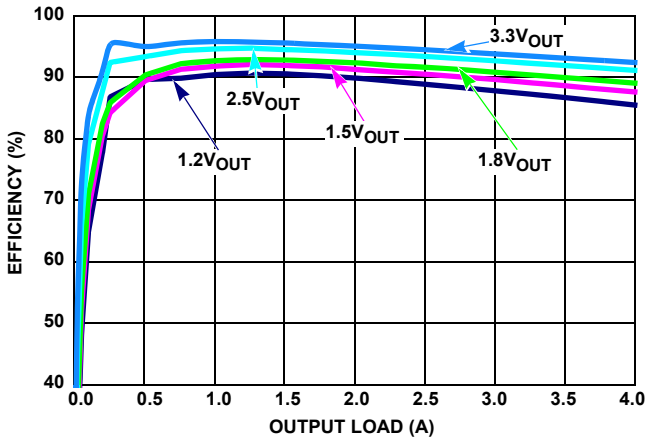


FIGURE 6. EFFICIENCY vs LOAD (2MHz, 5V_{IN} PWM)

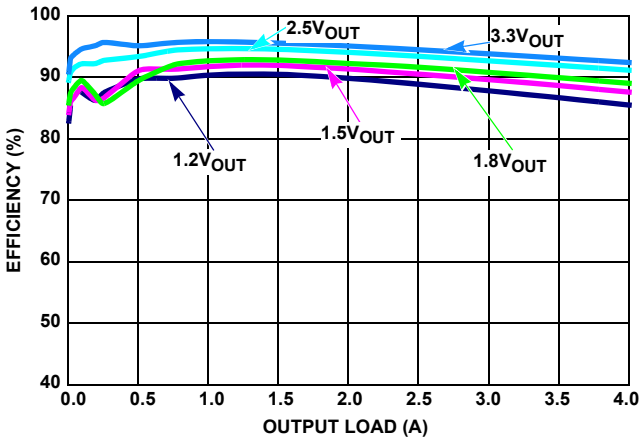


FIGURE 7. EFFICIENCY vs LOAD (2MHz, 5V_{IN} PFM)

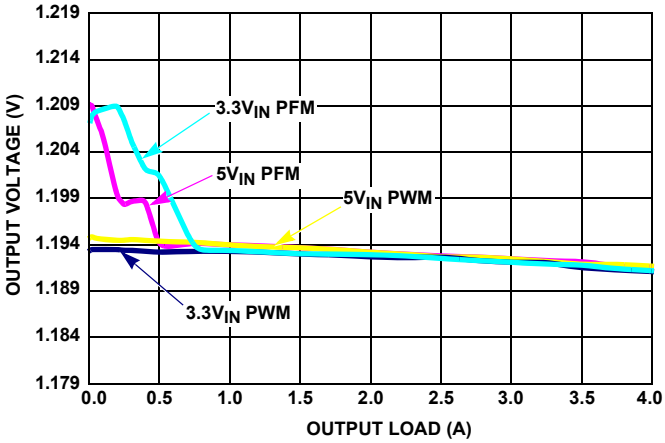


FIGURE 8. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.2V)

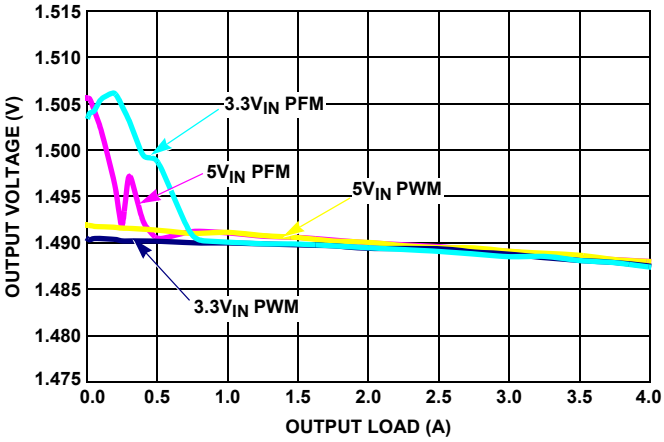


FIGURE 9. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.5V)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A. **(Continued)**

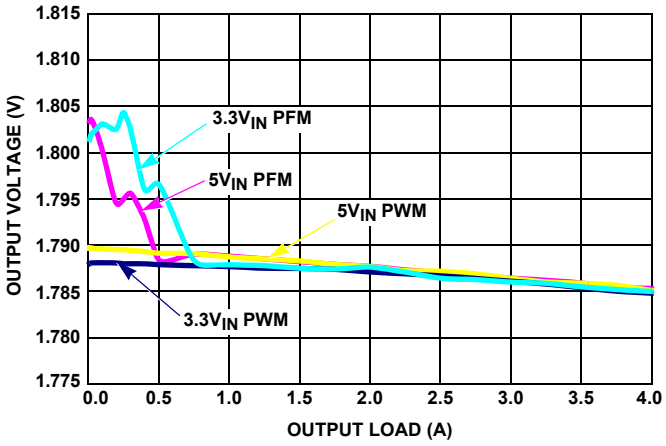


FIGURE 10. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.8V)

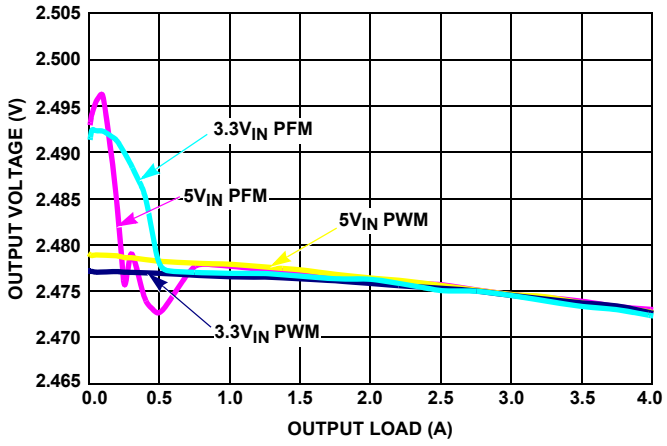


FIGURE 11. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 2.5V)

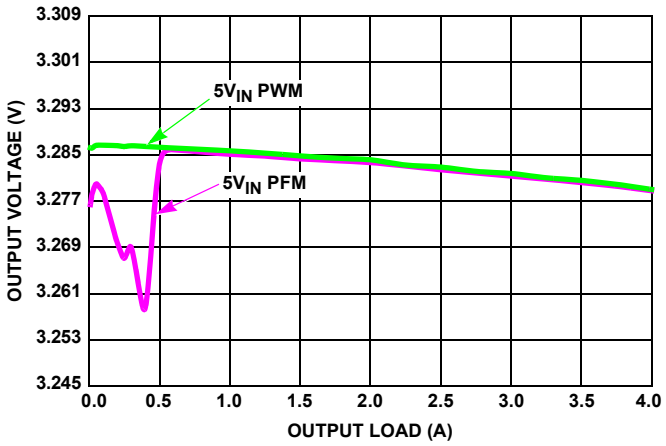


FIGURE 12. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 3.3V)

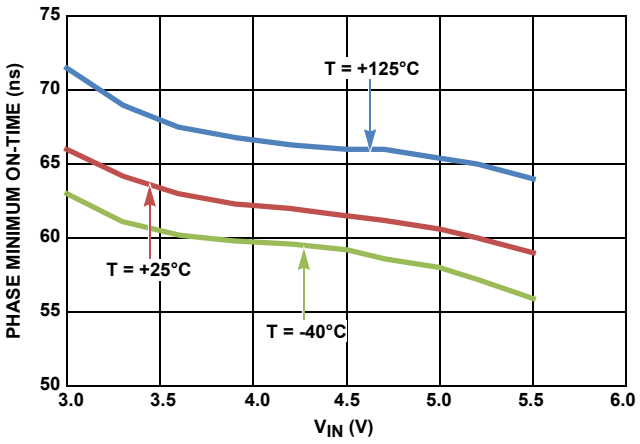


FIGURE 13. PHASE MINIMUM ON-TIME vs V_{IN} (2MHz)

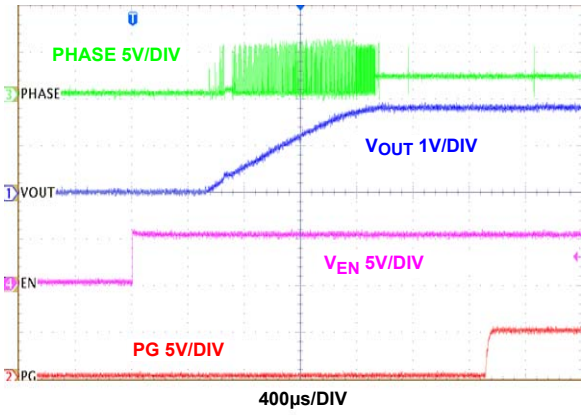


FIGURE 14. START-UP AT NO LOAD (PFM)

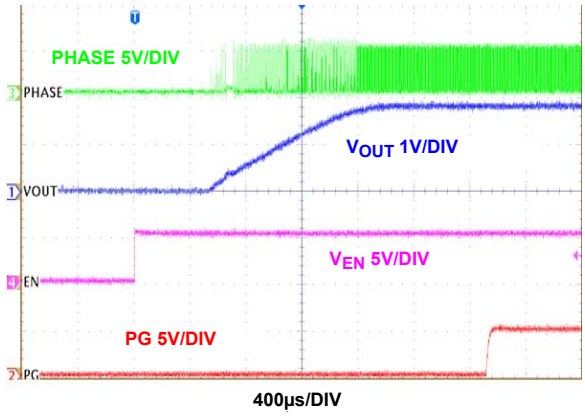
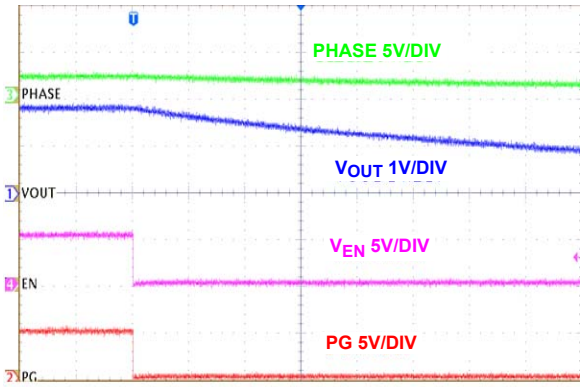


FIGURE 15. START-UP AT NO LOAD (PWM)

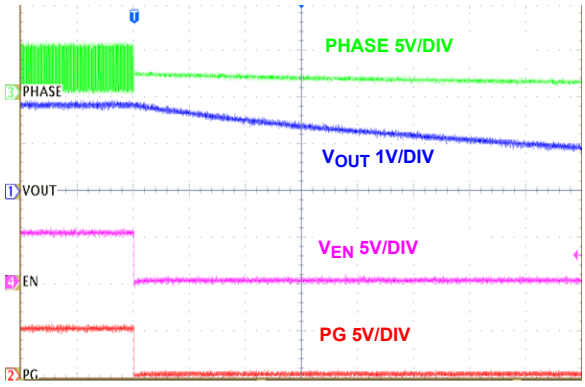
Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A. **(Continued)**



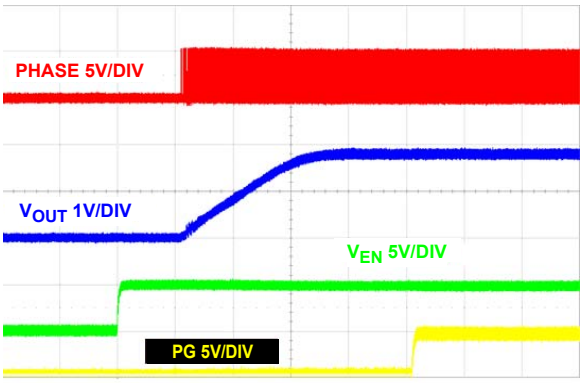
400µs/DIV

FIGURE 16. SHUTDOWN AT NO LOAD (PFM)



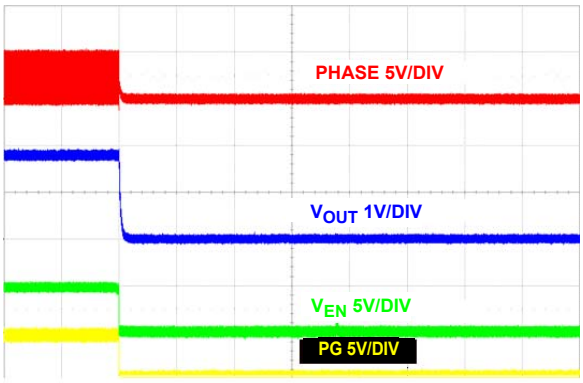
400µs/DIV

FIGURE 17. SHUTDOWN AT NO LOAD (PWM)



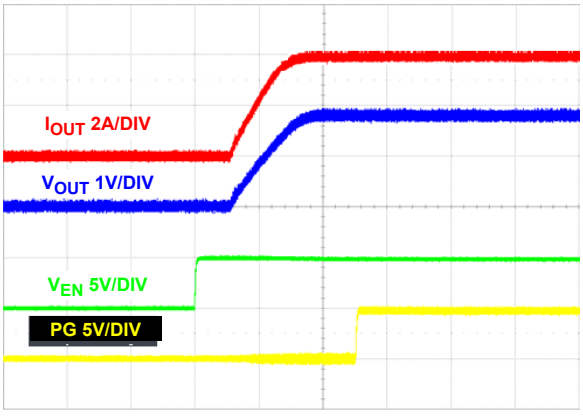
500µs/DIV

FIGURE 18. START-UP AT 4A LOAD (PWM)



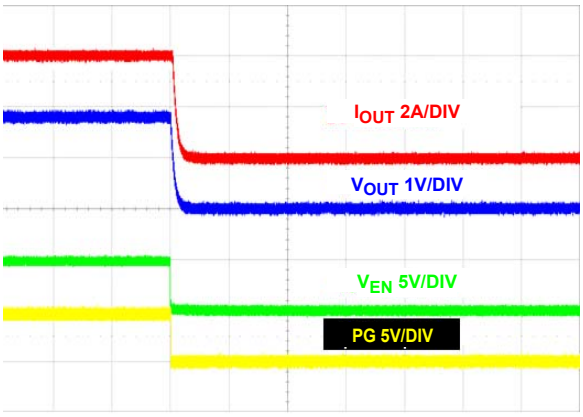
500µs/DIV

FIGURE 19. SHUTDOWN AT 4A LOAD (PWM)



500µs/DIV

FIGURE 20. START-UP AT 4A LOAD (PFM)



500µs/DIV

FIGURE 21. SHUTDOWN AT 4A LOAD (PFM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A. **(Continued)**

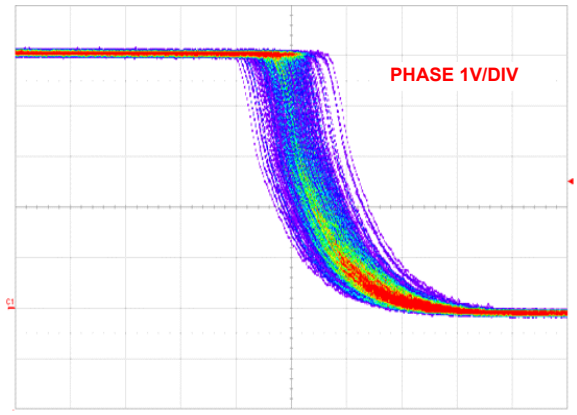


FIGURE 22. JITTER AT NO LOAD PWM (1MHz)

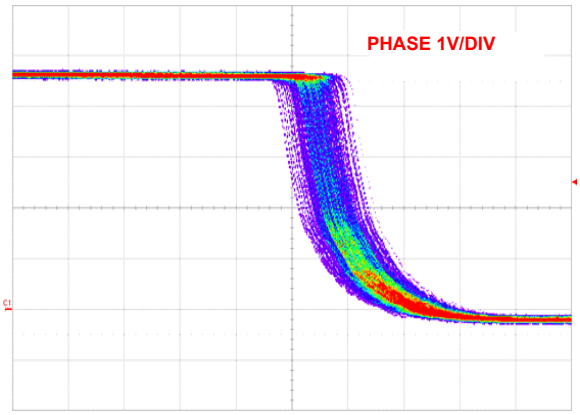


FIGURE 23. JITTER AT FULL LOAD PWM (1MHz)

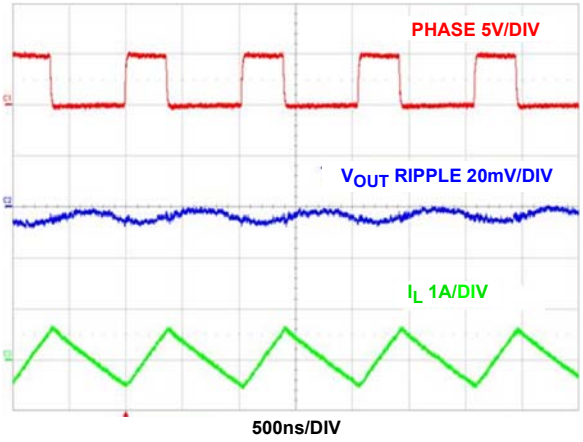


FIGURE 24. STEADY STATE AT NO LOAD PWM

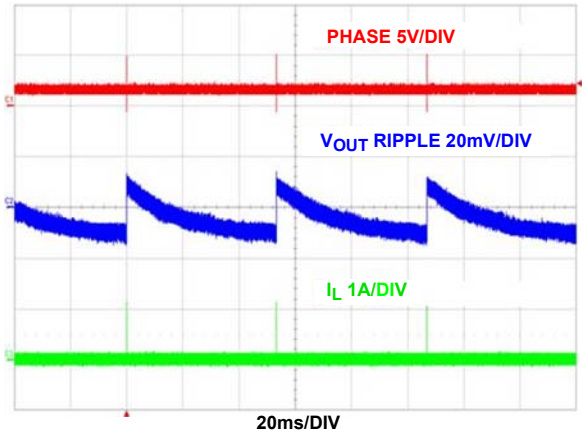


FIGURE 25. STEADY STATE AT NO LOAD PFM

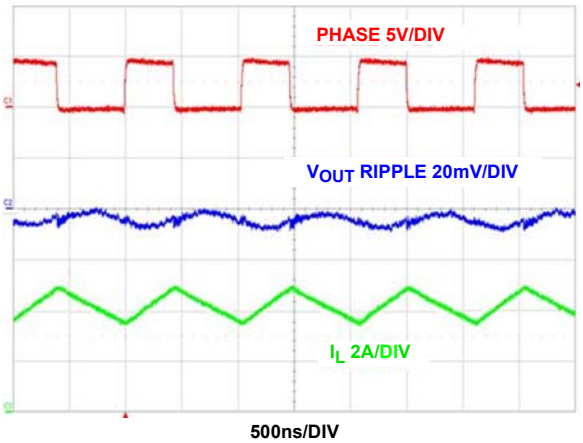
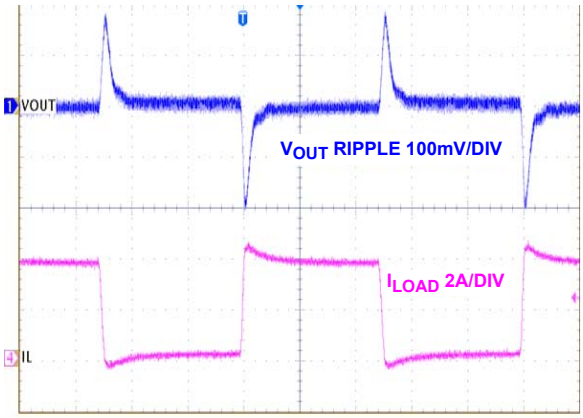


FIGURE 26. STEADY STATE AT 4A PWM

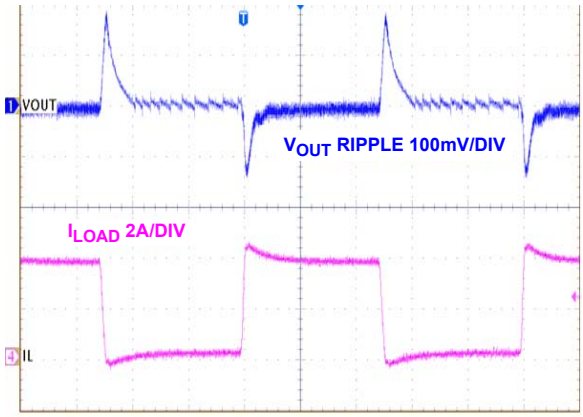
Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, SYNC = V_{IN}, L = 1.0µH, C_1 = 22µF, C_2 = 2 x 22µF, I_{OUT} = 0A to 4A. **(Continued)**



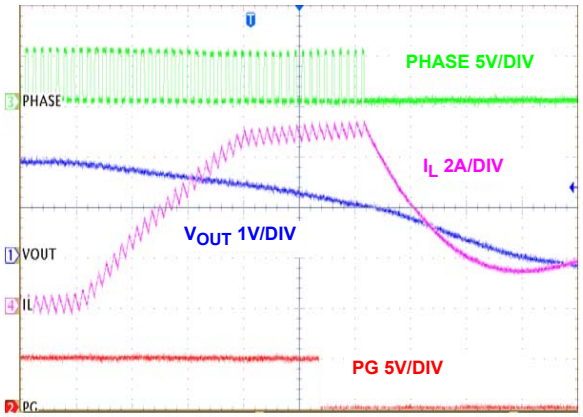
200µs/DIV

FIGURE 27. LOAD TRANSIENTS (PWM)



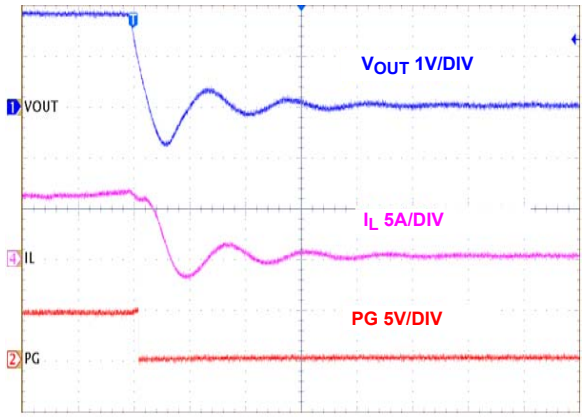
200µs/DIV

FIGURE 28. LOAD TRANSIENTS (PFM)



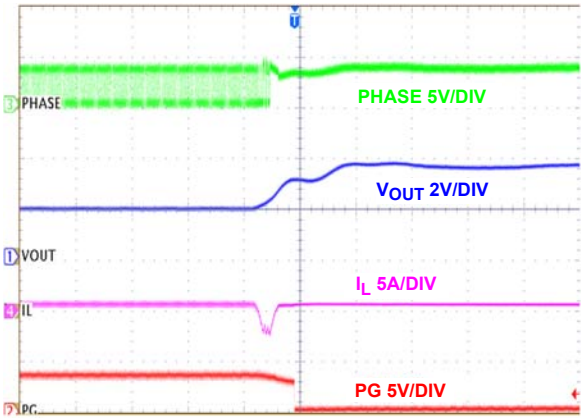
4µs/DIV

FIGURE 29. OUTPUT SHORT-CIRCUIT



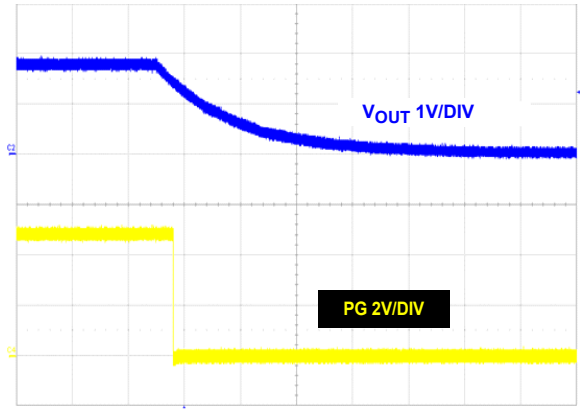
40µs/DIV

FIGURE 30. OVERCURRENT PROTECTION



20µs/DIV

FIGURE 31. OVERVOLTAGE PROTECTION



20ms/DIV

FIGURE 32. OVER-TEMPERATURE PROTECTION

Theory of Operation

The ISL78233, ISL78234 are step-down switching regulators optimized for automotive battery powered applications. The regulator operates at a 2MHz default switching frequency for high efficiency and allow smaller form factor, when FS is connected to VIN. By connecting a resistor from FS to SGND, the operational frequency adjustable range is 500kHz to 4MHz. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 45µA. The supply current is typically only 3.8µA when the regulator is shut down.

PWM Control Scheme

Pulling the SYNC pin HI (>0.8V) forces the converter into PWM mode, regardless of output current. The ISL78233, ISL78234 employs the current-mode Pulse Width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 3 on page 5 shows the Functional Block Diagram. The current loop consists of the oscillator, the PWM comparator, current-sensing circuit and the slope compensation for the current loop stability. The slope compensation is 440mV/Ts, which changes proportionally with frequency. The gain for the current-sensing circuit is typically 200mV/A. The control reference for the current loops comes from the Error Amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the PFET and turn on the N-channel MOSFET. The NFET stays on until the end of the PWM cycle. Figure 33 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 55pF and 100kΩ RC network. The maximum EAMP voltage output is precisely clamped to 2.5V.

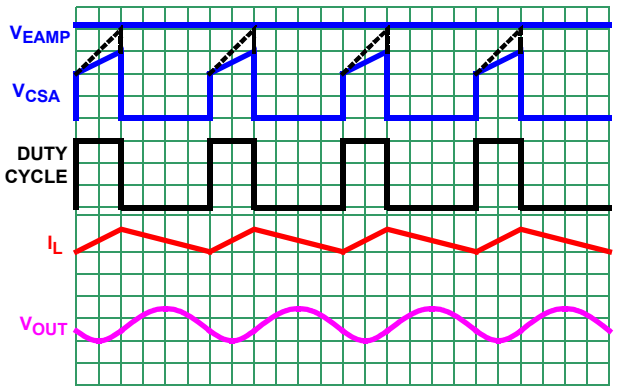


FIGURE 33. PWM OPERATION WAVEFORMS

Skip Mode

Pulling the SYNC pin LO (<0.4V) forces the converter into PFM mode. The ISL78233, ISL78234 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 34 on page 13 illustrates the Skip mode operation. A zero-cross sensing circuit shown in Figure 3 on page 5 monitors the NFET current for zero crossing. When 16 consecutive cycles are detected, the regulator enters the Skip mode. During the sixteen detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the Skip mode is entered, the pulse modulation starts being controlled by the Skip comparator shown in Figure 3 on page 5. Each pulse cycle is still synchronized by the PWM clock. The PFET is turned on at the clock's rising edge and turned off when the output is higher than 1.2% of the nominal regulation or when its current reaches the peak Skip current limit value. Then, the inductor current is discharging to 0A and stays at zero (the internal clock is disabled), and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the PFET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.2% below the nominal voltage.

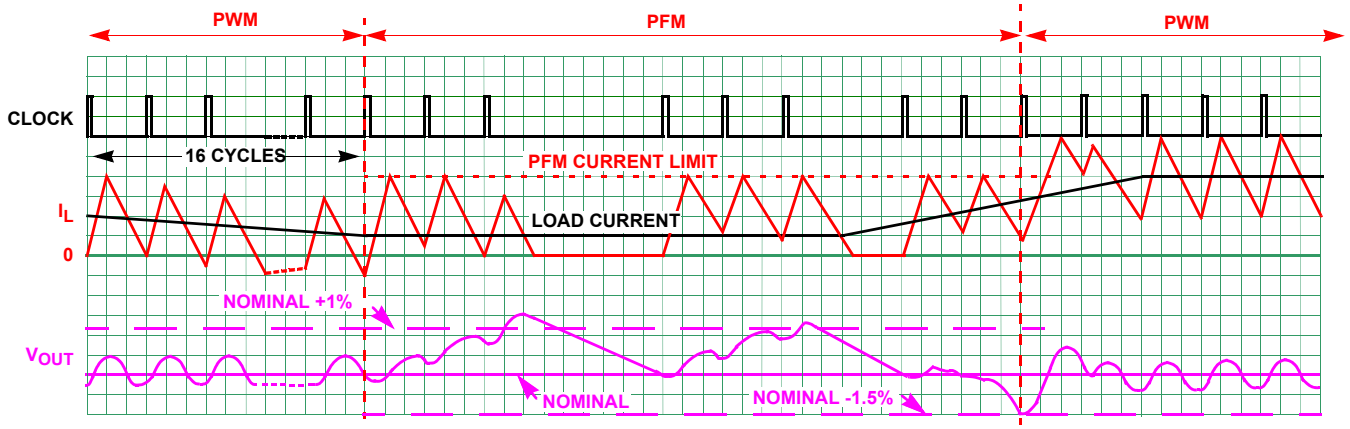


FIGURE 34. SKIP MODE OPERATION WAVEFORMS

Frequency Adjust

The frequency of operation is fixed at 2MHz when FS is tied to VIN. Adjustable frequency ranges from 500kHz to 4MHz via a simple resistor connecting FS to SGND according to Equation 1:

$$R_{FS}[k\Omega] = \frac{220 \cdot 10^3}{f_{OSC}[kHz]} - 14 \quad \text{(EQ. 1)}$$

The ISL78233, ISL78234 also has frequency synchronization capability by simply connecting the SYNC pin to an external square pulse waveform. The frequency synchronization feature will synchronize the positive edge trigger and its switching frequency up to 4MHz. The minimum external SYNC frequency is half of the free running frequency (either the default frequency or determined by the FS resistor).

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 3 on page 5. The current sensing circuit has a gain of 200mV/A, from the P-FET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripled to turn off the PFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shut down under an overcurrent fault condition. An overcurrent fault condition will result in the regulator attempting to restart in a hiccup mode within the delay of eight soft-start periods. At the end of the 8th soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of 8 soft-start periods, the output will resume back into regulation point after hiccup mode expires.

Negative Current Protection

Similar to overcurrent, the negative current protection is realized by monitoring the current across the low-side NFET, as shown in Figure 3 on page 5. When the valley point of the inductor current reaches -3A for 4 consecutive cycles, both PFET and NFET are off. The 100Ω in parallel to the NFET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The regulator will be in PFM for 20µs before switching to PWM if necessary.

PG

PG is an open-drain output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After 1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within nominal regulation voltage set by VFB. When VFB drops 15% below or raises 0.8V above the nominal regulation voltage, the ISL78233, ISL78234 pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. For logic level output voltages, connect an external pull-up resistor, R_1, between PG and VIN. A 100kΩ resistor works well in most applications.

UVLO

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the regulator is disabled.

Soft Start-Up

The soft start-up reduces the inrush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed, so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in the Skip mode to support prebiased output condition.

Tie SS to SGND for internal soft-start is approximately 1ms. Connect a capacitor from SS to SGND to adjust the soft-start time. This capacitor, along with an internal 2.1µA current source sets the soft-start interval of the converter, t_{SS} as shown by Equation 2.

$$C_{SS}[\mu F] = 3.1 \cdot t_{SS}[s] \quad \text{(EQ. 2)}$$

C_{SS} must be less than 33nF to insure proper soft-start reset after fault condition.

Enable

The Enable (EN) input allows the user to control the turning on or off of the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference and then the soft start-up begins.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the PFET is typically 35mΩ and the ON-resistance for the NFET is typically 11mΩ.

100% Duty Cycle

The ISL78233, ISL78234 features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL78233, ISL78234 can no longer maintain the regulation at the output, the regulator completely turns on the P-FET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the PFET.

Thermal Shutdown

The ISL78233, ISL78234 has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +125°C, the ISL78233, ISL78234 resumes operation by stepping through the soft-start.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, the ISL78233, ISL78234 typically uses a 1.0µH output inductor. The higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. It is recommended to set the ripple inductor current to approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 3:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 3)}$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL78233, ISL78234 protects the typical peak current 4.9A/6.7A. The saturation current needs to be over 7A for maximum output current application.

The ISL78233, ISL78234 uses an internal compensation network and the output capacitor value is dependent on the output voltage. The recommended ceramic capacitor is X5R or X7R. The recommended X5R or X7R minimum output capacitor values are shown in Table 2 on page 4.

In Table 2, the minimum output capacitor value is given for the different output voltages to make sure that the whole converter system is stable. Additional output capacitance should be added for better performance in applications where high load transient or low output ripple is required. It is recommended to check the system level performance along with the simulation model.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage, and feed it back to the inverting input of the error amplifier (see Figure 2 on page 4).

The output voltage programming resistor, R_2, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor, R_3, is typically between 10kΩ and 100kΩ, as shown in Equation 4.

$$R_2 = R_3\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 4)}$$

If the output voltage desired is 0.6V, then R_3 is left unpopulated and R_2 is shorted. There is a leakage current from VIN to PHASE. It is recommended to preload the output with 10µA minimum. For better performance, add 15pF in parallel with R_2 (200kΩ). Check loop analysis before use in application.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide a filtering function to prevent the switching current flowing back to the battery rail. At least two 22µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

Loop Compensation Design

When COMP is not connected to VDD, the COMP pin is active for external loop compensation. The ISL78233, ISL78234 uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current-sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 35 shows the small signal model of the synchronous buck regulator.

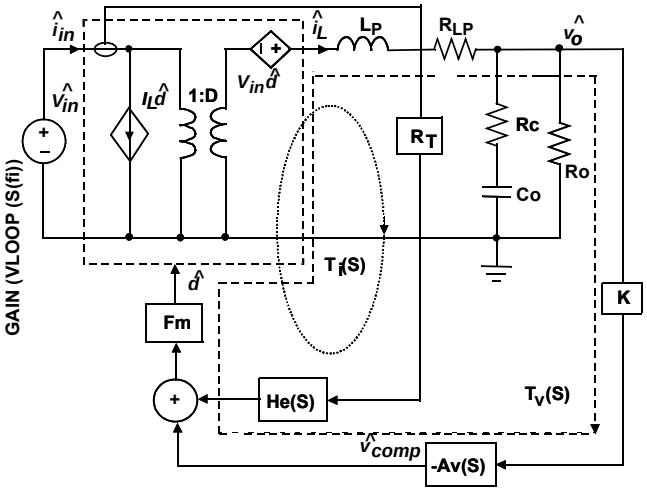


FIGURE 35. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

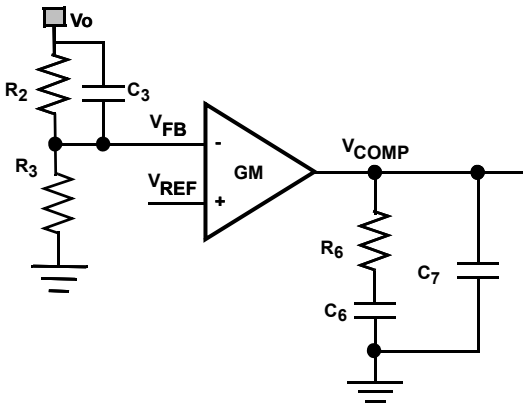


FIGURE 36. TYPE II COMPENSATOR

Figure 36 shows the type II compensator and its transfer function is expressed as Equation 5:

$$A_V(S) = \frac{\hat{v}_{comp}}{\hat{v}_{FB}} = \frac{GM \cdot R_3}{(C_6 + C_7) \cdot (R_2 + R_3)} \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp1}}\right)\left(1 + \frac{S}{\omega_{cp2}}\right)} \quad \text{(EQ. 5)}$$

Where,

$$\omega_{cz1} = \frac{1}{R_6 C_6}, \quad \omega_{cz2} = \frac{1}{R_2 C_3}, \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7}, \omega_{cp2} = \frac{R_2 + R_3}{C_3 R_2 R_3}$$

Compensator design goal:

High DC gain
Choose Loop bandwidth f_c less than 100kHz
Gain margin: >10dB
Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has a unity gain. Therefore, the compensator resistance R_6 is determined by Equation 6.

$$R_6 = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} = 17.45 \times 10^3 \cdot f_c V_o C_o \quad \text{(EQ. 6)}$$

Where GM is the sum of the transconductance, g_m, of the voltage error amplifier in each phase. Compensator capacitor C_6 is then given by Equation 7.

$$C_6 = \frac{R_o C_o}{R_6} = \frac{V_o C_o}{I_o R_6}, C_7 = \max\left(\frac{R_c C_o}{R_6}, \frac{1}{\pi f_s R_6}\right) \quad \text{(EQ. 7)}$$

Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower in Equation 7. An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_2 and C_3.

Put compensator zero 2 to 5 times f_c:

$$C_3 = \frac{1}{\pi f_c R_2} \quad \text{(EQ. 8)}$$

Example: V_{IN} = 5V, V_O = 1.8V, I_O = 4A, FS = 1MHz, R_2 = 200kΩ, R_3 = 100kΩ, C_o = 2x22µF/3mΩ, L = 1µH, f_c = 100kHz, then compensator resistance R_6:

$$R_6 = 17.45 \times 10^3 \cdot 100kHz \cdot 1.8V \cdot 44\mu F = 138k\Omega \quad \text{(EQ. 9)}$$

It is acceptable to use 137kΩ as the closest standard value for R_6.

$$C_6 = \frac{1.8V \cdot 44\mu F}{4A \cdot 137k\Omega} = 144pF \quad \text{(EQ. 10)}$$

$$C_7 = \max\left(\frac{3m\Omega \cdot 44\mu F}{137k\Omega}, \frac{1}{\pi \cdot 1MHz(137k\Omega)}\right) = (1pF, 2.3pF) \quad \text{(EQ. 11)}$$

It is also acceptable to use the closest standard values for C_6 and C_7. There is approximately 3pF parasitic capacitance from V_{COMP} to GND; Therefore, C_7 is optional. Use C_6 = 150pF and C_7 = OPEN.

$$C_3 = \frac{1}{\pi 100kHz \cdot 200k\Omega} = 16pF \quad \text{(EQ. 12)}$$

Use C_3 = 15pF. Note that C_3 may increase the loop bandwidth from previous estimated value. Figure 37 shows the simulated voltage loop gain. It is shown that it has a 150kHz loop bandwidth with a 42° phase margin and 10dB gain margin. It may be more desirable to achieve an increased phase margin. This can be accomplished by lowering R_6 by 20% to 30%.

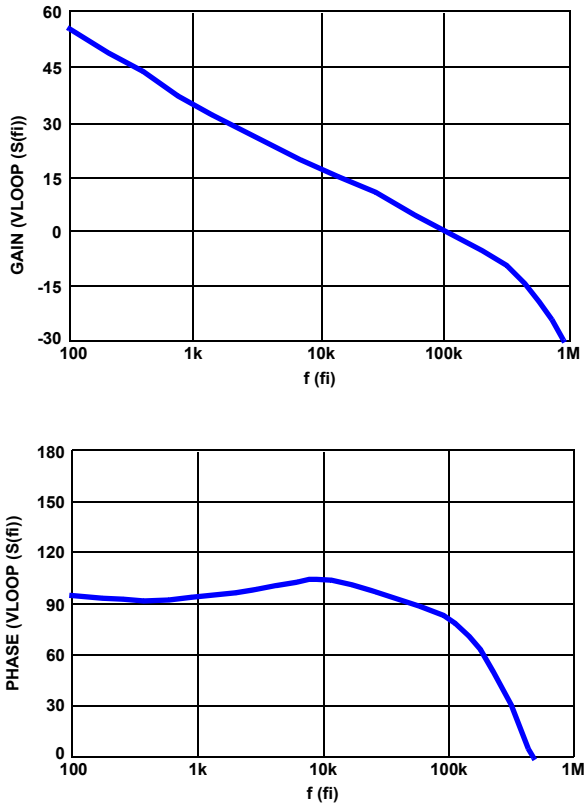


FIGURE 37. SIMULATED LOOP GAIN

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For the ISL78233, ISL78234 the power loop is composed of the output inductor L's, the output capacitor C_O, the PHASE pins and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the PHASE pins and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as close as possible to the VIN pin. The ground of the input and output capacitors should be connected as close as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. Refer to TB389 for via placement on the copper area of the PCB underneath the thermal pad for optimum thermal performance.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 4, 2015	FN8359.7	Added a new User Guide to Related Literature section on page 1. Added EVAL2 part numbers to the ordering information table on page 3. Added Table 1 on page 3.
November 10, 2015	FN8359.6	Added 5x5mmWFQFN information throughout datasheet. Updated Note 1 on page 3 from "Add "-T*" suffix for tape and reel." to "Add "-T" suffix for 6k unit or "-T7A" suffix for 250 unit tape and reel options." In "PWM Control Scheme" on page 13 (last sentence) corrected a typo by changing "1.6V to "2.5V". Table 2 on page 4: Updated L1 row. Updated the "PCB Layout Recommendation" section on page 17. Added POD L16.5x5D.
April 23, 2015	FN8359.5	Updated the 4th Features bullet page 1 by changing value from "0.8%" to "-1.2%/1%".
April 23, 2014	FN8359.4	Updated electrical table, changed Phase minimum on-time MAX from 133ns to 100ns on page 7 Updated electrical table, modified test conditions for Error Amplifier trans-conductance and Power-good Output Low Voltage on page 7 Removed references to VOUT = 0.8V, and 0.9V Added typical curve for Phase minimum on-time vs VIN on page 9 Added description on synchronized control on page 14
February 24, 2014	FN8359.3	Updated ESD rating qual references from Jedec standard references to AEC-Q100 standard references on page 6
December 13, 2013	FN8359.2	Last Features bullet on page 1: changed from "Qualified for automotive application" to "AEC-Q100 qualified"
October 16, 2013	FN8359.1	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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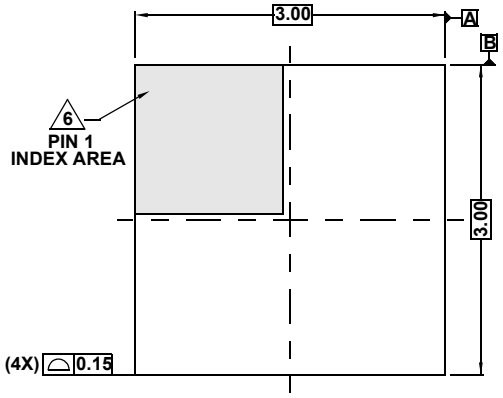
Package Outline Drawing

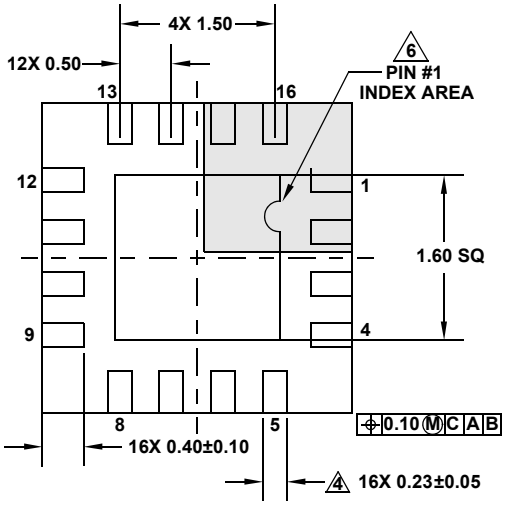
L16.3x3D

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

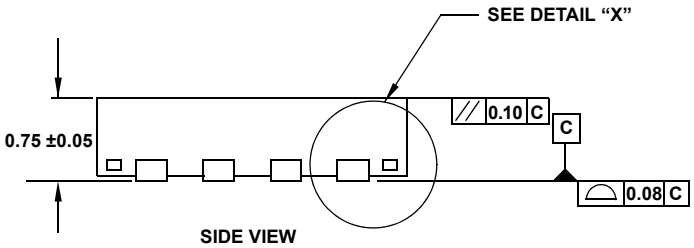
Rev 0, 3/10



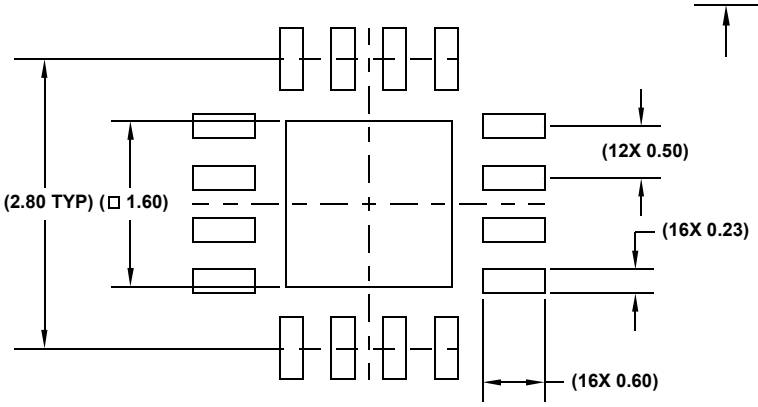
TOP VIEW



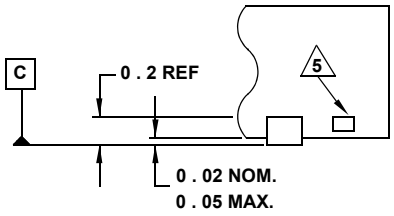
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

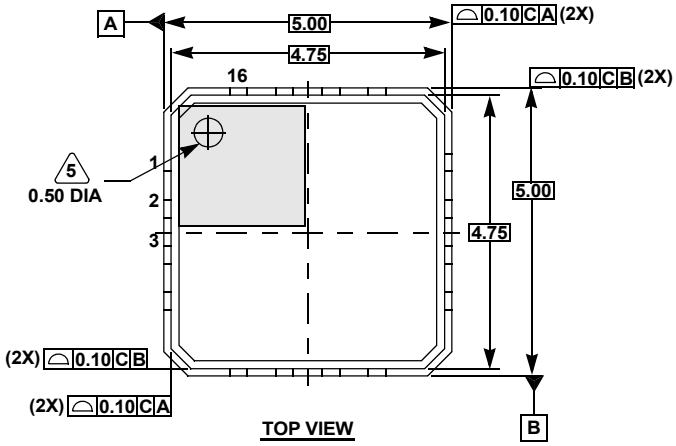
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.

Package Outline Drawing

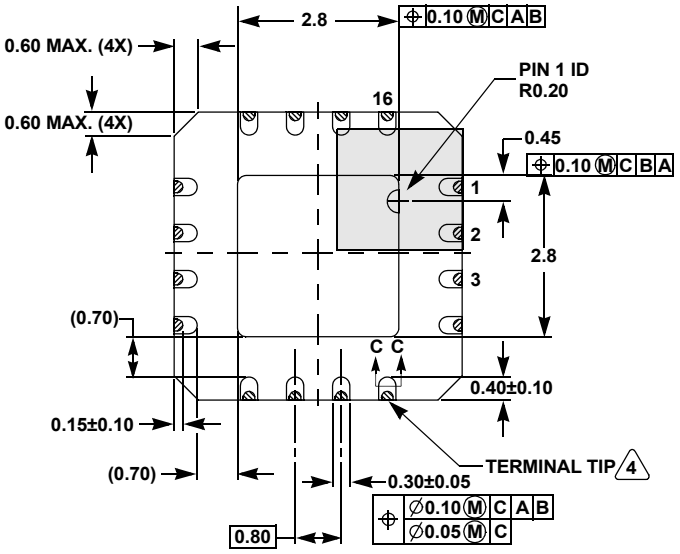
L16.5x5D

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN WITH WETTABLE FLANK)

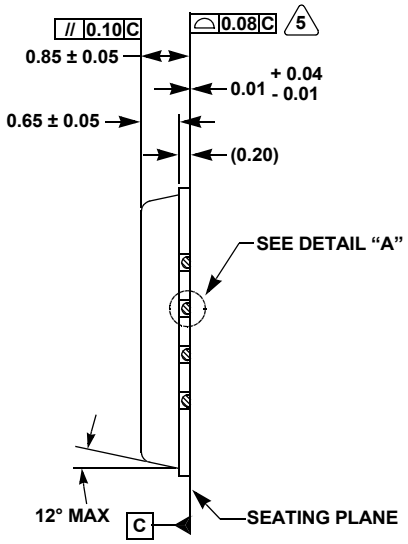
Rev 2, 5/14



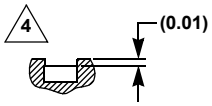
TOP VIEW



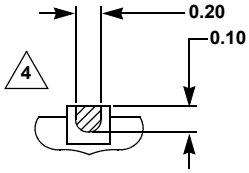
BOTTOM VIEW



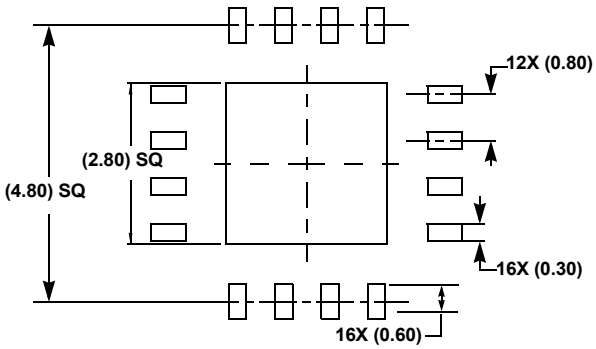
SIDE VIEW



SECTION "C-C"
SCALE: NONE



DETAIL "A" (DIMPLE DEPTH)
SCALE: NONE



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) are for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Reference document: JEDEC M0220.