19-2486; Rev 0; 7/02

MAXIM

+14dBm to +20dBm LO Buffers with ±1dB Variation

General Description

The MAX9989 and MAX9990 LO buffers provide the high output (+14dBm to +20dBm) necessary to drive the LO inputs of high-linearity passive mixers, while offering 40dB reverse isolation to prevent LO pulling. The MAX9989 is internally matched for the cellular/GSM bands, and the MAX9990 is matched for the DCS/PCS/UMTS bands.

The *Typical Application Circuit* provides a nominal +17dBm output power with ±1dB variation over supply, temperature, and input power. With two optional resistors, the output power can be precision set from +14dBm to +20dBm. The devices offer more than 35dB main driver output to PLL amp output isolation. Each device is offered in a 5mm × 5mm 20-pin thin QFN package with exposed paddle.

Applications

Cellular/GSM/DCS/PCS/UMTS Base Station Tx/Rx LO Drives

Coherent Receivers

ISM Wireless LAN

Wireless Local Loop

Local Multipoint Distribution Service

Point-to-Point Systems

Features

- ♦ **±1dB Output Power Variation**
- ♦ **+14dBm to +20dBm Adjustable Output Power**
- ♦ **40dB Reverse Isolation**
- ♦ **Better Than 35dB Main Driver Output to PLL Amp Output Isolation**
- ♦ **Low Output Noise: -170dBc/Hz at +17dBm**
- ♦ **110mA Supply Current at +17dBm**
- ♦ **ESD Protection**
- ♦ **Isolated PLL Output (+3dBm)**

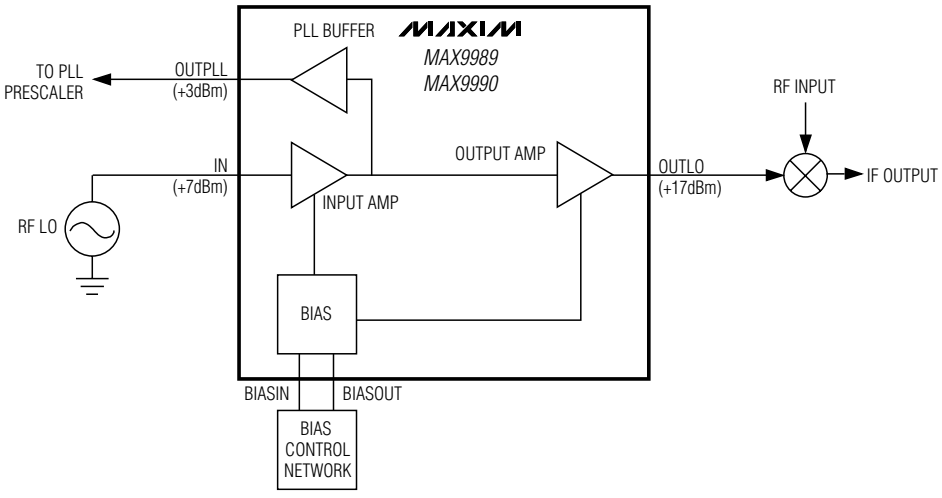
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FREQUENCY RANGE (MHz)
MAX9989ETP	-40°C to +85°C	20 Thin QFN-EP*	700 to 1100
MAX9990ETP	-40°C to +85°C	20 QFN-EP*	1500 to 2200

**EP = Exposed paddle.*

Typical Application Circuit/Pin Configuration appears at end of data sheet.

Typical Operating Circuit and Block Diagram



+14dBm to +20dBm LO Buffers with ±1dB Variation

ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2, VCC3, VCCREF to GND .....-0.3V to +6.0V
IN to GND .....-0.3V to (V_{CC} + 0.3V)
OUTLO, OUTPLL to GND .....-0.3V to (V_{CC} + 0.3V)
REF to GND .....Source/Sink 5mA
INBIAS, OUTBIAS to GND .....-0.3V to +0.75V
PLLBIAS .....Sink 25mA
RF Input Power .....+20dBm

Continuous Power Dissipation (T_A = +70°C)
20-Pin Thin QFN (derate 21mW/°C above +70°C) 1667mW
θ_{JA} .....+48°C/W
Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—MAX9989

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, input and outputs terminated in 50Ω, T_A = -40°C to +85°C. Typical specifications are for V_{CC} = 5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Supply Current	I_{CC}	Low power setting (see Table 1 for resistor values)		77		mA
		Nominal power setting (R2–R5 not installed) (Note 2)	94	105	116	
		High power setting (see Table 1 for resistor values)		146		

DC ELECTRICAL CHARACTERISTICS—MAX9990

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, input and outputs terminated in 50Ω, T_A = -40°C to +85°C. Typical specifications are for V_{CC} = 5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Supply Current	I_{CC}	Low power setting (see Table 1 for resistor values)		87		mA
		Nominal power setting (R2–R5 not installed) (Note 2)	98	111	122	
		High power setting (see Table 1 for resistor values)		154		

AC ELECTRICAL CHARACTERISTICS—MAX9989

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, 50Ω environment, +4dBm < P_{IN} < +10dBm, 700MHz < f_{IN} < 1100MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are for V_{CC} = 5.0V, P_{IN} = +7dBm, f_{IN} = 900MHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f		700		1100	MHz
Output Power	P_{OUTLO}	Low power setting, P_{IN} = +4dBm (see Table 1 for resistor values)		14.3		dBm
		Nominal power setting, +4dBm < P_{IN} < +10dBm, 4.75V < V_{CC} < 5.25V, -40°C < T_A < +85°C (R2–R5 not installed)		17.3 ±0.8		
		High power setting, P_{IN} = +10dBm (see Table 1 for resistor values)		19.7		
Output Power (PLL Driver)	P_{OUTPLL}			3.7		dBm
Input VSWR	$VSWR_{IN}$			1.2:1		
Output VSWR	$VSWR_{OUT}$			1.7:1		
Output-Noise Power Density	P_{NOISE}	V_{CC} = 5.0V, ±100MHz offset (R2–R5 not installed)		-152		dBm/Hz
OUTLO to RFIN Isolation	S12	V_{CC} = 5.0V, nominal power setting (R2–R5 not installed)		48		dB

AC ELECTRICAL CHARACTERISTICS—MAX9990

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, 50Ω environment, +6dBm < P_{IN} < +12dBm, 1500MHz < f_{IN} < 2200MHz, and T_A = -40°C to +85°C, unless otherwise noted. Typical specifications are for V_{CC} = 5.0V, P_{IN} = +9dBm, f_{IN} = 1800MHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f		1500		2200	MHz
Output Power	P_{OUTLO}	Low power setting, P_{IN} = +6dBm (see Table 1 for resistor values)		14.2		dBm
		Nominal power setting, +6dBm < P_{IN} < +12dBm, 4.75V < V_{CC} < 5.25V, -40°C < T_A < +85°C (R2–R5 not installed)		17.3 ±0.8		
		High power setting, P_{IN} = +12dBm (see Table 1 for resistor values)		19.5		
Output Power (PLL Driver)	P_{OUTPLL}			3.6		dBm
Input VSWR	$VSWR_{IN}$			1.5:1		
Output VSWR	$VSWR_{OUT}$			1.4:1		
Output-Noise Power Density	P_{NOISE}	V_{CC} = 5.0V, ±100MHz offset		-152		dBm/Hz
OUTLO to RFIN Isolation	S12	V_{CC} = 5.0V, nominal power setting (R2–R5 not installed)		49		dB

Note 1: Devices are 100% DC screened and AC production tested for functionality. Data sheet typical specifications are derived from the average of 30 units from a typical lot, and are tested under the conditions specified for the typical specifications.

Note 2: DC current limits at -40°C are guaranteed by design and characterization.

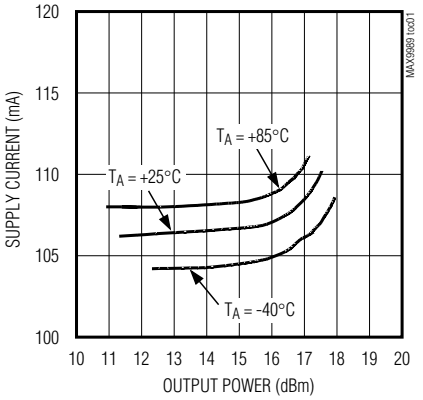
+14dBm to +20dBm LO Buffers with ±1dB Variation

Typical Operating Characteristics

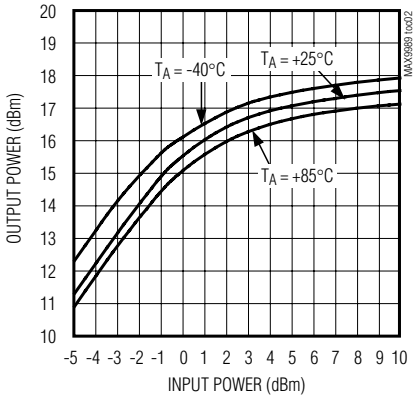
(V_{CC} = 5.0V, nominal bias, f_{IN} = 900MHz, P_{IN} = +7dBm, T_A = +25°C, unless otherwise noted.) (Shaded regions are outside the guaranteed operating range, and are provided for reference only.)

MAX9989

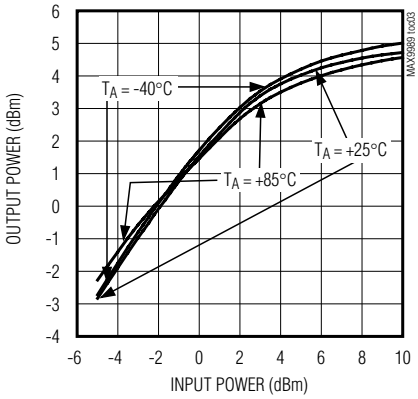
SUPPLY CURRENT vs. OUTPUT POWER OUTLO



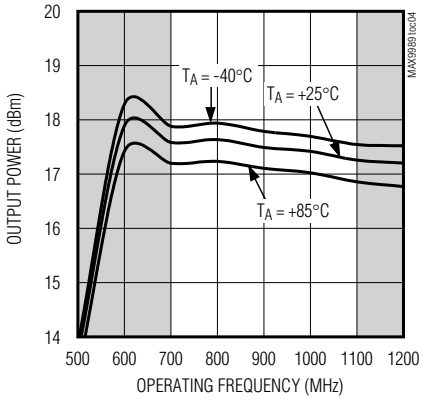
OUTPUT POWER vs. INPUT POWER OUTLO



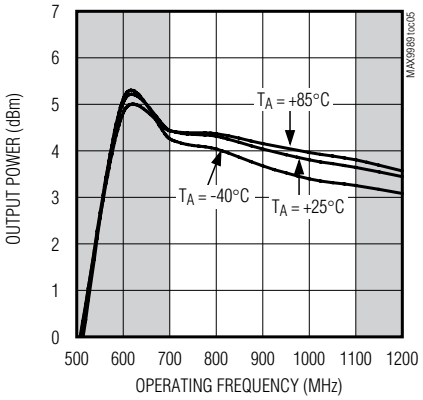
OUTPUT POWER vs. INPUT POWER OUTPLL



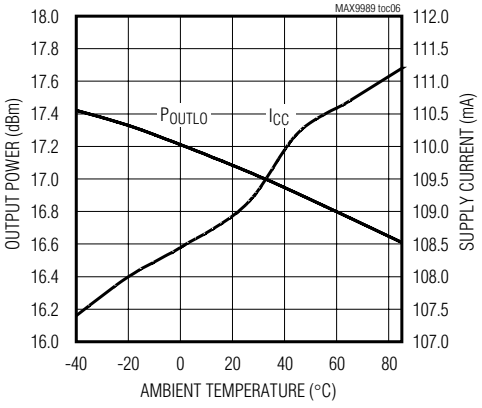
OUTPUT POWER vs. FREQUENCY OUTLO



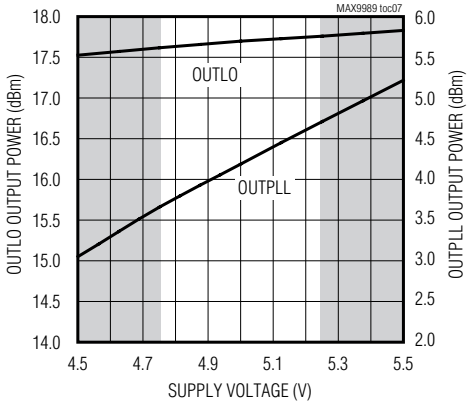
OUTPUT POWER vs. FREQUENCY OUTPLL



OUTPUT POWER AND SUPPLY CURRENT vs. TEMPERATURE



OUTPUT POWER vs. SUPPLY VOLTAGE

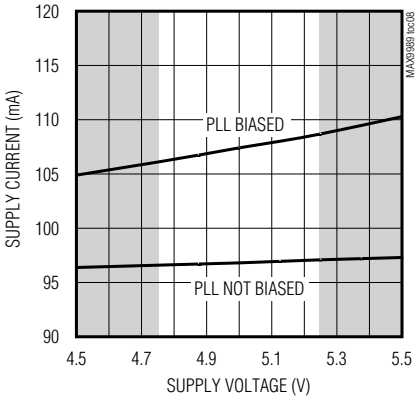


Typical Operating Characteristics (continued)

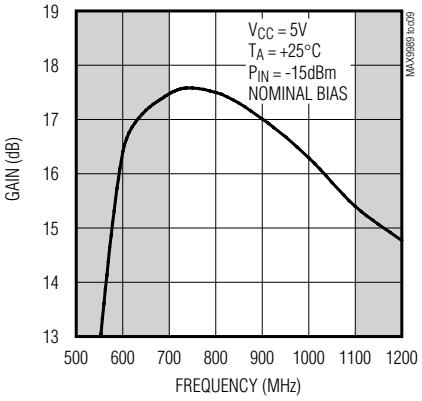
(V_{CC} = 5.0V, nominal bias, f_{IN} = 900MHz, P_{IN} = +7dBm, T_A = +25°C, unless otherwise noted.) (Shaded regions are outside the guaranteed operating range, and are provided for reference only.)

MAX9989

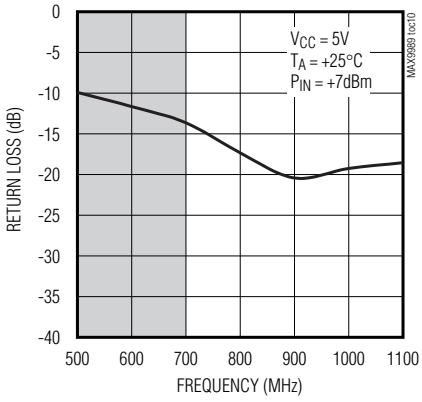
SUPPLY CURRENT vs. SUPPLY VOLTAGE



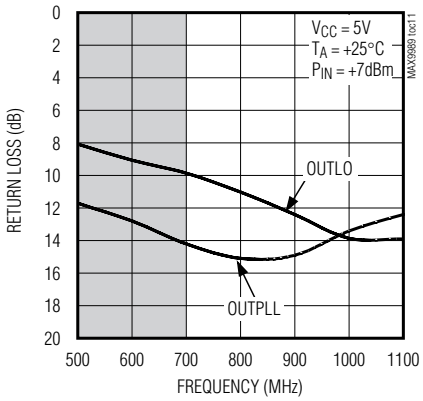
SMALL-SIGNAL GAIN vs. FREQUENCY



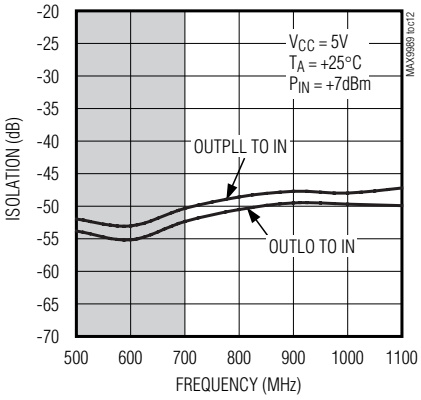
INPUT RETURN LOSS vs. FREQUENCY



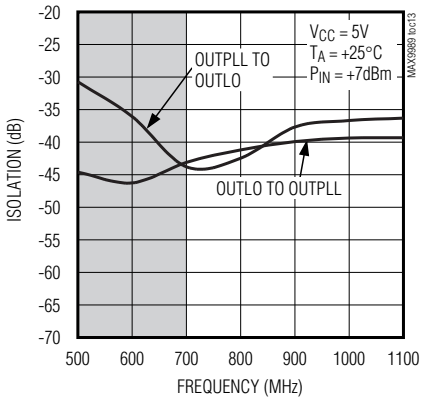
OUTPUT RETURN LOSS vs. FREQUENCY



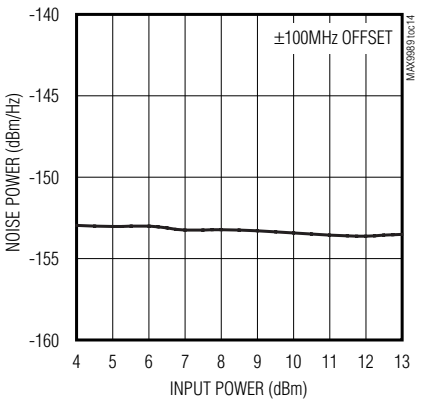
OUT-TO-IN ISOLATION vs. FREQUENCY



PLL ISOLATION vs. FREQUENCY



OUTPUT NOISE POWER vs. INPUT POWER



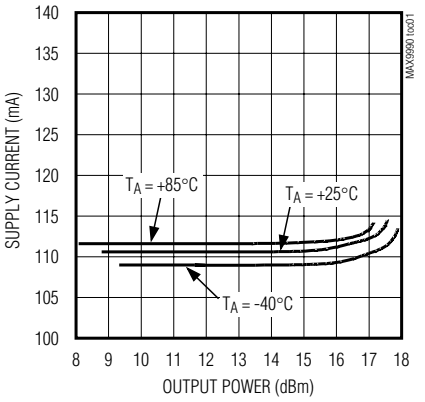
+14dBm to +20dBm LO Buffers with ±1dB Variation

Typical Operating Characteristics (continued)

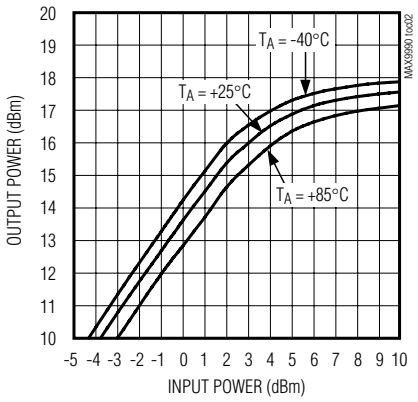
(V_{CC} = 5.0V, nominal bias, f_{IN} = 1800MHz, P_{IN} = +9dBm, T_A = +25°C, unless otherwise noted.) (Shaded regions are outside the guaranteed operating range, and are provided for reference only.)

MAX9990

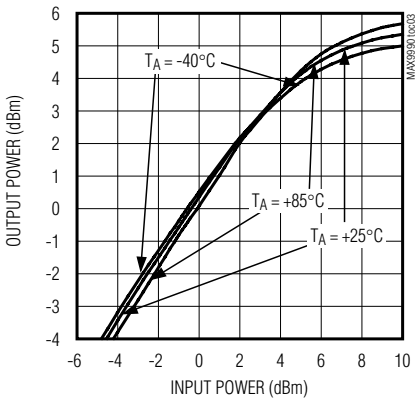
SUPPLY CURRENT vs. OUTPUT POWER OUTLO



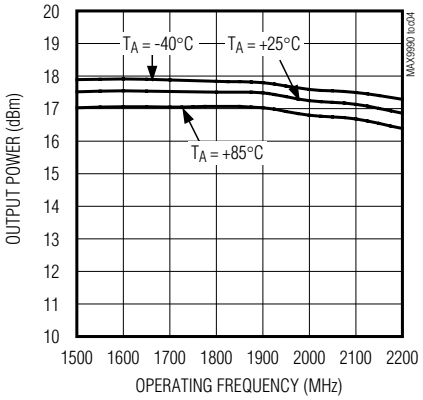
OUTPUT POWER vs. INPUT POWER OUTLO



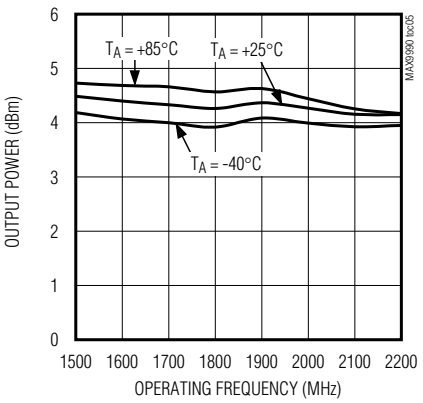
OUTPUT POWER vs. INPUT POWER OUTPLL



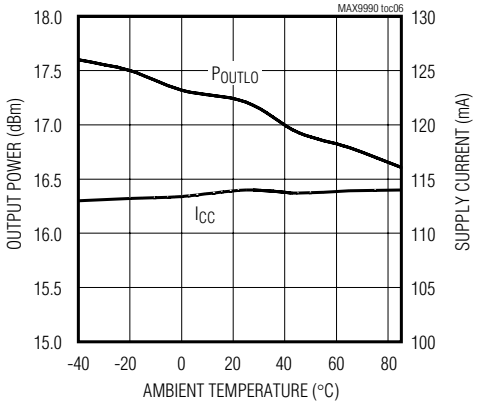
OUTPUT POWER vs. FREQUENCY OUTLO



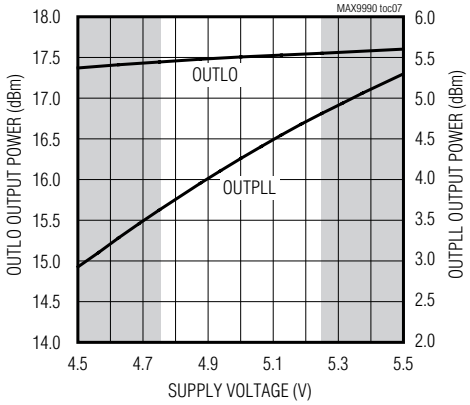
OUTPUT POWER vs. FREQUENCY OUTPLL



OUTPUT POWER AND SUPPLY CURRENT vs. TEMPERATURE



OUTPUT POWER vs. SUPPLY VOLTAGE

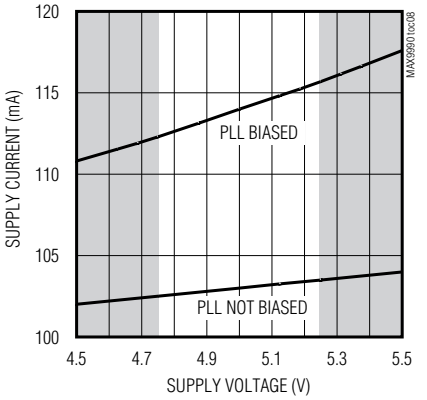


Typical Operating Characteristics (continued)

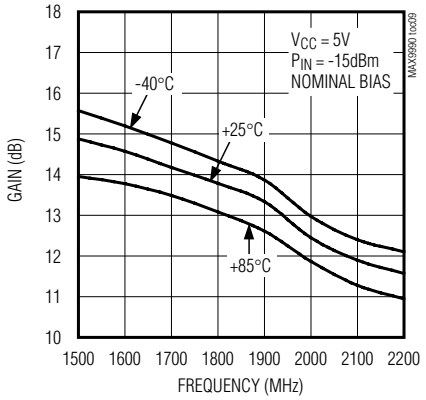
(V_{CC} = 5.0V, nominal bias, f_{IN} = 1800MHz, P_{IN} = +9dBm, T_A = +25°C, unless otherwise noted.) (Shaded regions are outside the guaranteed operating range, and are provided for reference only.)

MAX9990

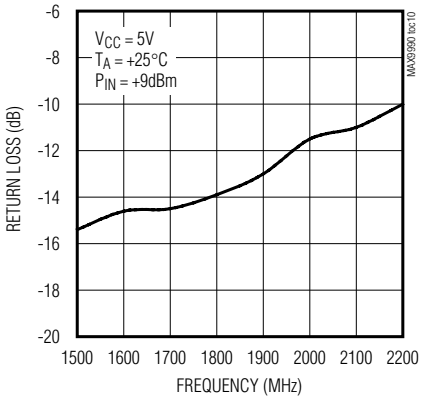
SUPPLY CURRENT vs. SUPPLY VOLTAGE



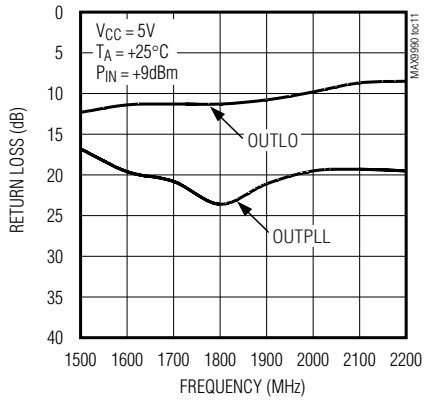
SMALL-SIGNAL GAIN vs. FREQUENCY OUTLO



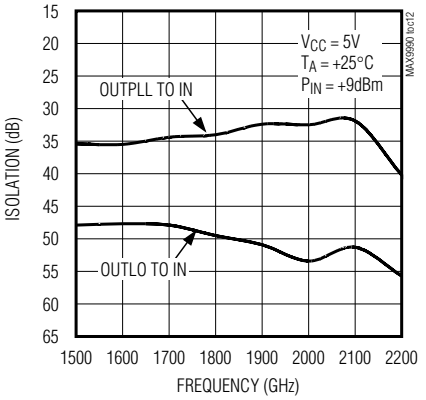
INPUT RETURN LOSS vs. FREQUENCY



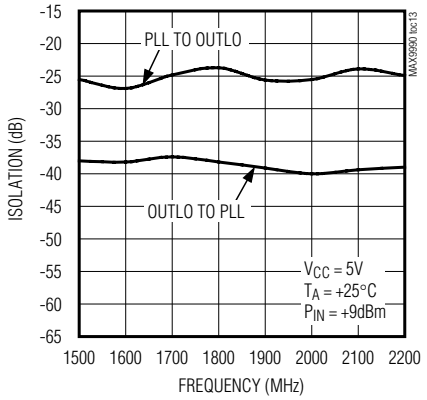
OUTPUT RETURN LOSS vs. FREQUENCY



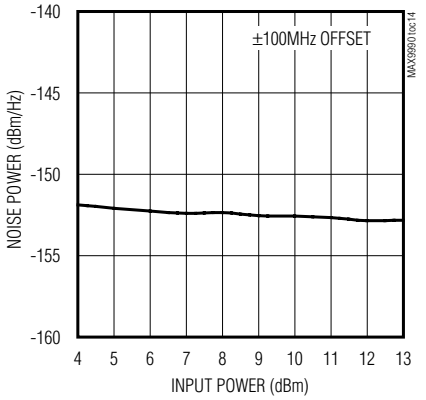
OUT-TO-IN ISOLATION vs. FREQUENCY



PLL ISOLATION vs. FREQUENCY



OUTPUT NOISE POWER vs. INPUT POWER



+14dBm to +20dBm LO Buffers with ±1dB Variation

Pin Description

PIN	NAME	FUNCTION
1, 4, 8, 9, 13–18, EP	GND	Ground. Provide 5–10 plated vias from EP to system ground plane for optimal thermal and RF performance.
2	IN	Input. Internally matched 50Ω RF input. AC couple to this pin so as not to disturb input bias level.
3	VCCREF	Supply. Supply connection for on-chip voltage and current references. See *Applications Information* for information on decoupling.
5	REF	Voltage Reference Output. Output for on-chip 1.5V bandgap voltage reference. See the *Applications Information* section for information on decoupling.
6	BIASIN	Bias Connection for Input Buffer. Set compressed power point for input amplifier with a resistor to REF or GND. For +17dBm output power, no external biasing resistors are required. See the *Applications Information* section for more information.
7	BIASOUT	Bias Connection for LO Output Amplifier. Set compressed power point for OUTLO with a resistor to REF or ground. For +17dBm output power, no external biasing resistors are required. See the *Applications Information* section for more information.
10	OUTLO	LO Output. Internally matched 50Ω RF output. AC couple to this pin so as not to disturb output bias level.
11, 12	VCC2	Supply. Supply connection for OUTLO.
19	VCC1	Supply. Supply connection for input amplifier.
20	OUTPLL	PLL Output. Output for driving optional external PLL. Requires external 100Ω pullup to V_{CC} for bias. For applications not requiring the PLL driver, removing R1 leaves OUTPLL unbiased, saving about 12mA current.

Detailed Description

The MAX9989/MAX9990 LO buffers each consist of a single-input amplifier, an output amplifier, and a second buffer amplifier to drive the LO's PLL. The bias currents for the amplifiers are adjustable through off-chip resistors, allowing the output level to be precision set anywhere from +14dBm to +20dBm. The PLL output is preset to +3dBm (about 900mV_{P-P} into 50Ω).

Power levels are typically ±1dB over the full supply, input power, and temperature range. Precision power control is achieved by internal control circuitry. Maintaining tight power control keeps the system engineer from over specifying the LO drive in order to guarantee a linearity specification in the base-station mixer. More than 40dB isolation between the LO output and the input prevents VCO pulling.

The MAX9989 is specified from 700MHz to 1100MHz, and the MAX9990 is specified from 1500MHz to 2200MHz. Both are offered in compact 5mm × 5mm 20-pin QFN thin packages with EP.

Input Amplifier

A single low-noise input amplifier provides gain and isolation. The compressed output power for this stage is controlled by the bias setting resistors R2 or R4 (see the *Typical Application Circuit*). These resistors are not required for the nominal +17dBm output; see Table 1 for bias resistor values to obtain +14dBm to +20dBm output power.

The input is internally matched to 50Ω, and typical VSWR is no more than 2:1 over all operating conditions. Since the input is internally biased, provide a DC block at the input pin.

PLL Amplifier and Output

A small amount of power is tapped off from the input amplifier's output, and fed to a high-isolation buffer to drive the PLL output at about +3dBm. If the PLL output is not required, it can be disabled by removing R1; disabling the PLL output saves 12mA supply current.

Table 1. External Resistor Values for +14dBm to +20dBm Output Power

NOMINAL OUTPUT POWER (dBm)	R2 (kΩ)	R4 (kΩ)	R3 (kΩ)	R5 (kΩ)	MAX9989 INPUT DRIVE (dBm)	MAX9990 INPUT DRIVE (dBm)
+20	1.35	Open	2.0	Open	10 ±3	12 ±3
+19	2.2	Open	3.0	Open	9 ±3	11 ±3
+18	5.0	Open	6.0	Open	8 ±3	10 ±3
+17	Open	Open	Open	Open	7 ±3	9 ±3
+16	Open	1.8	Open	3.0	6 ±3	8 ±3
+15	Open	0.9	Open	1.1	5 ±3	7 ±3
+14	Open	0.6	Open	0.6	4 ±3	6 ±3

Table 2. Component Values for Typical Application Circuit

DESIGNATION	COMPONENT VALUE	
	MAX9989 (LOWBAND)	MAX9990 (HIGHBAND)
C1, C2, C4, C6, C8, C9, C10	47pF	22pF
C3, C7, C11	0.1µF	0.1µF
C5	5pF	22pF
R2–R5	See Table 1	See Table 1
R1	100Ω	100Ω

Output Amplifier

The output amplifier is similar to the input amplifier, except it is biased higher to provide more output power. For example, with an input power of +10dBm, the MAX9989 can deliver +20dBm. The bias is adjustable; see Table 1 for details.

The RF output is internally matched to 50Ω, with a typical VSWR limit of 2:1. Provide DC-blocking capacitors at the outputs.

Applications Information

Input and Output Matching

All input and output matching is accomplished on chip; no external matching circuitry is required. Use a DC block of about 47pF (low band) or 22pF (high band) at the input and the outputs. Because these parts are internally broadband matched, adjusting external component values can optimize performance for a particular band.

Input Drive Level

In the case of the MAX9989, the typical required input drive level is +7dBm for +17dBm output, or +10dBm for +20dBm output. The MAX9990 uses slightly higher input levels (see Table 1). The typical VCO cannot provide sufficient drive by itself; the typical application follows the VCO with attenuation (about +3dB), and then with a low-noise gain block. This allows the VCO to drive the MAX9989/MAX9990 input at the required level without being load-pulled.

Output Drive Level

The output drive of the MAX9989/MAX9990 is nominally +17dBm ±1dB. This is the typical application, with no external bias-setting resistors at INBIAS and OUTBIAS. Output power can be set from +14dBm to +20dBm by using the bias-setting resistor values listed in Table 1.

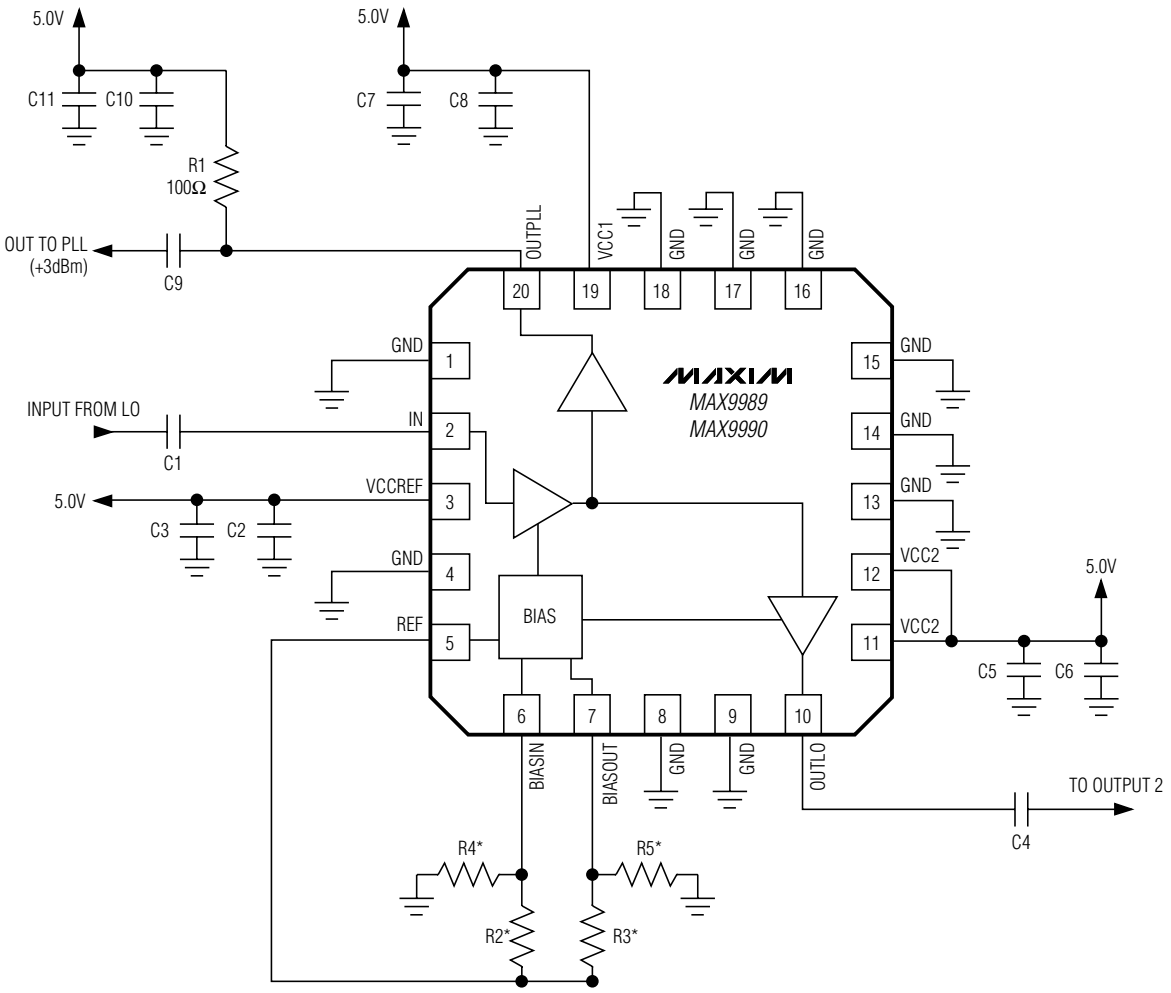
Chip Information

TRANSISTOR COUNT: 89

PROCESS: BiCMOS

+14dBm to +20dBm LO Buffers with ±1dB Variation

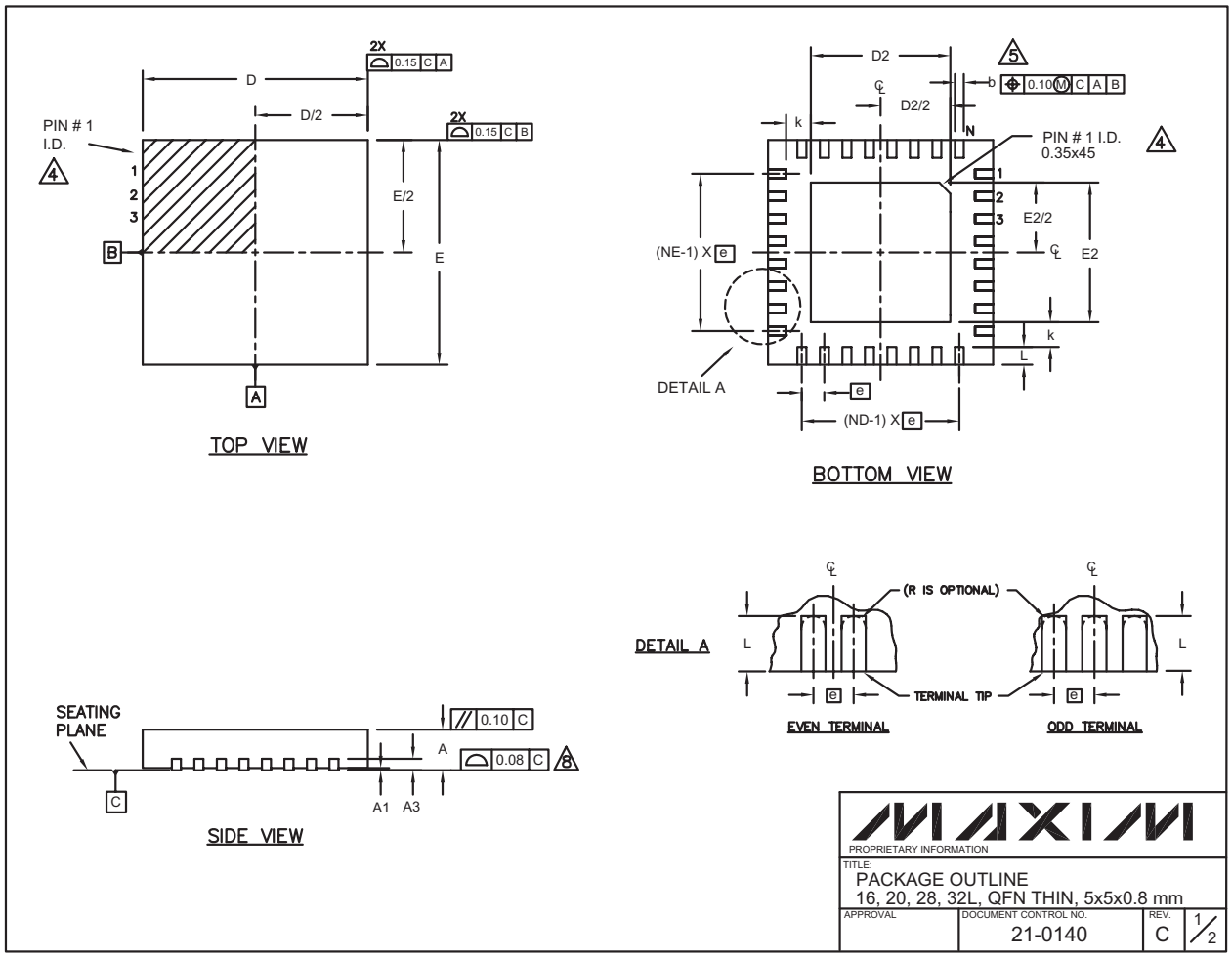
Typical Application Circuit/Pin Configuration



+14dBm to +20dBm LO Buffers with ±1dB Variation

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



+14dBm to +20dBm LO Buffers with ±1dB Variation

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	C	2/2