P3P623S00B, P3P623S00E

Product Preview

Timing-Safe™ Peak EMI Reduction IC

ON Semiconductor®

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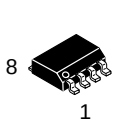
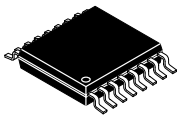


SOIC−8 NB
CASE 751



TSSOP−16
CASE 948AN

Functional Description

P3P623S00B/E is a versatile, 3.3 V Zero−delay buffer designed to distribute Timing−Safe clocks with Peak EMI reduction. P3P623S00B is an eight−pin version, accepts one reference input and drives out one low−skew Timing−Safe clock. P3P623S00E accepts one reference input and drives out eight low−skew Timing−Safe clocks.

P3P623S00B/E has an SS% that selects 2 different Deviation and associated Input−Output Skew (T_{SKEW}). Refer to the *Spread Spectrum Control* and *Input−Output Skew* table for details.

P3P623S00E has a CLKOUT for adjusting the Input−Output clock delay, depending upon the value of capacitor connected at this pin to GND.

P3P623S00B/E operates from a 3.3 V supply and is available in two different packages, as shown in the ordering information table.

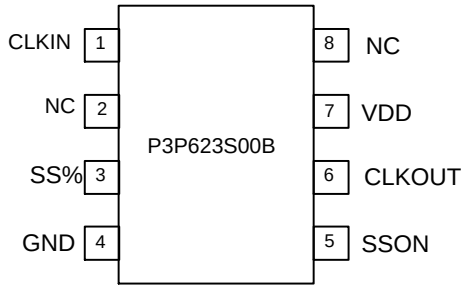
Application

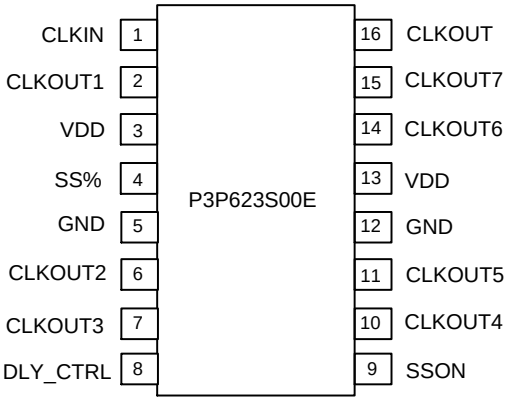
P3P623S00B/E is targeted for use in Displays and memory interface systems.

General Features

- Clock Distribution with Timing−Safe Peak EMI Reduction
- Input Frequency Range: 20 MHz − 50 MHz
- 2 Different Spread Selection Options
- Spread Spectrum can be Turned ON/OFF
- External Input−Output Delay Control Option
- Supply Voltage: 3.3 V ± 0.3 V
- P3P623S00B: 8 Pin SOIC
  P3P623S00E: 16 Pin TSSOP
- The First True Drop−in Solution
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

PIN CONFIGURATION





This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

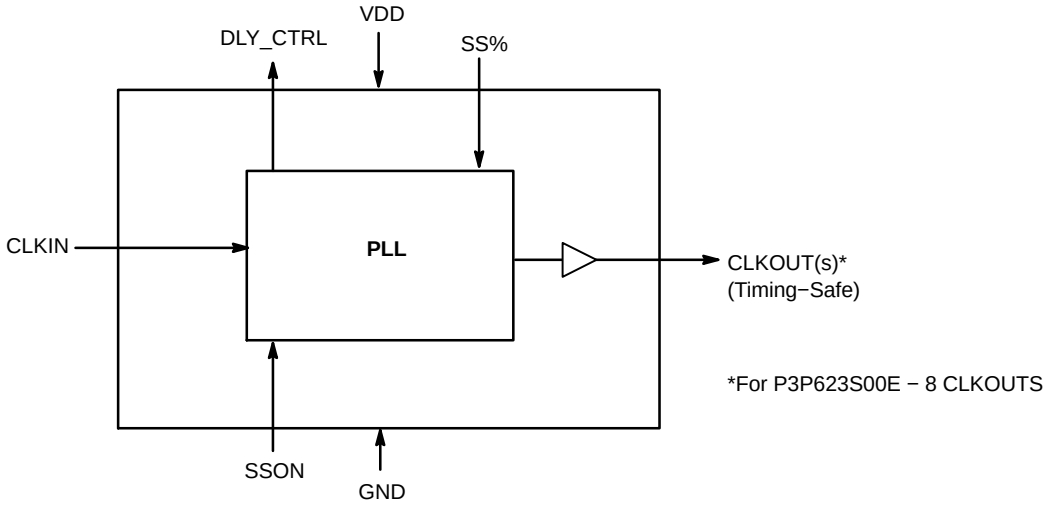


Figure 1. General Block Diagram

Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi−layer PCBs, etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The P3P623S00B/E uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation.

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input−output delay.

For applications requiring zero input−output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero input−output delay.

Timing−Safe Technology

Timing−Safe technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Table 1. PIN DESCRIPTION FOR P3P623S00B

Pin #	Pin Name	Type	Description
1	CLKIN (Note 1)	Input	External reference Clock input, 5 V tolerant input
2	NC		No Connect
3	SS% (Note 3)	Input	Spread Spectrum Selection. Has an internal pull up resistor
4	GND	Power	Ground
5	SSON (Note 3)	Input	Spread Spectrum enable and disable option. When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum. Has an internal pull up resistor
6	CLKOUT (Note 2)	Output	Buffered clock output (Note 4)
7	VDD	Power	3.3 V supply
8	NC		No Connect

1. Weak pull down
2. Weak pull−down on all outputs
3. Weak pull−up on these inputs
4. Buffered clock output is Timing−Safe

Table 2. PIN DESCRIPTION FOR P3P623S00E

Pin #	Pin Name	Type	Description
1	CLKIN (Note 1)	Input	External reference Clock input, 5 V tolerant input
2	CLKOUT1 (Note 2)	Output	Buffered clock output (Note 4)
3	V_{DD}	Power	3.3 V supply
4	SS% (Note 3)	Input	Spread Spectrum Selection. Refer to the *Spread Spectrum Control* and *Input−Output Skew* Table. Has an internal pull up resistor.
5	GND	Power	Ground
6	CLKOUT2 (Note 2)	Output	Buffered clock output (Note 4)
7	CLKOUT3 (Note 2)	Output	Buffered clock output (Note 4)
8	DLY_CTRL	Output	External Input−Output Delay control
9	SSON (Note 3)	Input	Spread Spectrum enable and disable option. When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum. Has an internal pull up resistor.
10	CLKOUT4 (Note 2)	Output	Buffered clock output (Note 4)
11	CLKOUT5 (Note 2)	Output	Buffered clock output (Note 4)
12	GND	Power	Ground
13	V_{DD}	Power	3.3 V supply
14	CLKOUT6 (Note 2)	Output	Buffered clock output (Note 4)
15	CLKOUT7 (Note 2)	Output	Buffered clock output (Note 4)
16	CLKOUT (Note 2)	Output	Buffered clock output (Note 4)

1. Weak pull down
2. Weak pull−down on all outputs
3. Weak pull−up on these inputs
4. Buffered clock output is Timing−Safe

Table 3. SPREAD SPECTRUM CONTROL AND INPUT−OUTPUT SKEW

Device	Input Frequency	SS %	Deviation	Input−Output Skew ($\pm T_{SKEW}$)
P3P623S00B/E	32 MHz	0	±0.25%	0.125
		1	±0.50%	0.25

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage to Ground Potential	−0.5 to +4.6	V
VIN	DC Input Voltage (CLKIN)	−0.5 to +7	
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Operating Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	−40	+85	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Table 6. ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage (Note 5)				0.8	V
V_{IH}	Input High Voltage (Note 5)		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0 V			50	μA
I_{IH}	Input HIGH Current	V_{IN} = VDD			100	μA
V_{OL}	Output LOW Voltage (Note 6)	I_{OL} = 8 mA			0.4	V
V_{OH}	Output HIGH Voltage (Note 6)	I_{OH} = −8 mA	2.4			V
I_{DD}	Supply Current	Unloaded outputs			27	mA
Z_O	Output Impedance			23		Ω

5. CLKIN input has a threshold voltage of VDD/2
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 7. SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Units
Input Frequency		20		50	MHz
Output Frequency	30 pF load	20		50	MHz
Duty Cycle (Notes 7, 8) = (t_2/ t_1) x 100	Measured at VDD/2	40	50	60	%
Output Rise Time (Notes 7, 8)	Measured between 0.8 V and 2.0 V			2.5	nS
Output Fall Time (Notes 7, 8)	Measured between 2.0 V and 0.8 V			2.5	nS
Output−to−Output Skew (Notes 7, 8)	All outputs equally loaded with SSOFF			250	pS
Delay, CLKIN Rising Edge to CLKOUT Rising Edge (Note 8)	Measured at VDD/2 with SSOFF			±350	pS
Device−to−Device Skew (Note 8)	Measured at VDD/2 on the CLKOUT pins of the device			700	pS
Cycle−to−Cycle Jitter (Notes 7, 8)	Loaded outputs			±250	pS
PLL Lock Time (Note 8)	Stable power supply, valid clock presented on CLKIN pin			1.0	mS

7. All parameters specified with 30 pF loaded outputs.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

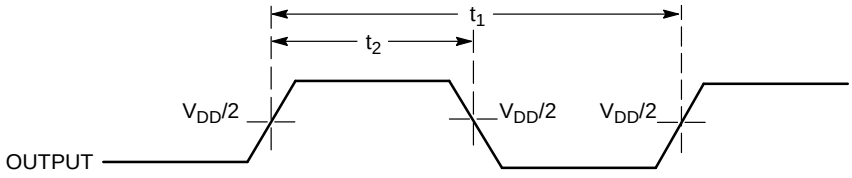


Figure 2. Duty Cycle Timing

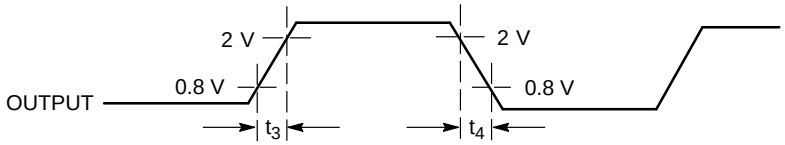


Figure 3. All Outputs Rise/Fall Time

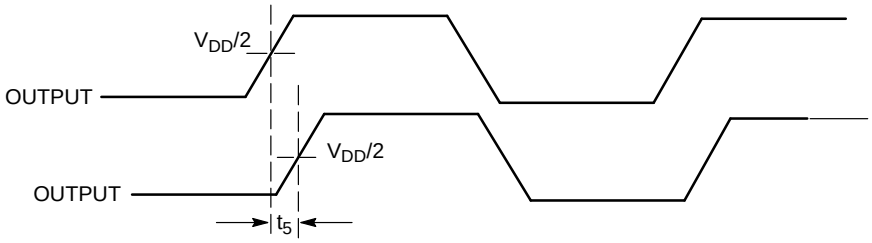


Figure 4. Output−Output Skew

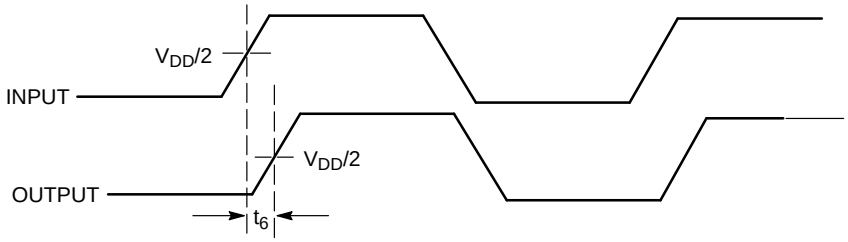


Figure 5. Input−Output Propagation Delay

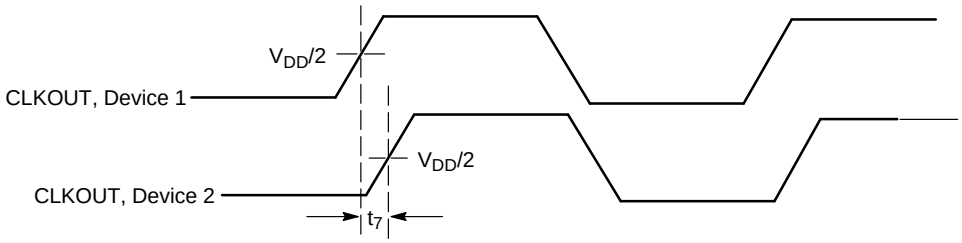


Figure 6. Device−Device Skew

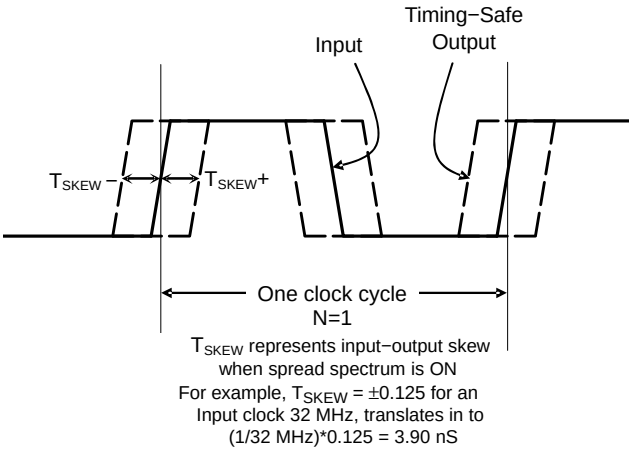


Figure 7. Input−Output Skew

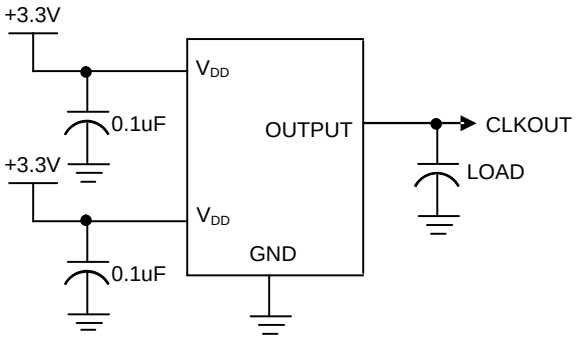


Figure 8. Test Circuit

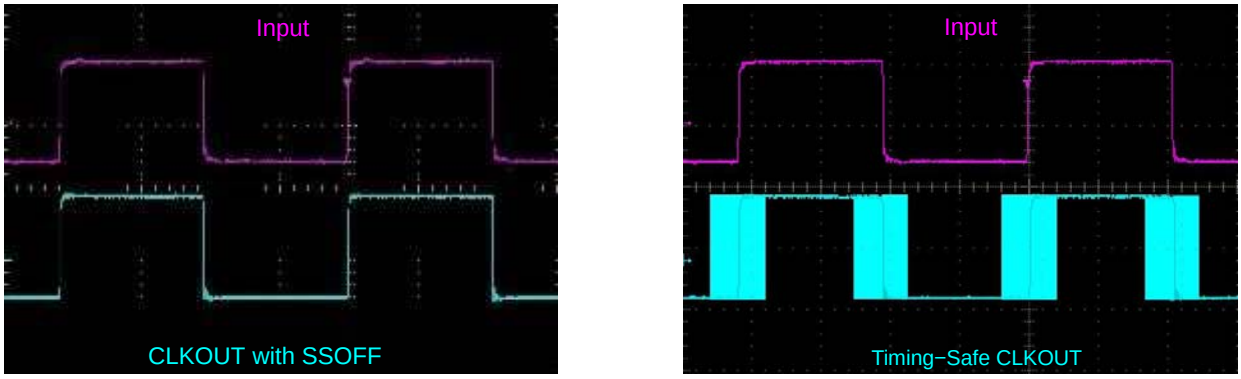
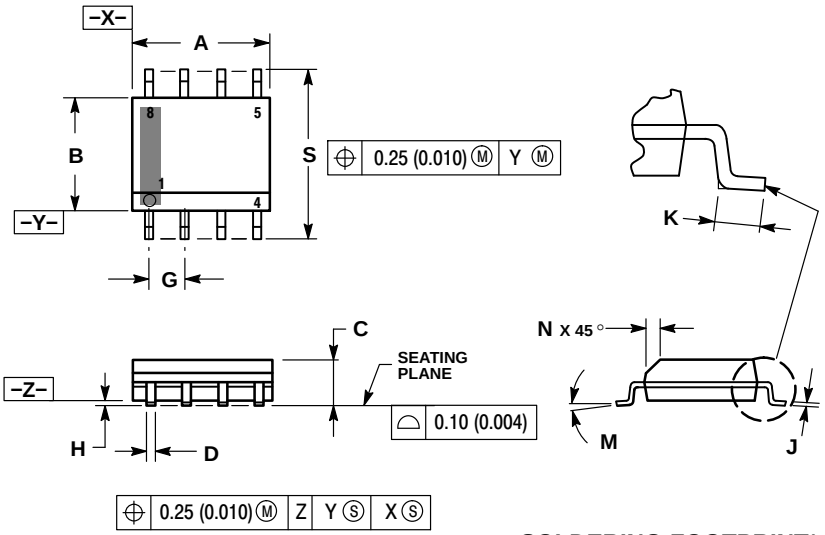


Figure 9. Typical Example of Timing−Safe Waveform

PACKAGE DIMENSIONS

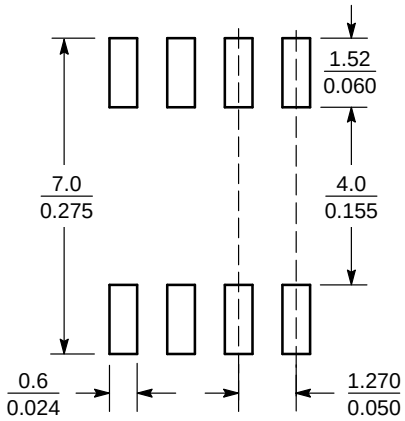
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

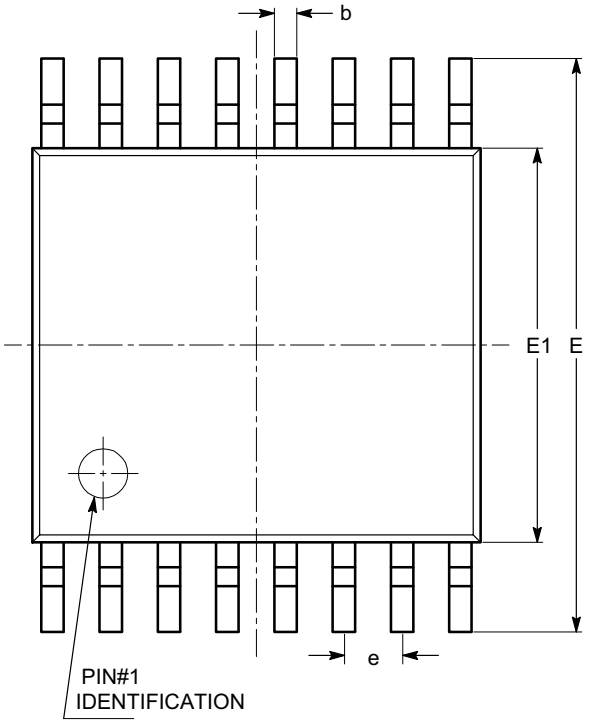


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

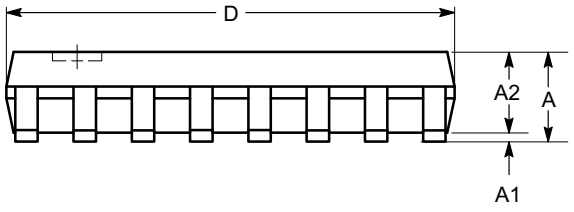
PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN
ISSUE O

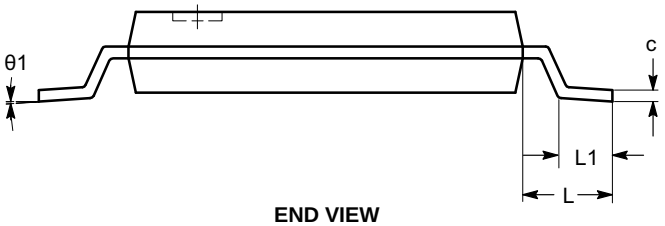


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Table 8. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
P3P623S00BG−08SR	ADO	8−pin 150−mil SOIC − TAPE & REEL, Green	0°C to +70°C
P3P623S00BG−08TR	ADO	8−pin 4.4 mm TSSOP − TAPE & REEL, Green	0°C to +70°C
P3I623S00BG−08TR	ADP	8−pin 4.4 mm TSSOP − TAPE & REEL, Green	−40°C to +85°C
P3P623S00EG−16TR	P623 S00E	16−Pin TSSOP − TAPE & REEL, Green	0°C to +70°C

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

TIMING SAFE is a trademark of Semiconductor Components Industries, LLC (SCILLC).

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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For additional information, please contact your local Sales Representative

P3P623S00/D