



# KSZ8061RNB/RND

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## 10BASE-T/100BASE-TX Physical Layer Transceiver

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### Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Quiet-WIRE<sup>®</sup> technology to reduce line emissions and enhance immunity
- Ultra-Deep Sleep standby mode
- AEC-Q100 Grade 2 Automotive Qualified

### Target Applications

- Industrial Control
- Vehicle On-Board Diagnostics (OBD)
- Automotive Gateways
- Camera and Sensor Networking
- Infotainment

### Key Benefits

- Quiet-WIRE Programmable EMI Filter
- RMII Interface with MDC/MDIO Management Interface for Register Configuration
- On-Chip Termination Resistors for Differential Pairs
- LinkMD<sup>®</sup>+ Receive Signal Quality Indicator
- Fast Start-Up and Link
- Ultra Deep Sleep Standby Mode; CPU or Signal Detect Activated.
- Loopback Modes for Diagnostics
- Programmable Interrupt Output

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# KSZ8061RNB/RND

## 1.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 1-1: 32-QFN PIN ASSIGNMENT (TOP VIEW)

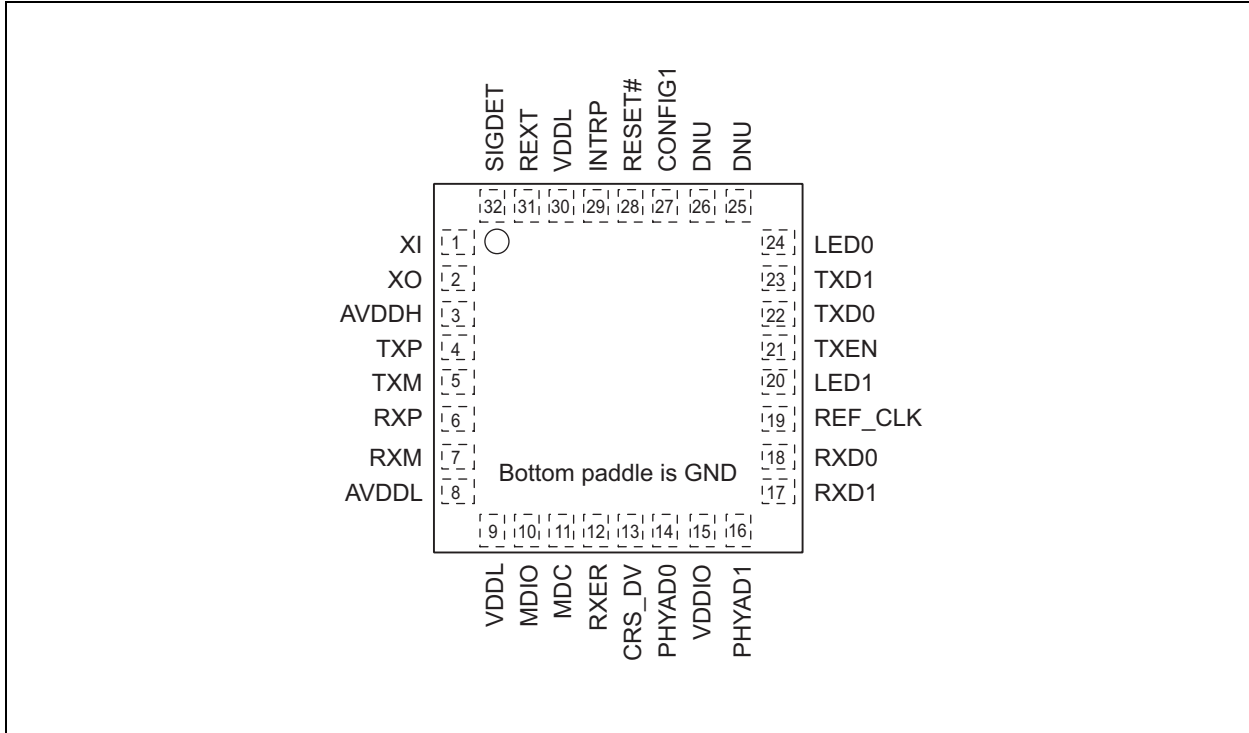


TABLE 1-1: SIGNALS

| Pin Number | Name  | Buffer Type<br>Note 1-1 | Description   |
|------------|-------|-------------------------|---|
| 1          | XI    | I                       | KSZ8061RNB: 25 MHz Crystal/Oscillator/External Clock Input. This input references the AVDDH power supply.                 |
|            |       |                         | KSZ8061RND: 50 MHz RMI Reference Clock Input. This input references the AVDDH power supply.                               |
| 2          | XO    | O                       | KSZ8061RNB: Crystal feedback for 25 MHz crystal. This pin is a no connect if oscillator or external clock source is used. |
|            |       |                         | KSZ8061RND: This pin is unused. Leave it unconnected.   |
| 3          | AVDDH | PWR                     | 3.3V Supply for analog TX drivers and XI/XO oscillator circuit.   |
| 4          | TXP   | I/O                     | Physical transmit or receive signal (+ differential)<br>Transmit when in MDI mode; Receive when in MDI-X mode.            |
| 5          | TXM   | I/O                     | Physical transmit or receive signal (- differential)<br>Transmit when in MDI mode; Receive when in MDI-X mode.            |
| 6          | RXP   | I/O                     | Physical receive or transmit signal (+ differential)<br>Receive when in MDI mode; Transmit when in MDI-X mode.            |
| 7          | RXM   | I/O                     | Physical receive or transmit signal (- differential)<br>Receive when in MDI mode; Transmit when in MDI-X mode.            |
| 8          | AVDDL | PWR                     | 1.2V (nominal) supply for analog core.  |

**TABLE 1-1: SIGNALS (CONTINUED)**

| Pin Number | Name                 | Buffer Type<br>Note 1-1 | Description   |
|------------|----------------------|-------------------------|---|
| 9          | VDDL                 | PWR                     | 1.2V (nominal) supply for digital core  |
| 10         | MDIO                 | IPU/OPU                 | Management Interface (MIIM) Data I/O<br>This pin has a weak pull-up, is open-drain like, and requires an external 1 kΩ pull-up resistor.  |
| 11         | MDC                  | IPU                     | Management Interface (MIIM) Clock Input<br>This clock pin is synchronous to the MDIO data pin.  |
| 12         | RXER / QWF           | IPD/O                   | RMII Receive Error Output<br>Config Mode: The pull-up/pull-down value is latched as QWF at the de-assertion of reset. See <a href="#">Table 1-2, "Strap-in Options"</a> for details.  |
| 13         | CRS_DV /<br>CONFIG2  | IPD/O                   | RMII Carrier Sense/Receive Data Valid Output<br>Config Mode: The pull-up/pull-down value is latched as CONFIG2 at the de-assertion of reset. See <a href="#">Table 1-2, "Strap-in Options"</a> for details.   |
| 14         | PHYAD0               | IPU/O                   | No function during normal operation<br>Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] at the de-assertion of reset. See <a href="#">Table 1-2, "Strap-in Options"</a> for details.   |
| 15         | VDDIO                | PWR                     | 3.3V or 2.5V supply for digital I/O.  |
| 16         | PHYAD1               | IPD/O                   | No function during normal operation<br>Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] at the de-assertion of reset. See <a href="#">Table 1-2, "Strap-in Options"</a> for details.   |
| 17         | RXD1 /<br>PHYAD2     | IPD/O                   | RMII Receive Data Output[1] ( <a href="#">Note 1-2</a> )<br>Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] at the de-assertion of reset. See <a href="#">Table 1-2, "Strap-in Options"</a> for details.  |
| 18         | RXD0 /<br>AUTONEG    | IPU/O                   | RMII Receive Data Output[0] ( <a href="#">Note 1-2</a> )<br>Config Mode: The pull-up/pull-down value is latched as AUTONEG at the de-assertion of reset. See <a href="#">Table 1-2, "Strap-in Options"</a> for details.   |
| 19         | REF_CLK /<br>CONFIG0 | IPD/O                   | KSZ8061RNB: RMII 50 MHz Reference Clock Output to the MAC<br>Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See <a href="#">Table 1-2, "Strap-in Options"</a> for details.<br><br>KSZ8061RND: This pin is unused during normal operation. Leave it unconnected except as required for Config Mode.<br>Config Mode: The pull-up/pull-down value is latched as CONFIG0 at the de-assertion of reset. See <a href="#">Table 1-2, "Strap-in Options"</a> for details. |
| 20         | LED1                 | O                       | LED1 Output<br>Active low. Its function is programmable; by default it indicates link speed.  |
| 21         | TXEN                 | I                       | PMII Transmit Enable Input.   |
| 22         | TXD0                 | I                       | RMII Transmit Data Input[0] ( <a href="#">Note 1-3</a> )  |
| 23         | TXD1                 | I                       | RMII Transmit Data Input[1] ( <a href="#">Note 1-3</a> )  |

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**TABLE 1-1: SIGNALS (CONTINUED)**

| Pin Number    | Name                      | Buffer Type<br><a href="#">Note 1-1</a> | Description  |
|---------------|---------------------------|---|--|
| 24            | LED0                      | IPD/O                                   | LED0 Output<br>Active low. Its function is programmable; by default it indicates link/activity.  |
| 25            | DNU                       | I                                       | Do Not Use. This unused input must be pulled to a logic-low level.   |
| 26            | DNU                       | I                                       | Do Not Use. This unused input should be pulled to a logic-low level.   |
| 27            | CONFIG1                   | IPD/O                                   | No function during normal operation.<br>Config Mode: The pull-up/pull-down value is latched as CONFIG1 at the de-assertion of reset. See <a href="#">Strap-in Options</a> for details.   |
| 28            | RESET#                    | IPU                                     | Chip Reset (active-low).   |
| 29            | INTRP /<br>NAND_TREE<br># | IPU/O                                   | Programmable Interrupt Output (active-low [default] or active-high)<br>This pin has a weak pull-up, is open-drain like, and requires an external 1.0 kΩ pull-up resistor.<br>Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset. See <a href="#">Strap-in Options</a> for details. |
| 30            | VDDL                      | PWR                                     | 1.2V (nominal) supply for digital (and analog).  |
| 31            | REXT                      | I                                       | Set PHY transmit output current.<br>Connect a 6.04Ω 1% resistor from this pin to ground.   |
| 32            | SIGDET                    | O                                       | Signal Detect, active-high.  |
| Bottom Paddle | GND                       | GND                                     | Ground. Bottom paddle.   |

**Note 1-1** Pwr = Power supply.  
Gnd = Ground.  
I = Input.  
O = Output.  
I/O = Bi-directional.  
Ipu = Input with internal pull-up (see [Electrical Characteristics](#) for value).  
Ipd = Input with internal pull-down (see [Electrical Characteristics](#) for value).  
Ipu/O = Input with internal pull-up (see [Electrical Characteristics](#) for value) during power-up/reset; output pin otherwise.  
Ipd/O = Input with internal pull-down (see [Electrical Characteristics](#) for value) during power-up/reset; output pin otherwise.  
Ipu/Opu = Input and output with internal pull-up (see [Electrical Characteristics](#) for value).

**Note 1-2** RMII Mode: The RXD[3:0] bits are synchronous with RXC. When RXDV is asserted, RXD[3:0] presents valid data to the MAC device.

**Note 1-3** RMII Mode: The TXD[3:0] bits are synchronous with TXC. When TXEN is asserted, TXD[3:0] accepts valid data from the MAC device.

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The strap-in pins are latched at the de-assertion of reset. In some systems, the MAC RMIi receive input pins may drive high/low during power-up or reset, and consequently cause the PHY strap-in pins on the RMIi signals to be latched to the unintended high/low states. In this case, external pull-up or pull-down resistors (4.7 k $\Omega$ ) should be added on these PHY strap-in pins to ensure the intended values are strapped-in correctly.

**TABLE 1-2: STRAP-IN OPTIONS**

| Pin Number | Name                 | Buffer Type<br>Note 1-4 | Description  |                     |                         |
|------------|----------------------|-------------------------|--|---------------------|-------------------------|
| 17         | RXD1/PHYAD2          | IPD/O                   | The PHY Address is latched at de-assertion of reset and is configurable to any value from 0 to 7.<br>The default PHY Address is 00001.<br>PHY Address bits [4:3] are set to 00 by default.             |                     |                         |
| 16         | PHYAD1               | IPD/O                   |  |                     |                         |
| 14         | PHYAD0               | IPU/O                   |  |                     |                         |
| 13         | CRS_DV/<br>CONFIG2   | IPD/O                   | The CONFIG[2:0] strap-in pins are latched at the de-assertion of reset.  |                     |                         |
|            |                      |                         | 000  | Reserved - not used |                         |
| 27         | CONFIG1              | IPD/O                   | 001  | RMIi normal mode    | Auto MDI/MDI-X disabled |
|            |                      |                         | 010 - 100  | Reserved - not used |                         |
|            |                      |                         | 101  | RMIi Back-to-Back   | Auto MDI/MDI-X enabled  |
| 19         | REF_CLK/CON-<br>FIG0 | IPD/O                   | 110  | Reserved - not used |                         |
|            |                      |                         | 111  | RMIi normal mode    | Auto MDI/MDI-X enabled  |
| 18         | RXD0/<br>AUTONEG     | IPU/O                   | Auto-Negotiation Disable<br>Pull-up (default) = Disable Auto-Negotiation<br>Pull-down = Enable Auto-Negotiation<br>At the de-assertion of reset, this pin value is latched into register 0h, bit [12]. |                     |                         |
| 29         | INTRP/<br>NAND_TREE# | IPU/O                   | NAND Tree Mode<br>Pull-up (default) = Disable NAND Tree (normal operation)<br>Pull-down = Enable NAND Tree<br>At the de-assertion of reset, this pin value is latched by the chip.                     |                     |                         |
| 12         | RXER/QWF             | IPD/O                   | Quiet-WIRE Filtering Disable<br>Pull-up = Disable Quiet-WIRE Filtering<br>Pull-down (default) = Enable Quiet-WIRE Filtering<br>At the de-assertion of reset, this pin value is latched by the chip.    |                     |                         |

**Note 1-4** Ipu/O = Input with internal pull-up during power-up/reset; output pin otherwise. (See the [Electrical Characteristics](#) section for each value.) Ipd/O = Input with internal pull-down (see the [Electrical Characteristics](#) section for each value during power-up/reset; output pin otherwise.

# KSZ8061RNB/RND

## 2.0 INTRODUCTION

### 2.1 General Description

The KSZ8061RNB/RND is a single-chip 10BASE-T/100BASE-TX Ethernet physical layer transceiver for transmission and reception of data over unshielded twisted pair (UTP) cable.

The KSZ8061RNB/RND features Quiet-WIRE<sup>®</sup> internal filtering to reduce line emissions. It is ideal for applications, such as automotive or industrial networks, where stringent radiated emission limits need to be met. Quiet-WIRE can utilize low cost unshielded cable, where previously only shielded cable solutions were possible. The KSZ8061RNB/RND also features enhanced immunity to environmental EM noise.

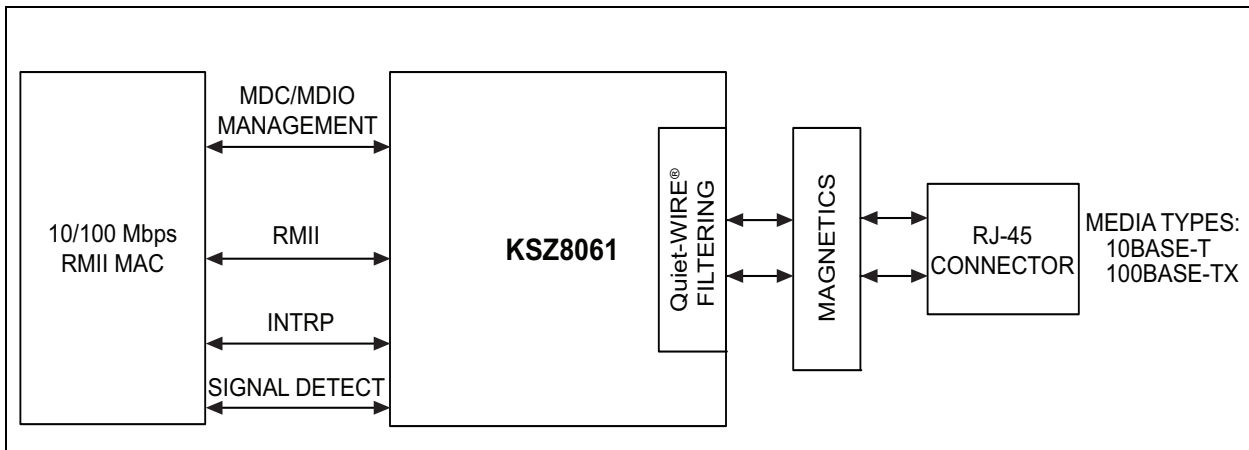
The KSZ8061RNB/RND features a Reduced Media Independent Interface (RMII) for direct connection with RMII-compliant Ethernet MAC processors and switches.

The KSZ8061RNB generates a 50 MHz RMII reference clock for use by the connected MAC device. In contrast, the KSZ8061RND receives the 50 MHz RMII reference clock as an input.

The KSZ8061RNB/RND meets Automotive AEC-Q100 and EMC requirements, with an extended temperature range of -40°C to +105°C. It is supplied in 32-pin, 5 mm × 5 mm QFN and WQFN packages.

The KSZ8061MNX and KSZ8061MNG devices have a MII interface and are described in a separate data sheet.

**FIGURE 2-1: SYSTEM BLOCK DIAGRAM**





## 3.0 FUNCTIONAL DESCRIPTION

The KSZ8061RNB/RND is an integrated Fast Ethernet transceiver that features Quiet-WIRE<sup>®</sup> internal filtering to reduce line emissions. When Quiet-WIRE filtering is disabled, it is fully compliant with the IEEE 802.3 specification. The KSZ8061RNB/RND also has high noise immunity.

On the copper media side, the KSZ8061RNB/RND supports 10BASE-T and 100BASE-TX for transmission and reception of data over a standard CAT-5 or similar unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8061RNB/RND offers the Reduced Media Independent Interface (RMII) for direct connection with RMII-compliant Ethernet MAC processors and switches.

The RMII management bus gives the MAC processor complete access to the KSZ8061RNB/RND control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

Auto-negotiation and Auto MDI/MDIX can be disabled at power-on to significantly reduce initial time to link up.

A signal detect pin (SIGDET) is available to indicate when the link partner is inactive. An option is available for the KSZ8061RNB/RND to automatically enter Ultra-Deep Sleep mode automatically when SIGDET is de-asserted. Ultra-Deep Sleep mode may also be entered by command of the MAC processor. Additional low power modes are available.

### 3.1 10BASE-T/100BASE-TX Transceiver

#### 3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the RMII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by a precision external resistor on REXT for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

#### 3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes, such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RMII format and provided as the input data to the MAC.

#### 3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The scrambler is used to spread the power spectrum of the transmitted signal to reduce EMI and baseline wander. The de-scrambler is needed to recover the scrambled signal.

#### 3.1.4 10BASE-T TRANSMIT

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, then output 10BASE-T signals with a typical amplitude of 2.5V peak. The 10BASE-T signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

# KSZ8061RNB/RND

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## 3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP and RXM inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8061RNB/RND decodes a data frame. The receive clock is kept active during idle periods in between data reception.

## 3.1.6 PLL CLOCK SYNTHESIZER

The KSZ8061RNB/RND generates all internal clocks and all external clocks for system timing from the clock received at the XI pin. For the KSZ8061RNB, this is an external 25 MHz crystal, oscillator, or reference clock. For the KSZ8061RND, this is the externally supplied RMII 50 MHz reference clock.

## 3.1.7 AUTO-NEGOTIATION

The KSZ8061RNB/RND conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

If the KSZ8061RNB/RND is using auto-negotiation, but its link partner is not, then the KSZ8061RNB/RND sets its operating speed by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8061RNB/RND to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. Duplex is set by register 0h, bit [8] because the KSZ8061RNB/RND cannot determine duplex by parallel detection.

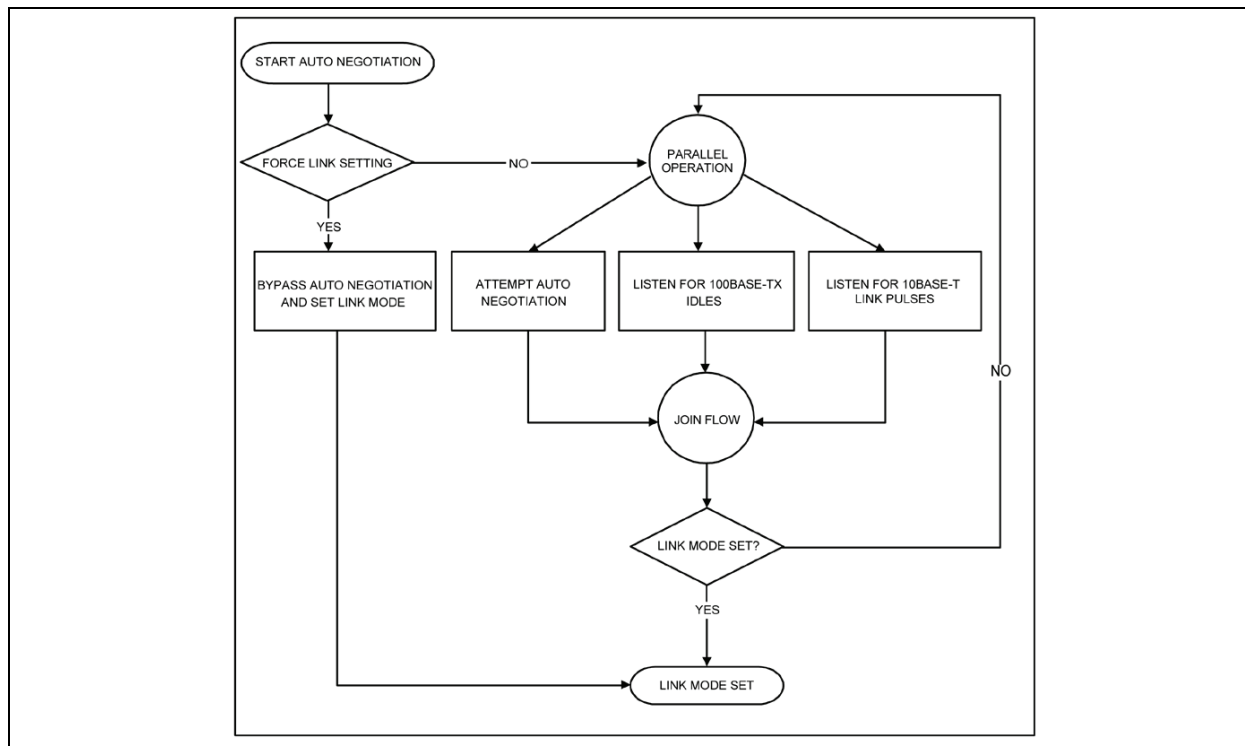
If auto-negotiation is disabled, the speed is set by register 0h, bit [13], and the duplex is set by register 0h, bit [8]. The default is 100BASE-TX, full-duplex.

Auto-negotiation is enabled or disabled by hardware pin strapping (AUTONEG) and by software (register 0h, bit [12]). By default, auto-negotiation is disabled after power-up or hardware reset, but it may be enabled by pulling the RXD0 pin low at that time. Afterwards, auto-negotiation can be enabled or disabled by register 0h, bit [12].

When the link is 10BASE-T or the link partner is using auto-negotiation and the Ultra-Deep Sleep mode is used, then the Signal Detect assertion timing delay bit, register 14h bit [1], must be set.

The auto-negotiation link-up process is shown in [Figure 3-1](#).

**FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART**



## 3.2 Quiet-WIRE® Filtering

Quiet-WIRE is a feature to enhance 100BASE-TX EMC performance by reducing both conducted and radiated emissions from the TXP/M signal pair. It can be used either to reduce absolute emissions or to enable replacement of shielded cable with unshielded cable, all while maintaining interoperability with standard 100BASE-TX devices.

Quiet-WIRE filtering is implemented internally, with no additional external components required. It is enabled or disabled at power-up and reset by a strapping option on the RXER pin. Once the KSZ8061 is powered up, Quiet-WIRE filtering can be disabled by writing to register 16h, bit [12]. Note that Quiet-WIRE cannot be enabled via this register bit.

The default setting for Quiet-WIRE reduces emissions primarily above 60 MHz, with less reduction at lower frequencies. Several dB of reduction is possible. Signal attenuation is approximately equivalent to increasing the cable length by 10 to 20 meters, thus reducing cable reach by that amount. For applications needing more modest improvement in emissions, the level of filtering can be reduced by writing a series of registers.

## 3.3 Fast Link-Up

Link-up time is normally determined by the time it takes to complete auto-negotiation. Additional time may be added by the auto MDI/MDI-X feature. The total link-up time from power-up or cable connect is typically a second or more.

Fast Link-up mode significantly reduces 100BASE-TX link-up time by disabling both auto-negotiation and auto MDI/MDI-X, and fixing the TX and RX channels. This is done via the CONFIG[2:0] and AUTONEG strapping options. Because these are strapping options, fast link-up is available immediately upon power-up. Fast Link-up is available only for 100BASE-TX link speed. To force the link speed to 10BASE-TX requires a register write.

Fast Link-up mode is intended for specialized applications where both link partners are known in advance. The link must also be known so that the fixed transmit channel of one device connects to the fixed receive channel of the other device, and vice versa.

If a device in Fast Link-up mode is connected to a normal device (auto-negotiate and auto-MDI/MDI-X), there will be no problems linking, but the speed advantage of Fast Link-up will be realized only on one end.

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## 3.4 Internal and External RX Termination

By default, the RX differential pair is internally terminated. This minimizes board component count by eliminating all components between the KSZ8061RNB/RND and the magnetics (transformer and common mode choke). The KSZ8061RNB/RND has the option to turn off the internal termination, to allow the use of external termination. External termination does increase the external component count, but these external components can be of tighter tolerance than the internal termination resistors. Enabling or disabling of internal RX termination is controlled by register 14h, bit [2].

If external termination is used in place of the internal termination, it should consist of two 50Ω resistors in series between RXP and RXM, with a 0.1μF to 1μF capacitor from the midpoint of the two resistors to ground.

## 3.5 RMII Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface. It provides a common interface between RMII PHYs and MACs and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, and 1 pin for the 50 MHz reference clock).
- 10 Mbps and 100 Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2-bit wide, a di-bit.

## 3.6 RMII Signal Definition

Table 3-1 describes the RMII signals. Refer to RMII Specification v1.2 for detailed information.

**TABLE 3-1: RMII SIGNAL DEFINITION**

| RMII Signal Name | KSZ8061RNB/RND Signal and Direction | Direction (with respect to MAC device) | Description  |
|------------------|-------------------------------------|--|--|
| REF_CLK          | <b>KSZ8061RNB</b> REF_CLK, Output   | Input                                  | Synchronous 50 MHz reference clock for receive, transmit and control interface |
|                  | <b>KSZ8061RND</b> XI, Input         | Input or Output                        |  |
| TX_EN            | TXEN, Input                         | Output                                 | Transmit Enable  |
| TXD[1:0]         | TXD[1:0], Input                     | Output                                 | Transmit Enable  |
| CRS_DV           | CRS_DV, Output                      | Input                                  | Carrier Sense/Receive Data Valid   |
| RXD[1:0]         | RXD[1:0], Output                    | Input                                  | Receive Data [1:0]   |
| RX_ER            | RXER, Output                        | Input                                  | Receive Error  |

### 3.6.1 REFERENCE CLOCK (REF\_CLK)

REF\_CLK is a continuous 50 MHz clock that provides the timing reference for TXEN, TXD[1:0], CRS\_DV, RXD[1:0] and RXER. The KSZ8061RNB generates and outputs the 50 MHz RMII REF\_CLK to the MAC device at REF\_CLK (pin 19). The KSZ8061RND receives the 50 MHz RMII REF\_CLK from the MAC or system board at XI (pin 1), and leaves the REF\_CLK (pin 19) as no connect.

### 3.6.2 TRANSMIT ENABLE (TXEN)

TXEN indicates the MAC is presenting di-bits on TXD[1:0] for transmission. It is asserted synchronously with the first di-bit of the preamble and remains asserted while all di-bits to be transmitted are presented on the RMII. It is negated prior to the first REF\_CLK following the final di-bit of a frame.

TXEN transitions synchronously with respect to REF\_CLK.

### 3.6.3 TRANSMIT DATA [1:0] (TXD[1:0])

When TXEN is asserted, the PHY accepts TXD[1:0] for transmission. When TXEN is de-asserted, the MAC drives TXD[1:0] to 00 for the idle state.

TXD[1:0] transitions synchronously with respect to REF\_CLK.

## 3.6.4 CARRIER SENSE/RECEIVE DATA VALID (CRS\_DV)

The PHY asserts CRS\_DV when the receive medium is non-idle. It is asserted asynchronously when a carrier is detected. This happens when squelch is passed in 10 Mbps mode and when two non-contiguous 0s in 10 bits are detected in 100 Mbps mode. Loss of carrier results in the de-assertion of CRS\_DV.

While carrier detection criteria are met, CRS\_DV remains asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit. It is negated before the first REF\_CLK that follows the final di-bit. The data on RXD[1:0] is considered valid after CRS\_DV is asserted. However, because the assertion of CRS\_DV is asynchronous relative to REF\_CLK, the data on RXD[1:0] is 00 until receive signals are properly decoded.

## 3.6.5 RECEIVE DATA[1:0] (RXD[1:0])

For each clock period in which CRS\_DV is asserted, RXD[1:0] transfers a di-bit of recovered data from the PHY. When CRS\_DV is de-asserted, the PHY drives RXD[1:0] to 00 for the idle state.

RXD[1:0] transitions synchronously with respect to REF\_CLK.

## 3.6.6 RECEIVE ERROR (RXER)

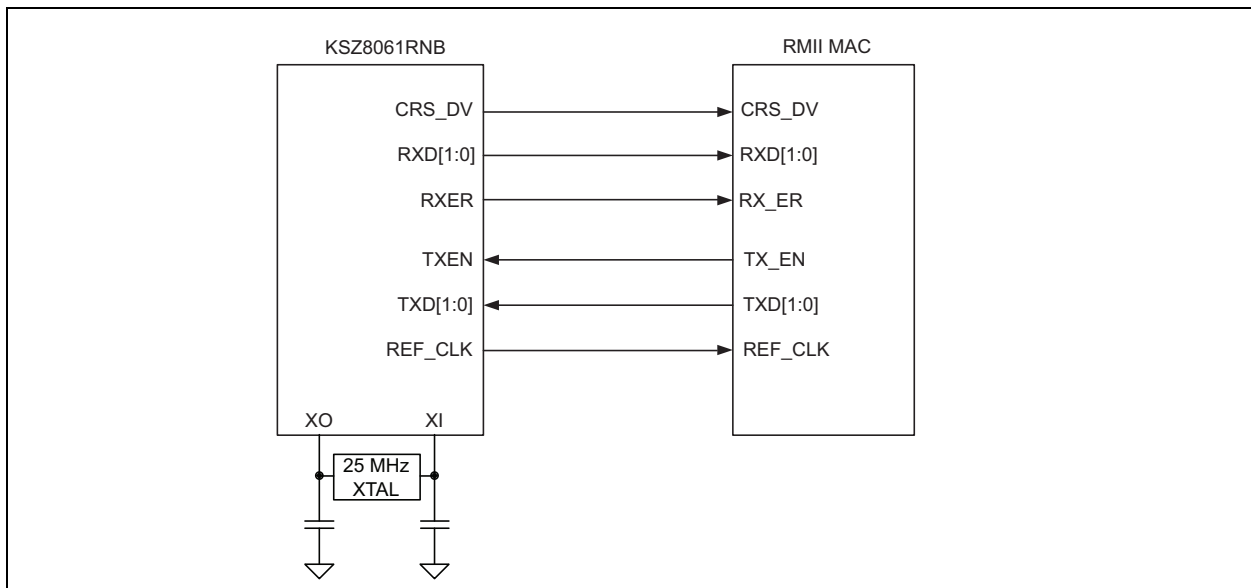
When CRS\_DV is asserted, RXER is asserted for one or more REF\_CLK periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) is detected somewhere in the frame that is being transferred from the PHY to the MAC.

RXER transitions synchronously with respect to REF\_CLK.

## 3.6.7 RMII SIGNAL DIAGRAMS

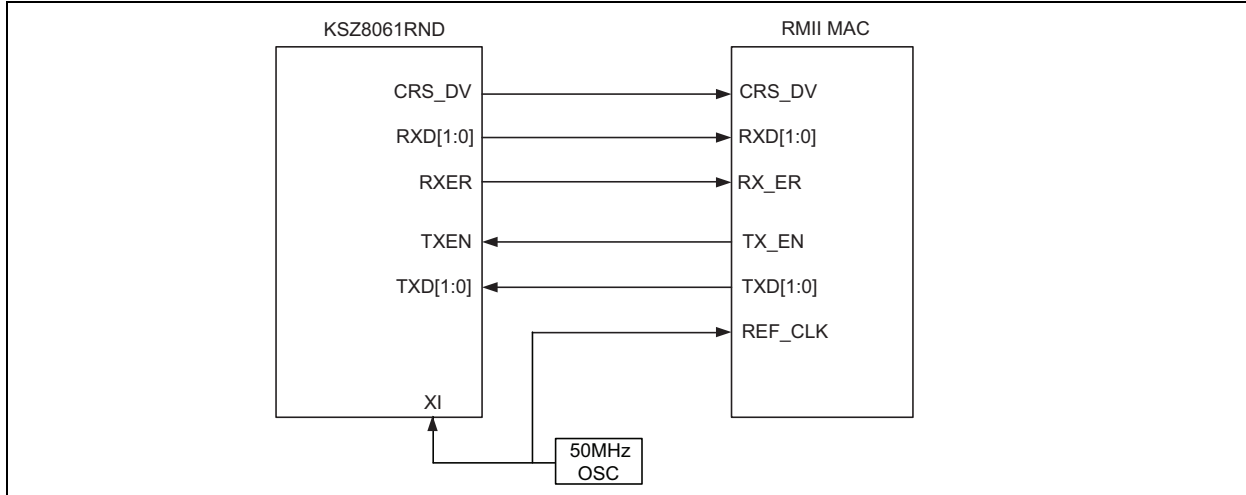
The KSZ8061RNB RMII pin connections to the MAC are shown in [Figure 3-2](#). The connections for the KSZ8061RND are shown in [Figure 3-3](#).

**FIGURE 3-2: KSZ8061RNB RMII INTERFACE**



# KSZ8061RNB/RND

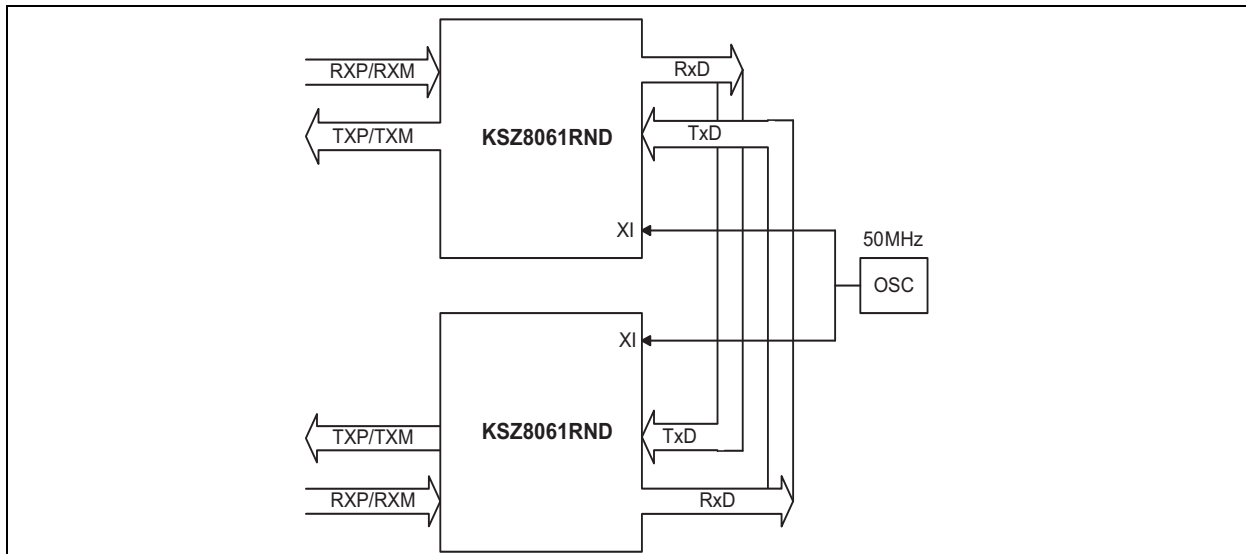
**FIGURE 3-3: KSZ8061RND RMII INTERFACE**



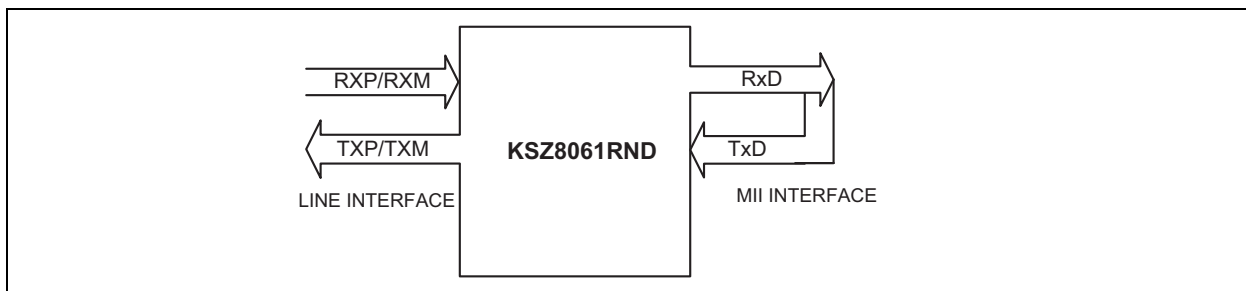
## 3.7 Back-to-Back Mode - 100 Mbps Repeater

Two KSZ8061RND devices can be connected back-to-back to form a 100BASE-TX to 100BASE-TX repeater. For testing purposes, it can also be used to loopback data on the RMII bus by physically connecting the RMII receive bus to the RMII transmit bus.

**FIGURE 3-4: KSZ8061RND TO KSZ8061RND BACK-TO-BACK REPEATER**



**FIGURE 3-5: KSZ8061RND BACK-TO-BACK FOR RMII BUS LOOPBACK**



## 3.8 RMII Back-to-Back Mode

In RMII back-to-back mode, a KSZ8061RND interfaces with another KSZ8061RND to provide a complete 100 Mbps repeater solution.

The KSZ8061RND devices are configured to RMII Back-to-Back mode after power-up or reset with the following:

- Strapping pin CONFIG[2:0] set to '101'.
- A common 50 MHz reference clock connected to XI of both KSZ8061RND devices.
- RMII signals connected as shown in [Table 3-2](#).

**TABLE 3-2: RMII SIGNAL CONNECTION FOR RMII BACK-TO-BACK MODE**

| KSZ8061RND (100BASE-TX)<br>[Device 1] |          | KSZ8061RND (100BASE-TX)<br>[Device 1 or 2] |          |
|---------------------------------------|----------|--|----------|
| Pin Name                              | Pin Type | Pin Name                                   | Pin Type |
| CRS_DV                                | OUTPUT   | TXEN                                       | INPUT    |
| RXD1                                  | OUTPUT   | TXD1                                       | INPUT    |
| RXD0                                  | OUTPUT   | TXD0                                       | INPUT    |
| TXEN                                  | INPUT    | CRS_DV                                     | OUTPUT   |
| TXD1                                  | INPUT    | RXD1                                       | OUTPUT   |
| TXD0                                  | INPUT    | RXD0                                       | OUTPUT   |

## 3.9 MII Management (MIIM) Interface

The KSZ8061RNB/RND supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface enables an upper-layer device, like a MAC processor, to monitor and control the state of the KSZ8061RNB/RND. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Supported registers [0:8] are standard registers, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See "[Register Map](#)" section for details.

The KSZ8061RNB/RND supports unique PHY addresses 1 to 7, and broadcast PHY address 0. The broadcast address is defined per the IEEE 802.3 specification, and can be used to write to multiple KSZ8061RNB/RND devices simultaneously.

The PHYAD[2:0] strapping pins are used to assign a unique PHY address between 1 and 7 to each KSZ8061RNB/RND device.

[Table 3-3](#) shows the MII Management frame format.

**TABLE 3-3: MII MANAGEMENT FRAME FORMAT**

|              | Preamble | Start of Frame | Read/Write OP Code | PHY Address Bits [4:0] | REG Address Bits [4:0] | TA | Data Bits [15:0]  | Idle |
|--------------|----------|----------------|--------------------|------------------------|------------------------|----|-------------------|------|
| <b>Read</b>  | 32 1's   | 01             | 10                 | 00AAA                  | RRRRR                  | Z0 | DDDDDDDD_DDDDDDDD | Z    |
| <b>Write</b> | 32 1's   | 01             | 01                 | 00AAA                  | RRRRR                  | 10 | DDDDDDDD_DDDDDDDD | Z    |

## 3.10 LED Output Pins

The LED0 and LED1 pins indicate link status and is intended for driving LEDs. They are active low and can sink current directly from the LEDs. By default, LED0 indicates Link/Activity and LED1 indicates Link Speed. Bits [5:4] in register 1Fh allow the definition of these pins to be changed to Link Status and Activity respectively.

# KSZ8061RNB/RND

- Link Status: The LED indicates that the serial link is up.
- Link/Activity: When the link is up, but there is no traffic, the LED will be on. When packets are being received or transmitted, the LED will blink.
- Activity: The LED blinks when packets are received or transmitted. It is off when there is no activity.
- Speed: When the link is up, the LED is on to indicate a 100BASE-TX link and is off to indicate a 10BASE-T link.

## 3.11 Interrupt (INTRP)

INTRP is an interrupt output signal that may be used to inform the external controller that there has been a status update to the KSZ8061RNB/RND PHY register. This eliminates the need for the processor to poll the PHY for status changes such as link up or down.

Register 1Bh, bits [15:8] are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Register 1Bh, bits [7:0] are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Register 1Fh, bit [9] sets the interrupt level to active-high or active-low. The default is active-low.

## 3.12 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the KSZ8061RNB/RND and its link partner. This feature allows the KSZ8061RNB/RND to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and then assigns transmit and receive pairs of the KSZ8061RNB/RND accordingly.

Auto MDI/MDI-X is initially enabled or disabled at hardware reset by hardware pin strapping (CONFIG[2:0]). Afterwards, it can be enabled or disabled by register 1Fh, bit [13]. When Auto MDI/MDI-X is disabled, serial data is normally transmitted on the pin pair TXP/TXM, and data is received on RXP/RXM. However, this may be reversed by writing to register 1Fh, bit [14].

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

[Table 3-4](#) illustrates how the IEEE 802.3 Standard defines MDI and MDI-X.

**TABLE 3-4: MDI/MDI-X PIN DEFINITION**

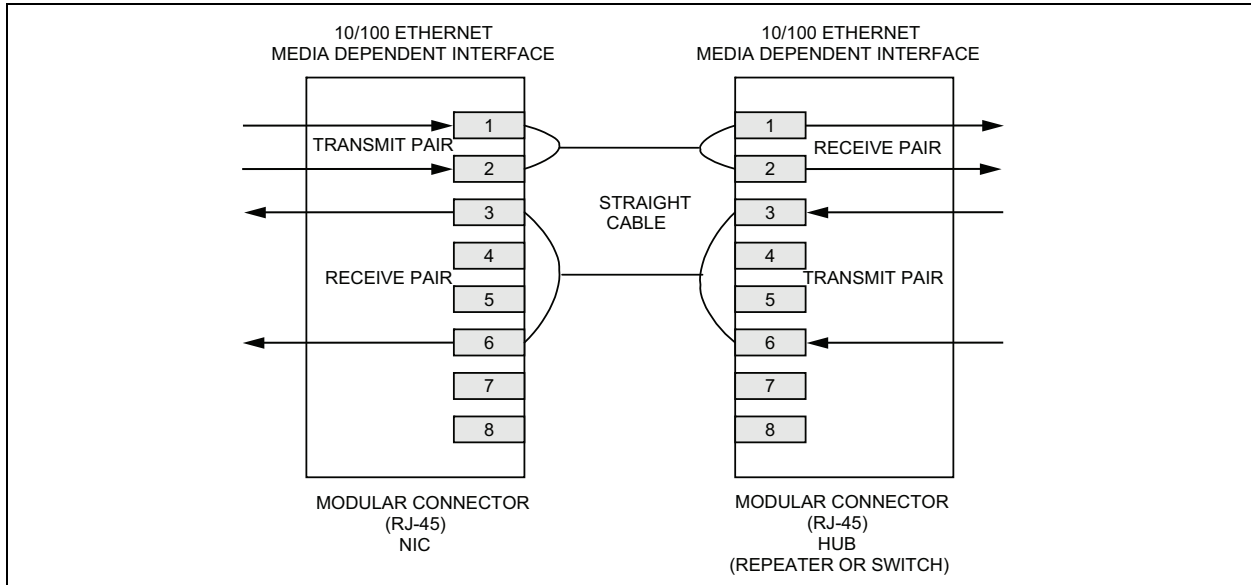
| MDI       |        | MDI-X     |        |
|-----------|--------|-----------|--------|
| RJ-45 Pin | Signal | RJ-45 Pin | Signal |
| 1         | TX+    | 1         | RX+    |
| 2         | TX-    | 2         | RX-    |
| 3         | RX+    | 3         | TX+    |
| 6         | RX-    | 6         | TX-    |

## 3.13 Straight Cable

A straight cable connects a MDI device to a MDI-X device, or a MDI-X device to a MDI device. [Figure 3-6](#) depicts a typical straight cable connection between a NIC card (MDI device) and a switch, or hub (MDI-X device).



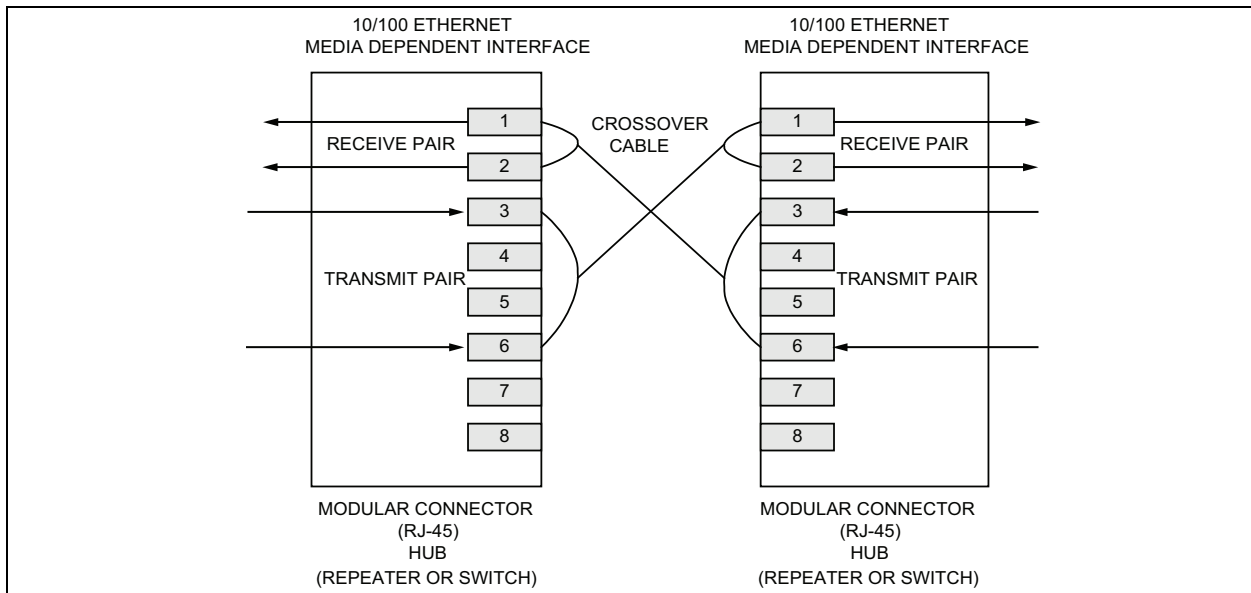
**FIGURE 3-6: TYPICAL STRAIGHT CABLE CONNECTION**



### 3.14 Crossover Cable

A crossover cable connects a MDI device to another MDI device, or a MDI-X device to another MDI-X device. [Figure 3-7](#) depicts a typical crossover cable connection between two switches or hubs (two MDI-X devices).

**FIGURE 3-7: TYPICAL CROSSOVER CABLE CONNECTION**



### 3.15 Loopback Modes

The KSZ8061RNB/RND supports the following loopback operations to verify analog and/or digital data paths:

- Local (Digital) Loopback
- Remote (Analog) Loopback

# KSZ8061RNB/RND

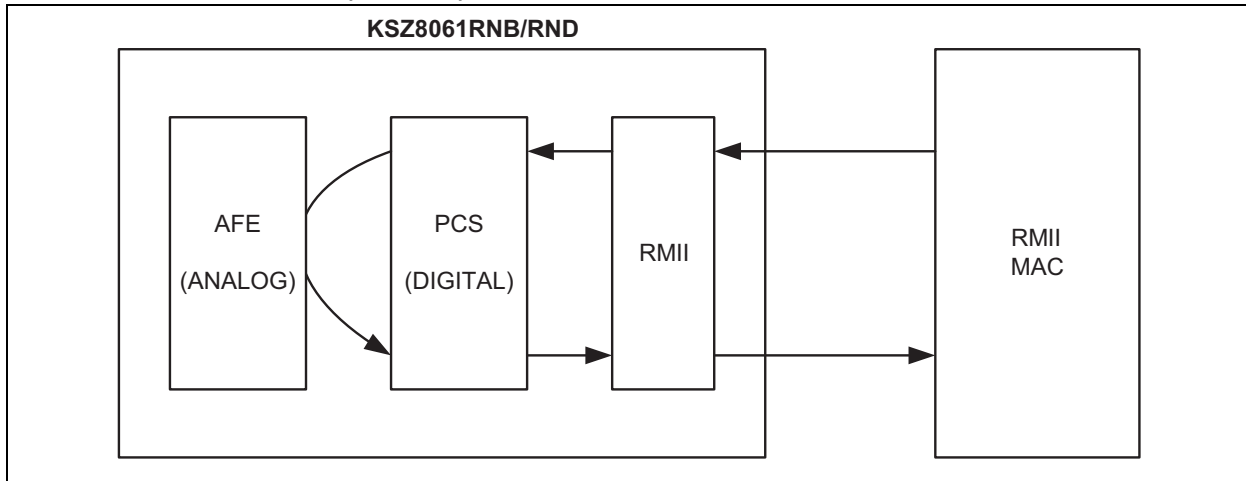
## 3.15.1 LOCAL (DIGITAL) LOOPBACK MODE

This loopback mode is a diagnostic mode for checking the RMIi transmit and receive data paths between KSZ8061RNB/RND and external MAC, and is supported for both speeds (10/100 Mbps) at full-duplex.

The loopback data path is shown in [Figure 3-8](#).

1. RMIi MAC transmits frames to KSZ8061RNB/RND.
2. Frames are wrapped around inside KSZ8061RNB/RND.
3. KSZ8061RNB/RND transmits frames back to RMIi MAC.

**FIGURE 3-8: LOCAL (DIGITAL) LOOPBACK**



The following programming steps and register settings are used for Local Loopback mode.

For 10/100 Mbps loopback,

Set Register 0h,

- Bit [14] = 1 // Enable Local Loopback mode
- Bit [13] = 0 / 1 // Select 10 Mbps / 100 Mbps speed
- Bit [12] = 0 // Disable Auto-Negotiation
- Bit [8] = 1 // Select full-duplex mode

Set Register 1Ch,

- Bit [5] = 1

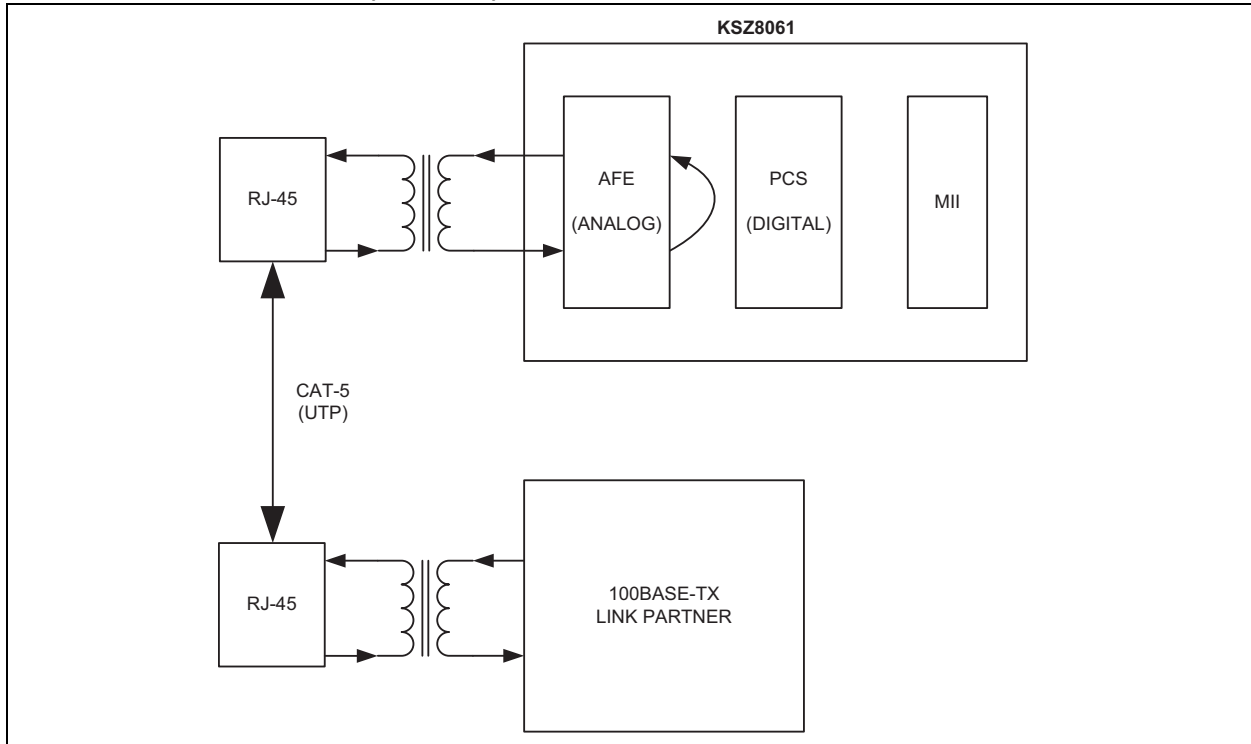
## 3.15.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between KSZ8061RNB/RND and its link partner, and is supported for 100BASE-TX full-duplex mode only.

The loopback data path is shown in the following [Figure 3-9](#).

- Fast Ethernet (100BASE-TX) PHY link partner transmits frames to KSZ8061RNB/RND.
- Frames are wrapped around inside KSZ8061RNB/RND.
- KSZ8061RNB/RND transmits frames back to fast Ethernet (100BASE-TX) PHY link partner.

**FIGURE 3-9: REMOTE (ANALOG) LOOPBACK**



The following programming steps and register settings are used for Remote Loopback mode.

Set Register 0h,

- Bit [13] = 1 // Select 100 Mbps speed
- Bit [12] = 0 // Disable Auto-Negotiation
- Bit [8] = 1 // Select full-duplex mode

Or just simply auto-negotiate and link up at 100BASE-TX full-duplex mode with link partner

Set Register 1Fh,

- Bit [2] = 1 // Enable Remote Loopback mode

### 3.16 LinkMD<sup>®</sup> Cable Diagnostics

The LinkMD<sup>®</sup> function utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, and then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing the LinkMD Control/Status Register (register 1Dh) and the PHY Control 2 Register (register 1Fh). The latter register is used to disable auto MDI/MDIX and to select either MDI or MDI-X as the cable differential pair for testing.

A two-step process is used to analyze the cable. The first step uses a small pulse (for short cables), while the second step uses a larger pulse (for long cables). The steps are shown here:

Step 1

- Write MMD address 1Bh, register 0, bits [7:4] = 0x2. Note that this is the power-up default value.
- Write register 13h, bit [15] = 0. Note that this is the power-up default value.
- Write register 1Fh. Disable auto MDI/MDI-X in bit [13], and select either MDI or MDI-X in bit [14] to specify the twisted pair to test.
- Write register 1Dh bit [15] to initiate the LinkMD test.

# KSZ8061RNB/RND

- Read register 1Dh to determine the result of the first step. Bit [15] = 0 indicates that the test is complete. After that, the result is read in bits [14:12]. Remember the result.

## Step 2

- Write MMD address 1Bh, register 0, bits [7:4] = 0x7.
- Write register 13h, bit [15] = 1.
- Write register 1Dh bit [15] to initiate the LinkMD test.
- Read register 1Dh to determine the result of the first step. Bit [15] = 0 indicates that the test is complete. After that, the result is read in bits [14:12].
- If either step reveals a short, then there is a short. If either step reveals an open, then there is an open. If both tests indicate normal, then the cable is normal.

## 3.17 LinkMD<sup>®</sup>+ Enhanced Diagnostics: Receive Signal Quality Indicator

The KSZ8061RN provides a receive Signal Quality Indicator (SQI) feature, which indicates the relative quality of the 100BASE-TX receive signal. It approximates a signal-to-noise ratio, and is affected by cable length, cable quality, and coupled of environmental noise.

The raw SQI value is available for reading at any time from indirect register: MMD 1Ch, register ACh, bits [14:8]. A lower value indicates better signal quality, while a higher value indicates worse signal quality. Even in a stable configuration in a low-noise environment, the value read from this register may vary. The value should therefore be averaged by taking multiple readings. The update interval of the SQI register is 2  $\mu$ s, so measurements taken more frequently than 2  $\mu$ s will be redundant. In a quiet environment, 6 to 10 readings are suggested for averaging. In a noisy environment, individual readings are unreliable, so a minimum of 30 readings are suggested for averaging. The SQI circuit does not include any hysteresis.

Table 3-5 lists typical SQI values for various CAT5 cable lengths when linked to a typical 100BASE-TX device in a quiet environment. In a noisy environment or during immunity testing, the SQI value will increase.

**TABLE 3-5: TYPICAL SQI VALUES**

| CAT5 Cable Length | Typical SQL Value (MMD 1Ch, register ACh, bits [14:8]) |
|-------------------|--|
| 10m               | 2  |
| 30m               | 2  |
| 50m               | 3  |
| 80m               | 3  |
| 100m              | 4  |
| 130m              | 5  |

## 3.18 NAND Tree Support

The KSZ8061RNB/RND provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8061RNB/RND digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the CONFIG1 pin provides the output for the next NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving low each NAND tree input pin sequentially per the NAND tree pin order
- Checking the NAND tree output to ensure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 3-6 lists the NAND tree pin order.

**TABLE 3-6: KSZ8061RNB/RND NAND TREE TEST PIN ORDER**

| Pin Number | Pin Name | NAND Tree Description |
|------------|----------|-----------------------|
| 10         | MDIO     | INPUT                 |
| 11         | MDC      | INPUT                 |
| 12         | RXER     | INPUT                 |
| 13         | CRS_DV   | INPUT                 |
| 14         | PHYAD0   | INPUT                 |
| 16         | PHYAD1   | INPUT                 |
| 17         | RXD1     | INPUT                 |
| 18         | RXD0     | INPUT                 |
| 19         | REF_CLK  | INPUT                 |
| 20         | DNU      | INPUT                 |
| 21         | TXEN     | INPUT                 |
| 22         | TXD0     | INPUT                 |
| 23         | TXD1     | INPUT                 |
| 24         | LED0     | INPUT                 |
| 25         | DNU      | INPUT                 |
| 26         | DNU      | INPUT                 |
| 29         | INTRP    | INPUT                 |
| 27         | CONFIG   | OUTPUT                |

### 3.19 NAND Tree I/O Testing

The following procedure can be used to check for faults on the KSZ8061RNB/RND digital I/O pin connections to the board:

1. Enable NAND tree mode by INTRP pin strapping option.
2. Use board logic to drive all KSZ8061RNB/RND NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, per KSZ8061RNB/RND NAND Tree pin order, as follows:
  - a) Toggle the first pin (MDIO) from high to low, and verify the CONFIG1 pin switch from high to low to indicate that the first pin is connected properly.
  - b) Leave the first pin (MDIO) low.
  - c) Toggle the second pin (MDC) from high to low, and verify the CONFIG1 pin switch from low to high to indicate that the second pin is connected properly.
  - d) Leave the first pin (MDIO) and the second pin (MDC) low.
  - e) Toggle the third pin (RXER) from high to low, and verify the CONFIG1 pin switch from high to low to indicate that the third pin is connected properly.
  - f) Continue with this sequence until all KSZ8061RNB/RND NAND tree input pins have been toggled.

Each KSZ8061RNB/RND NAND tree input pin must cause the CONFIG1 output pin to toggle high-to-low or low-to-high to indicate a good connection. If the CONFIG1 pin fails to toggle when the KSZ8061RNB/RND input pin toggles from high to low, the input pin has a fault.

### 3.20 Power Management

The KSZ8061RNB/RND offers the following power management modes which are enabled and disabled by register control.

# KSZ8061RNB/RND

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## 3.20.1 POWER SAVING MODE

Power Saving Mode is used to reduce the transceiver power consumption when the cable is unplugged. This mode does not interfere with normal device operation. It is enabled by writing a one to register 1Fh, bit [10], and is in effect when auto-negotiation mode is enabled and cable is disconnected (no link). In this mode, the KSZ8061RNB/RND shuts down all transceiver blocks except for the transmitter, energy detect and PLL circuits. By default, Power Saving Mode is disabled after power-up.

## 3.20.2 ENERGY-DETECT POWER-DOWN MODE

Energy-Detect Power-Down (EDPD) Mode is used to further reduce the transceiver power consumption when the cable is unplugged, relative to Power Saving Mode. This mode does not interfere with normal device operation. It is enabled by writing a zero to register 18h, bit [11], and is in effect when auto-negotiation mode is enabled and cable is disconnected (no link).

EDPD Mode can be optionally enhanced with a PLL Off feature, which turns off all KSZ8061RNB/RND transceiver blocks, except for transmitter and energy detect circuits. PLL Off is set by writing a one to register 10h, bit [4].

Further power reduction is achieved by extending the time interval in between transmissions of link pulses while in this mode. The periodic transmission of link pulses is needed to ensure two link partners in the same low powered state with auto MDI/MDI-X disabled can wake up when the cable is connected between them.

By default, Energy-Detect Power-Down Mode is disabled after power-up.

## 3.20.3 POWER-DOWN MODE

Power-Down Mode is used to power down the KSZ8061RNB/RND when it is not in use after power-up. It is enabled by writing a one to register 0h, bit [11].

In this mode, the KSZ8061RNB/RND disables all internal functions except the MII management interface. The KSZ8061RNB/RND exits (disables) Power-Down Mode after register 0h, bit [11] is set back to zero.

## 3.20.4 SLOW OSCILLATOR MODE

Slow Oscillator Mode is used to disconnect the input reference crystal/clock on XI (pin 1) and select the on-chip slow oscillator when the KSZ8061RNB/RND is not in use after power-up. It is enabled by writing a one to register 11h, bit [6].

Slow Oscillator Mode works in conjunction with Power-Down Mode to put the KSZ8061RNB/RND into a lower power state with all internal functions disabled, except for the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1. Disable Slow Oscillator Mode by writing a zero to register 11h, bit [6].
2. Disable Power-Down Mode by writing a zero to register 0h, bit [11].
3. Initiate software reset by writing a one to register 0h, bit [15].

## 3.20.5 ULTRA-DEEP SLEEP MODE

Ultra-Deep Sleep Mode is used to achieve the lowest possible power consumption while retaining the ability to detect activity on the Tx/Rx cable pairs, and is intended for achieving negligible battery drain during long periods of inactivity. It is controlled by several register bits, and Ultra-Deep Sleep Mode may be entered by writing to a register, or it may be initiated automatically when Signal Detect (SIGDET) is de-asserted. Details are given in the Signal Detect (SIGDET) and Ultra-Deep Sleep Mode section.

In Ultra-Deep Sleep Mode, the KSZ8061RNB/RND disables all internal functions and I/Os except for the ultra-low power signal detect circuit and the Signal Detect pin (SIGDET), which are powered from VDDIO. For lowest power consumption, the 1.2V supply (VDDL and AVDDL) may be turned off externally. Hardware reset is required to exit Ultra-Deep Sleep Mode.

## 3.20.6 NON-VOLATILE REGISTERS

Most of the logic circuitry of the KSZ8061RNB/RND, including the status and control registers, is powered by the 1.2V supply. When the 1.2V supply is turned off in Ultra-Deep Sleep Mode, the content of the registers is lost. Because of the importance of register 14h and bit [0] of register 13h, which control the various power modes, these bits are duplicated in a logic block powered by the 3.3V supply. These register bits are therefore “non-volatile” while in Ultra-Deep Sleep Mode.

To access the non-volatile (3.3V) registers, bit [4] of register 14h must first be set. Otherwise, writes to these registers will modify only the volatile versions of these registers, and not the non-volatile versions.

## 3.21 Signal Detect (SIGDET) and Ultra-Deep Sleep Mode

SIGDET is an output signal which may be used for power reduction, either by directly turning off selected power or by signaling to a host controller when no signal is detected on the line interface. It is asserted when sufficient energy is detected on either of the differential pairs, and is de-asserted when cable energy is not detected. The signal detection circuit consumes almost no power from the VDDIO supply, and does not use the 1.2V supply at all.

Ultra-Deep Sleep Mode may be entered either automatically in unison with the Signal Detect signal (Automatic method), or manually by setting a register bit (CPU Control method).

The signal detect feature and Ultra-Deep Sleep Mode are controlled via multiple bits in register 14h:

- Register 14h, bit [6] Ultra-Deep Sleep method: either Automatic or CPU Control.
- Register 14h, bit [5] Manually enter Ultra Deep Sleep Mode when CPU Control method is selected.
- Register 14h, bit [4] Enable R/W access to non-volatile versions of register 14h and bits [9:8] and [1:0] of register 13h. Set this bit when bit [3] is set.
- Register 14h, bit [3] Enable Ultra Deep Sleep Mode and SIGDET
- Register 14h, bit [1] Extend timing for SIGDET de-assertion and entry into Ultra-Deep Sleep Mode
- Register 14h, bit [0] SIGDET output polarity

### 3.21.1 CPU CONTROL METHOD (MIIM INTERFACE)

- KSZ8061RNB/RND drives SIGDET signal to the CPU.
- SIGDET defaults to force high, in order to not interfere with PHY initialization by the CPU. At power-on, the KSZ8061RNB/RND drives SIGDET high, without consideration of cable energy level.
- During initialization, the CPU writes data 0x0058 to register 14h
  - Bit [4] enables access to the non-volatile copy of register 14h
  - Enable Ultra-Deep Sleep Mode and SIGDET by setting register 14h, bit [3].
  - Automatic Ultra-Deep Sleep functionality is disabled by setting register 14h, bit [6].
- SIGDET is now enabled and will change state as cable energy changes.
- In response to the de-assertion of SIGDET, the CPU puts KSZ8061RNB/RND into Ultra-Deep Sleep mode by setting register 14h, bit [5]. To further reduce power, the CPU may disable the 1.2V supply to the KSZ8061RNB/RND.
- The KSZ8061RNB/RND will assert SIGDET when energy is detected on the cable.
- To activate the KSZ8061RNB/RND, the CPU enables the 1.2V supply and asserts hardware reset (RESET#) to the KSZ8061RNB/RND. Because the KSZ8061RNB/RND is completely reset, the registers must be re-initialized.
- Alternately, it is possible to maintain register access during Ultra-Deep Sleep Mode by preserving the 1.2V power supply and setting register 13h, bit [0] to enable slow oscillator mode. Ultra-Deep Sleep Mode can then be exited by writing to register 14h. The 1.2V supply results in increased power consumption.

### 3.21.2 AUTOMATIC STANDBY METHOD

- The board may be designed such that the KSZ8061RNB/RND SIGDET signal enables the 1.2V power supply to KSZ8061RNB/RND.
- At power-on, the KSZ8061RNB/RND drives SIGDET high, without consideration of cable energy level.
- During initialization, CPU writes data 0x001A or 0x0018 to register 14h.
  - Bit [4] enables access to the non-volatile copy of register 14h.
  - Enable Ultra-Deep Sleep Mode and SIGDET by setting register 14h, bit [3].
  - Automatic Ultra-Deep Sleep functionality is enabled by clearing register 14h, bit [6].
  - SIGDET timing bit [1] must be set unless the link partner is not using auto-negotiation, auto-MDI/MDI-X is disabled, and link is at 100 Mbps.
- When the KSZ8061RNB/RND detects signal loss, it automatically enters Ultra-Deep Sleep Mode and de-asserts SIGDET. SIGDET may be used to disable the 1.2V supply.
- When the KSZ8061RNB/RND detects a signal, it asserts SIGDET (which enables the 1.2V supply) and automatically wakes up. SIGDET may be used to wake up the CPU, which then re-initializes the KSZ8061RNB/RND.
- Alternatively, a hardware reset (RESET#) will bring the KSZ8061RNB/RND out of Ultra-Deep Sleep Mode.

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- The contents of register 14h and bits [9:8] and [1:0] of register 13h are preserved during Ultra-Deep Sleep Mode, but are lost during hardware reset.



## 4.0 REGISTER MAP

The register space within the KSZ8061RNB/RND consists of two distinct areas.

- Standard registers // Direct register access
- MDIO Manageable device (MMD) registers // Indirect register access

**TABLE 4-1: STANDARD REGISTERS**

| Register Number (hex)            | Description                                     |
|----------------------------------|---|
| <b>IEEE-Defined Registers</b>    |   |
| 0h                               | Basic Control                                   |
| 1h                               | Basic Status                                    |
| 2h                               | PHY Identifier 1                                |
| 3h                               | PHY Identifier 2                                |
| 4h                               | Auto-Negotiation Advertisement                  |
| 5h                               | Auto-Negotiation Link Partner Ability           |
| 6h                               | Auto-Negotiation Expansion                      |
| 7h                               | Auto-Negotiation Next Page                      |
| 8h                               | Auto-Negotiation Link Partner Next Page Ability |
| 9h - Ch                          | Reserved  |
| Dh                               | MMD Access Control Register                     |
| Eh                               | MMD Access Address Data Register                |
| Fh                               | Reserved  |
| <b>Vendor-Specific Registers</b> |   |
| 10h                              | Digital Control                                 |
| 11h                              | AFE Control 0                                   |
| 12h                              | AFE Control 1                                   |
| 13h                              | AFE Control 2                                   |
| 14h                              | AFE Control 3                                   |
| 15h                              | RXER Counter                                    |
| 16h                              | Operation Mode                                  |
| 17h                              | Operation Mode Strap Status                     |
| 18h                              | Expanded Control                                |
| 19h - 1Ah                        | Reserved  |
| 1Bh                              | Interrupt Control/Status                        |
| 1Ch                              | Function Control                                |
| 1Dh                              | LinkMD <sup>®</sup> Control/Status              |
| 1Eh                              | PHY Control 1                                   |
| 1Fh                              | PHY Control 2                                   |

**TABLE 4-2: MMD REGISTERS**

| Device Address (Hex) | Register Address (Hex) | Description    |
|----------------------|------------------------|----------------|
| 7h                   | 3Ch                    | Reserved       |
|                      | 3Dh                    | Reserved       |
| 1Bh                  | 0h                     | AFED Control   |
| 1Ch                  | ACh                    | Signal Quality |

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## 4.1 Standard Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 standard. Within this address space, the first 16 registers (0h to Fh) are defined according to the IEEE specification, while the remaining 16 registers (10h to 1Fh) are defined specific to the PHY vendor.

**TABLE 4-3: STANDARD REGISTER DESCRIPTION**

| Address                            | Name                     | Description   | Mode<br>(Note 1) | Default   |
|------------------------------------|--------------------------|---|------------------|---|
| <b>Register 0h - Basic Control</b> |                          |   |                  |   |
| 0.15                               | Reset                    | 1 = Software reset<br>0 = Normal operation<br>This bit is self-cleared after a '1' is written to it.  | RW/SC            | 0   |
| 0.14                               | Loopback                 | 1 = Loop-back mode (RMII TX to RMII RX. Line side is disconnected.)<br>0 = Normal operation<br>Loopback must be enabled both here and in register 1Ch.  | RW               | 0   |
| 0.13                               | Speed Select             | 1 = 100 Mbps<br>0 = 10 Mbps<br>This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).  | RW               | 1   |
| 0.12                               | Auto-Negotiation Enable  | 1 = Enable auto-negotiation process<br>0 = Disable auto-negotiation process<br>If enabled, auto-negotiation result overrides settings in register 0.13 and 0.8.   | RW               | Set by AUTONEG strapping pin.<br>See <a href="#">Table 1-2</a> for details. |
| 0.11                               | Power Down               | 1 = Power down mode<br>0 = Normal operation<br>If software reset (register 0.15) is used to exit Power Down mode (register 0.11 = 1), two software reset writes (register 0.15 = 1) are required. First write clears Power Down mode; second write resets chip and re-latches the pin strapping pin values. | RW               | 0   |
| 0.10                               | Isolate                  | 1 = Electrical isolation of PHY from RMII<br>0 = Normal operation   | RW               | 0   |
| 0.9                                | Restart Auto-Negotiation | 1 = Restart auto-negotiation process<br>0 = Normal operation.<br>This bit is self-cleared after a '1' is written to it.   | RW/SC            | 0   |
| 0.8                                | Duplex Mode              | 1 = Full-duplex<br>0 = Half-duplex  | RW               | 1   |
| 0.7                                | Collision Test           | 1 = Enable COL test<br>0 = Disable COL test   | RW               | 0   |
| 0.6:0                              | Reserved                 | —   | RO               | 000_0000  |
| <b>Register 1h - Basic Status</b>  |                          |   |                  |   |
| 1.15                               | 100BASE-T4               | 1 = T4 capable<br>0 = Not T4 capable  | RO               | 0   |
| 1.14                               | 100BASE-TX Full-Duplex   | 1 = Capable of 10 Mbps half-duplex<br>0 = Not capable of 10 Mbps half-duplex  | RO               | 1   |
| 1.13                               | 100BASE-TX Half-Duplex   | 1 = Capable of 10 Mbps half-duplex<br>0 = Not capable of 10 Mbps half-duplex  | RO               | 1   |
| 1.12                               | 10BASE-TX Full-Duplex    | 1 = Capable of 10 Mbps half-duplex<br>0 = Not capable of 10 Mbps half-duplex  | RO               | 1   |

**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address   | Name                      | Description  | Mode<br>(Note 1) | Default                    |
|---|---------------------------|--|------------------|----------------------------|
| 1.11  | 10BASE-TX Half-Duplex     | 1 = Capable of 10 Mbps half-duplex<br>0 = Not capable of 10 Mbps half-duplex   | RO               | 1                          |
| 1.10:7  | Reserved                  | —  | RO               | 000_0                      |
| 1.6   | No Preamble               | 1 = Preamble suppression acceptable<br>0 = Normal preamble required  | RW               | 1                          |
| 1.5   | Auto-Negotiation Complete | 1 = Auto-negotiation process completed<br>0 = Auto-negotiation process not completed   | RO               | 0                          |
| 1.4   | Remote Fault              | 1 = Remote fault<br>0 = No remote fault  | RO/LH            | 0                          |
| 1.3   | Auto-Negotiation Ability  | 1 = Capable to perform auto-negotiation<br>0 = Not capable to perform auto-negotiation   | RO               | 1                          |
| 1.2   | Link Status               | 1 = Link is up<br>0 = Link is down   | RO/LL            | 0                          |
| 1.1   | Jabber Detect             | 1 = Jabber detected<br>0 = Jabber not detected (default is low)  | RO/LH            | 0                          |
| 1.0   | Extended Capability       | 1 = Supports extended capabilities registers   | RO               | 1                          |
| <b>Register 2h - PHY Identifier 1</b>               |                           |  |                  |                            |
| 2.15.0  | PHY ID Number             | Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)  | RO               | 0022h                      |
| <b>Register 3h - PHY Identifier 2</b>               |                           |  |                  |                            |
| 3.15:10   | PHY ID Number             | Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex) | RO               | 0001_01                    |
| 3.0:4   | Model Number              | Six bit manufacturer's model number  | RO               | 01_0111                    |
| 3.3:0   | Revision Number           | Four bit manufacturer's revision number  | RO               | Indicates silicon revision |
| <b>Register 4h - Auto-Negotiation Advertisement</b> |                           |  |                  |                            |
| 4.15  | NextPage                  | 1 = Next page capable<br>0 = No next page capability   | RW               | 1                          |
| 4.14  | Reserved                  | —  | RO               | 0                          |
| 4.13  | Remote Fault              | 1 = Remote fault supported<br>0 = No remote fault  | RW               | 0                          |
| 4.12  | Reserved                  | —  | RO               | 0                          |
| 4.11:10   | Pause                     | [00] = No PAUSE<br>[10] = Asymmetric PAUSE<br>[01] = Symmetric PAUSE<br>[11] = Asymmetric & Symmetric PAUSE                        | RW               | 00                         |
| 4.9   | 100BASE-T4                | 1 = T4 capable<br>0 = No T4 capability   | RO               | 0                          |
| 4.8   | 100BASE-TX Full-Duplex    | 1 = 100 Mbps full-duplex capable<br>0 = No 100 Mbps full-duplex capability   | RW               | 1                          |
| 4.7   | 100BASE-TX Half-Duplex    | 1 = 100 Mbps half-duplex capable<br>0 = No 100 Mbps half-duplex capability   | RW               | 1                          |

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**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address  | Name                               | Description  | Mode<br>(Note 1) | Default       |
|--|------------------------------------|--|------------------|---------------|
| 4.6  | 100BASE-TX Full-Duplex             | 1 = Capable of 10 Mbps half-duplex<br>0 = Not capable of 10 Mbps half-duplex                                   | RW               | 1             |
| 4.5  | 100BASE-TX Half-Duplex             | 1 = Capable of 10 Mbps half-duplex<br>0 = Not capable of 10 Mbps half-duplex                                   | RW               | 1             |
| 4.4:0  | Selector Field                     | [00001] = IEEE 802.3   | RW               | 0_0001        |
| <b>Register 5h - Auto-Negotiation Link Partner Ability</b> |                                    |  |                  |               |
| 5.15   | Next Page                          | 1 = Next page capable<br>0 = No next page capability   | RO               | 0             |
| 5.14   | Acknowledge                        | 1 = Link code word received from partner<br>0 = Link code word not yet received                                | RO               | 0             |
| 5.13   | Remove Fault                       | 1 = Remote fault detected<br>0 = No remote fault   | RO               | 0             |
| 5.12   | Reserved                           | —  | RO               | 0             |
| 5.11:10  | Pause                              | [00] = No PAUSE<br>[10] = Asymmetric PAUSE<br>[01] = Symmetric PAUSE<br>[11] = Asymmetric & Symmetric PAUSE    | RO               | 00            |
| 5.9  | 100BASE-T4                         | 1 = T4 capable<br>0 = No T4 capability   | RO               | 0             |
| 5.8  | 100BASE-TX Full-Duplex             | 1 = 100 Mbps full-duplex capable<br>0 = No 100 Mbps full-duplex capability                                     | RO               | 0             |
| 5.7  | 100BASE-TX Half-Duplex             | 1 = 100 Mbps half-duplex capable<br>0 = No 100 Mbps half-duplex capability                                     | RO               | 0             |
| 5.6  | 10BASE-TX Full-Duplex              | 1 = 10 Mbps full-duplex capable<br>0 = No 10 Mbps full-duplex capability                                       | RO               | 0             |
| 5.5  | 10BASE-TX Half-Duplex              | 1 = 10 Mbps half-duplex capable<br>0 = No 10 Mbps half-duplex capability                                       | RO               | 0             |
| 5.4:0  | Selector Field                     | [00001] = IEEE 802.3   | RO               | 0_0001        |
| <b>Register 6h - Auto-Negotiation Expansion</b>            |                                    |  |                  |               |
| 6.15:5   | Reserved                           | —  | RO               | 0000_0000_000 |
| 6.4  | Parallel Detection Fault           | 1 = Fault detected by parallel detection<br>0 = No fault detected by parallel detection                        | RO/LH            | 0             |
| 6.3  | Link Partner Next Page Able        | 1 = Link partner has next page capability<br>0 = Link partner does not have next page capability               | RO               | 0             |
| 6.2  | Next Page Able                     | 1 = Local device has next page capability<br>0 = Local device does not have next page capability               | RO               | 1             |
| 6.1  | Page Received                      | 1 = New page received<br>0 = New page not received yet   | RO/LH            | 0             |
| 6.0  | Link Partner Auto-Negotiation Able | 1 = Link partner has auto-negotiation capability<br>0 = Link partner does not have auto-negotiation capability | RO               | 0             |
| <b>Register 7h - Auto-Negotiation Next Page</b>            |                                    |  |                  |               |
| 7.15   | Next Page                          | 1 = Additional Next Page(s) will follow<br>0 = Last page   | RW               | 0             |
| 7.14   | Reserved                           | —  | RO               | 0             |

**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address   | Name                 | Description  | Mode<br>(Note 1) | Default                 |
|---|----------------------|--|------------------|-------------------------|
| 7.13  | Message Page         | 1 = Message page<br>0 = Unformatted page   | RW               | 1                       |
| 7.12  | Acknowledge2         | 1 = Will comply with message<br>0 = Cannot comply with message   | RW               | 0                       |
| 7.11  | Toggle               | 1 = Previous value of the transmitted link code word equal to logic one<br>0 = Logic zero  | RO               | 0                       |
| 7.10:0  | Message Field        | 11-bit wide field to encode 2048 messages  | RW               | 000_0000_0001           |
| <b>Register 8h - Link Partner Next Page Ability</b>   |                      |  |                  |                         |
| 8.15  | Next Page            | 1 = Additional Next Page(s) will follow<br>0 = Last page   | RO               | 0                       |
| 8.14  | Acknowledge          | 1 = Successful receipt of link word<br>0 = No successful receipt of link word  | RO               | 0                       |
| 8.13  | Message Page         | 1 = Message page<br>0 = Unformatted page   | RO               | 0                       |
| 8.12  | Acknowledge2         | 1 = Able to act on the information<br>0 = Not able to act on the information   | RO               | 0                       |
| 8.11  | Toggle               | 1 = Previous value of transmitted link code word equal to logic zero<br>0 = Previous value of transmitted link code word equal to logic one                  | RO               | 0                       |
| 8.10:0  | Message Field        | —  | RO               | 000_0000_0000           |
| <b>Register Dh - MMD Access Control Register</b>      |                      |  |                  |                         |
| D.15:14   | Function             | 00 = address<br>01 = data, no post increment<br>10 = data, post increment on reads and writes<br>11 = data, post increment on writes only                    | RW               | 00                      |
| D.13:5  | Reserved             | Write as 0, ignore on read   | RW               | 00_0000_000             |
| D.4:0   | DEVAD                | Device address   | RW               | 0_0000                  |
| <b>Register Eh - MMD Access Address Data Register</b> |                      |  |                  |                         |
| E.15:0  | Address Data         | If D.15:14 = 00, this is MMD DEVAD's address register.<br>Otherwise, this is MMD DEVAD's data register as indicated by the contents of its address register. | RW               | 0000_0000_0000_00<br>00 |
| <b>Register 10h - Digital Control Register</b>        |                      |  |                  |                         |
| 10.15:5   | Reserved             | —  | RW               | 0000_0000_000           |
| 10.4  | PLL off in EDPD Mode | This mode may optionally be combined with EDPD mode for additional power reduction.<br>1 = PLL is off in EDPD mode<br>0 = PLL is on in EDPD mode             | RW               | 0                       |
| 10.3:0  | Reserved             | —  | RW               | 0000                    |
| <b>Register 11h - AFE Control 0 Register</b>          |                      |  |                  |                         |
| 11.15:7   | Reserved             | —  | RW               | 0000_0000_0             |

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**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address                                      | Name   | Description  | Mode<br>(Note 1) | Default           |
|--|--|--|------------------|-------------------|
| 11.6   | Slow Oscillator Mode                           | This mode substitutes the 25 MHz clock with a slow oscillator clock, to save oscillator power during power down.<br>1 = Slow Oscillator mode enabled<br>0 = Slow Oscillator mode disabled  | RW               | 0                 |
| 11.5:0                                       | Reserved                                       | —  | RW               | 00_0000           |
| <b>Register 12h - AFE Control 1 Register</b> |  |  |                  |                   |
| 12.15:12                                     | 100BT amplitude                                | Trim 100BT TX amplitude<br>Sequence of values:<br>1000 = maximum amplitude<br>1001<br>1010<br>1011<br>1100<br>1101<br>1110<br>1111<br>0000 = default<br>0001<br>0010<br>0011<br>0100<br>0101<br>0110<br>0111 = minimum amplitude   | RW               | 0000              |
| 12.11:0                                      | Reserved                                       | —  | RW               | 0000_0000_0000    |
| <b>Register 13h - AFE Control 2 Register</b> |  |  |                  |                   |
| 13.15  | LinkMD Detector Threshold                      | Sets the threshold for the LinkMD pulse detector. Use high threshold with the large LinkMD pulse, and the low threshold with the small LinkMD pulse.<br>Also see MMD address 1Bh, register 0h bits [7:4].<br>1 = Enable high threshold comparator<br>0 = Disable high threshold comparator     | RW               | 0                 |
| 13.14:1                                      | Reserved                                       | —  | RW               | 000_0000_0000_000 |
| 13.0   | Slow Oscillator Mode for Ultra-Deep Sleep Mode | This mode substitutes the 25 MHz clock with a slow oscillator clock, to save oscillator power if register access is required during Ultra-Deep Sleep Mode. Note that the 1.2V supply is required if this mode is used.<br>1 = Slow Oscillator mode enabled<br>0 = Slow Oscillator mode disable | RW               | 0                 |
| <b>Register 14h - AFE Control Register 3</b> |  |  |                  |                   |
| 14.15:7                                      | Reserved                                       | —  | RW               | 0000_0000_0       |
| 14.6   | Ultra-Deep Sleep method                        | 1 = CPU Control method. Entry into Ultra-Deep Sleep Mode determined by value of register bit 14.5<br>0 = Automatic method. Enter into Ultra-Deep Sleep Mode automatically when no cable energy is detected   | RW               | 0                 |

**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address                              | Name                                    | Description   | Mode<br>(Note 1) | Default                     |
|--------------------------------------|---|---|------------------|-----------------------------|
| 14.5                                 | Manual Ultra-Deep Sleep Mode            | 1 = Enter into Standby Mode<br>0 = Normal Mode<br>This bit is used to enter Ultra-Deep Sleep Mode when the CPU Control method is selected in bit 14.6. To exit Ultra-Deep Sleep Mode, a hardware reset is required.   | RW               | 0                           |
| 14.4                                 | NV Register Access                      | 1 = Enable the non-volatile copy of register 14h and bits [9:8] and [1:0] of 13h.<br>0 = Disable access to non-volatile registers<br>When Ultra-Deep Sleep Mode is enabled, this bit must be set to 1.  | RW               | 0                           |
| 14.3                                 | Ultra-Deep Sleep Mode and SIGDET Enable | 1 = Ultra-Deep Sleep Mode is enabled (but not necessarily entered), and SIGDET indicates cable energy detected<br>0 = Ultra-Deep Sleep Mode is disabled, and SIGDET output signal is forced true.   | RW               | 0                           |
| 14.2                                 | Disable RX internal termination         | 1 = Disable RX internal termination<br>0 = Enable RX internal termination<br>[Has no effect on TX internal termination.]  | RW               | 0                           |
| 14.1                                 | Signal Detect de-assertion timing delay | When Ultra-Deep Sleep Mode is enabled, this bit determines the delay from loss of cable energy to de-assertion of SIGDET. When automatic method is selected for Ultra-Deep Sleep Mode, this delay also applies to powering down.<br>1 = Increased delay. This setting is required to allow automatic exiting of Ultra Deep Sleep Mode (automatic method) if the link partner auto-negotiation is enabled, if auto-MDI/MDI-X is enabled, or if linking at 10BASE-T.<br>0 = Minimum delay. When using the Automatic method for Ultra-Deep Sleep Mode, use this setting only if the link partner's auto-negotiation is disabled, auto-MDI/MDI-X is disabled, and linking is at 100BASE-TX. This setting may also be used for CPU Control method. | RW               | 0                           |
| 14.0                                 | Signal Detect polarity                  | 1 = SIGDET is active low (low = signal detected)<br>0 = SIGDET is active high (high = signal detected)  | RW               | 0                           |
| <b>Register 15h - RXER Counter</b>   |   |   |                  |                             |
| 15.15:0                              | RXER Counter                            | Receive error counter for symbol error frames   | RO/SC            | 0000h                       |
| <b>Register 16h - Operation Mode</b> |   |   |                  |                             |
| 16.15:13                             | Reserved                                | —   | RW               | 000                         |
| 16.12                                | QWF disable                             | 1 = Disable Quiet-WIRE Filtering<br>0 = Enable Quiet-WIRE Filtering<br>Quiet-WIRE filtering can be disabled by setting this bit. However, it cannot be enabled by clearing this bit to 0.   | RW               | Strapping input at RXER pin |

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**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address   | Name                                   | Description  | Mode<br>(Note 1) | Default        |
|---|--|--|------------------|----------------|
| 16.11:0   | Reserved                               | —  | RW               | 0000_0000_0000 |
| <b>Register 17h - Operation Mode Strap Status</b> |  |  |                  |                |
| 17.15:13  | PHYAD[2:0] strap-in status             | [000] = Strap to PHY Address 0<br>[001] = Strap to PHY Address 1<br>[010] = Strap to PHY Address 2<br>[011] = Strap to PHY Address 3<br>[100] = Strap to PHY Address 4<br>[101] = Strap to PHY Address 5<br>[110] = Strap to PHY Address 6<br>[111] = Strap to PHY Address 7 | RO               | —              |
| 17.12:9   | Reserved                               | —  | RO               | —              |
| 17.8  | QWF strap-in status                    | 1 = Strap to enable Quiet-WIRE Filtering   | RO               | —              |
| 17.7  | Reserved                               | —  | RO               | 0              |
| 17.6  | RMII B-to-B strap-in status            | 1 = Strap to RMII Back-to-Back mode  | RO               | —              |
| 17.5  | NAND Tree strap-in status              | 1 = Strap to NAND Tree mode  | RO               | —              |
| 17.4:2  | Reserved                               | —  | RO               | 0              |
| 17.1  | RMII strap-in status                   | 1 = Strap to RMII normal mode  | RO               | —              |
| 17.0  | Reserved                               | —  | RO               | 0              |
| <b>Register 18h - Expanded Control</b>            |  |  |                  |                |
| 18.15:12  | Reserved                               | —  | RW               | 0000           |
| 18.11   | Energy Detect Power Down Mode disable  | 1 = Disable Energy Detect Power Down (EDPD) Mode<br>0 = Enable EDPD Mode   | RW               | 1              |
| 18.10   | RX PHY Latency                         | 1 = Variable RX PHY latency with no preamble suppression<br>0 = Fixed RX PHY latency with possible suppression of one preamble octet   | RW               | 0              |
| 18.9:7  | Reserved                               | —  | RW               | 00_0           |
| 18.6  | Enable 10BT Preamble                   | When in Back-to-Back Mode and in 10BASE-T, this bit must be set.   | RW               | 0              |
| 18.5:0  | Reserved                               | —  | RW               | 00_0001        |
| <b>Register 1Bh - Interrupt Control/Status</b>    |  |  |                  |                |
| 1B.15   | Jabber Interrupt Enable                | 1 = Enable Jabber Interrupt<br>0 = Disable Jabber Interrupt  | RW               | 0              |
| 1B.14   | Receive Error Interrupt Enable         | 1 = Enable Receive Error Interrupt<br>0 = Disable Receive Error Interrupt  | RW               | 0              |
| 1B.13   | Page Received Interrupt Enable         | 1 = Enable Page Received Interrupt<br>0 = Disable Page Received Interrupt  | RW               | 0              |
| 1B.12   | Parallel Detect Fault Interrupt Enable | 1 = Enable Parallel Detect Fault Interrupt<br>0 = Disable Parallel Detect Fault Interrupt  | RW               | 0              |



**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address   | Name                                      | Description   | Mode<br>(Note 1) | Default      |
|---|---|---|------------------|--------------|
| 1B.11   | Link Partner Acknowledge Interrupt Enable | 1 = Enable Link Partner Acknowledge Interrupt<br>0 = Disable Link Partner Acknowledge Interrupt   | RW               | 0            |
| 1B.10   | Link Down Interrupt Enable                | 1 = Enable Link Down Interrupt<br>0 = Disable Link Down Interrupt   | RW               | 0            |
| 1B.9  | Remote Fault Interrupt Enable             | 1 = Enable Remote Fault Interrupt<br>0 = Disable Remote Fault Interrupt   | RW               | 0            |
| 1B.8  | Link Up Interrupt Enable                  | 1 = Enable Link Up Interrupt<br>0 = Disable Link Up Interrupt   | RW               | 0            |
| 1B.7  | Jabber Interrupt                          | 1 = Jabber occurred<br>0 = Jabber did not occurred  | RO/SC            | 0            |
| 1B.6  | Receive Error Interrupt                   | 1 = Receive Error occurred<br>0 = Receive Error did not occurred  | RO/SC            | 0            |
| 1B.5  | Page Receive Interrupt                    | 1 = Page Receive occurred<br>0 = Page Receive did not occur   | RO/SC            | 0            |
| 1B.4  | Parallel Detect Fault Interrupt           | 1 = Parallel Detect Fault occurred<br>0 = Parallel Detect Fault did not occur   | RO/SC            | 0            |
| 1B.3  | Link Partner Acknowledge Interrupt        | 1 = Link Partner Acknowledge occurred<br>0 = Link Partner Acknowledge did not occur   | RO/SC            | 0            |
| 1B.2  | Link Down Interrupt                       | 1 = Link Down occurred<br>0 = Link Down did not occur   | RO/SC            | 0            |
| 1B.1  | Remote Fault Interrupt                    | 1 = Remote Fault occurred<br>0 = Remote Fault did not occur   | RO/SC            | 0            |
| 1B.0  | Link Up Interrupt                         | 1 = Link Up occurred<br>0 = Link Up did not occur   | RO/SC            | 0            |
| <b>Register 1Ch - Function Control</b>                  |   |   |                  |              |
| 1C.15:6   | Reserved                                  | —   | RW               | 0000_0000_00 |
| 1C.5  | Local Loopback Option                     | 1 = Enable local loopback<br>0 = Disable local loopback<br>Local loopback must be enabled both here and in register 0h.   | RW               | 0            |
| 1C.4:0  | Reserved                                  | —   | RW               | 1_0000       |
| <b>Register 1Dh - LinkMD<sup>®</sup> Control/Status</b> |   |   |                  |              |
| 1D.15   | Cable Diagnostic Test Enable              | 1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared.<br>0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read. | RW/SC            | 0            |
| 1D.14:13  | Cable Diagnostic Test Result              | [00] = normal condition<br>[01] = open condition has been detected in cable<br>[10] = short condition has been detected in cable<br>[11] = cable diagnostic test has failed                           | RO               | 00           |

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**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address                             | Name                        | Description   | Mode<br>(Note 1) | Default                                  |
|-------------------------------------|-----------------------------|---|------------------|--|
| 1D.12                               | Short Cable Indicator       | 1 = Short cable (<10 meter) has been detected by LinkMD <sup>®</sup> .  | RO               | 0  |
| 1D.11:9                             | Reserved                    | —   | RW               | 000                                      |
| 1D.8:0                              | Cable Fault Counter         | Distance to fault   | RO               | 0_0000_0000                              |
| <b>Register 1Eh - PHY Control 1</b> |                             |   |                  |  |
| 1E.15:10                            | Reserved                    | —   | RO               | 0000_00                                  |
| 1E.9                                | Enable Pause (Flow Control) | 1 = Flow control capable<br>0 = No flow control capability  | RO               | 0  |
| 1E.8                                | Link Status                 | 1 = Link is up<br>0 = Link is down  | RO               | —  |
| 1E.7                                | Polarity Status             | 1 = Polarity is reversed<br>0 = Polarity is not reversed  | RO               | —  |
| 1E.6                                | Reserved                    | —   | RO               | 0  |
| 1E.5                                | MDI/MDI-X State             | 1 = MDI-X<br>0 = MDI  | RO               | —  |
| 1E.4                                | Energy Detect               | 1 = Presence of signal on receive differential pair<br>0 = No signal detected on receive differential pair  | RO               | —  |
| 1E.3                                | PHY Isolate                 | 1 = PHY in isolate mode<br>0 = PHY in normal operation<br>[Same as register bit 0.10]   | RW               | 0  |
| 1E.2:0                              | Operation Mode Indication   | [000] = still in auto-negotiation<br>[001] = 10BASE-T half-duplex<br>[010] = 100BASE-TX half-duplex<br>[011] = reserved<br>[100] = reserved<br>[101] = 10BASE-T full-duplex<br>[110] = 100BASE-TX full-duplex<br>[111] = reserved | RO               | —  |
| <b>Register 1Fh - PHY Control 2</b> |                             |   |                  |  |
| 1F.15                               | HP_MDIX                     | 1 = HP Auto MDI/MDI-X mode<br>0 = Auto MDI/MDI-X mode   | RW               | 1  |
| 1F.14                               | MDI/MDI-X Select            | When Auto MDI/MDI-X is disabled,<br>1 = MDI-X Mode<br>Transmit on RXP,RXM andReceive on TXP,TXM<br>0 = MDI Mode<br>Transmit on TXP,TXM andReceive on RXP,RXM  | RW               | 0  |
| 1F.13                               | Pair Swap Disable           | 1 = Disable auto MDI/MDI-X<br>0 = Enable auto MDI/MDI-X   | RW               | Value determined by pin strapping option |

**TABLE 4-3: STANDARD REGISTER DESCRIPTION (CONTINUED)**

| Address | Name                    | Description   | Mode<br>(Note 1) | Default |
|---------|-------------------------|---|------------------|---------|
| 1F.12   | Reserved                | —   | RW               | 0       |
| 1F.11   | Force Link              | 1 = Force link pass<br>0 = Normal link operation<br>This bit bypasses the control logic and allow transmitter to send pattern even if there is no link. | RW               | 0       |
| 1F.10   | Power Saving            | 1 = Enable power saving<br>0 = Disable power saving   | RW               | 0       |
| 1F.9    | Interrupt Level         | 1 = Interrupt pin active high<br>0 = Interrupt pin active low   | RW               | 0       |
| 1F.8    | Enable Jabber           | 1 = Enable jabber counter<br>0 = Disable jabber counter   | RW               | 1       |
| 1F.7:6  | Reserved                | -   | RW               | 00      |
| 1F.5:4  | LED Mode                | [00] = LED1: Speed, LED0: Link / Activity<br>[01] = LED1: Activity, LED0: Link<br>[10] = reserved<br>[11] = reserved                                    | RW               | 00      |
| 1F.3    | Disable Transmitter     | 1 = Disable transmitter<br>0 = Enable transmitter   | RW               | 0       |
| 1F.2    | Remote Loopback         | 1 = Remote (analog) loopback is enabled<br>0 = Normal mode  | RW               | 0       |
| 1F.1    | Enable SQE Test         | 1 = Enable SQE test<br>0 = Disable SQE test   | RW               | 0       |
| 1F.0    | Disable Data Scrambling | 1 = Disable scrambler<br>0 = Enable scrambler   | RW               | 0       |

**Note 1:** RW = Read/Write.  
RO = Read only.  
SC = Self-cleared.  
LH = Latch high.  
LL = Latch low.

## 4.2 MMD Registers

MMD registers provide indirect read/write access to up to 32 MMD Device Addresses with each device supporting up to 65,536 16-bit registers, as defined in clause 22 of the IEEE 802.3 specification. The KSZ8061RNB/RND, however, uses only a small fraction of the available registers. See [Register Map](#) for a list of supported MMD device addresses and their associated register addresses.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- Standard register Dh - MMD Access - Control
- Standard register Eh - MMD Access - Register/Data

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**TABLE 4-4: MMD REGISTERS**

| Address   | Name         | Description  | Mode | Default     |
|---|--------------|--|------|-------------|
| <b>Register Dh - MMD Access Control Register</b>      |              |  |      |             |
| D.15:14   | Function     | 00 = address<br>01 = data, no post increment<br>10 = data, post increment on reads and writes<br>11 = data, post increment on writes only  | RW   | 00          |
| D.13:5  | Reserved     | Write as 0, ignore on read   | RW   | 00_0000_000 |
| D.4:0   | DEVAD        | These five bits set the MMD device address   | RW   | 0_0000      |
| <b>Register Eh - MMD Access Address Data Register</b> |              |  |      |             |
| E.15:0  | Address/Data | When register Dh, bits [15:14] = 00, this register contains the MMD DEVAD's address register.<br>Otherwise, this register contains the MMD DEVAD's data register as indicated by the contents of its address register. | RW   | 0000_0000_0 |

Examples:

**MMD Register Write**

Write MMD - Device Address 7h, Register 3Ch = 0002h.

1. Write Register Dh with 0007h // Set up register address for MMD - Device Address 7h.
2. Write Register Eh with 003Ch // Select register 3Ch of MMD - Device Address 7h.
3. Write Register Dh with 4007h // Select register data for MMD - Device Address 7h, Register 3Ch.
4. Write Register Eh with 0002h // Write value 0002h to MMD - Device Address 7h, Register 3Ch.

**MMD Register Read**

Read MMD - Device Address 1Fh, Register 19h - 1Bh

1. Write Register Dh with 001Fh // Set up register address for MMD - Device Address 1Fh.
2. Write Register Eh with 0019h // Select register 19h of MMD - Device Address 1Fh.
3. Write Register Dh with 801Fh // Select register data for MMD - Device Address 1Fh, Register 19h  
// with post increments.
4. Read Register Eh // Read data in MMD - Device Address 1Fh, Register 19h.
5. Read Register Eh // Read data in MMD - Device Address 1Fh, Register 1Ah.
6. Read Register Eh // Read data in MMD - Device Address 1Fh, Register 1Bh.

**TABLE 4-5: MMD REGISTERS**

| Address  | Name                     | Description   | Mode | Default   |
|--|--------------------------|---|------|-----------|
| <b>MMD Address 7h, Register 3Ch - Reserved</b>                 |                          |   |      |           |
| 7.3C.15:8  | Reserved                 | Reserved  | RW   | 0         |
| 7.3C.7:3   | Reserved                 | Reserved  | RW   | 0         |
| 7.3C.2   | Reserved                 | Reserved  | RW   | 0         |
| 7.3C.1   | Reserved                 | Reserved  | RW   | 0         |
| 7.3C.0   | Reserved                 | Reserved  | RW   | 0         |
| <b>MMD Address 7h, Register 3Dh - Reserved</b>                 |                          |   |      |           |
| 7.3D.15:3  | Reserved                 | Reserved  | RO   | 0         |
| 7.3D.2   | Reserved                 | Reserved  | RO   | 0         |
| 7.3D.1   | Reserved                 | Reserved  | RO   | 0         |
| 7.3D.0   | Reserved                 | Reserved  | RO   | 0         |
| <b>MMD Address 1Bh, Register 0h - AFED Control Register</b>    |                          |   |      |           |
| 1B.0.15:8  | Reserved                 | Reserved  | RW   | 0000_0000 |
| 1B.0.7:4   | LinkMD Pulse Amplitude   | Sets the amplitude of the LinkMD pulse. Default value (0x2) is a small pulse. Set to 0x7 for a large pulse. Also see register 13h bit [15]. | RW   | 0010      |
| 1B.0.3:0   | Reserved                 | Reserved  | RW   | 0000      |
| <b>MMD Address 1Ch, Register ACh - Signal Quality Register</b> |                          |   |      |           |
| 1C.AC.15   | Reserved                 | Reserved  | RO   |           |
| 1C.AC.14:8   | Signal Quality Indicator | SQI indicates relative quality of the signal. A lower value indicates better signal quality.  | RO   |           |
| 1C.AC.7:0  | Reserved                 | Reserved  | RO   |           |

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## 5.0 OPERATIONAL CHARACTERISTICS

### 5.1 Absolute Maximum Ratings\*

|  |                                |
|--|--------------------------------|
| Supply Voltage (VDDIO, AVDDH) .....        | -0.5V to +5.0V                 |
| (VDDL, AVDDL).....                         | -0.5V to +1.8V                 |
| Input Voltage (all inputs).....            | -0.5V to +5.0V                 |
| Output Voltage (all inputs).....           | -0.5V to +5.0V                 |
| Lead Temperature (soldering, 10sec.).....  | +260°C                         |
| Storage Temperature (T <sub>S</sub> )..... | -55°C to +150°C                |
| Lead Temperature Range.....                | Refer to JEDEC Spec. J-STD-020 |
| HBM ESD Rating.....                        | 5 kV                           |

\* Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

### 5.2 Operating Conditions\*\*

#### Supply Voltage

|                     |                    |
|---------------------|--------------------|
| (AVDDH @ 3.3V)..... | +3.135V to +3.465V |
| (VDDIO @ 3.3V)..... | +3.135V to +3.465V |
| (VDDIO @ 2.5V)..... | +2.375V to +2.625V |
| (VDDL, AVDDL).....  | +1.14V to +1.26V   |

#### Ambient Temperature

|  |                 |
|--|-----------------|
| (T <sub>A</sub> , Extended) .....                            | -40°C to +105°C |
| Maximum Junction Temperature (T <sub>J</sub> max).....       | +125°C          |
| Thermal Resistance (Θ <sub>JA</sub> , 32-QFN, 32-WQFN) ..... | 34°C/W          |
| Thermal Resistance (Θ <sub>JC</sub> , 32-QFN, 32-WQFN) ..... | 6°C/W           |

\*\* The device is not guaranteed to function outside its operating ratings.

## 6.0 ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = 25°C, bold values indicate -40°C ≤ T<sub>A</sub> ≤ +85°C, unless noted.

| TABLE 6-1: ELECTRICAL CHARACTERISTICS   |                               |   |                               |                                       |      |       |
|---|-------------------------------|---|-------------------------------|---------------------------------------|------|-------|
| Symbol  | Parameter                     | Condition   | Min.                          | Typ.                                  | Max. | Units |
| <b>Supply Current for VDDL, AVDDL</b>   |                               |   |                               |                                       |      |       |
| I <sub>CORE</sub>   | 1.2V Current for VDDL + AVDDL | No link, attempting to auto-negotiate   | —                             | 59                                    | —    | mA    |
|   |                               | 100BASE-TX full-duplex at 100% utilization  | —                             | 45                                    | —    |       |
|   |                               | 100BASE-TX link up, no traffic  | —                             | 45                                    | —    |       |
|   |                               | 10BASE-T full-duplex at 100% utilization  | —                             | 17                                    | —    |       |
|   |                               | 10BASE-T link up, no traffic  | —                             | 17                                    | —    |       |
|   |                               | Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)                             | —                             | 16                                    | —    |       |
|   |                               | EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)                           | —                             | 0.7                                   | —    |       |
|   |                               | Power Down mode (reg. 0h.11 = 1)  | —                             | 0.5                                   | —    |       |
|   |                               | Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1) | —                             | 0.05                                  | —    |       |
|   |                               | Ultra-Deep Sleep mode with 1.2V (reg. 14h = 0x0078)   | —                             | 46                                    | —    | μA    |
|   |                               | Ultra-Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)                                      | —                             | 0                                     | —    |       |
|   |                               | I <sub>VDDIO_2.5</sub>  | 2.5V Current for Digital I/Os | No link, attempting to auto-negotiate | —    | 3.3   |
| 100BASE-TX full-duplex at 100% utilization  | —                             |   |                               | 5.9                                   | —    |       |
| 100BASE-TX link up, no traffic  | —                             |   |                               | 3.3                                   | —    |       |
| 10BASE-T full-duplex at 100% utilization  | —                             |   |                               | 1.0                                   | —    |       |
| 10BASE-T link up, no traffic  | —                             |   |                               | 0.6                                   | —    |       |
| Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)                             | —                             |   |                               | 3.9                                   | —    |       |
| EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)                           | —                             |   |                               | 0.23                                  | —    |       |
| Power Down mode (reg. 0h.11 = 1)  | —                             |   |                               | 0.23                                  | —    |       |
| Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1) | —                             |   |                               | 0.10                                  | —    |       |
| Ultra-Deep Sleep mode with 1.2V (reg. 14h = 0x0078)   | —                             |   |                               | 100                                   | —    | μA    |
| Ultra-Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)                                      | —                             |   |                               | 0.01                                  | —    |       |

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**TABLE 6-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

| Symbol   | Parameter                     | Condition   | Min. | Typ. | Max. | Units |
|--|-------------------------------|---|------|------|------|-------|
| I <sub>VDDIO_3.3</sub>   | 3.3V Current for Digital I/Os | No link, attempting to auto-negotiate   | —    | 6.5  | —    | mA    |
|  |                               | 100BASE-TX full-duplex at 100% utilization  | —    | 11   | —    |       |
|  |                               | 100BASE-TX link up, no traffic  | —    | 6.5  | —    |       |
|  |                               | 10BASE-T full-duplex at 100% utilization  | —    | 1.7  | —    |       |
|  |                               | 10BASE-T link up, no traffic  | —    | 1.1  | —    |       |
|  |                               | Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)                             | —    | 6.6  | —    |       |
|  |                               | EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)                           | —    | 0.56 | —    | μA    |
|  |                               | Power Down mode (reg. 0h.11 = 1)  | —    | 0.51 | —    |       |
|  |                               | Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1) | —    | 0.18 | —    |       |
|  |                               | Ultra-Deep Sleep mode with 1.2V (reg. 14h = 0x0078)   | —    | 180  | —    |       |
| Ultra-Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)         | —                             | 0.01  | —    |      |      |       |
| <b>Supply Current for AVDDH</b>  |                               |   |      |      |      |       |
| I <sub>AVDDH_3.3</sub>   | 3.3V Current for Transceiver  | No link, attempting to auto-negotiate   | —    | 19   | —    | mA    |
|  |                               | 100BASE-TX full-duplex at 100% utilization  | —    | 24   | —    |       |
|  |                               | 100BASE-TX link up, no traffic  | —    | 24   | —    |       |
|  |                               | 10BASE-T full-duplex at 100% utilization  | —    | 28   | —    |       |
|  |                               | 10BASE-T link up, no traffic  | —    | 16   | —    |       |
|  |                               | Energy Detect Power Down (EDPD) mode, no link partner (reg. 18h.11 = 0)                             | —    | 4.3  | —    |       |
|  |                               | EDPD mode with PLL off, no link partner (reg. 18h.11 = 0; reg. 10h.4 = 1)                           | —    | 2.2  | —    | μA    |
|  |                               | Power Down mode (reg. 0h.11 = 1)  | —    | 10   | —    |       |
|  |                               | Power Down mode, MII isolate, slow oscillator mode (reg. 0h.11 = 1; reg. 0h.10 = 1; reg. 11h.6 = 1) | —    | 0.18 | —    |       |
|  |                               | Ultra-Deep Sleep mode with 1.2V (reg. 14h = 0x0078)   | —    | 0.5  | —    |       |
| Ultra-Deep Sleep mode, VDDL and AVDDL = 0V (reg. 14h = 0x0078)         | —                             | 0.4   | —    |      |      |       |
| <b>CMOS Inputs (MDC, RESET, TXD, TXEN, TXER)</b>                       |                               |   |      |      |      |       |
| V <sub>IH</sub>  | Input High Voltage            | VDDIO = 3.3V  | 2.0  | —    | —    | V     |
|  |                               | VDDIO = 2.5V  | 1.5  | —    | —    |       |
| V <sub>IL</sub>  | Input Low Voltage             | VDDIO = 3.3V  | —    | —    | 1.3  | V     |
|  |                               | VDDIO = 2.5V  | —    | —    | 1.0  |       |
| I <sub>IN</sub>  | Input Current                 | V <sub>IN</sub> = GND ~ VDDIO   | —    | —    | 10   | μA    |
| <b>CMOS Outputs (COL, CRS, LED, RXC, RXD, RXDV, RXER, SIGDET, TXC)</b> |                               |   |      |      |      |       |
| V <sub>OH</sub>  | Output High Voltage           | VDDIO = 3.3V, I <sub>OH</sub> = 12 mA   | 2.4  | —    | —    | V     |
|  |                               | VDDIO = 2.5V, I <sub>OH</sub> = 6 mA  | 2.0  | —    | —    |       |
| V <sub>OL</sub>  | Output Low Voltage            | VDDIO = 3.3V, I <sub>OL</sub> = 6 mA  | —    | —    | 0.4  | V     |
|  |                               | VDDIO = 2.5V, I <sub>OL</sub> = 5 mA  | —    | —    | 0.4  |       |



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**TABLE 6-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

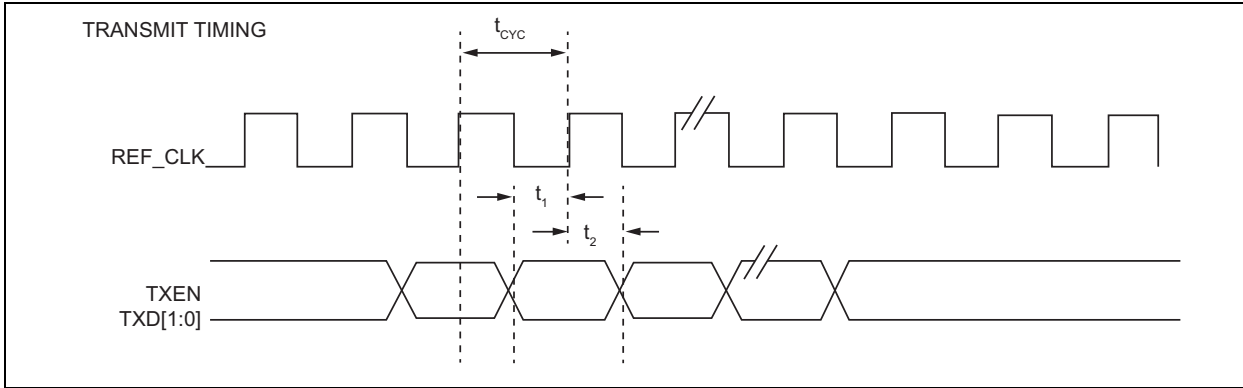
| Symbol   | Parameter                            | Condition   | Min. | Typ. | Max.       | Units      |
|--|--------------------------------------|---|------|------|------------|------------|
| $I_{OZL}$  | Output Tri-State Leakage             | $V_{OUT} = GND \sim VDDIO$  | —    | —    | 10         | $\mu A$    |
| <b>All Pull-Up/Pull-Down Pins (including Strapping Pins)</b>               |                                      |   |      |      |            |            |
| pu   | Internal Pull-Up Resistance          | VDDIO = 3.3V, external 4.7 k $\Omega$ pull-down   | —    | 33   | —          | k $\Omega$ |
|  |                                      | VDDIO = 2.5V, external 4.7 k $\Omega$ pull-down   | —    | 47   | —          |            |
| pd   | Internal Pull-Down Resistance        | VDDIO = 3.3V, external 4.7 k $\Omega$ pull-up   | —    | 36   | —          | k $\Omega$ |
|  |                                      | VDDIO = 2.5V, external 4.7 k $\Omega$ pull-up   | —    | 48   | —          |            |
| <b>100BASE-TX Transmit (measured differentially after 1:1 transformer)</b> |                                      |   |      |      |            |            |
| $V_O$  | Peak Differential Output Voltage     | 100 $\Omega$ termination across differential output   | 0.95 | —    | 1.05       | V          |
| $V_{IMB}$  | Output Voltage Imbalance             | 100 $\Omega$ termination across differential output   | —    | —    | 2          | %          |
| $t_r/t_f$  | Rise/Fall Time                       | —   | 3    | —    | 5          | ns         |
| —  | Rise/Fall Time Imbalance             | —   | 0    | —    | 0.5        |            |
| —  | Duty Cycle Distortion                | —   | —    | —    | $\pm 0.25$ |            |
| —  | Overshoot                            | —   | —    | —    | 5          | %          |
| —  | Output Jitter                        | Peak-to-peak  | —    | 0.7  | —          | ns         |
| <b>10BASE-T Transmit (measured differentially after 1:1 transformer)</b>   |                                      |   |      |      |            |            |
| $V_P$  | Peak Differential Output Voltage     | 100 $\Omega$ termination across differential output   | 2.2  | —    | 2.8        | V          |
| —  | Jitter Added                         | Peak-to-peak  | —    | —    | 3.5        | ns         |
| $t_r/t_f$  | Rise/Fall Time                       | —   | —    | 25   | —          |            |
| <b>10BASE-T Receive</b>  |                                      |   |      |      |            |            |
| $V_{SQ}$   | Squelch Threshold                    | 5 MHz square wave   | —    | 400  | —          | mV         |
| <b>100 Mbps Mode - Industrial Applications Parameters</b>                  |                                      |   |      |      |            |            |
| $t_{lir}$  | Link Loss Reaction (Indication) Time | Link loss detected at receive differential inputs to PHY signal indication time for each of the following:<br>1. For LED Mode "01", Link LED output change from low (link-up) to high (link-down).<br>2. INTRP pin assertion for link-down status change. | —    | 4.8  | —          | $\mu s$    |

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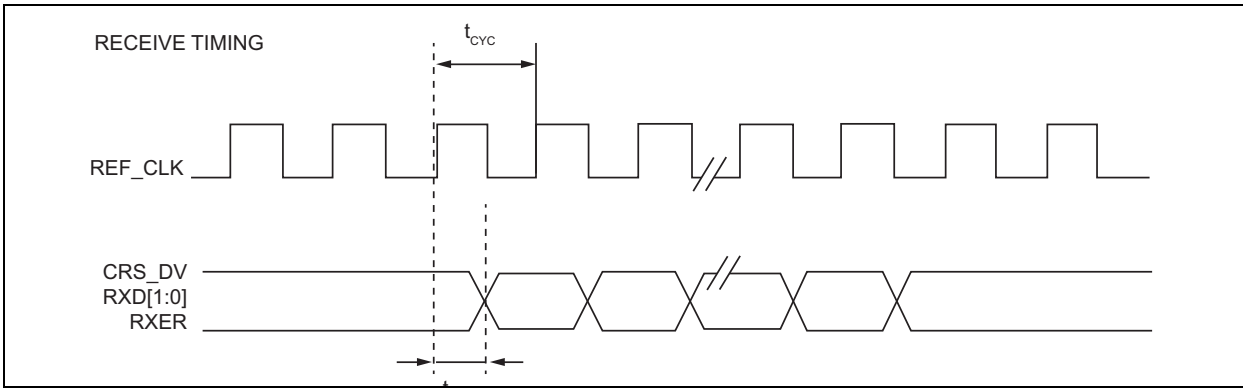
## 7.0 TIMING DIAGRAMS

### 7.1 RMII Transmit Timing

**FIGURE 7-1: RMII TRANSMIT TIMING**



**FIGURE 7-2: RMII RECEIVE TIMING**

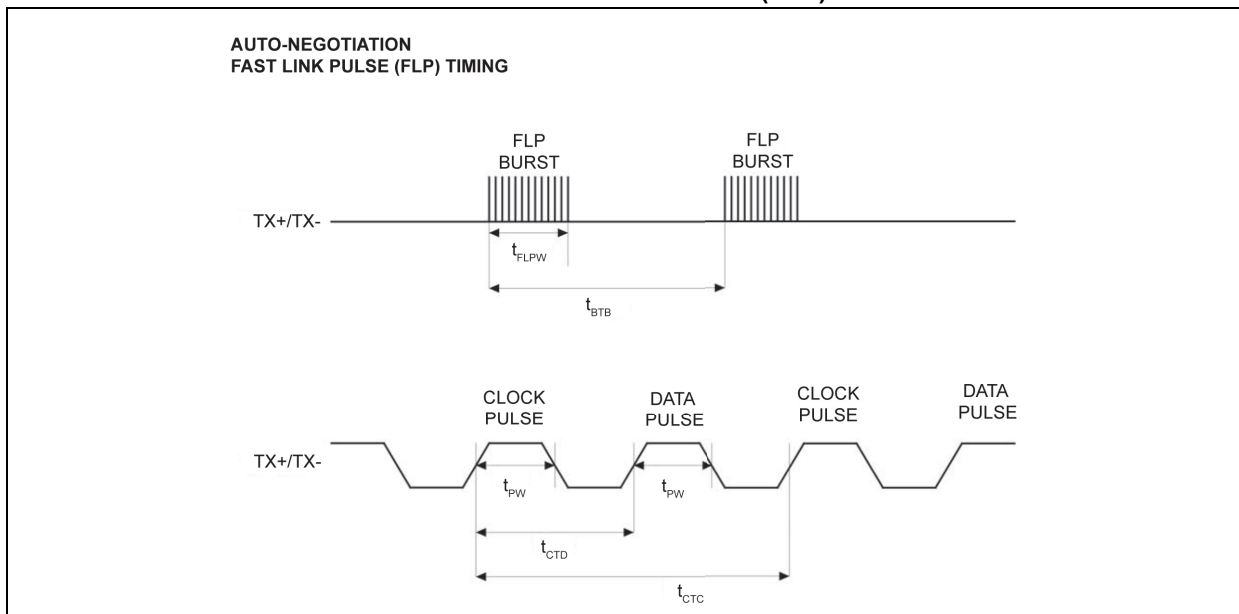


**TABLE 7-1: RMII TIMING PARAMETERS**

| Timing Parameter | Description  | Min. | Typ. | Max. | Units |
|------------------|--------------|------|------|------|-------|
| $t_{CYC}$        | Clock period | —    | 20   | —    | ns    |
| $t_1$            | Setup time   | 4    | —    | —    |       |
| $t_2$            | Hold time    | 2    | —    | —    |       |
| $t_{OD}$         | Output delay | 7    | 10   | 13   |       |

## 7.2 Auto-Negotiation Timing

**FIGURE 7-3: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING**



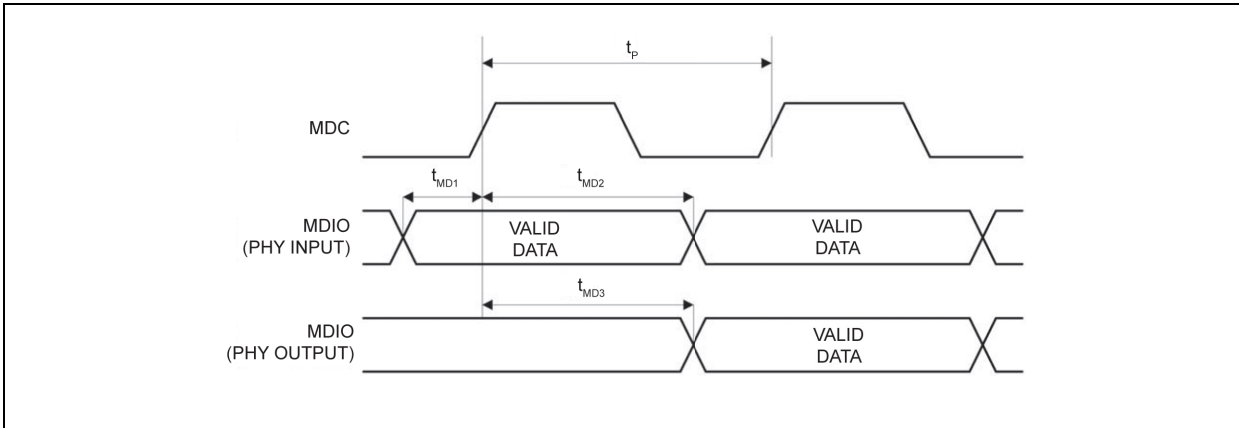
**TABLE 7-2: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING**

| Timing Parameter | Description                              | Min. | Typ. | Max. | Units   |
|------------------|--|------|------|------|---------|
| $t_{BTB}$        | FLP Burst to FLP Burst                   | 8    | 16   | 24   | ms      |
| $t_{PLPW}$       | FLP Burst width                          | —    | 2    | —    | ms      |
| $t_{PW}$         | Clock/Data Pulse width                   | —    | 100  | —    | ns      |
| $t_{CTD}$        | Clock Pulse to Data Pulse                | 55.5 | 64   | 69.5 | $\mu$ s |
| $t_{CTC}$        | Clock Pulse to Clock Pulse               | 111  | 128  | 139  | $\mu$ s |
| —                | Number of Clock/Data Pulse per FLP Burst | 17   | —    | 33   | —       |

# KSZ8061RNB/RND

## 7.3 MDC/MDIO Timing

**FIGURE 7-4: MDC/MDIO TIMING**



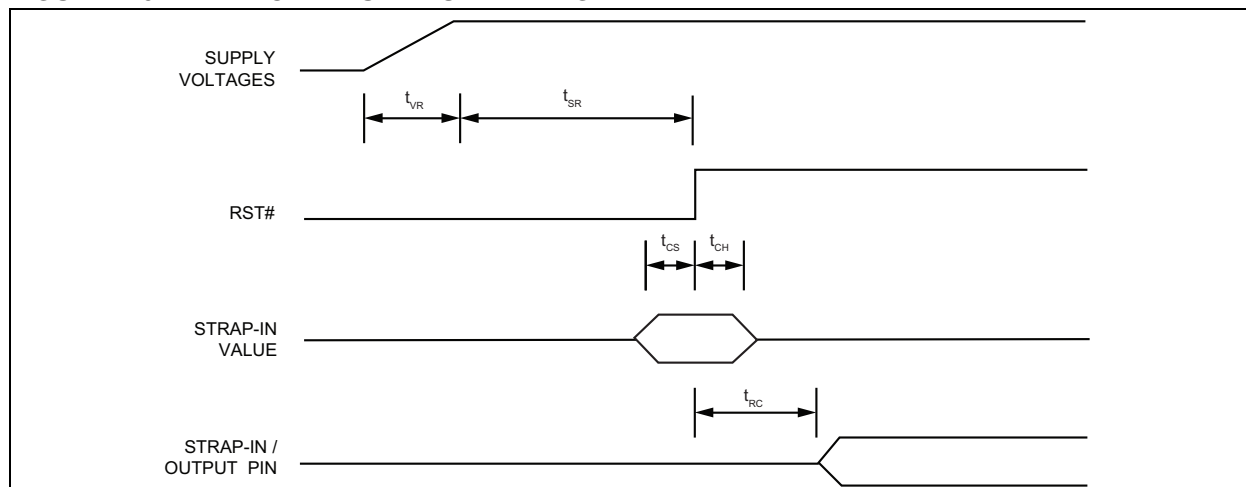
**TABLE 7-3: MDC/MDIO TIMING PARAMETERS**

| Timing Parameter | Description                                     | Min. | Typ. | Max. | Units |
|------------------|---|------|------|------|-------|
| $t_p$            | MDC period                                      | 400  | —    | —    | ns    |
| $t_{MD1}$        | MDIO (PHY input) setup to rising edge of MDC    | 10   | —    | —    |       |
| $t_{MD2}$        | MDIO (PHY input) hold from rising edge of MDC   | 4    | —    | —    |       |
| $t_{MD3}$        | MDIO (PHY output) delay from rising edge of MDC | 5    | —    | —    |       |

## 7.4 Power-up/Reset Timing

The KSZ8061RNB/RND reset timing requirement is summarized in [Figure 7-5](#) and [Figure 7-4](#).

**FIGURE 7-5: POWER-UP/RESET TIMING**



**TABLE 7-4: POWER-UP/RESET TIMING PARAMETERS**

| Parameter | Description  | Min. | Typ. | Max. | Units         |
|-----------|--|------|------|------|---------------|
| $t_{VR}$  | Supply voltage (VDDIO, AVDD, VDDL, AVDDL) rise time            | 300  | —    | —    | $\mu\text{s}$ |
| $t_{SR}$  | Stable supply voltage (VDDIO, AVDD, VDDL, AVDDL) to reset high | 10   | —    | —    | ms            |
| $t_{CS}$  | Configuration setup time                                       | 5    | —    | —    | ns            |
| $t_{CH}$  | Configuration hold time  | 5    | —    | —    | ns            |
| $t_{RC}$  | Reset to strap-in pin output                                   | 6    | —    | —    | ns            |

The supply voltage (VDDIO, AVDD, VDDL, AVDDL) power-up waveforms should be monotonic, and the 300  $\mu\text{s}$  minimum rise time is from 10% to 90%.

For warm reset, the reset (RESET#) pin should be asserted low for a minimum of 500  $\mu\text{s}$ . The strap-in pin values are read and updated at the de-assertion of reset.

After the de-assertion of reset, it is recommended to wait a minimum of 100  $\mu\text{s}$  before starting programming on the MIIM (MDC/MDIO) Interface.

# KSZ8061RNB/RND

## 8.0 RESET CIRCUIT

Figure 8-1 shows a reset circuit recommended for powering up the KSZ8061RNB/RND if reset is triggered by the power supply.

**FIGURE 8-1: RECOMMENDED RESET CIRCUIT**

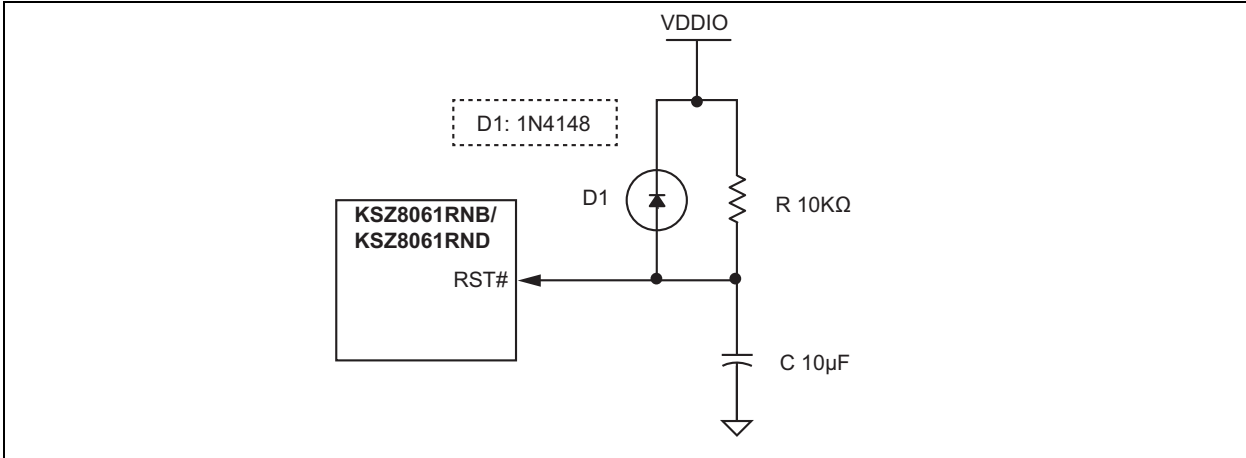
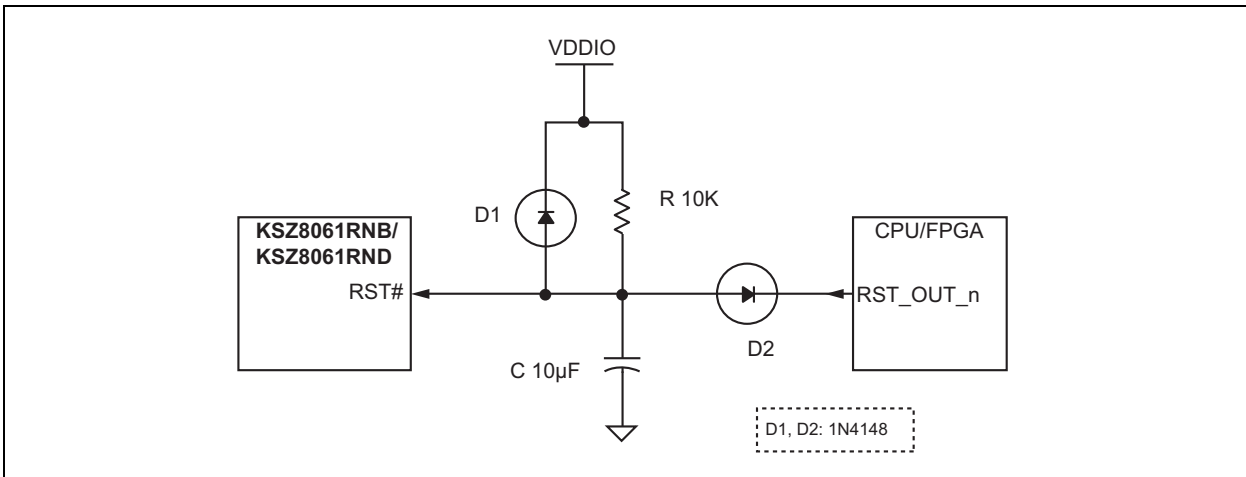


Figure 8-2 represents a reset circuit recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8061RNB/RND. The RST\_OUT\_n from CPU/FPGA provides the warm reset after power up.

**FIGURE 8-2: RECOMMENDED RESET CIRCUIT FOR INTERFACING WITH CPU/FPGA RESET OUTPUT**

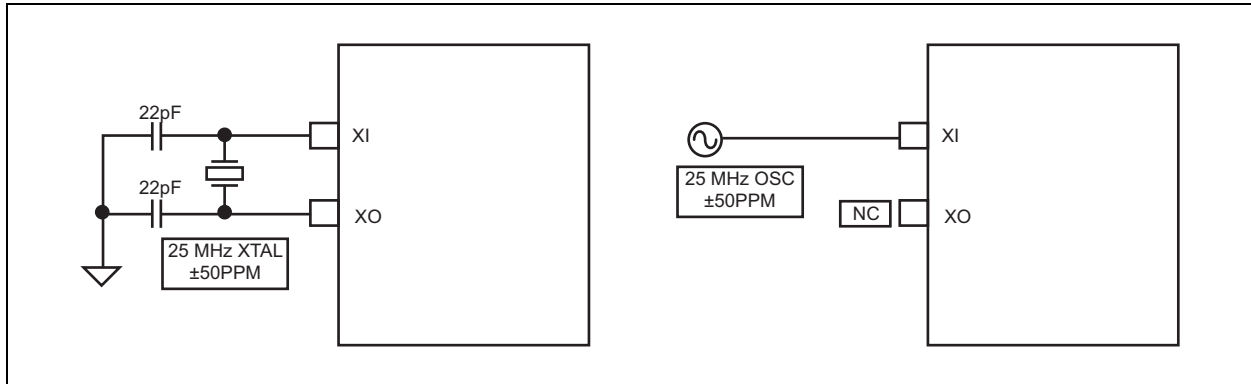


## 9.0 REFERENCE CLOCK CONNECTION AND SELECTION - KSZ8061RNB

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ8061RNB. For the KSZ8061RNB in all operating modes, the reference clock is 25 MHz. The reference clock connections to XI (pin 1) and XO (pin 2), and the reference clock selection criteria are provided in [Figure 9-1](#) and [Table 9-1](#).

The KSZ8061RNB outputs a 50 MHz RMI reference clock on the REF\_CLK pin.

**FIGURE 9-1: KSZ8061RNB 25 MHz CRYSTAL/OSCILLATOR REFERENCE CLOCK CONNECTION**



**TABLE 9-1: 25 MHz CRYSTAL/REFERENCE CLOCK SELECTION CRITERIA**

| Characteristics            | Value | Units |
|----------------------------|-------|-------|
| Frequency                  | 25    | MHz   |
| Frequency Tolerance (Max.) | ±50   | ppm   |

**TABLE 9-2: RECOMMENDED CRYSTALS**

| Manufacturer | Part Number        |
|--------------|--------------------|
| NDK          | NX2016SA           |
| Murata       | XRCGB25M000F3A00R0 |

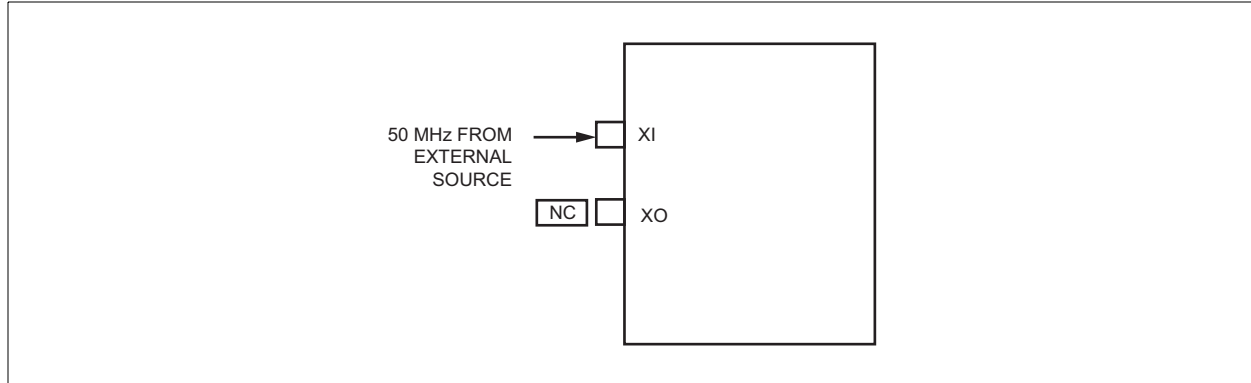
# KSZ8061RNB/RND

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## 10.0 REFERENCE CLOCK CONNECTION - KSZ8061RND

The KSZ8061RND uses a 50 MHz RMI reference clock input for all of its timing. The 50 MHz clock connects to the XI pin as shown in [Figure 10-1](#). Note that XI is powered from the AVDDH power rail, not VDDIO. The XO and REF\_CLK pins are unconnected.

**FIGURE 10-1: KSZ8061RND 50 MHZ CLOCK CONNECTION**

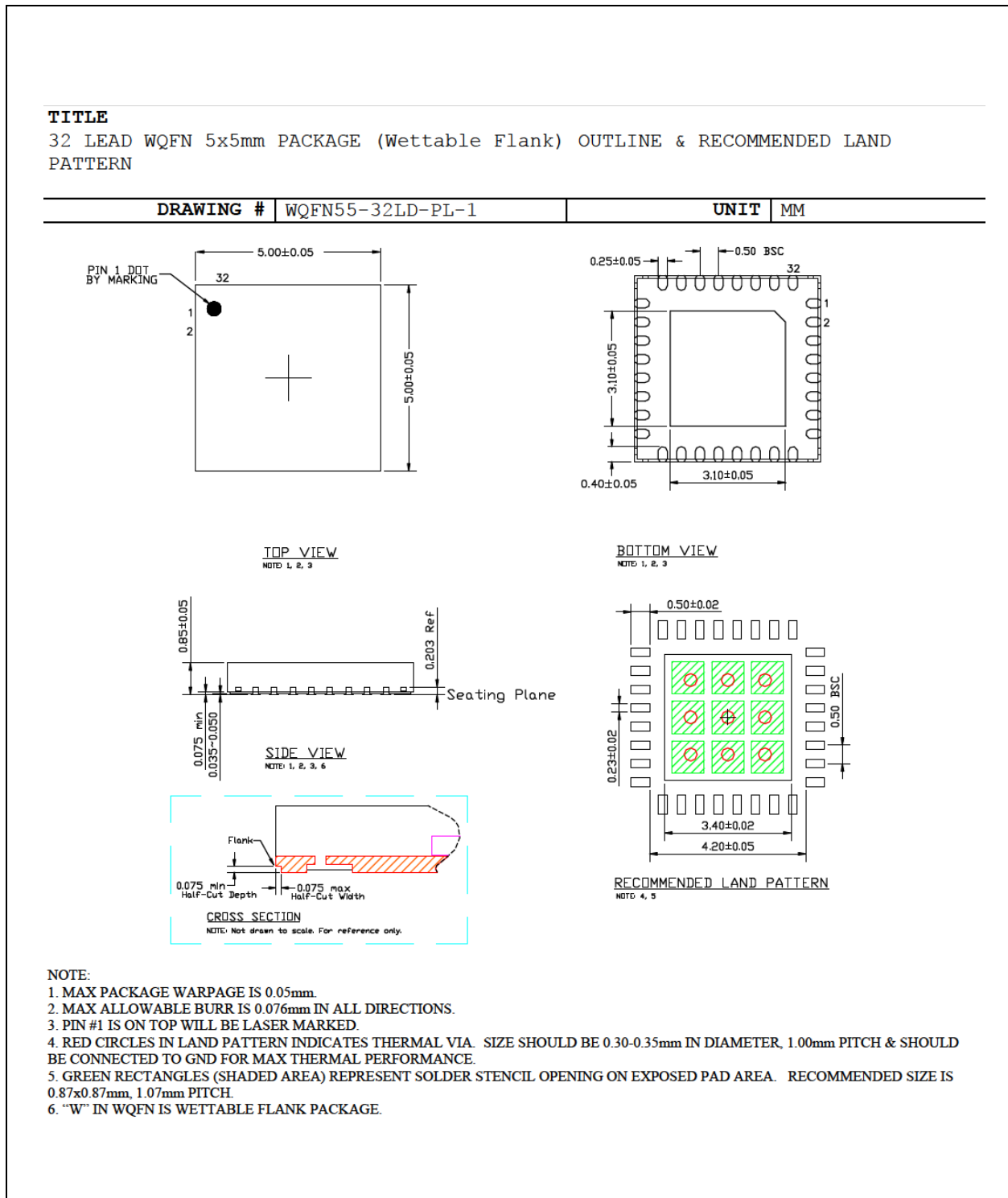




## 11.0 PACKAGE OUTLINES

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

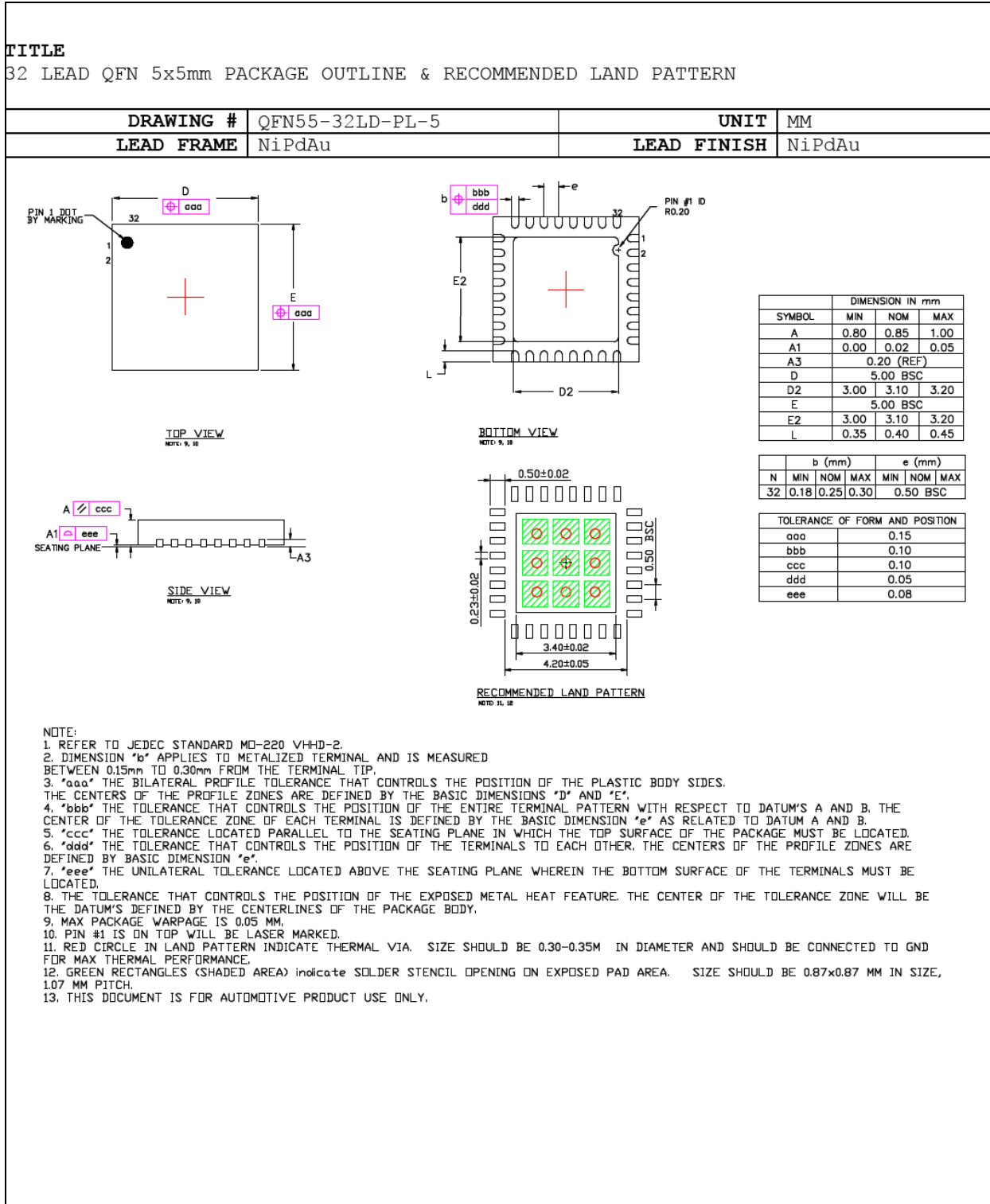
**FIGURE 11-1: 32-PIN 5MM × 5MM WQFN PACKAGE OUTLINE AND RECOMMENDED LAND PATTERN**



# KSZ8061RNB/RND

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>

**FIGURE 11-2: 32-PIN 5MM × 5MM QFN PACKAGE OUTLINE AND RECOMMENDED LAND PATTERN**



## APPENDIX A: DATA SHEET REVISION HISTORY

**TABLE A-1: CUSTOMER REVISION HISTORY**

| Revision Level and Date                             | Section/Figure/Entry   | Correction   |
|---|--|--|
| DS00002197C<br>(03-03-17)                           | Table of Contents, Section 11.0, "Package Outlines", Appendix A: "Data Sheet Revision History"         | Minor update to page headers.  |
|   | Product Identification System on page 53   | Minor correction Examples section.   |
| DS00002197B<br>(01-27-17)                           | All  | Sales listing and cover pages updated. Minor text changes throughout.  |
|   | Highlights on page 1   | Added this section.  |
|   | Table 1-2, "Strap-in Options," on page 7   | CONFIG[2:0] 101 and 111 descriptions updated (Auto-MDI/MDI-X enabled).   |
|   | Product Identification System on page 53   | PIS ordering code temperature descriptions corrected. Removed note.  |
|   | Table 4-1, "Standard Registers," on page 25 and Table 4-3, "Standard Register Description," on page 26 | AFE Control 1 register information added.  |
| Table 6-1, "Electrical Characteristics," on page 39 | Removed IVDDIO_1.8 section.  |  |
| DS00002197A<br>(08-08-16)                           | Whole Document   | Conversion of Micrel KSZ8061RNB/ KSZ8061RND datasheet into Microchip DS00002197C. Minor text changes throughout. |

# KSZ8061RNB/RND

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# KSZ8061RNB/RND

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u>           | X              | X   | X               | X           |
|---------------------------|----------------|---|-----------------|-------------|
| Device                    | Interface      | Package   | Reference Clock | Temperature |
| <b>Device:</b>            | KSZ8061RNB/RND |   |                 |             |
| <b>Interface:</b>         | R =            | RMII Interface                                  |                 |             |
| <b>Package:</b>           | N =            | 32-pin QFN or WQFN                              |                 |             |
| <b>Reference Clock:</b>   | B =            | 50 MHz RMII clock output                        |                 |             |
|                           | D =            | 50 MHz RMII clock input                         |                 |             |
| <b>Temperature Range:</b> | I =            | -40°C to +85°C (Industrial)                     |                 |             |
|                           | V =            | -40°C to +105°C (Automotive-Qualified Extended) |                 |             |
|                           | W =            | -40°C to +105°C (Industrial Extended)           |                 |             |

**Examples:**

- a) KSZ8061RNBV  
RMII Interface, 32-pin WQFN,  
50 MHz RMII clock output,  
AEC-Q100 Automotive-Qualified Extended  
temperature
- b) KSZ8061RNBW  
RMII Interface, 32-pin QFN, 50 MHz RMII clock  
output, Industrial Extended temperature
- c) KSZ8061RNDV  
RMII Interface, 32-pin WQFN, 50 MHz RMII  
clock input, AEC-Q100 Automotive-Qualified  
Extended temperature
- d) KSZ8061RNDW  
RMII Interface, 32-pin QFN, 50 MHz RMII clock  
input, Industrial Extended temperature

# KSZ8061RNB/RND

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ISBN: 978-1-5224-1439-1

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