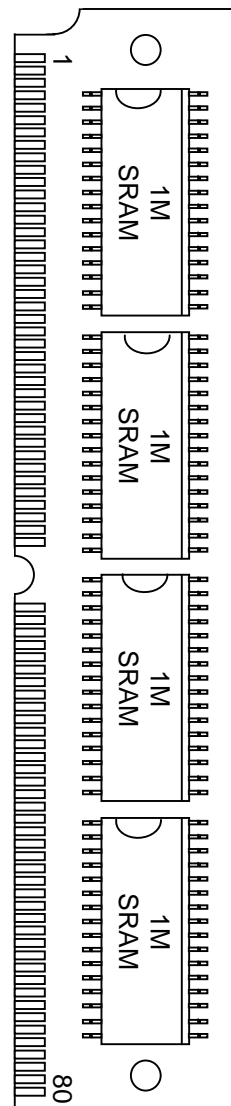


## FEATURES

- Organized as a high density 512k x 16 bit Stik™
- Fast access time of 85 ns
- Unlimited write cycles
- Employs popular JEDEC standard 80-position SIMM connector
- Full  $\pm 10\%$  operating range
- Read cycle time equals write cycle time
- Ultra-low standby current  $< 10 \mu\text{A}$
- Suitable for battery-backed applications

## PIN ASSIGNMENT



80-PIN SIP STIK

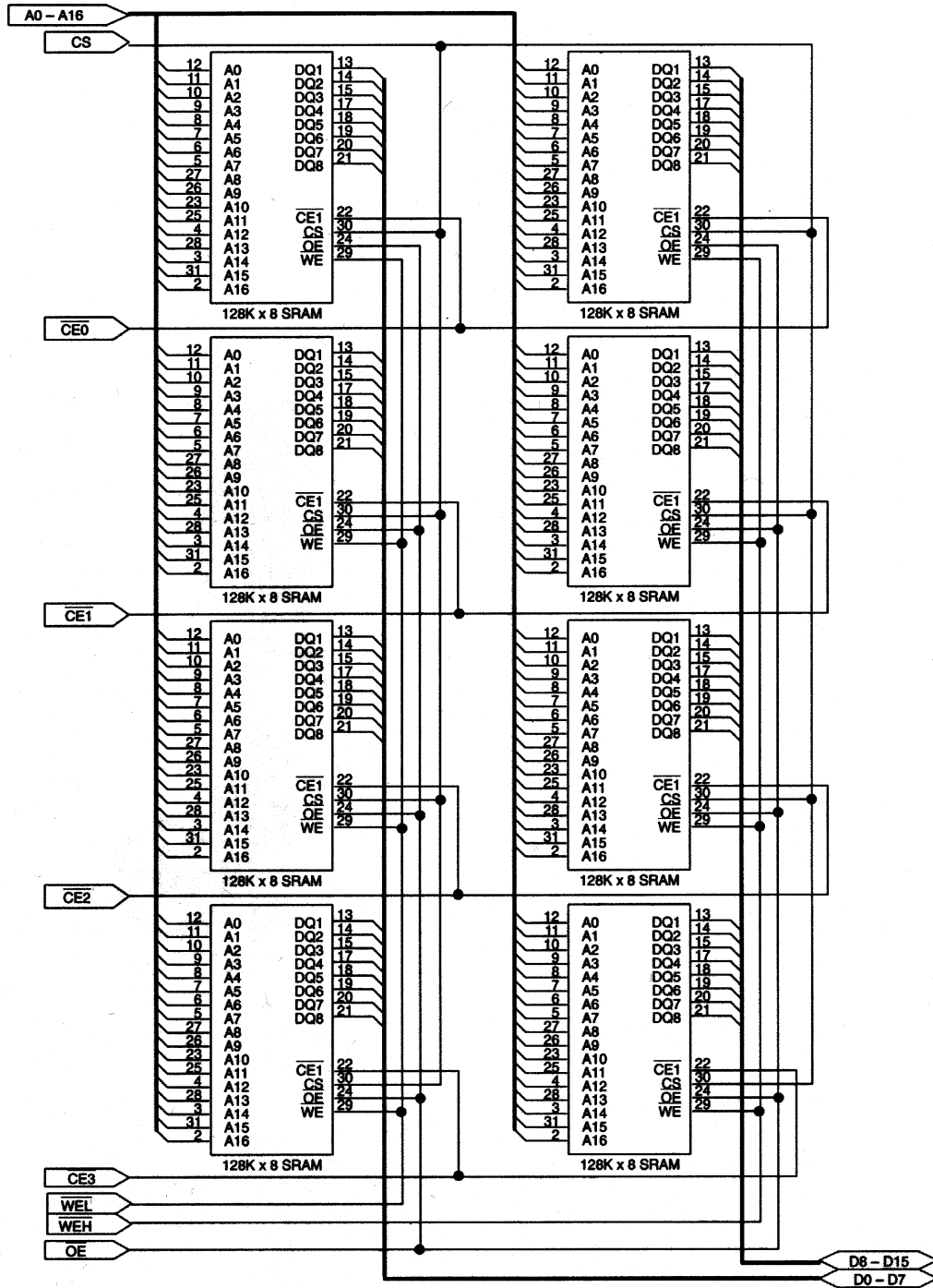
## DESCRIPTION

The DS2229 is an 8,388,608-bit low-power fully static Random Access Memory organized as a 524,888 word by 16 bits using CMOS technology. The device employs the popular JEDEC standard 80-pin SIMM connection scheme with no additional circuitry required. The device operates from a single power supply with a voltage input of 4.5 to 5.5 volts. The Chip Enable inputs ( $\overline{\text{CE0}}$ ,  $\overline{\text{CE1}}$ ,  $\overline{\text{CE2}}$ ,  $\overline{\text{CE3}}$ ) are used for device selection and can be used in order to achieve the minimum standby current mode which facilitates battery backup. The device provides a fast access time of 85 ns. The DS2229 maintains TTL levels over input voltage range 4.5V to 5.5V. The DS2229 is JEDEC pin compatible (see Figure 1) with flash EEPROM memory SIMM boards of similar density.

**PIN DESCRIPTION** Figure 1

<b>PIN #</b>	<b>PIN NAME</b>	<b>PIN #</b>	<b>PIN NAME</b>	<b>PIN #</b>	<b>PIN NAME</b>	
1	GND	32	NC	63	DQ <sub>7</sub>	
2	V <sub>CC</sub>	33	NC	64	DQ <sub>6</sub>	
3	NC	34	NC	65	DQ <sub>5</sub>	
4	$\overline{\text{OE}}$	35	NC	66	DQ <sub>4</sub>	
5	$\overline{\text{WEH}}$	36	A <sub>16</sub>	67	DQ <sub>3</sub>	
6	$\overline{\text{WEL}}$	37	A <sub>15</sub>	68	DQ <sub>2</sub>	
7	NC	38	A <sub>14</sub>	69	DQ <sub>1</sub>	
8	CS	39	A <sub>13</sub>	70	DQ <sub>0</sub>	
9	NC	40	A <sub>12</sub>	71	NC	
10	NC	41	A <sub>11</sub>	72	V <sub>CC</sub>	
11	NC	42	A <sub>10</sub>	73	NC	
12	NC	43	A <sub>9</sub>	74	GND	
13	NC	44	A <sub>8</sub>	75	NC	
14	NC	45	A <sub>7</sub>	76	GND	
15	NC	46	A <sub>6</sub>	77	GND	
16	NC	47	A <sub>5</sub>	78	NC	
17	NC	48	A <sub>4</sub>	79	NC	
18	NC	49	A <sub>3</sub>	80	GND	
19	NC	50	A <sub>2</sub>			
20	NC	51	A <sub>1</sub>			
21	$\overline{\text{CE3}}$	52	A <sub>0</sub>	<b>PIN NAME</b>	<b>DESCRIPTION</b>	
22	$\overline{\text{CE2}}$	53	GND	A <sub>0</sub> - A <sub>16</sub>	Address Input	
23	$\overline{\text{CE1}}$	54	GND	$\overline{\text{WEL}}$	Write Enable Input Low	
24	$\overline{\text{CE0}}$	55	DQ <sub>15</sub>	$\overline{\text{WEH}}$	Write Enable Input High	
25	GND	56	DQ <sub>14</sub>	$\overline{\text{OE}}$	Output Enable Input	
26	NC	57	DQ <sub>13</sub>	NC	No Connect	
27	NC	58	DQ <sub>12</sub>	$\overline{\text{CE0}}$ - $\overline{\text{CE3}}$	Chip Enable Input	
28	NC	59	DQ <sub>11</sub>	CS	Chip Select	
29	NC	60	DQ <sub>10</sub>	DQ <sub>0</sub> - DQ <sub>15</sub>	Data Input/Output	
30	NC	61	DQ <sub>9</sub>	V <sub>CC</sub>	+5 Volts	
31	NC	62	DQ <sub>8</sub>	GND	Ground	

DS2229 STATIC RAM MODULE FUNCTION DIAGRAM Figure 2



**ABSOLUTE MAXIMUM RATINGS\***

Power Supply Voltage	-0.3V to +7.0V
Input, Input/Output Voltage	-0.3 to $V_{CC} + 0.3V$
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**OPERATION MODE**

MODE	$\overline{CE0} - \overline{CE3}$	CS	$\overline{OE}$	$\overline{WE}$	A0 - A16	DQ - DQ15	POWER
READ	L	H	L	H	STABLE	DATA OUT	$I_{CC0}$
WRITE	L	H	X	L	STABLE	DATA IN	$I_{CC0}$
DESELECT	L	H	H	H	X	HIGH-Z	$I_{CC0}$
STANDBY	H	X	X	X	X	HIGH-Z	$I_{CCS1}, I_{CCS2}$
STANDBY	X	L	X	X	X	HIGH-Z	$I_{CCS1}, I_{CCS2}$

**CAPACITANCE** $(t_A = 25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$			64	pF	
Input/Output Capacitance	$C_{I/O}$			80	pF	

**RECOMMENDED DC OPERATING CONDITIONS** $(t_A = 0^\circ\text{C to } 70^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	
Input High Voltage	$V_{IH}$	2.0		$V_{CC} + 0.3$	V	
Input Low Voltage	$V_{IL}$	-0.3		0.8	V	

**DC CHARACTERISTICS** $(t_A = 0^\circ\text{C to } 70^\circ\text{C}; V_{CC} = 5V \pm 10\%)$ 

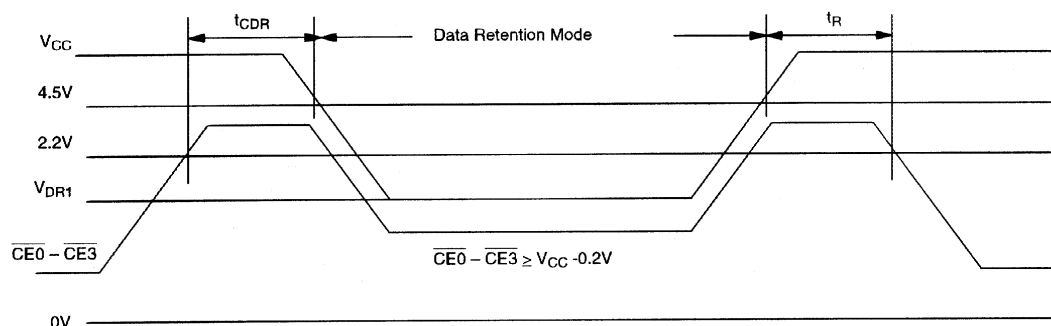
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Input Leakage Current	$I_{IL}$	$0V \leq V_{IN} \leq V_{CC}$		8	$\mu\text{A}$	
I/O Leakage Current	$I_{LO}$	$\overline{CE0} - \overline{CE3} = V_{IH}$ , $0V \leq V_{IO} \leq V_{CC}$		8	$\mu\text{A}$	
Output High Current	$I_{OH}$	$V_{OH} = 2.4V$	-1.0		mA	
Output Low Current	$I_{OL}$	$V_{OL} = 0.4V$	2.1		mA	
Standby Current	$I_{CCS1}$	$\overline{CE0} - \overline{CE3} = 2.0V$ $t_A = 25^\circ\text{C}$		8	mA	
Standby Current	$I_{CCS2}$	$\overline{CE0} - \overline{CE3} \geq V_{CC} - 0.3V$ $t_A = 25^\circ\text{C}$		10	$\mu\text{A}$	
Operating Current	$I_{CC0}$	$\overline{CE0} - \overline{CE3} = 0.8V$ ; Cycle=100 ns $t_A = 25^\circ\text{C}$		100	mA	9

**LOW V<sub>CC</sub> DATA RETENTION CHARACTERISTICS** $(t_A = 0^\circ\text{C to } 70^\circ\text{C})$ 

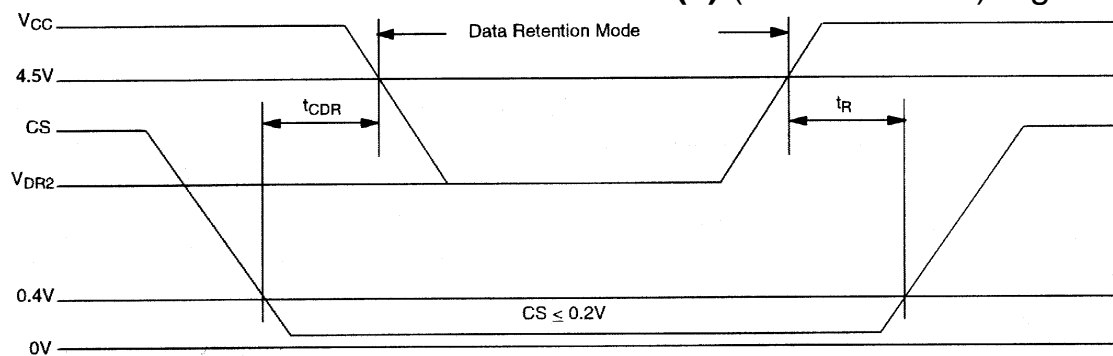
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONTIDION
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	2.0	-	-	V	$\overline{\text{CE0}} - \overline{\text{CE3}} \geq V_{\text{CC}} - 0.2\text{V}$ , $\text{CS} \geq V_{\text{CC}} - 0.2\text{V}$ or $0\text{V}$ $\leq \text{CS} \leq 0.2\text{V}$ $V_{\text{IN}} \geq 0\text{V}$
Data Retention Current	I <sub>CCDR</sub>	-	1	8	$\mu\text{A}$	$V_{\text{CC}} = 3.0\text{V}$ , $V_{\text{IN}} \geq 0\text{V}$ $\overline{\text{CE0}} - \overline{\text{CE3}} \geq V_{\text{CC}} - 0.2\text{V}$ , $\text{CS} \geq V_{\text{CC}} - 0.2\text{V}$ or $0\text{V} \leq$ $\text{CS} \leq 0.2\text{V}$ $t_A = 25^\circ\text{C}$
Chip Deselect to Data Retention Time	t <sub>CDR</sub>	0	-	-	ns	See Retention Waveform
Operation Recovery Time	t <sub>R</sub>	5	-	-	ms	

**LOW V<sub>CC</sub> DATA RETENTION TIMING WAVEFORM (1) ( $\overline{\text{CE0}} - \overline{\text{CE3}}$  Controlled)**

Figure 3

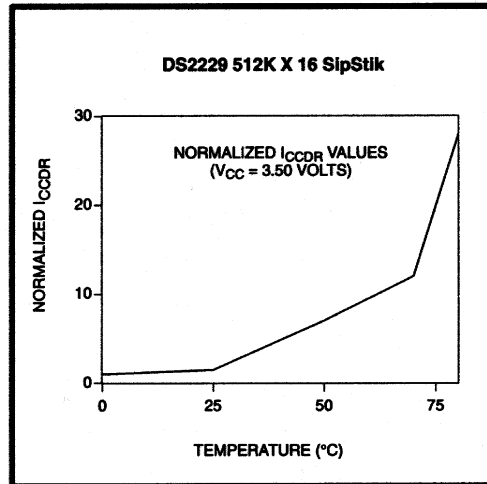
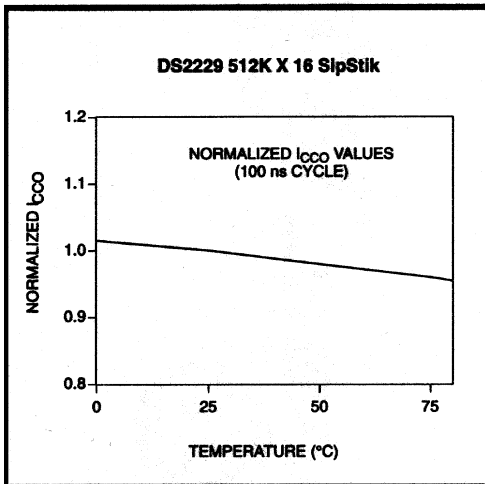
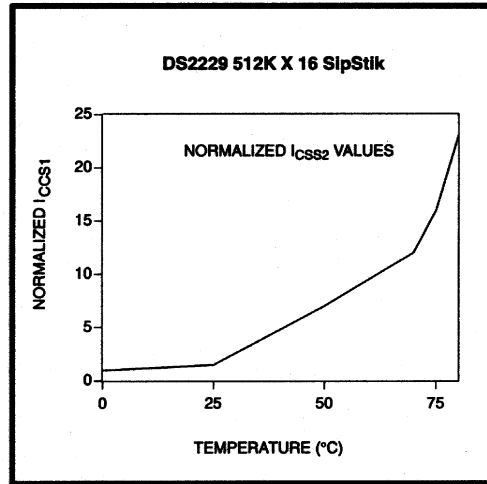
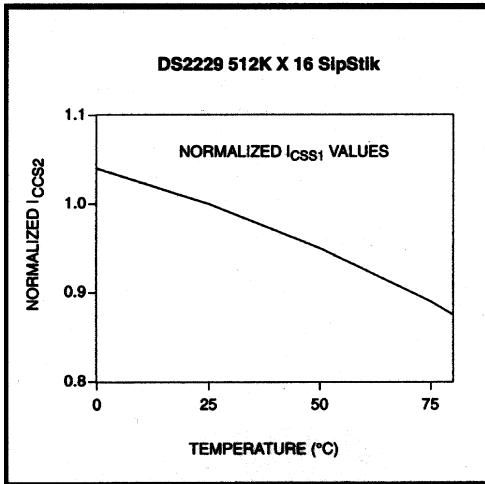


SEE NOTE 5

**LOW V<sub>CC</sub> DATA RETENTION TIMING WAVEFORM (2) (CS Controlled) Figure 4**

SEE NOTE 5

PRODUCT CHARACTERISTICS



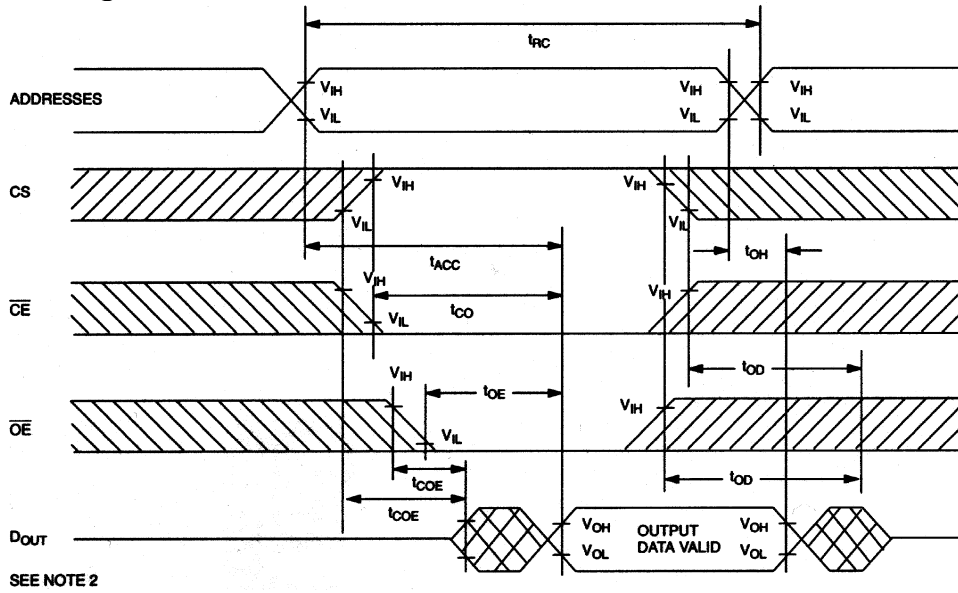
**AC ELECTRICAL CHARACTERISTICS****READ CYCLE**(0°C to 70°C;  $V_{CC} = 5V + 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	$t_{RC}$	85			ns	
Access Time	$t_{ACC}$			85	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$			45	ns	
$\overline{CE0} - \overline{CE3}$ to Output Valid	$t_{CO}$			85	ns	
$\overline{OE}$ or $\overline{CE0} - \overline{CE3}$ to Output In Low-Z	$t_{COE}$	10			ns	8
Output High-Z from Deselection	$t_{OD}$	0		30	ns	8
Output Hold from Address Change	$t_{OH}$	10			ns	

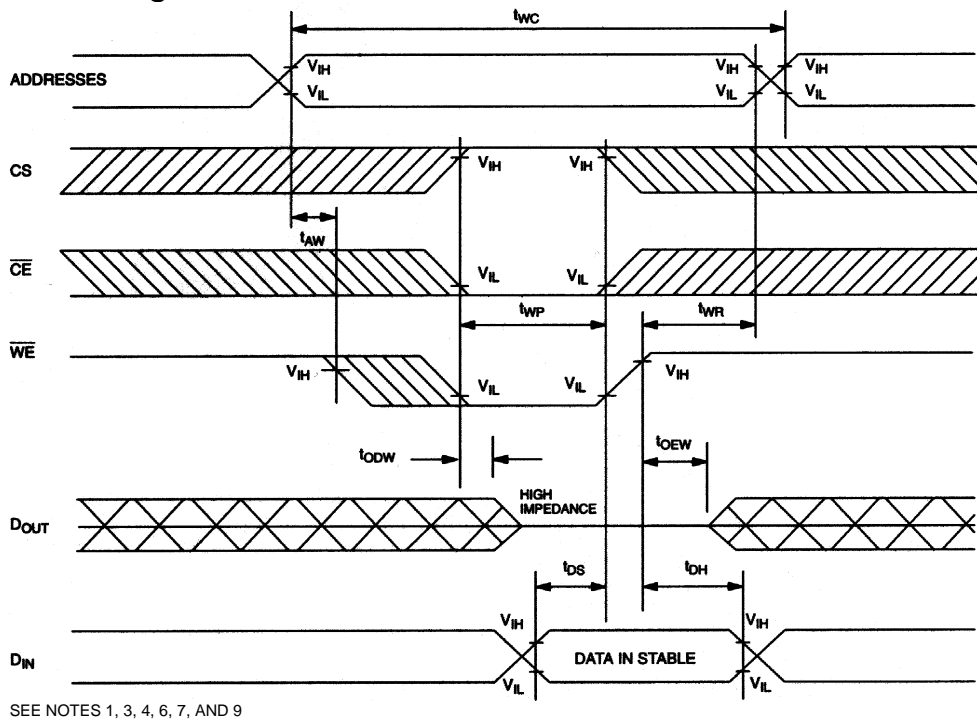
**AC ELECTRICAL CHARACTERISTICS****WRITE CYCLE**(0°C to 70°C;  $V_{CC} = 5V + 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	$t_{WC}$	85			ns	
Write Pulse Width	$t_{WP}$	65			ns	1
Address Setup Time	$t_{AW}$	0			ns	
Write Recovery Time	$t_{WR}$	10			ns	4
Output High-Z from $\overline{WE}$	$t_{ODW}$	0		30	ns	8
Output Active from $\overline{WE}$	$t_{OEw}$	5			ns	8
Data Setup Time	$t_{DS}$	35			ns	3
Data Hold Time from $\overline{WE}$	$t_{DH}$	0			ns	3

### READ CYCLE Figure 5

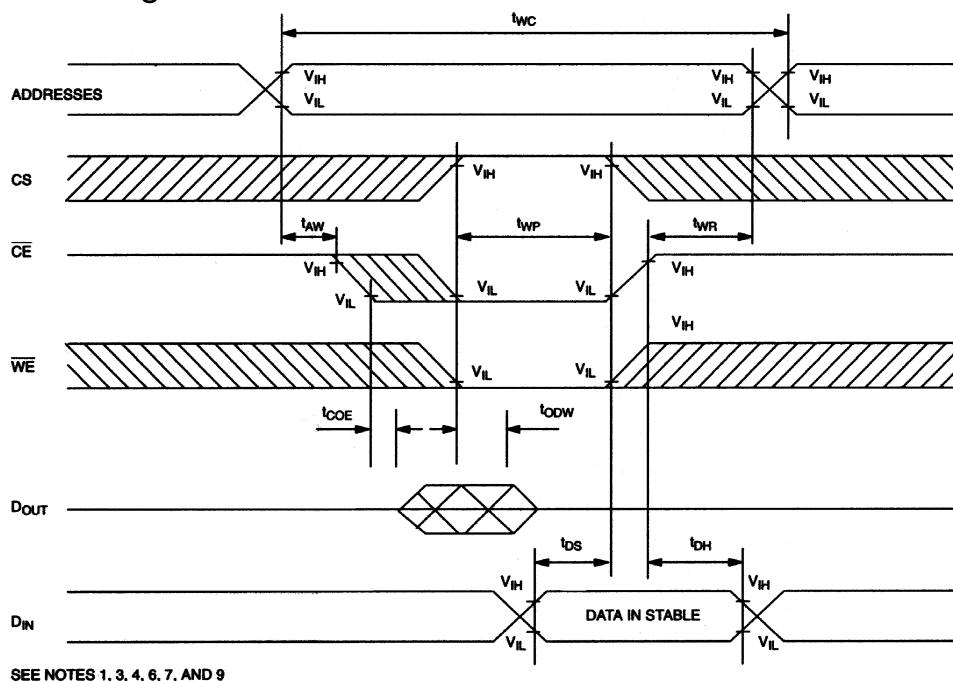


### WRITE CYCLE 1 Figure 6



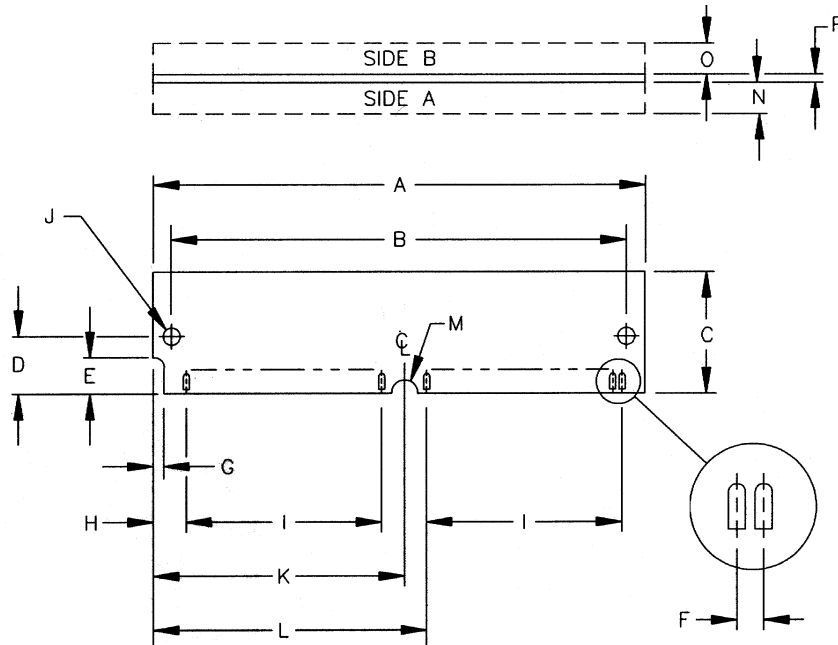


## WRITE CYCLE 2 Figure 7

**NOTES:**

1. A write occurs during the overlap of a low  $\overline{CE0} - \overline{CE3}$ , a high CS, and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CE0} - \overline{CE3}$  going low, CS going high, and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CE0} - \overline{CE3}$  going high, CS going low and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $\overline{WE}$  is high for a read cycle.
3.  $t_{DS}$  ends and  $t_{DH}$  begins at the earliest transition among  $\overline{CE0} - \overline{CE3}$  going high.
4.  $t_{WR}$  is measured from the earliest of  $\overline{CE0} - \overline{CE3}$  or  $\overline{WE}$  going high or CS going low to the end of write cycle.
5. CS controls address buffer,  $\overline{WE}$  buffer,  $\overline{CE0} - \overline{CE3}$  buffer,  $\overline{OE}$  buffer and D<sub>IN</sub> buffer. If CS controls data retention mode, V<sub>IN</sub> levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CE0} - \overline{CE3}$ , I/O) can be in the high impedance state. If  $\overline{CE0} - \overline{CE3}$  controls data retention mode, CS must be  $CS \geq V_{CC} - 0.2V$  or  $0V < CS < 0.2V$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.
6. If  $\overline{CE0} - \overline{CE3}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in a high impedance state.
7. If  $\overline{CE0} - \overline{CE3}$  is low and CS is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
8. This parameter is sampled and not 100% tested.
9. Only one  $\overline{CE}$  active during any read or write cycle.

## DS2229 80-PIN SIP STIK



PKG	80-PIN	
DIM	MIN	MAX
A	4.645	4.655
B	4.379	4.389
C	0.729	0.739
D	0.395	0.405
E	0.245	0.255
F	0.050 BSC	
G	0.075	0.085
H	0.245	0.255
I	1.950 BSC	
J	0.120	0.130
K	2.320	2.330
L	2.445	2.455
M	0.057	0.067
N		0.130
O		0.130
P		0.054