Using the ISL6401 RSLIC PWM Controller Evaluation Board

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Functional Description

The ISL6401 pulse width modulating (PWM) current mode controller is designed for a wide range of DC/DC conversion applications including boost, flyback, and isolated output configurations. The device is optimized to provide high performance, low-cost solution for Ringing SLIC (RSLIC) Ring (Vbh) and Talk (Vbl) power supplies in VoIP applications. The IC features an integrated inverter that is ideal for generating negative output voltage like RSLIC Ring Vbh (-72V) and Talk Vbl (-24V), -48V for IP Phones, -5V and -15V for DSL CO line drivers. The output voltages are adjusted with an external voltage divider.

Peak current mode control architecture effectively handles Ring trip transients and provides inherent overcurrent protection. Flyback topology allows the operation close to 50% duty cycle, offering optimum transformer utilization, low ripple current and less stress on input/output capacitors. Internal soft-start minimizes start-up stress without any external components. The switching frequency can be programmed from 50kHz to 600kHz or alternatively, the internal oscillator can be locked to an external clock fed at SYNC input for noise sensitive applications. A logic level shutdown input is included, which reduces supply current to 55µA in the shutdown mode. DC/DC conversion efficiency is optimized by use of a low current sense voltage.

For a detailed functional description, complete specifications and component selection guidelines, please refer to the ISL6401 Data Sheet (“ISL6401: Synchronizing Current Mode PWM for Subscriber Line Interface Circuits”), Intersil Corporation, FN9007, available on Intersil’s website, http://www.intersil.com/data/fn/fn9007.pdf

Application Information

As worldwide demand for inexpensive Voice over Internet Protocol telephony grows, so will the need for Integrated Circuits that are specialized to enable compatibility between new telephony systems and older telephones based on analog standards. Analog ring signal generation and off hook loop current supply are two analog functions that are performed by Subscriber Line Interface Circuits (SLICs). This application note discusses the special power supply implementation to generate the high negative voltages needed by SLICs.

Overview of Telephone Loop System

Traditionally, a telephone network consists of a circuit between the subscriber and the central office. However, the advent of new high speed digital technologies has created the need to control and manage the functions of the phone locally as opposed to the central office. In both instances the principals governing the operation of the phone loop are essentially the same.

In a telephone loop, the subscriber is connected to the network via 2 wires, commonly known as Tip and Ring. The actual digital telecommunications trunk line however, operates on 4 wires; two of which are allocated for transmitting and two for receiving. This 2 to 4-wire interface consists of the SLIC and CODEC. A SLIC is the primary interface between the 4-wire (ground referenced) low voltage switch environment and the 2-wire (floating) high voltage loop environment. It performs a number of important functions including Battery feed, Overvoltage protection, Ringing, Signaling, Coding, Hybrid Balancing and also Testing.

The Ringing SLIC (RSLIC) typically requires two high voltage power supply inputs. The first is a tightly regulated voltage around -24V or -48V for off-hook signal transmission. The second is a loosely regulated -70V to -100V for ring tone generation. When the switch hook is released the phone puts approximately 200Ω of resistance across the phone terminals. Intersil RSLICs feature internal current limiting so this load is not presented to the power supply. However, not all of the SLICs available in the market offer this feature and the power supply is expected to maintain output during the remainder of the ring cycle. Once voice transmission begins, the SLIC, in many cases, requires a lower voltage input to establish a 20mA to 25mA current loop. The loop feeds the 200Ω, protection resistors, and line resistances within the phone. In some cases, the lower supply and higher supply voltage are combined and the SLIC runs from a compromise voltage of approximately -53V.

The specifications listed in the following table are for a 4-line requirement with 5 REN per line.

TABLE 1. TYPICAL POWER SUPPLY REQUIREMENT FOR VoIP RESIDENTIAL GATEWAY

PARAMETER	REQUIREMENT
Input Voltage	5V or 12V
Output Power	3W to 10W
Efficiency	80% to 90%
Output Voltages	-24V, -72 to -100V and/or -48V
-24V Requirements (4 lines)	Regulation: ±5% Maximum Output Current: 0.10A Ripple: Less than $0.25V_{P-P}$
-72V Requirements (4 lines)	Regulation: ±10% Maximum Output Current: 0.10A Ripple: Less than $1V_{P-P}$

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Using the ISL6401EVAL1Z Evaluation Board

The ISL6401EVAL1Z Schematic shows a current mode power supply using the Intersil ISL6401 in standard flyback topology. The ISL6401EVAL1Z evaluation board is shipped “ready to use” right from the box. The IC requires +5V Bias. The evaluation board input voltage can be 10V to 16V with the specified transformer and external components. The output voltages are -24V at 120mA and -72V at 120mA. The board is capable of evaluating device operation with loads that simulate one, two, three or four line operation. The use of an electronic load enables evaluation over a wide range of operating conditions. Simply vary the load on each output from 0mA to 120mA in any combination to match exact application requirements. The circuit uses off-the-shelf inexpensive transformers to generate both outputs using a single controller. The transformer turns ration is 1:1:1:1 where 24V appear across each secondary winding and the primary during the switch off-time. The remaining secondary windings are stacked in series to develop -48V. The -48V section is then stacked on the -24V section to get the -72V. This technique provides good cross regulation, lowers the voltage rating required for the output capacitors and lowers the RMS current, allowing the use of cheaper output capacitors. Also, the selection of a transformer with multifilar winding lowers the leakage inductance and cost. The cross regulation of both output is achieved by using split feedback for both outputs where the feedback factor can be weighed based on load condition on both outputs.

TABLE 2. ISL6401EVAL1Z EVALUATION BOARD

BOARD NAME	IC	PACKAGE
ISL6401EVAL1Z	ISL6401CBZ	14 Ld SOIC

The evaluation board kit also includes 5 samples of ISL6401CBZ and ISL6401CRZ each.

Recommended Test Equipment

- A 5V power supply to bias the IC.
- A 12V power supply capable of supplying 2A of current
- Two electronic loads
- Precision digital multimeters
- A 4-channel scope with probes

Power and Load Connections

The ISL6401EVAL1Z evaluation board has three sets of terminal posts and a jumper that are used to supply the input voltages and to monitor and load the outputs.

Jumper Settings - Jumper JP1 allows the ISL6401 to be biased from a separate 5V supply or from the input voltage at VIN using a zener diode.

If a 5V supply is being used for the VCC input, place a jumper connecting the pins to the left (pin 1 and pin 2) of JP1. Placing a jumper to the right (pin 2 and pin 3) of JP2 will supply the bias of the ISL6401 from the input voltage at VIN using a zener diode (D1).

Input Voltage - Adjust the power supplies to provide the 5V and 12V input voltages. With the power supplies turned off, connect the positive lead of the 5V supply to the VCC post (P3). Connect the ground lead of the supply to the GND post (P4). Connect the positive lead of the 12V supply to the VIN post (P1). Connect the ground lead to the GND post (P2).

Output Voltage Loading and Monitoring - To exercise and monitor VOUT1, connect the positive lead of one of the electronic loads to the GND post (P7). Connect the ground lead of the electronic load to the VOUT1 post (P8). Connect the positive end of a digital multimeter to the VOUT1 post (P8). Connect the digital multimeter ground terminal to the GND post (P7).

To exercise and monitor VOUT2, connect the positive lead of the other electronic load to the GND post (P10). Connect the ground lead of the electronic load to the VOUT1 post (P9). Connect the positive end of a digital multimeter to the VOUT1 post (P9). Connect the digital multimeter ground terminal to the GND post (P10).

Each output can be viewed with an oscilloscope using the two scope probes, SP1 (VOUT1) and SP2 (VOUT2).

Start-up

The ISL6401 features an internal digital soft-start to reduce transformer and output capacitor stress and to reduce the inrush current surge on the input circuits. Figure 1 shows the start-up sequence.

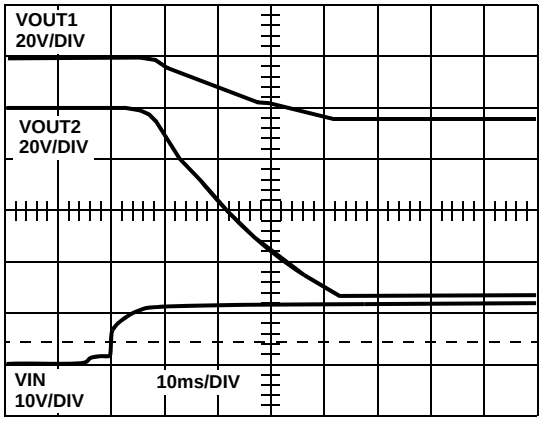


FIGURE 1. SOFT-START WAVEFORMS (2ms/DIV)

Output Performance

Output Ripple - Figure 2 shows the output voltage ripple for VOUT1 and VOUT2 both at 100mA load.

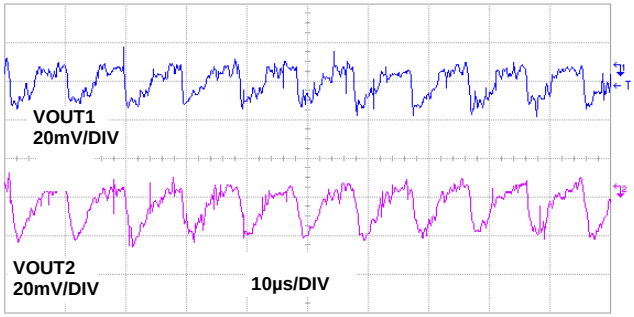


FIGURE 2. OUTPUT 1 AND 2 RIPPLE VOLTAGE

Transient Response - Figures 3 and 4 show the transient performance of the each output for a step load from 0mA to 100mA.

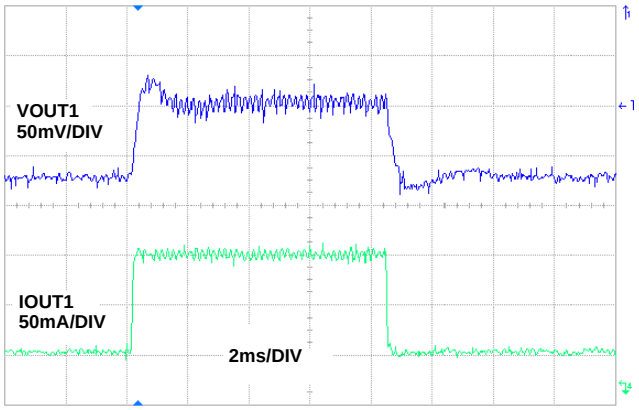


FIGURE 3. VOUT1 TRANSIENT RESPONSE

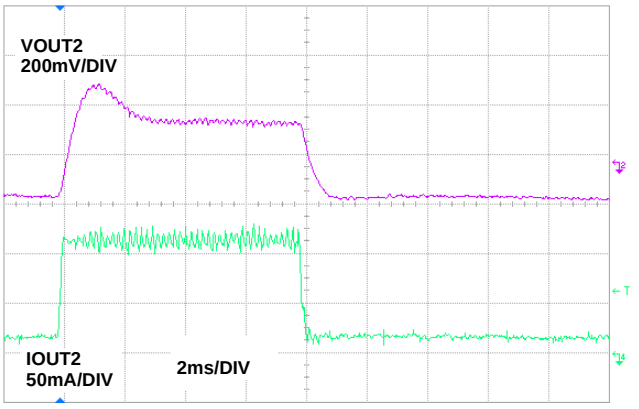


FIGURE 4. VOUT2 TRANSIENT RESPONSE

Oscillator

Switching Frequency - The gate driver output switching frequency can be programmed from 50kHz to 600kHz by adjusting the capacitor value on the CT pin (C5). Figure 5 can be used as a guideline in selecting the capacitor value required for a given frequency.

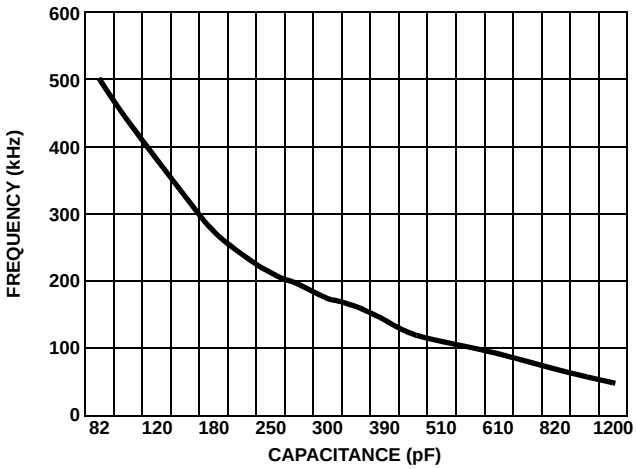


FIGURE 5. OUTPUT SWITCHING FREQUENCY vs CT

External Synchronization - The internal oscillator can be synchronized by an external clock connected to the SYNC pin (P6). Program the free running frequency of the oscillator to be 10% slower than the desired synchronous frequency. The external clock signal should have a minimum pulse width of 20ns.

Shutdown

When the SD pin (P5) is pulled low, the PWM is turned off and the output capacitors discharge. A typical shutdown waveform using the SD pin is shown in Figure 6.

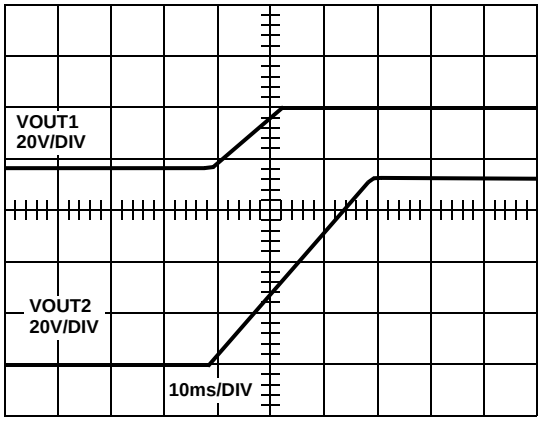


FIGURE 6. OUTPUT SHUTDOWN WAVEFORMS

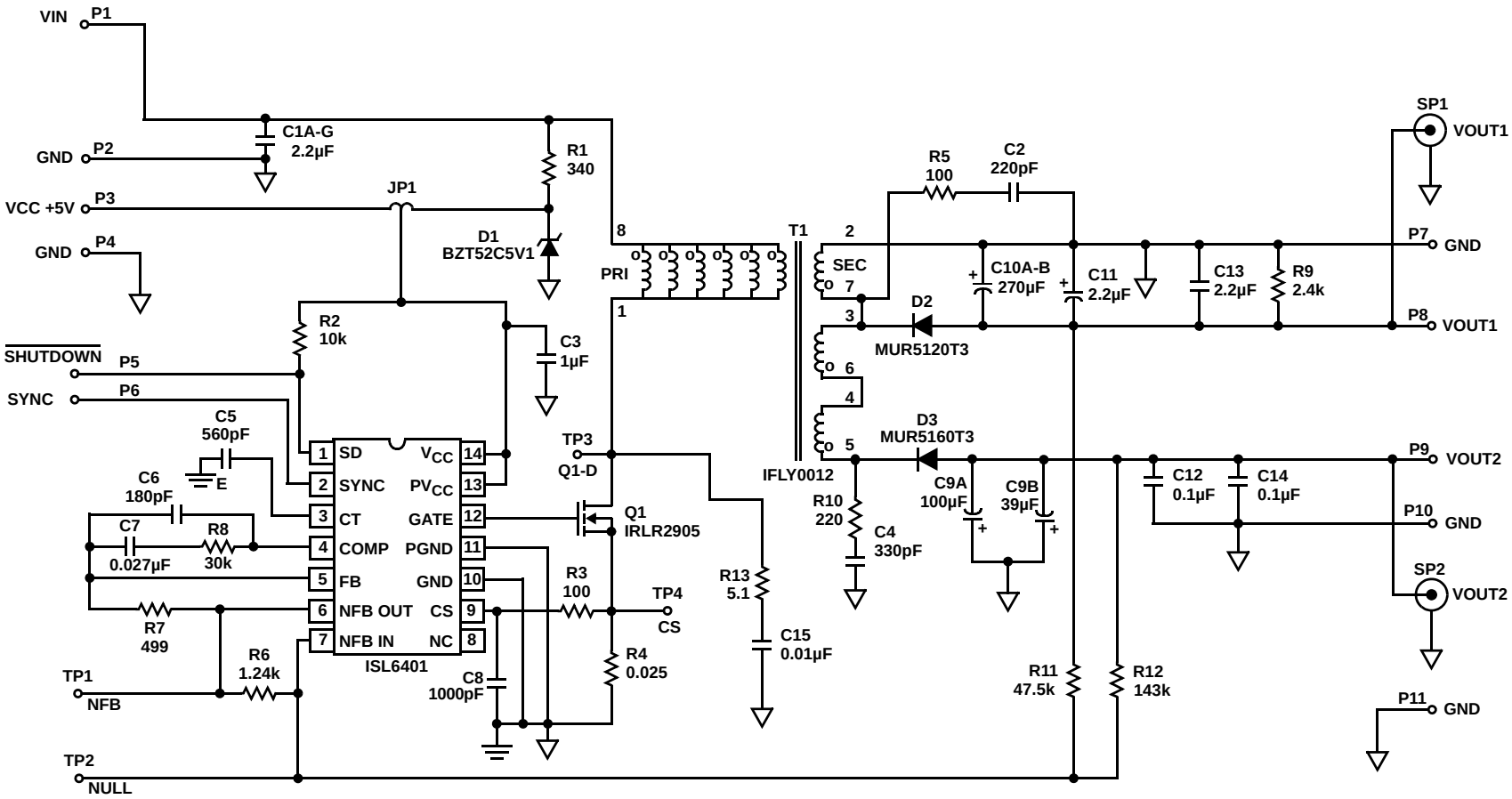
Conclusion

The ISL6401EVAL1Z evaluation board is a flyback reference design optimized to provide a high performance, low-cost solution for RSLIC Ring and Talk power supplies in VoIP application. It has the capability of evaluating device operation with loads that simulate one, two, three, or four line operation.

References

1. ISL6401 Datasheet (“ISL6401: Synchronizing Current Mode PWM for Subscriber Line Interface Circuits”), Intersil Corporation, FN9007. For Intersil documents available on the web, see http://www.intersil.com/

ISL6401EVAL1Z Schematic



ISL6401EVAL1Z Bill of Materials

QTY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
1		PWB-PCB, ISL6401EVAL1Z, REVA, SOIC, ROHS	TITAN	ISL6401EVAL1ZREVAPCB
1	C9A	CAP, RADIAL, 10µF,100V, 20%, AL E, ROHS	SANYO	100ME100AX
1	C9B	CAP, RADIAL, 39µF, 100V, 20%, AL ELEC, ROHS	SANYO	100ME39AX
1	C10A	CAP, RADIAL, 10x16, 270µF, 35V, 20%, AL.EL., ROHS	SANYO	35ME270AX
1	C8	CAP, SMD, 0805, 1000pF, 50V, 5%, NPO, ROHS	PANASONIC	ECU-V1H102JCX
1	C15	CAP, SMD, 0805, 0.01µF, 50V, 5%, X7R, ROHS	VENKEL	C0805X7R500-103JNE
1	C6	CAP, SMD, 0805, 180pF, 50V, 5%, NPO, ROHS	VENKEL	C0805COG500-181JNE
1	C2	CAP, SMD, 0805, 220pF, 50V, 10%, X7R, ROHS	VENKEL	C0805X7R500-221KNE
1	C7	CAP, SMD, 0805, 0.027µF, 50V, 10%, X7R, ROHS		
1	C5	CAP, SMD, 0805, 560pF, 50V, 5%, NPO, ROHS	MINI-REEL	605-356
1	C4	CAP, SMD, 1206, 330pF, 100V, 5%, NPO, ROHS	VENKEL	C1206COG101-331JNE
9	C1A-C1G, C11, C13	CAP, SMD, 1210, 2.2µF, 50V, 10%, X7R, ROHS	TDK	C3225X7R1H225K
2	C12, C14	CAP, SMD, 1812, 0.1µF, 100V, 20%, X7R, ROHS	VENKEL	C1812X7R101-104MNE
1	C3	CAP, SMD, 1812, 1µF, 50V, 10%, X7R, ROHS	VENKEL	C1812X7R500-105KNE
2	SP1, SP2	CONN-GEN, SHIELDED TEST JACK, VERTICAL, ROHS	JOHNSON COMPONENTS	129-0701-202
10	P1-P10	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2
4	TP1-TP4	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
1	JP1	CONN-HEADER, 1x3, BRKAWY 1x36, 2.54mm, ST	BERG/FCI	68000-236-1X3
1	JP1 (place on pin 1 and 2)	CONN-JUMPER, SHORTING, 2PIN, BLACK, GOLD, ROHS	SULLINS	SPC02SYAN
1	D1	DIODE-ZENER, SMD, SOD-123, 5.1V, 500mW, ROHS	DIODES, INC.	BZT52C5V1-7-F
1	D2	DIODE-RECTIFIER, SMD, SMB, 2P, 1A, 200V, ROHS	ON SEMICONDUCTOR	MURS120T3G
1	D3	DIODE-RECTIFIER, SMD, SMB, 2P, 1A, 600V, ROHS	ON SEMICONDUCTOR	MURS160T3G
5	PURCHASE, DNP. BAG AND SHIP W/BOARD.	IC-RSLIC PWM, 14P, SOIC, ROHS	INTERSIL	ISL6401CBZ
1	U1	IC-RSLIC PWM, 14P, SOIC, ROHS	INTERSIL	ISL6401CBZ
5	PURCHASE, DNP. BAG AND SHIP W/BOARD.	IC-RSLIC PWM CONTROLLER, 16P, QFN, 4x4, ROHS	INTERSIL	ISL6401CRZ
1	Q1	TRANSIST-MOS, N-CHANNEL, SMD, D-PAK, 42A, ROHS	INTERNATIONAL RECTIFIER	IRLR2905PBF
1	R3	RESISTOR, 0805, 100Ω, 1/8W, 1%, TF, ROHS	VENKEL	CR0805-8W-1000FT
1	R2	RES, SMD, 0805, 10k, 1/8W, 1%, TF, ROHS	VENKEL	CR0805-8W-1002FT(PbFREE)
1	R6	RES, SMD, 0805, 1.24k, 1/8W, 1%, TF, ROHS	PANASONIC	ERJ-6ENF1241V
1	R12	RES, SMD, 0805, 143k, 1/8W, 1%, TF, ROHS	PANASONIC	ERJ-6ENF1433V
1	R8	RES, SMD, 0805, 30k, 1/8W, 1%, TF, ROHS		
1	R11	RES, SMD, 0805, 47.5k, 1/8W, 1%, TF, ROHS	KOA	RK73H2AT4752F
1	R7	RES, SMD, 0805, 499Ω, 1/8W, 1%, TF, ROHS	YAGEO	RC0805FR-07499RL
1	R5	RES, SMD, 1206, 100Ω, 1/4W, 1%, TF, ROHS	STACKPOLE	RMC1/8 100R 1% T/R
1	R10	RES, SMD, 1206, 220Ω, 1/4W, 5%, TF, ROHS	VISHAY	CRCW1206221J
1	R13	RES, SMD, 1210, 5.1Ω, 1/4W, 5%, TF, ROHS	PANASONIC	ERJ-14YJ5R1U
1	R4	RES, SMD, 2512, 0.025Ω, 1W, 1%, TF, ROHS	DALE	WSL-2512-.0251%
1	R1	RES, SMD, 2010, 332Ω, 1/2W, 1%, TF, ROHS	PANASONIC	ERJ-12SF3320U

ISL6401EVAL1Z Bill of Materials (Continued)

QTY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
1	T1	TRANSFORMER-FLYBACK, 6.0µH, 10%, SMD, 8P, 25x17, ROHS	GCI TECHNOLOGIES	IFLY0012/G013064LF
4	Four corners.	SCREW, 4-40x1/2in, PAN, NYLON, PHILLIPS, ROHS		
4	Four corners.	STANDOFF, 4-40x3/4in, F/F, HEX, NYLON	KEYSTONE	1902D
1	Place assy in bag	BAG, STATIC, 5x8, ZIP LOC	INTERSIL	212403-013
0	C10B	DO NOT POPULATE OR PURCHASE		
0	R9	DO NOT POPULATE OR PURCHASE		
1		LABEL, FOR SERIAL NUMBER AND BOM REV #		

ISL6401EVAL1Z Layout

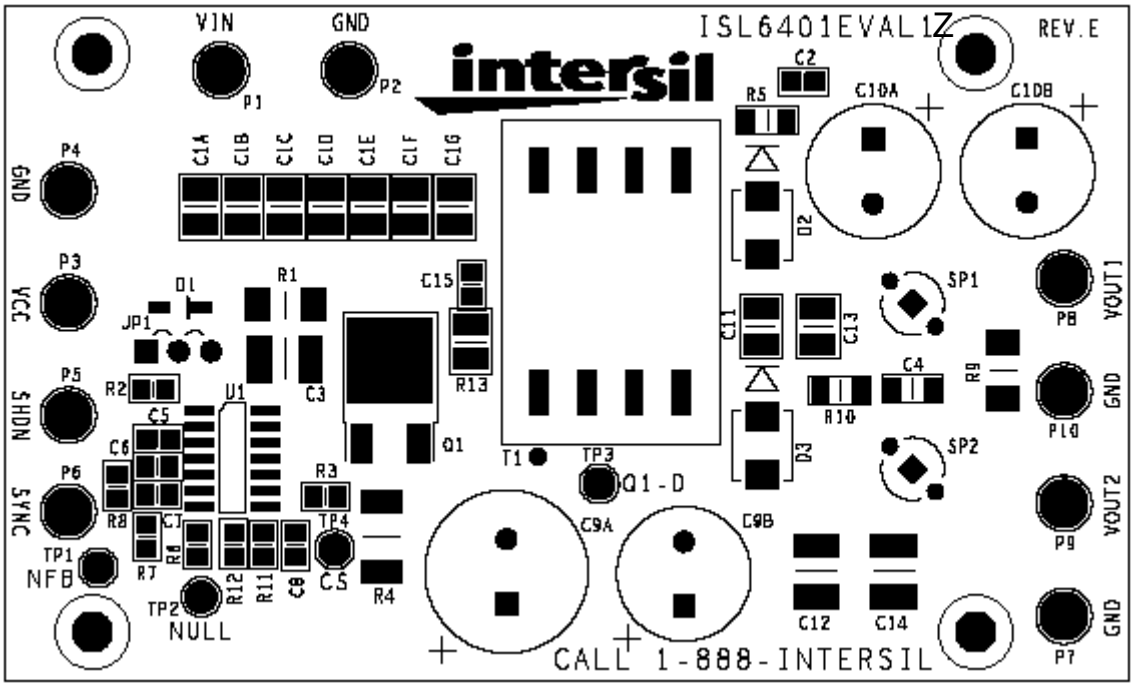


FIGURE 7. TOP SILKSCREEN

ISL6401EVAL1Z Layout (Continued)

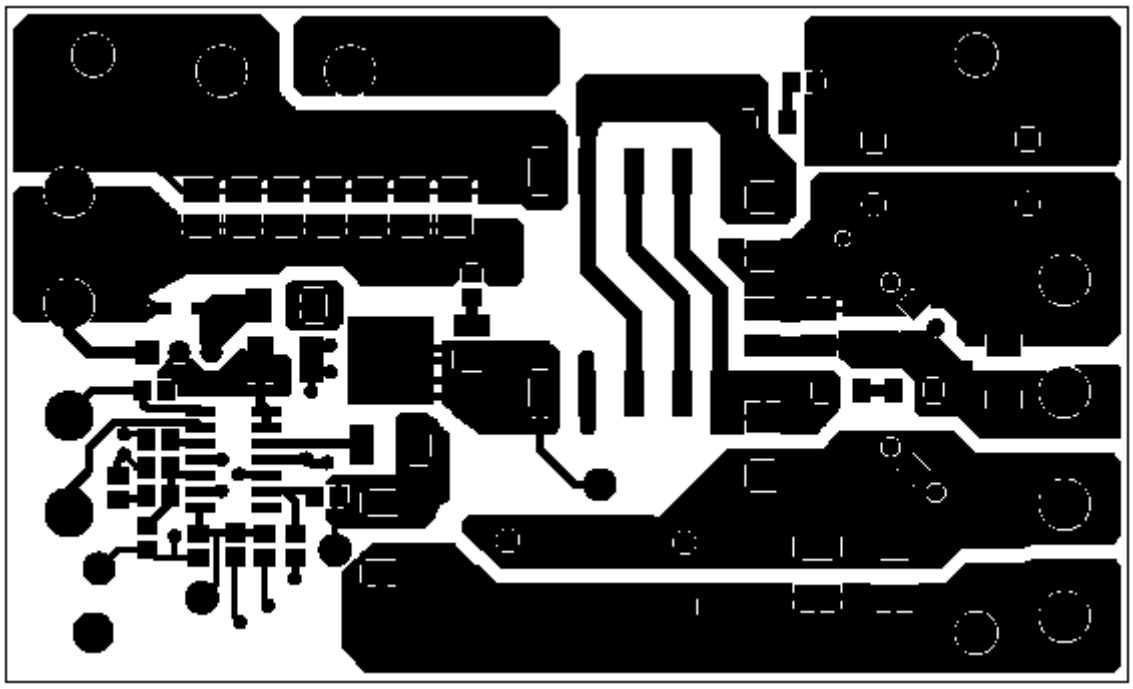


FIGURE 8. TOP LAYER 1

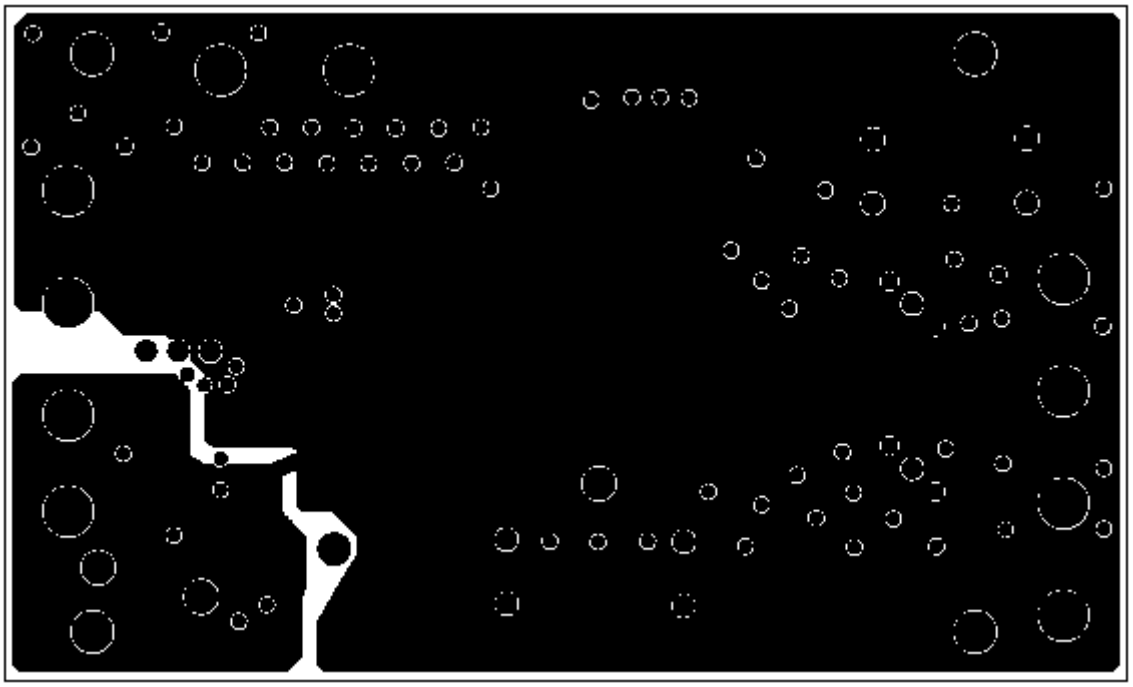


FIGURE 9. TOP LAYER 2

ISL6401EVAL1Z Layout (Continued)

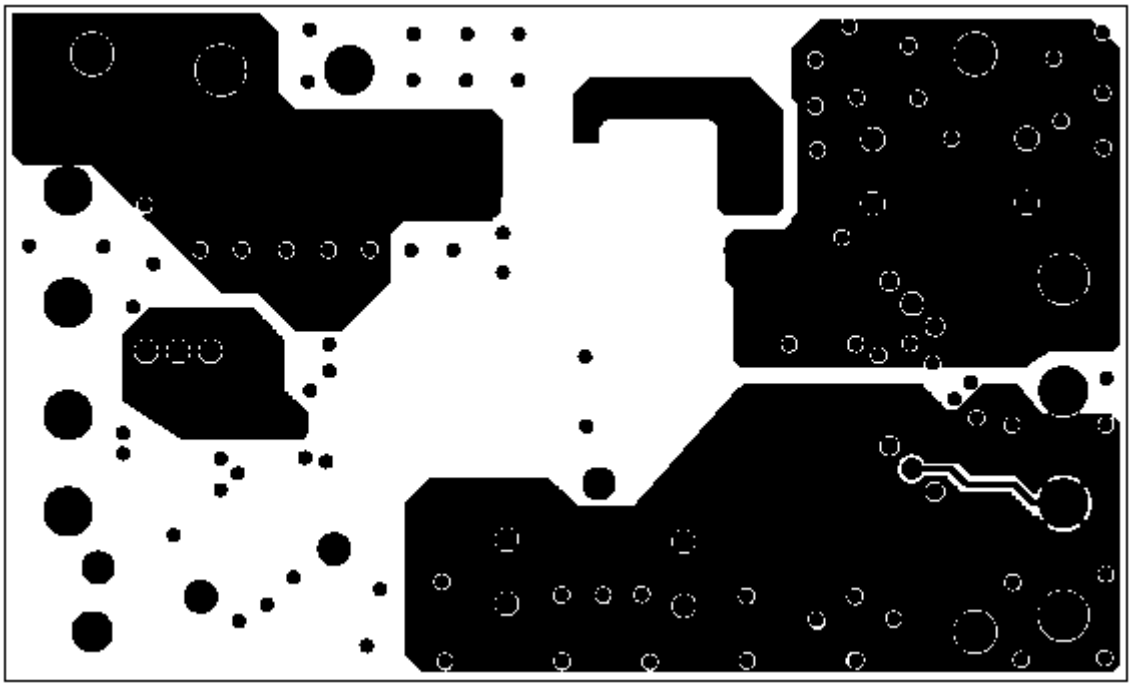


FIGURE 10. TOP LAYER 3

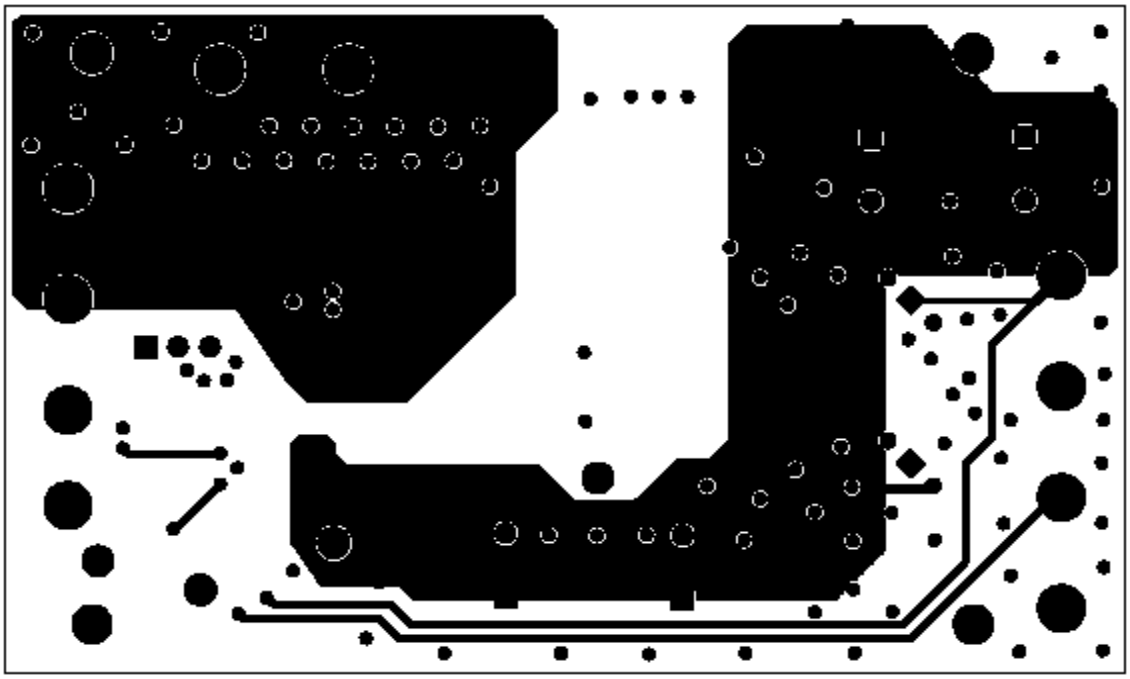


FIGURE 11. BOTTOM SILKSCREEN

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